Through-Life Monitoring of the impact of vibration on the reliability of area array packages using Non- Destructive Testing

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Abstract

In order to keep up with the demands for faster, cheaper and smaller electronics, the packaging industry has evolved tremendously. Area array packages like flip chips and ball grid arrays are therefore widely used in modern day electronics. However, from the reliability standpoint, solder joints in these area array packages are often the weakest link. In case of harsh vibration environments like military and automobile applications, joint failure mainly occurs due to the high stress incurred during extreme environmental conditions that lead to fatigue failures. This thesis aims to study the effects of real time vibration on area array packages (flip chips in particular) using acoustic micro imaging for through life monitoring of the solder joints. Since real time vibration on solder joints have not been studied before, the various steps for successful testing, through life monitoring of the solder joints and data analysis will be investigated and discussed.

Based on automobile industry standards, a real time vibration profile was obtained with the help of Delphi experts, who are the industry collaborators of this project. Due to its strong capability to detect discontinuities within materials and interconnections, Acoustic Micro Imaging (AMI) also known as Scanning Acoustic Microscopy (C-SAM) has been used to monitor the solder joints. This approach has not previously been used as an effective tool in monitoring solder joints through life performance in vibration testing. The research regime proposed in this thesis was to monitor the health of solder joints through ultrasound images from beginning to failure, and to see how cracks initiate and propagate in them. The effect of the relative position and orientation on the reliability of the solder joints and the flip chips in the PCB was also studied. The data collected was analysed using MATLAB.

The results have shown that three types of solder joints- healthy, partially fractured or fractured are formed near the time of complete failure of a flip chip. When about 70-80% of the flip chips are either partially fractured or fractured a flip chip is expected to fail. The mean pixel intensity and area change in the acoustic image of a partially fractured or fully fractured joint tends to be higher compared to a healthy joint. Crack initiation in a joint occurs at around 35-40% cycling and propagates linearly till 80-85% cycling after which a joint fails. A statistical analysis done on the solder joints showed that the intensity distribution of healthy joints follow a simple Gaussian distribution while that of partially fractured or fractured joint can only be represented by using a mixture of Gaussians. The solder joints near the board edges are the least reliable in a vibration environment. However, solder joints with back to back connections are more reliable than the ones placed in one sided orientation. The most reliable flip chip orientation in a vibration environment is the back to back connection with no offset which was actually found to be the least reliable in the case of thermal cycling. Based on the analysis of the results, a few design guidelines for flip chip layout and orientations in a PCB has also been proposed in this work.

Acknowledgement

First and foremost, I would like to take this opportunity to gratefully acknowledge all those who provided support, guidance and help throughout this research project.

I would like to express my deepest gratitude towards my supervisors, Professor David Harvey, Dr. Guang Ming Zhang and Dr. Derek Braden, for their guidance, support and assistance in every stage of this research project. I would also like to express my gratitude towards Delphi for providing the test samples, expert support and extensive access to the vibration chamber at Liverpool. This thesis would not have been possible without their help. Finally, I would like to express my sincere thanks and appreciation to my family and friends for their constant encouragement and understanding during this journey.

Contents

List of Figures

List of Tables

List of Publications

1. Baishya. K, Zhang, G.M., Harvey, D.M. and Braden. Derek(2016) Toolbox for 3D Acoustic Imaging of Manufactured Electronics Circuits, IEEE ESTC conference, Grenoble, 13-16 September

2. Braden Derek, Harvey, D.M., Zhang, G.M. and Baishya. K(2016) Real World Modelling of Circuit Board assemblies to help Inform Prognostic Predictions, IEEE ESTC conference, Grenoble, 13-16 September

3. Adeniyi A. Olumide, Baishya. K, Zhang, G.M., Harvey, D.M. and Braden. Derek(2018*)* Non-destructive Evaluation and Life Monitoring of Solder Joints in Area Array Packaging 2018. 7th Electronic System-Integration Technology Conference, 2018.

List of Abbreviations

Abbreviations	Meaning
AMI	Acoustic Micro Imaging
AOI	Automated Optical Inspection
ATC	Accelerated thermal cycling
BGA	Ball Grid Arrays
CCD	Charged Coupled Device
CSP	Chip Scale Package
CTE	Coefficient of thermal expansion
CT	Computed Tomography
DCA	Direct chip attachment
DIL	Dual in Line
ENIG	Electro less nickel immersion gold
FAMI	Frequency domain acoustic micro imaging
FC	Flip Chip
FCIP	Flip Chip in Package
FCOB	Flip Chip on Board
FCBGA	Flip chip ball grid array
FR-4	Flame retardant class 4
HASL	Hot air solder levelling
HCF	High cycle fatigue
IC	Integrated Circuit
MAPBGA	Moulded array process ball grid array
NDT	Non Destructive testing
PCB	Printed Circuit Board
PBGA	Plastic ball grid array

PoP	Package on package
PSD	Power Spectral Density
QFP	Quad flat package
RMS	Root mean square
ROI	Region of interest
SAM	Scanning acoustic microscopy
SLT	Solid Logic Technology
SMT	Surface Mount Technology
TBGA	Tape ball grid array
TDR	Time domain reflectometry
TEPBGA	Thermally enhanced plastic ball grid array
TFDAMI	Time frequency domain acoustic micro imaging
TOF	Time of flight
UBM	Under bump metallization
VRM	Virtual rescanning mode

Chapter 1

Introduction

1.1 Motivation and Overview

Electronic packaging is a technology to package the integrated circuit (IC) in a modular form that can be used in an end product (Baldwin and Higgins, 2005). It is the last stage of semiconductor device fabrication. A package refers to the encapsulating case around the semiconductor material in electronic devices. It serves as the electrical connect between the device and the circuit board in integrated circuits and also protects the semiconductor from physical damage and corrosion. The rapid evolution of the electronics industry has resulted in the ever increasing demand for devices with higher packaging density, greater intelligence, higher speed, and higher input/output performance. However, all these demands come with the added challenge of reduced sizes and lower costs. The result is, today, we have all sorts of lightweight, multi-functional devices such as smartphones, smart watches, smart television and so on. This miniaturisation of electronic devices in turn led to the necessity for higher pin counts to facilitate higher interconnections. This necessity thereby, led to the evolution of the electronic packaging industry from through hole technology to surface mount technology (SMT). In Through Hole Mounting technique, different components, which have lead wires are led to the circuit board through holes. In this method, leads rely on holes in a multilayer printed circuit board (PCB) which are then soldered on the opposite side to the component to offer permanent mounting. A Dual in Line(DIL) package (Figure 1.1) is an example of this technology. However in SMT, the leads are soldered directly on to the component side of a PCB surface , rather than using hole mounting, thus, utilizing the entire chip surface area and hence, providing a higher number of pin counts and interconnections between integrated circuits and PCB. Flip Chips (FCs), Ball grid arrays (BGAs) (Figure 1.2) and Chip scale packages (CSPs)

(Figure 1.3) use this technology. Figure 1.3 shows a typical multi-layer alumina chip scale package used in automotive.

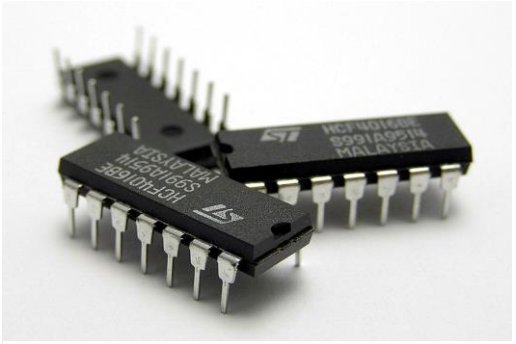


Figure 1.1: Three 14-pin (DIP14) plastic dual in-line packages containing IC

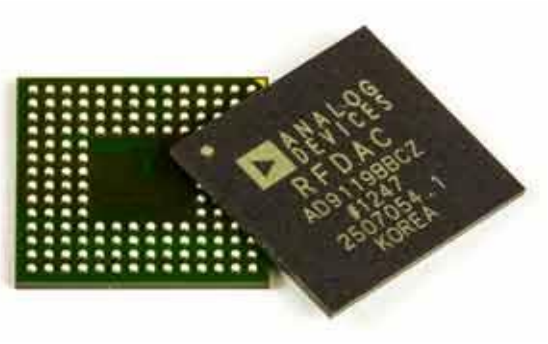


Figure 1.2: A close-up photo of a ball grid array package

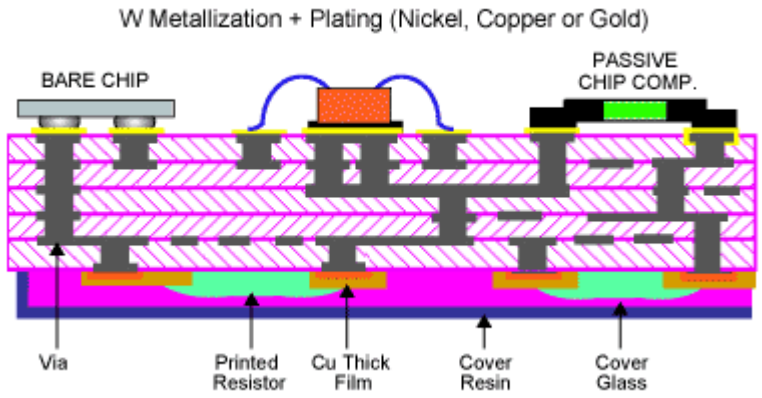


Figure 1.3: Multi-layer ceramic substrates used in engine control units of automotive (Kyocera Corporation)

Another trend that emerged soon after was to shrink the interconnect spacing in the ICs from typically 0.1 inch used for DIL, towards a sub-millimetre scale for SMT, to accommodate denser interconnections and allow more components per PCB area.

Internal connections inside packages have progressed even faster with die to package and die to die internal connections now in the micron range. This was predicted by the 2005 ITRS roadmaps(ITRS,2005) that wire bond interconnect in ICs would shrink to the range of 25µm pitch with almost double thermal efficiency by 2010((Tai & Chen 2006).

As stated in the 2015 ITRS Roadmap, on April 19, 1965 Gordon Moore said, "With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip. What could

you do with 65,000 components?" On February 26, 2015 Paolo Gargini said, "With unit cost falling as the number of components per circuit rises, by 2015 economics may dictate squeezing as many as 6,500,000,000 components on a single silicon chip. What could you do with 6,500,000,000 components?"(Gargini 2015) This increase in component count inside and outside ICs can cause manufacturing and reliability problems, since there can be 6,500,000,000 failure sites inside a single IC.
Indeed, as all good things come at a price, miniaturised products do too. Miniaturisation of electronics has given rise to numerous reliability issues. The intensity of these issues can be very severe depending on the applications the electronic devices are designed for, especially in fields like aerospace, automobile and military where a failed device can result in fatalities. Devices used in these areas operate in very harsh environmental conditions including extreme pressure variations, temperature and humidity and are also exposed to harsh vibrations(Richard D. Parker 2000).

In the automobile industry, as the electronic content in a motor vehicle continues to increase, so also does the complexity of the vehicle embedded systems. Consequently, the reliability expectation of both the customer and vehicle manufacturer has also increased. In the first twelve months of a vehicle's life, electrical problems account for up to 70% of customer complaints and warranty problems (MIRA (Motor Industry Research Association)). This is a generalised figure that includes all electrical and electronic equipment. No figures were presented for the proportion of failures within the quoted percentage that were attributed to either Ball Grid Array (BGA) or Chip Scale Packaged (CSP) devices. To put this in context, within Delphi Corporation itself, it is estimated that the daily production of solder joints is approximately 1 billion (Delphi et. al 2013). This represents some 1 billion or more failure site opportunities at the component to circuit board assembly interface. Delphi, is a high-technology automotive electronics company that integrates safer, greener and more connected solutions for the automotive sector. Delphi operates technical centers, manufacturing sites and customer support services in 44 countries.

In 2009, the ITRS Roadmap addressed the reliability issue. Under the Assembly and Packaging roadmap (ITRS 2009), it was stated that new package designs, materials and technologies will not be capable of the reliability required in all market applications.

More in depth knowledge of failure mechanisms and 'in-field' conditions are required to bring reliable new package technologies to the market place. The Executive Summary of the ITRS 2013 again addressed the reliability issue stating that, "Enhanced customer visibility for quality assurance of high reliability products, including manufacturing outsourcing, continues to be a challenge." (ITRS 2013). In summary, a solution to these challenges has yet to be found.

To overcome this reliability issue, environmental testing has been a long research initiative to understand the causes of failures in electronic devices. Normally an electronic package consists of a semiconductor chip that is mounted on an encapsulated substrate using solder interconnects. The encapsulation of the substrate seals the device from the outside environment thereby providing a safe electrical and mechanical connection from the PCB to the chip (Batra et al. n.d.). However, the solder interconnects happen to be the weakest link in terms of product reliability (Braden et al. 2010). The most common causes of failure of interconnects are found to be fatigue, creep, corrosion and mechanical overstress (Kwon et al. 2009). The failure of a solder joint typically begins with the initiation and then propagation of a crack at a surface or interface until it causes a loss in electrical continuity (Manfredi et al. 2011).
The most commonly used techniques used for testing the reliability of solder joints are (Batra et al. n.d.):

1. Accelerated thermal cycling (ATC)
2. Isothermal mechanical cycling

In ATC, the solder joints or interconnects are subjected to accelerated cyclic temperature variations similar to the real life thermal variations. During ATC, due to the difference in the coefficient of thermal expansion (CTE) of the materials, they expand and contract at different rates when exposed to varying temperatures due to thermal mismatch between them. This thermal mismatch starts causing cyclic shear strain on the solder joints and starts increasing as the temperature is cycled leading to deformations like crack initiation and finally fatigue failure of the device.

In addition to thermally induced stresses, electronic systems also experience vibration environments during shipping, handling and operation. So, reliability of the solder

joints under vibration is a very important issue, especially in the automobile industry(Ham & Lee 1996). So in isothermal mechanical cycling, the solder joints or interconnects are subjected to accelerated cyclic mechanical variations like vibration under isothermal conditions mimicking real life mechanical variations until they fail. Amy , Aglietti and Richardson in their paper, 'Reliability analysis of electronic equipment subjected to shock and vibration – A review', have illustrated the many difficulties in predicting electronic equipment reliability(Amy, Aglietti&Richardson 2009) and showed why progress in this field has been slow thereby pointing out the major difficulty of making a model that works across a broad range of equipment configurations.

Although a lot of research has been done on ATC, vibration testing is relatively less studied. This is because:

Heating is a problem common to almost all electronic equipment while vibration exposure is very specific to electronics used in certain fields such as automotive, aerospace and military.

It is fairly easy to conduct an ATC test. All one needs is an oven and a test board. Hence the cost is also low. But vibration testing requires an elaborate set up which is very expensive and hence not easily available.

Although less researched, solder joint fatigue failure under vibration loading has always been a great concern in the microelectronic industry. Vibration was identified to be one of the most important causes of electronic failure by the US Air force(Steinberg 2000). Therefore, solder joint reliability testing is expected for high frequency vibration particularly for these electronics which are prone to encounter harsh environment in practice(Che & Pang 2015). Liu and Meng (Liu & Meng 2014) studied the lead-free solder joint behavior of BGA packages under different random vibration loadings and results showed that the corresponding failure modes were converted from ductile fracture to brittle fracture with the increase of vibration intensity. Wong (Wong et al. 2007) presented a methodology to characterize and predict fatigue failure of BGA package solder joints under vibration loading based on board strain versus number-of-cycles-to-failure (or S-N) curve. The comparison of SnAgCu and SnPb solders in fatigue curves clearly indicated the better performance of SnAgCu solder system under high-cycle fatigue test, while this trend was reversed in low-cycle fatigue, where SnPb

solder has superior fatigue resistance. Che and Pang (Che & Pang 2009) carried out the sinusoidal vibration reliability test for flip chip solder joints and applied linear cumulative damage analysis method (Miner's rule) to predict the life of solder joints. However none of these studies attempted to conduct real time vibration tests or were able to monitor the exact dynamics, location and size of the crack. Solder joint reliability is also affected by the component's floor plan, the thickness of the PCB and the influence of the surrounding components (Braden *et al*., 2010). This work reported in this thesis will deal with these issues.

1.2 Aims and Objectives

The main aims of this work are to firstly, investigate the reliability of solder joints in area array packages in a real time vibration environment at room temperature. Research will be done to see when, how and where the solder joints crack within the test boards when exposed to vibration and investigate how any cracks propagate. Secondly, the effects of the component floor plan layout on the reliability of solder joints and individual flip chips will then be inspected. Finally, feasibility of using different inspection techniques like novel resistance spectroscopy techniques, and innovative 3D acoustic imaging techniques and commonly used imaging methods like 2D X-ray and 1D/2D ultrasonic scans will be analysed in order to monitor the solder joints through their lifetime till complete mechanical failure. Although flip chips (FCs) and BGAs both belong to area array packaging, the material used in interposers of BGAs does not allow ultrasound to penetrate them. So for analysis purposes they cannot be scanned for further image processing. Hence, FCs will be used as a test vehicle to monitor the solder joints non-destructively.

The main research objectives hence include:

1. **Investigating a range of vibration testing profiles to determine the one best suited for testing flip chips:** Normally, the purpose of product vibration testing is to simulate the vibration environment encountered during typical automotive operation and normal transportation. It is intended to insure that the product survives and functions as per customer requirements for its defined mission life. These tests

are typically engineered to condense field exposure time into a relatively short laboratory test while imparting equivalent mission stress. The tests are typically specified to sequentially expose the product under test to vibration in each of three mutually perpendicular planes.

Vibration testing can be categorised as (Delphi E&S n.d.)

i. **Broadband Random Vibration**: This method exposes the test sample to a non-periodic motion where all of the frequencies within the test bandwidth are present all of the time. The random motion can be defined as a series of overlapping sinusoids, each with their own frequency and amplitude. The acceleration and displacement magnitudes vary in a Gaussian fashion resulting in a normal distribution of peaks. Vehicle data has shown the automotive chassis response to typical driving conditions such as rough road, gravel surface, pot holes, etc. is random in nature. Thus, the random vibration test method provides a basis for laboratory simulation of the field vibration exposure and durability demonstration testing. Fatigue or overstress failure modes based on single and multiple system resonances within the test sample can be tested by this method.

ii. **Swept Sinusoidal Vibration**: This method involves exposing the test sample to a periodic motion which at any moment in time consists of a single frequency at a defined acceleration, displacement or velocity level. During the test the frequency will be swept, logarithmically or linearly, up and down through the test bandwidth. Sinusoidal vibration as performed in the lab rarely exists in the natural environment and therefore has little or no relationship to product's field exposure. Unlike random, the test sample is exposed to only one frequency at a time. Failures based on exciting multiple resonant modes will most likely not be detected. The sinusoidal vibration test method is best used as a tool to evaluate the resonance and transmissibility characteristics of a test sample or subassembly.

   In conjunction with broadband random, swept sinusoids can be used to create tests which simulate engine vibration environments.

iii. **Sine-on-Random**: The vibration environment of many on-engine applications consists of a combination of both broadband random and sinusoidal components. Broadband Random component is the result of a complex array of moving parts within the engine structure, combustion events, turbulent airflow through intake and exhaust channels, panel and bracket resonances. The sinusoidal component is related to crankshaft rotation, imbalance, firing frequency or all of the above. The lab simulation of the sine-on-random environment is performed by superimposing the swept sinusoid on the broadband random signal. These two modes are run simultaneously and for the same duration.

iv. **Long Waveform Replication**: Long waveform replication involves capturing a dynamic event such as vibration input to a radio while the vehicle traverses rumble strips. Following data processing, the recorded time history is "played back" through laboratory vibration test equipment. With the exception of performing this, a single axis at a time in the lab, the field exposure is replicated. Since this test is performed at field levels, it is not utilized for durability purposes as are the test methods described previously in this section

2. **Determination of the duration for which the FCs have to be vibrated /axis for the test**

   Accelerated vibration tests are typically done by vibrating the test board on each of the three perpendicular axis for a predetermined amount of time which is normally 6 hours/axis. Since for the proposed experiment, vibration testing will be done in real time, the duration of the test needs to be freshly determined. Based on that, the total time will be broken down to smaller cycles and the solder joint degradation will be monitored at the end of each shorter cycle.

3. **Research the feasibility of different inspection methods**

   Once the appropriate test and duration per cycle has been determined, the next step will be to design an inspection technique that will constantly monitor the solder joint's health at the end of each test cycle.

4. **Ultrasound Inspection during tests**

   At the end of each test cycle the board will be ultrasonically scanned using acoustic micro imaging to obtain images (Zhang et al. n.d.). Acoustic micro imaging (AMI) is a widely used non-destructive inspection technique for failure analysis, capable of evaluating defects like voids, delaminations, disbonds and thin cracks in electronic packages. This technique will be described in details in chapter 2. New 3D acoustic processing (Baishya. K et. al 2016) will be used, if possible, to enhance the ultrasound images by filtering and separating overlapping acoustic waves.

5. **Data Analysis using MATLAB**

   The data and images will be analysed using MATLAB software to observe in what order and which joint position the solder joints start failing. The effect of the component floor plan layout on the reliability of flip chips will also be investigated.

6. **Design guidelines for PCB layout**

   Based on the results obtained from the data analysis, a set of guidelines will be proposed for component floor layouts in PCBs in order to achieve maximum performance from the flip chips in terms of reliability.

1.3 Novelty and contribution to knowledge

This work investigated the reliability of solder joints in area array packages through real time vibration and a non-destructive solder joint health monitoring system. The system monitored the health of solder joints in flip chip (Yang et. al 2012) under a real time vibration environment, by detecting changes in mechanical integrity in the solder joints till their complete mechanical failure. Further research was done to develop a floor plan guideline for area array packages in a vibration environment. This is very challenging and to our knowledge has never been done in real time before.

Although some research has been done on solder joints in an accelerated vibration environment, no study has been able to identify when and where the crack in a solder joint starts or how it propagates. This project was able to estimate two trigger points

within the life time of a solder joint, the first of which indicates crack initiation occurs at around 35-40% of their lifetime while the second trigger point indicated the point just before complete mechanical failure and occurred at around 80-85%. In order to achieve this, acoustic micro-imaging techniques were used. At the end of each test cycle, the flip chips were ultrasonically scanned and the image were analyzed using image processing techniques to estimate the health of the solder joints. The idea was, as soon as the joint starts degrading, the mean pixel intensity of the solder joint acoustic images changes (Yang et al. 2012).

Knowledge of the trigger points will save a lot of time and resources in an industrial environment where otherwise devices are tested until complete failure and can take months for testing. However, now that the first trigger point of probable crack initiation is known the devices can be tested and monitored until this point and if signs of crack initiation do appear, the rest of the test can be discarded, resulting in a much more efficient use of time and resources.

The PCBs used in this study have 14 flip chips (FCs) that were placed in different orientations and relative positions. The reliability of solder joints based on the flip chip orientations and positions were studied based on which, floor plan design guidelines for area array packages in printed circuit boards(Braden et al. 2010) were proposed. Currently, no such design guidelines for PCBs were found available in the public domain.

The project provided a good comparison between the reliability of solder joints in an accelerated thermal cycling environment and a vibration cycling environment in order to study the similarities/ differences in their degradation pattern.

This research successfully studied the effects of vibration on the floor plan layout based on the reliability of solder joints in flip chips placed at different positions and relative orientations in the PCB. Based on that, a few design guidelines have been proposed which will ensure better susceptibility of solder joints and flip chips in a real life vibration environment.

1.4 Industry collaboration

The experimental work of the project will be equally divided between the laboratory in Liverpool John Moores University, LJMU and Delphi, Liverpool. The proposed project will be backed by Delphi Electronics and Safety at its Liverpool and Krakow sites.

1.5 Thesis Structure

Chapter 1: Introduction: It is this chapter which provides an introduction to the thesis.

Chapter 2: Background and literature review: As the name suggests, this chapter focuses on the background of the research work and discusses in detail the basic concepts like flip chip packaging, vibration testing and nondestructive reliability testing techniques like acoustic imaging, X-ray and resistance spectroscopy. It also discusses the constraints of each of the testing techniques when applied to the monitoring of flip chips in a vibration environment. Research works of other researchers relevant to the topic will also be discussed in order to identify the loopholes that led to the conception of this research idea.

Chapter 3: Experimental Plan: This chapter outlines the various challenges that finally led to the development of the algorithm for efficient inspection of the solder joints in a flip chip subjected to vibration using nondestructive acoustic imaging.

Chapter 4: Results: This chapter documents the results of the research work obtained after implementing the algorithm developed in chapter 3.

Chapter 5: Conclusion and discussion: This chapter summarizes the entire research work and discusses in details if the goals set out at the beginning of the research have been achieved successfully.

Chapter 6: Future work: Finally, this chapter dives into the possibilities of all the new directions that can be pursued to make the current research work more accurate and informative for future researchers.

Chapter 2

Background and Literature Review

Before diving into the details of the experiment, this chapter provides a brief insight into the background and relevant literature pertaining to the proposed research idea. While dealing with the topics of area array packaging, various non-destructive testing methods and vibration testing this chapter will also outline the various developments in the field of reliability and through life monitoring of area array packages particularly in connection to vibration testing.

2.1 Area array packages

As was discussed in chapter 1, section 1.1, in order to meet the increasing demands for faster, smaller and cheaper electronic devices, the packaging industry evolved from through hole to surface mount technology (SMT). Today, SMT is one of the most common packaging processes and is growing by the day. Area array packages are a type of SMT. In area array packages almost all of the area on the bottom of the package is used for connecting to the circuit board. Modern area array packages include ball grid arrays (BGAs), chip-scale package (CSPs), and flip chips (FCs). The early IBM solid logic technology (SLT) package developed in the 1960s, used for transistors at the time, is regarded as the very first area array package (Tsukada, 1992). It was not only a BGA but also a CSP and was the very first surface-mount technology (SMT) product (Ken Gilleo, 2002). It measured around 12.7 mm^2 and is shown in figure 2.1. Ball Grid Array (BGA) technology was first designed jointly by Motorola and Citizen in 1989. They have small conductive solder balls or columns that are soldered directly onto the surface of printed circuit boards as illustrated in Figure 1.2 of chapter 1.

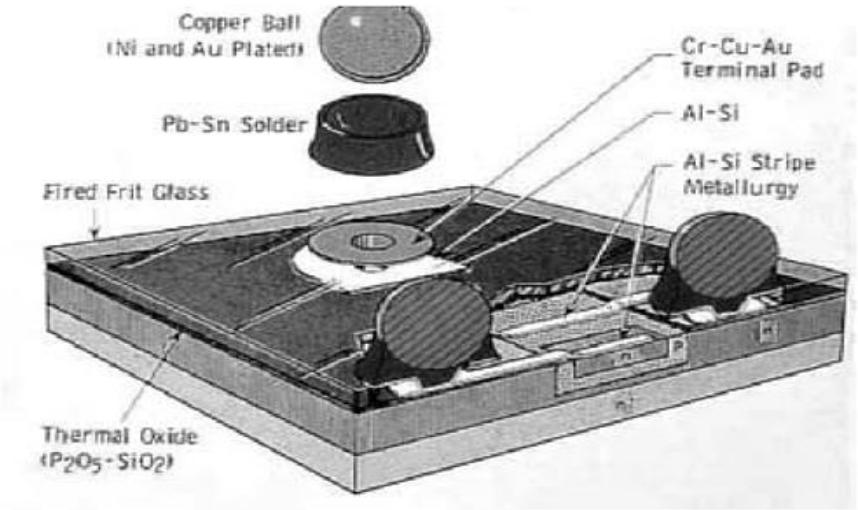


Figure 2.1: Solid logic technology (SLT). (IBM Corp.)

A BGA package can typically be characterized by the following three general statements **(**The Nordic Electronics Packaging Guideline, 2000):

1. It is an IC package for active devices intended for surface mount applications.
2. It is an area array package, i.e. utilizing whole or part of the device footprint for interconnections.
3. The interconnections are made of balls (spheres) of most often a solder alloy or sometimes other metals.
4. More specifically, the BGA package usually fulfils the following additional requirements:
    a. The length of the package body (most often square) ranges from 7 to 50 mm.
    b. Lead counts over 1000 possible, but 50 to 500 range most common around the millennium.
    c. The pitch, i.e centre-to-centre distance, of the balls is generally between 1.0 and 1.5 mm.

Based on industry needs, different types of BGA have been developed (Intel,2000). Some of them are: Moulded Array Process Ball Grid Array(MAPBGA), Plastic Ball Grid Array (PBGA), Thermally Enhanced Plastic Ball Grid Array (TEPBGA), Tape Ball Grid Array(TBGA), Package on Package (PoP) and MicroBGA.

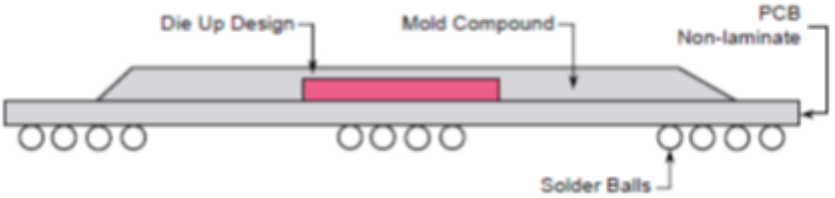


Figure 2.2: Die up cross section of a PBGA(Intel Packaging databook, 2000)

The basic construction of an area array device is illustrated in Figure 2.2. The base material of the package is formed from substrates such as alumina (ceramic material), glass reinforced epoxy based laminate such as FR-4 or FR-5 or polyimide flex-film. The substrate which provides a mounting structure for die attachment also functions as a compliant interposer between the silicon die in the package and the printed circuit board onto which the package is soldered.

Wire bonding was the traditional method for connecting die to substrate in the package, but with the emergence of flip chips, wire bonding has become less dominant. When flip chips are used to connect the die to substrate in a package it is referred to as flip chip in package (FCIP). Nowadays, both flip chip and wire bonds are used to connect die to a substrate such as flip chip ball grid array packages (FCBGA) (ITRS, 2009). Flip chip is also used in direct chip attachment (DCA) where the chip is mounted on the final printed circuit board, known as flip chip on board (FCOB) assembly. Figure 2.3 shows an example of FCIP and FCOB.

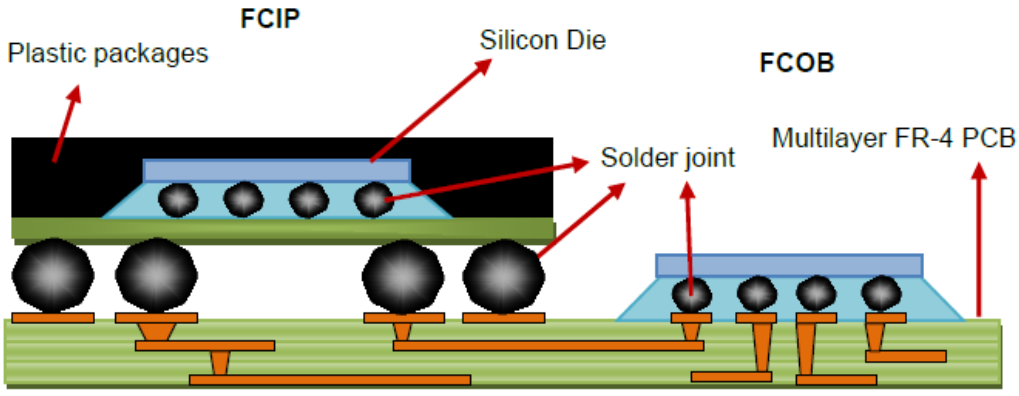


Figure 2.3: Flip chip in Package (FCIP) and flip chip on Board (FCOB). (Yang, 2012)

In flip chip assemblies, the silicon die is flipped over and the active surface is attached directly to a chip carrier, substrate or printed circuit board using soldering technologies

(Tummula and Rymaszewski, 1989; DeHaven and Dietz, 1994). As described in Tummula and Rymaszewski (1989), the flip chip assembly process, also known as Controlled Collapse Chip Connection or the C4 process invented by IBM, places solder bumps on a solder wettable metal pad on the active die surface. The chip is then 'flipped' and placed on a matching pad on the substrate, subsequently reflowed up to 365ºC peak temperature. During the reflow process, the solder bumps are self-aligned by surface tension forces. The shape and the wettable area of the solder bump are defined by under bump metallization (UBM). Finally, a liquid underfill is dispensed under the flip chip to fill the gap between the die and substrate to enhance the reliability performance. Figure 2.4 shows a schematic of a flip chip and its interconnect system.

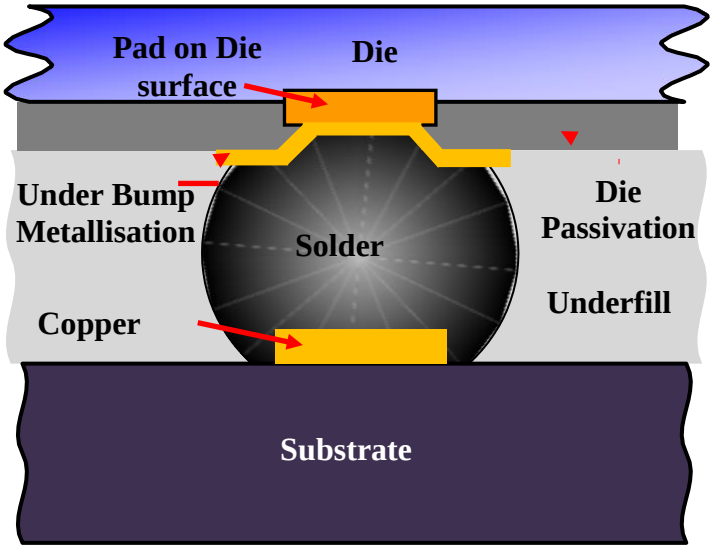


Figure 2.4: Schematic of a flip chip and its interconnect system (Yang, 2012)

The emergence of commercially used flip chip technologies can be traced back to the early 1960s when it was first introduced by IBM in main frame computers. In 1962, IBM used the flip chip process with ceramic substrates (Tummula and Rymaszewski, 1989). In the seventies, Delco Electronics (now part of Aptiv) introduced flip chips in automotive applications. Delphi Delco has employed FCOB technology into a broad product range for passenger compartment, under-hood and on engine applications (Witty *et al*., 1998; Li *et al*., 2000). Since then, flip chips have become very common in automotive applications. It is now widely used in many other sectors such as mobile phones, watches, disk drives, portable devices, LCD displays as well as electronic

hearing aids.

According to a market report published in the Herald Keeper (2011), the global flip chip Technologies market was estimated at USD 25.89 billion in 2015 and is poised to reach USD 57.04 billion by 2022, growing at a Compound Annual Growth Rate (CAGR) of 11.94% during the forecast period. Some of the major players in Flip Chip Technology market are Samsung Group (South Korea), Intel Corporation (U.S.), Global Foundries (U.S.), UMC (Taiwan), ASE, Inc. (Taiwan), Amkor Technology (U.S.), STATS ChipPAC (Singapore), Powertech Technology (Taiwan), and STMicroelectronics (Switzerland), Texas Instruments (U.S.) (Market Research Future, 2018). The popularity of flip chip in many application areas is motivated by several factors. For instance, increasing demands of compact, smaller and thinner die and packaging, increasing complexity in silicon and higher I/O counts, improved heat dissipation and reliable interconnects.

Flip chip assemblies offer a number of possible solutions due to the advantages summarized as follows (Riley, 2000; Vähäkangas *et al*., n.d.):

1) Smaller size – total package size can be reduced as no extra space is required for wire bonding, therefore reducing the package footprint, height and weight as well as increasing the wafer usage.
2) Increased functionality – use the die surface directly for die to substrate connections, it is not limited to the perimeter of the die thus can support relatively high numbers and flexible interconnections.
3) Improved performance – interconnect is much shorter in length, i.e. 0.1mm vs 1-5mm, delivering lower resistance, capacitance and inductances in signal paths. Therefore high speed communication and switching can be achieved. Moreover, power can be delivered more quickly, hence reducing power consumption and noise.
4) Improved thermal dissipation – the back side of the chip is not encapsulated, thus can be used as a thermal path for effective cooling.
5) Low cost – eliminating the use of gold wires in the package reduces the cost. Also, costs are reduced through efficiency in the manufacturing process, high volume automated production, and through the development of new bumping and underfill processes.

6) Reliability – Flip chip is a highly reliable interconnect method, together with an epoxy underfill can survive millions of cumulative hours of use.

Just like many other technologies, flip chip technology also has its challenges. The legislative enforcement of the Restriction of the Use of Certain Hazardous Substances (RoHS) in Electrical and Electronic Equipment (NMO, 2006) called for the elimination of the use of lead (Pb) in solder joints in electronic packages. This has led to the use of unfamiliar lead free solder materials in flip chips as well. One example of a lead free solder joint is the SnAgCu or SAC joint. These restrictions and developments in flip chip technology are thereby introducing new reliability challenges especially in harsh operating environments like automotive applications (Witty *et al*., 1998, Braden, 2010, M. Bâzu, 2012). Also, the shift away from using conventional Sn-Pb solder in favour of lead-free Sn-Ag-Cu solder on the mounted parts is well under way, and the test standards for reliability were not yet clearly defined (Yuichi Aoki, 2001).

There are many factors affecting the reliability of the flip chips like thermo- mechanical mismatch, mechanical loading and creep, delamination and voids in underfill during processing. Full package failure modes can be found in ITRS (2009). Among the issues, fatigue failure led by thermo-mechanical mismatch is the most critical issue that cannot be prevented. The cyclic fatigue failure during thermal cycling is unavoidable especially in irregular operating conditions. It is caused by large coefficient of thermal expansion (CTE) differences between a silicon die and substrate/PCB. During temperature cycling, the materials expand and contract at a rate based on the differing CTE of the materials as shown in Figure 2.5.

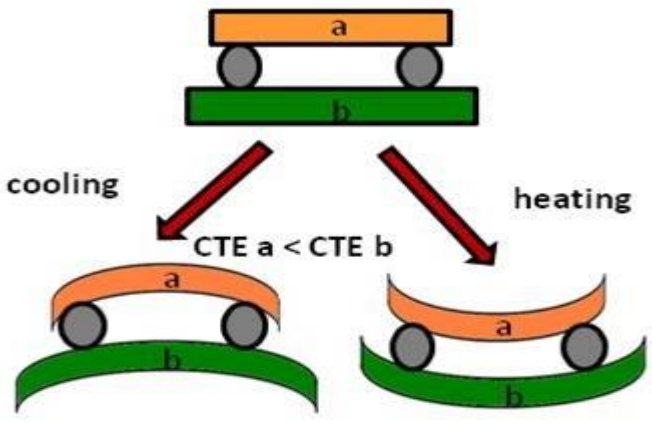


Figure 2.5: Plastic deformation during thermal cycling (Yang, 2012)

The reason for the thermal expansion is because the particles in a material vibrate more and produce a greater atomic spacing. The difference in the expansion rate imposes a thermo-mechanical stress on the solder joint between the die and substrate (Pang *et al*., 2001). When the shear stress applied exceeds the fracture toughness of the solder alloy, cracks nucleate and propagate at the bonding interface and cause a fatigue failure (Lau, 1996). Once a fracture occurs, the load or fatigue damage is moved to adjacent joints and causes fracture propagation within joints.

Generally, electronics packages often operate under different environmental conditions. Field failures related to the operating environments of electronic equipment reveal that about fifty-five percent of failures are due to high temperature and temperature cycling, twenty percent are related to vibration and shock, and another twenty percent are due to humidity (Steinberg, 2000). An extreme example of thermal variation is that of cyclic thermal excursions in the automobile engine compartment. During this thermal cycling, the CTE mismatch between the substrate and PCB causes solder joints to deform by applying a shear stress to the solder joint. The solder joint fatigue could occur after hundreds or thousands of cycles which could require 10 or 20 years of usage. Therefore, accelerated testing is commonly used to generate rapid ageing of the components so that the effects of ageing or solder joint fatigue can be studied in a shorter period of time. The function of accelerated testing is widely recognized. As described in Engelmaier (1989), the two primary purposes for accelerated testing are firstly, to obtain a measurement of long term solder joint reliability and secondly to provide a process verification and product validation test. Additionally, vibration loading, particularly, in cases of harsh operating conditions such as aerospace, military and automobiles (Nishi, 1979) is another leading cause of solder joint failure.

2.2 Vibration cycling

As was discussed in section 1.1 of chapter 1, vibration loading was identified to be one of the most important causes of electronic failure by the US Air force (Steinberg, 2000). The American Air Force discovered that about 20% of the electronic equipment would fail under a vibration and shock environment (F. Liu, 2014). An extreme example of such a case is the Indonesia Air Asia flight A320 crash that occurred in December 2014. Indonesia's National Transportation Safety Committee later revealed that the crash that led to the death of all 162 aboard was triggered by a cracked solder joint on the plane's

rudder control warning system (Buetow, 2015). In addition to harsh operating conditions, electronic systems also experience vibration loading during shipping and handling (Suhir, 2011). Despite this, vibration loading in electronics is a lesser researched topic as compared to thermal cycling the reasons for which have already been discussed in detail in section 1.1 of chapter 1.

Typically, in vibration testing, the test samples are mounted into fixtures specially designed for testing. The fixture along with the sample is then vibrated in a vibration chamber using a suitable vibration profile to monitor its reliability and life time until complete mechanical failure.

As discussed in detail in section 1.2 of Chapter 1, the vibration profiles may be (Delphi, 2013):

1. Broadband random vibration: In this method, the test sample is exposed to a non-periodic motion or random motion where all the frequencies within the test band are present. Because a Random Vibration signal is essentially shaped white noise, it is most commonly quantified statistically. Random Vibration inputs and responses are typically represented as a power spectral density (PSD) plot with magnitude expressed in squared acceleration units per hertz (G^2/Hz) on the Y axis and frequency (Hz) on the X axis. Figure 2.6 shows a typical random profile.

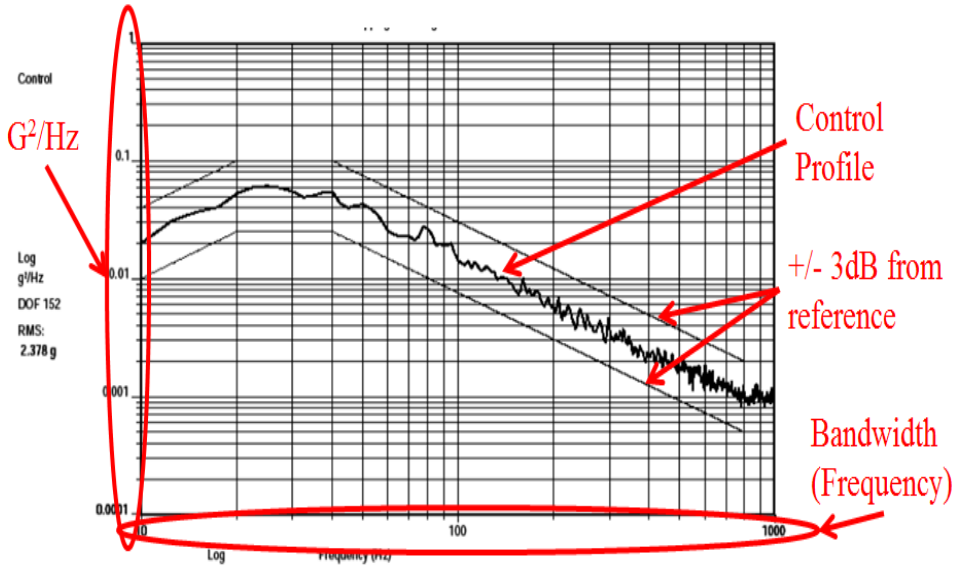


Figure 2.6: A typical random vibration test profile (Delphi)

Root Mean Square (RMS) acceleration levels are related to the area under the PSD

curve and can be obtained by integrating under this curve. The square root of the area then determines the RMS acceleration level, G_{RMS} :

$$\sqrt{area} = \sqrt{\frac{G^2}{Hz} xHz} = \sqrt{G^2} = G_{RMS} \qquad \text{Eq. 2-1}$$

2. Swept Sinusoidal Vibration: This method involves exposing the sample to a periodic sine motion that at any moment has a single frequency at defined acceleration, displacement or velocity level. Figure 2.7 shows a swept sinusoidal profile.

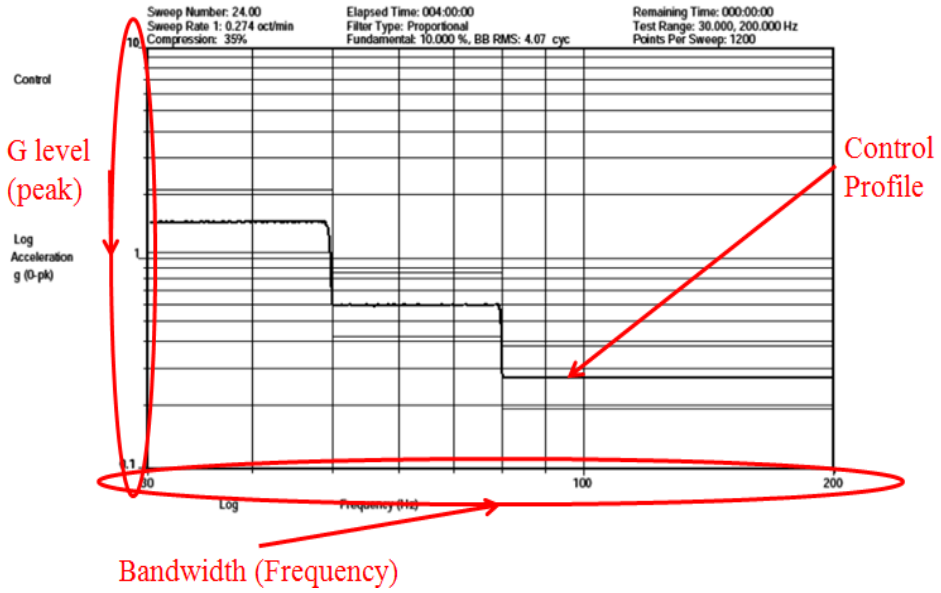


Figure 2.7: A typical swept sinusoidal vibration test profile (Delphi)

3. Sine-on-Random: The lab simulation of the sine-on-random environment is performed by superimposing the swept sinusoid on the broadband random signal. The two modes are run simultaneously and for the same duration. If test equipment limitations prevent this mixed mode approach, the sine and random can be performed separately as long as the same test samples are used. Figure 2.8 shows the sine on random profile.

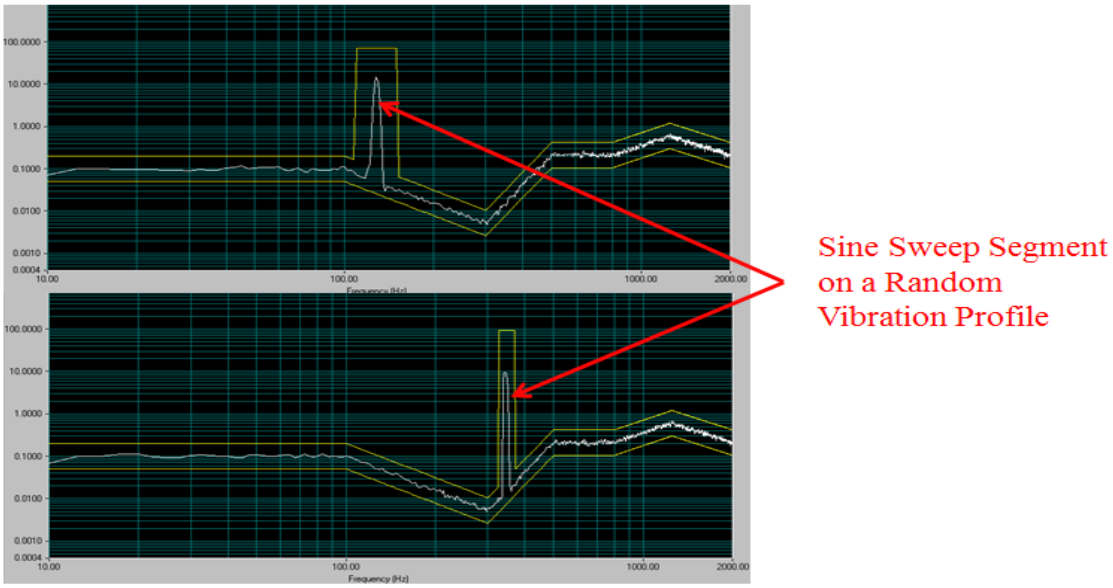


Figure 2.8: A typical sine on random vibration test profile (Delphi)

4. Long Waveform Replication: It involves capturing a dynamic event such as vibration input to a radio while the vehicle traverses rumble strips. It is not used for reliability testing.

While thermal cycling induces low cycle fatigue on the electronic components, vibration cycling induces high cycle fatigue (HCF) (Sissa et al, 2014) (Kim et al., 2006). The majority of material failure data that exists for solders and components is principally concerned with thermal failures and there is relatively little data relevant to vibration induced failure or HCF (Aglietti, 2002). YB Kim (Kim et al. 2006) studied the high cycle vibration fatigue life characteristics of SnPb and Pb-free solder joints under various mixed mode stresses by a torsion fatigue machine. Yang (Yang et al. 2002) adopted the out-of-plane sweep sinusoidal vibration test to assess the reliability of a plastic BGA (PBGA) assembly against vibration fatigue. Chen (Chen et al. 2008), Pang (Pang et al. 2004) and Che (Che and Pang, 2009) carried out the reliability test of sinusoidal vibration for PBGA and flip chip solder joints, and applied the linear cumulative damage analysis method (Miner's rule) to predict the life of solder joints. High cycle vibration tests were conducted at different strain levels and frequencies for BGA packages. Wang and Guo (Wang et al. 2004; Guo et al. 2005) investigated the narrow- band random vibration fatigue failure of PBGA and flip chip BGA. Liu and Wu (Liu et al.2006 ;Wu 2009) studied the high cycle vibration fatigue life of BGA

solder joints. All these research was aimed at the vibration reliability of SnPb solder joints. Zhou (Zhou Y, Bassyiouni 2009; Zhou Y, Plaza G, 2009; Zhou Y, Al-Bassyiouni M, Dasgupta 2010) compared the vibration reliability between SnPb and Pb-free solder joints under harmonic excitation and broad-band random vibration excitation. Some researchers like P. Yang (Yang, 2009), Yu (Yu D , 2011) and Han (Han CW, 2011) also investigated the life prediction model under random vibration. Zhou (Zhou B, 2011) studied the effect of voids and pad type on the maximum vibration stress of solder under vibration loading including swept vibration and random vibration (F.Liu, 2014).

Another problem that has been scarcely researched is the effect of simultaneous vibration and temperature cycling test on solder joints referred to as mixed testing. Mattila (Mattila et al. 2012) found that temperature has an important impact on solder joint reliability during drop tests for different packaging design. The mean lifetime for WL-CSP packaging component increased when temperature increased in steps as; (23, 75, 100, 125 ºC).Zhang, Liu and Wang (Zhang et al. 2015) in their paper conducted a combined test of temperature and vibration to statistically analyse the influence of temperature on lifetime and failure of SAC305 solder joint subjected to random vibration. They found vibration resistance of solder joint is greatly improved with temperature increase. The mean lifetime of solder joints at 65 ºC and 105 ºC was increased by 70% and 174 % respectively compared to that of solder joint at room temperature, 25 ºC. In 2018, Tong (Tong An, 2018) studied the failure of Sn37Pb PBGA solder joints using temperature cycling, random vibration and combined temperature and random cycling. It was found that simultaneous application of temperature and vibration cycling significantly reduced the fatigue life of solder joints. Samativan (Samativan et al. 2019) studied the effects of directional random vibration on solder joints in a power module. It was concluded from a simulation study, that the fatigue evolution in a solder joint under normal loading at a perpendicular direction proceeded slower than other loading directions.

While real FCs with over hundred solder joints have been investigated in this work, many related works on vibration loading such as those by T. Eckert (Eckert, 2009) studied only four solder joints per FC while Hunt (Hunt, 2008) only investigated one solder joint. Hence, the test setup of this work is industrially more realistic and relevant compared to other experimental set ups that involved smaller number of solder joints.

2.3 Inspection Techniques

Environmental testing methods like ATC or vibration loading are always used in conjunction with certain inspection techniques in order to monitor the reliability of electronic devices. This is because ATC or vibration cycling tests are only the medium to reciprocate the degradation incurred by the device or components in their life time. In order to quantify the health and hence, reliability of the components, or locate defects in the devices, certain parameters such as resistance, stress and strain need to be monitored. This is done with inspection techniques. Inspection techniques can be of two types – destructive and non-destructive. If the inspection technique involves cutting or damaging the device then it is termed as destructive testing. However, if the device is inspected without damaging it, then it is termed as non- destructive testing or NDT. NDT was first used in the 1990s (Nab et al. 1991; Masnata, 1996).. It was used to classify defects, with the ability to monitor electronics throughout their life time. Inspection techniques can be used either individually or simultaneously depending on the types of defect or failure. Some common non-destructive inspection techniques are reviewed in the following subsection.

2.3.1 Electrical Testing

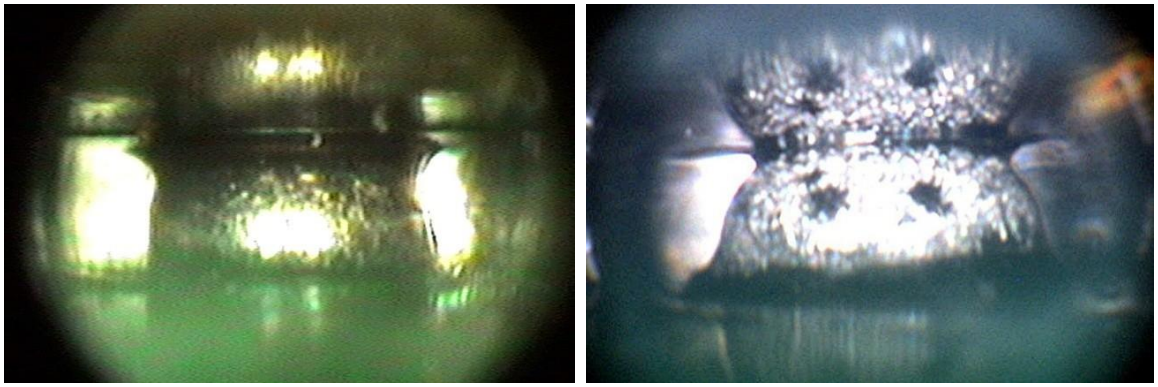
Electrical testing can be used in either conventional functional testing of the end product or monitoring certain test points and circuits on the chip (Burdett *et al*., 1989). For monitoring purposes, during environmental testing the electrical continuity is monitored or alternatively, the resistance of the connected solder joint is measured. Whenever a fracture occurs in a solder joint, its resistance will increase dramatically thus indicating a crack initiation. However, as the fractured solder joint may still remain in contact with the substrate the electrical indications of failure can be intermittent (Engelmaier, n.d.).

According to the IPC-9701A standards (IPC, 2006), the solder joint failure manifests itself electrically only during the shear loading caused by thermal changes. According to the standard, a solder joint is electrically failed only when the resistance spikes higher than 1000 ohms and last for a period greater than 1 microsecond (Pan, 2014). Therefore the monitoring needs to be continuous throughout the environmental cycling as intermittent faults will more likely occur at transient transition periods.

2.3.2 Optical Inspection

Optical inspection or visual inspection is commonly used for solder joint inspection. The images obtained enable direct inspection that can be easily interpreted as no difficult physical formulas are needed to translate the information into an image. The advantages of optical inspection are the capability of inspecting the completeness of the assembly, the position and orientation of all components, the shape and the surface appearance of the solder (Gnieser and Tutsch, 2011). A standard optical inspection system includes an electronic camera, illumination source, imaging optics and image processor. Optical inspection is available in both 2D and 3D systems. A 2D system captures a single image for evaluation, whereas a 3D system uses laser triangulation (Dorsch *et al*., 1994) to construct the 3D image. Optical inspection is often associated with digital image processing and artificial intelligence systems for automatic inspection, known as automated optical inspection (AOI). For instance, Acciani *et al*. (2006) extracted the wavelet properties and geometrical characteristics from an optical solder joint image via image processing techniques, and fed this into a neural network based defect classification system to locate and classify the defects automatically.

Optical microscopy and endoscopy are two typical optical inspection tools in solder joint inspection. Optical microscopy is limited to only packaging types where the solder joint can be inspected visually, e.g. SOIC (Small-outline integrated circuit) and QFP (Quad flat package). Endoscopic inspection, adopted from medical instrument technology gained popularity when commercial endoscopic systems became available, e.g Ersascope-2 (Chan *et al*., 2000) and Optilia Digital BGA Inspection System (Optilia, n.d.). The endoscopy inspection system places the micro-endoscopic optics with the deflecting prism down to the board and chip level to capture the image. The illumination source can be either placed at the other side of the chip or at the same side as the endoscopic optics depending on the desired inspection task. The example of a single flip chip solder joint inspected by an endoscopy system is depicted in Figure 2.9.



(a) **(b)**

Figure 2.9: Flip chip solder joint image from Endoscopy inspection (a) good solder joint (b) cold solder joint (Image courtesy of Kurtz Ersa Corporation)

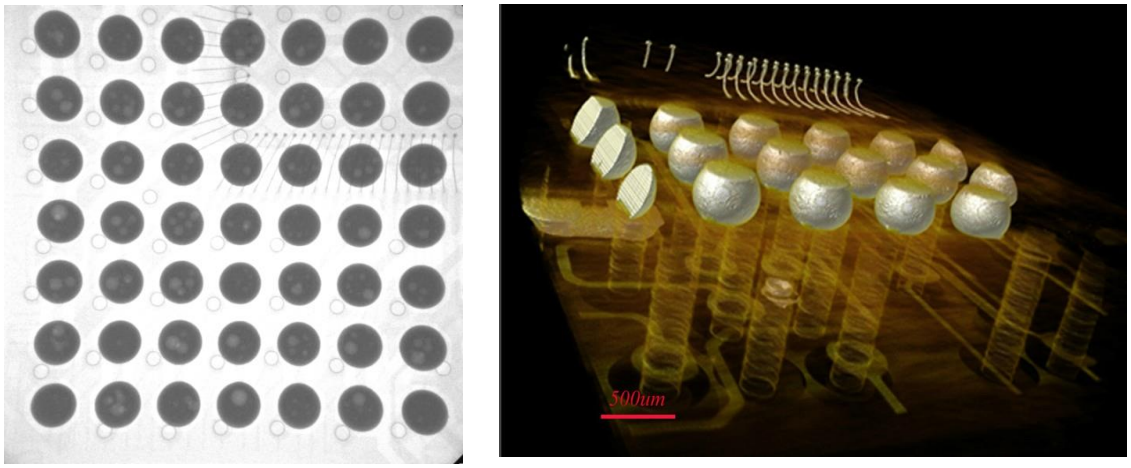
The endoscopic system can have a magnification up to 700 times and is able to inspect through a gap of approximately 30µm (Kurtz Ersa Corporation, n.d.). The system can be used in flip chip solder joint inspection. However, the application of endoscopy optical inspection is limited to the peripheral column of the chip as the light beam is blocked by the outer rows of solder joints. It is also not suitable for inspecting flip chips with underfill and defects inside the solder joints such as voids.

2.3.3 X-ray

X-ray inspection is a powerful inspection tool for revealing the internal structure of flip chips and other electronic packages. X-rays are a form of electro-magnetic energy with wavelengths of 10 to 0.01 nanometres and energy range typically of 120eV to 150keV. Due to their short wavelength and high energy level, X-rays can penetrate an object and do not reflect or refract easily. When x-rays pass through materials, they experience a variety of scattering interactions. These interactions lead to energy attenuation and the resulting energy is detected by an image intensifier. The images are then directed to a Charge Coupled Device (CCD), processed and displayed on a screen. X-ray imaging is a contrast imaging technique where high density materials lead to higher attenuation and produce a darker image than those with less density or thickness.

Two basic X-ray imaging systems are currently used in the electronics industry: Conventional 2D x-ray systems are the most cost effective systems available, and 3D computed tomography (CT) systems, which can reconstruct hundreds of 2D X-ray

images into 3D volumetric data. A 3D CT system is useful in inspecting inner defects because the 3D data can be visualized from any angle. Moreover, X-ray virtual cross-sectional images allow the product to be inspected layer by layer. Figure 2.10 show examples of 2D and 3D X-ray images of solder joints. The conventional 2D x-ray is a useful tool to inspect for volumetric defects such as voids, solder bridging and missing solder balls. However, due to the high level of interfering features typically in the field of view such as multilayer interconnects, fatigue cracking and non-wetting solder joints, detection present significant challenges to 2D X-ray inspection (Pacheco and Goyal, 2008).



(a) **(b)**

Figure 2.10: (a) 2D image of solder joints, (b) 3D image of solder joints (Image Courtesy of xRadia Inc.)

Though 3D X-ray CT systems are able to overcome some 2D limitations, they have several technical challenges that limit usage in monitoring the fatigued solder joint. A typical 3D X-ray of a flip chip can take up to 12 hours. Also the data acquisition and reconstruction time are greatly dependent on the sample size and image quality. For example, in order to obtain the virtual cross section and plane view of a flip chip solder joint, a $6cm^2$ sample required a data collection time of 60 minutes per corner for a reconstruction data set of $2mm^2$ (Pacheco and Goyal, 2011). As a result, the size limitation and long data acquisition and reconstruction throughput time remain a challenge in monitoring the end product reliability for through-life testing.

2.3.4 Laser Ultrasound

Laser ultrasound inspection techniques (Liu *et al*., 2001; Zhang *et al*., 2006; Yang and Ume, 2010) use a pulsed Nd: YAG (neodymium-doped yttrium aluminium garnet) laser as an excitation source to induce ultrasound on the chip surface in the thermoelastic regime. The interaction between electromagnetic radiation and atoms near the surface generates heat and causes thermal elastic expansion, thus generating acoustic waves. The transient out-of-plane displacement response due to ultrasonic arrival (or structural vibration response) is then measured by a laser Doppler vibrometer. The displacement response reacts differently when there are abnormal solder joints lying under the measurement points (Liu *et al.* 2001). Therefore, comparison of the transient responses of the tested electronic packages and known good packages is performed, using signal processing analysis to verify the solder joint defects. Liu (Liu *et al.* 2001) measured the Error Ratio (ER) between a reference signal and test chip signal to confirm the defects. Zhang (Zhang, *et al*. 2006) used correlation coefficient analysis between the responded laser ultrasound signals and reference signals to evaluate the solder joint defects. Spectral analysis and frequency domain based FFT analysis were carried out in Liu and Ume, (2002b and 2003) respectively. Defect pattern recognition using laser ultrasound transient responses have also been developed and reported in Liu and Ume (2002a).

Solder joint defects such as cracks, missing or misaligned solder joints in flip chip, chip scale packages and land grid array packages can be detected by analysing the ultrasound response signal from a laser ultrasound system. However, if the defect features are more prominent in a specific frequency range, the sensitivity of the detection is compromised. Although laser ultrasound inspection techniques are helpful in examining the existence of solder joint defects, they do not give sufficient and detailed information about each solder joint's crack propagation and initiation (Howard *et al*., 2002).

2.3.5 Acoustic Micro Imaging

Acoustic Micro Imaging (AMI) is another non-destructive inspection technique used to reveal the internal structure of electronics packages that is extensively used during the failure analysis process. AMI inspection is often used in detecting gap-type defects such as voids, delamination, disbands and cracks due to the strong reflection of ultrasound in

solid air interfaces (Zhang *et al*., 2006). For example, it was used to detect BGA cracks and delaminations (Semmens *et al*., 1996) and to evaluate the quality of flip chip attachment like voids in the underfill and solder joint cracks (Semmens and Lawrence 1997). It was also used in inspecting multilayer thick film structures (Harsanyi, 2000) and stack die packages (Semmens, 2005). Section 2.4 discusses AMI in detail.

2.4 Acoustic Micro Imaging

Acoustic Micro Imaging (AMI) technique, also known as Scanning Acoustic Microscopy (SAM) makes use of the properties of ultrasonic waves to 'look' inside objects and reveal the defects non-destructively. Ultrasound waves are mechanical waves that transport energy through oscillations of discrete particles in solids, liquids or air. There are two commonly used ultrasound waves: *longitudinal waves and transverse waves*. Longitudinal waves, also known as compression waves, propagate in the same direction as the particle motion, whereas transverse waves, or shear waves propagate in a direction perpendicular to the particle motion. Since transverse waves are unable to transmit in liquids and gases, longitudinal waves are usually used in AMI applications. The typical frequency range of AMI is 5MHz to 2GHz as shown in Figure 2.11.

The ultrasonic waves are usually generated by a piezoelectric transducer from which they travel and pass through a test object. Once the waves are inside the sample, the ultrasound signal is reflected, scattered or absorbed depending on the material's acoustic characteristics. This phenomenon is illustrated in Figure 2.12.

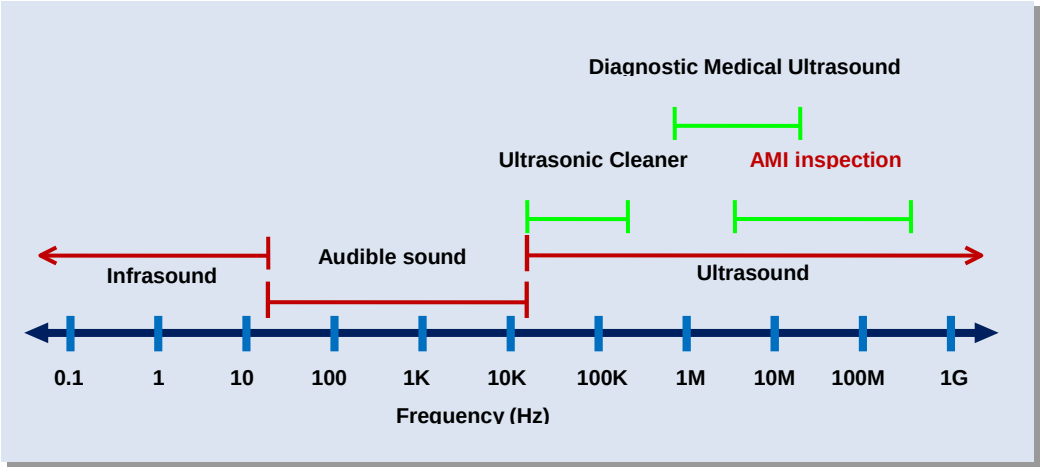


Figure 2.11: Frequency spectrum of sound (Sonoscan, n.d.))

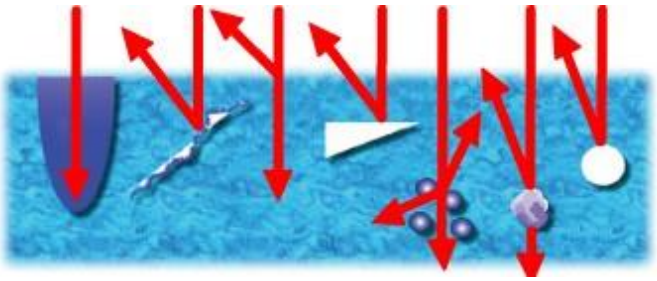


Figure 2.12: Reaction of ultrasound waves in an object (Image Courtesy of Sonoscan Inc.)

The acoustic properties of a material are measured by its acoustic impedance; *Z*. *Z* is defined as the product of the material's density, ρ and its ultrasonic velocity, *V*.

$$Z = \rho V \qquad \text{Eq. 2-2}$$

$$V = f\,\lambda \qquad \text{Eq. 2-3}$$

where f is frequency and λ is the wavelength of the ultrasound wave.

The acoustic impedance of typical electronic packaging material is illustrated in Table 2-1.

Table 2-1: Acoustic impedance of common electronic packaging material (Sonoscan n.d)

Material	Longitudinal Velocity (m/s×10^3)	Density (kg/m^3×10^3)	Acoustic Impedance (kg/sm^2×10^6)
Air	0.35	0.00118	0.0004
Water	1.48	1.0	1.48
Glass silica	5.9	2.2	13
Aluminium	10.52	3.86	40.6
Silicon	8.43	2.34	19.7
Silver	3.6	10.6	38
Copper	5.01	8.93	44.6
Gold	3.24	19.7	63.8

Tungsten	5.2	19.4	101.0
Tin	3.3	7.3	24.2
Lead	2.2	11.2	24.6
Zinc	4.2	7.0	29.6

When scanning a test object with two materials, the amount of reflected and transmitted energy at the boundary of the materials is determined by their acoustic impedances. The reflected and transmitted energy on the interface at normal incidence can be calculated by the following equations:

$$S_R = S_{in} \frac{Z_2 - Z_1}{Z_2 + Z_1} \quad \text{Eq. 2.4}$$

$$S_T = S_{in} \frac{2Z_2}{Z_2 + Z_1} \quad \text{Eq. 2.5}$$

where S_{in} is the amplitude of the incident pulse at the interface, S_R is the amplitude of the reflection signal and S_T is the amplitude of the transmitted signal. Z_1 and Z_2 are the acoustic impedances of top and bottom materials respectively. S_R and S_T are fractional amounts of the incident pulse and therefore the summation of the reflection and transmission signal is equal to the incident pulse S_{in}. The reflected or transmitted waves are detected by a receiving transducer, analysed and subsequently an ultrasound image is generated.

Generally, two imaging modes are used in AMI, Pulse-Echo and Through-Transmission. In pulse-echo mode, the same ultrasonic transducer is used to transmit the excitation waves and receive the reflected waves. In through-transmission mode an AMI pulse is sent through the entire sample and is received by a separate transducer that lies underneath the sample. Different imaging modes provide different inspection capability. Pulse-echo mode is preferable in electronic package inspection due to its capability of displaying features at various levels in the same package. In an electronic package inspection, the ultrasound is pulsed into the sample, the wave travels downwards until it encounters an interface of dissimilar materials, for instance, the die to solder bump interface, where a portion of signal is reflected back to the transducer and the rest

continues to travel deeper into the sample. By gating the return echoes at the level of interest and capturing the reflection strength of the signal, an ultrasonic grey scale image can be generated. As shown in Table 2-1, the acoustic impedance of air (0.0004) is far smaller than a solid, thus the incident pulse is almost fully reflected at a solid-air interface. Therefore, gap type defects such as voids, delamination and cracks appear as bright spots compared to the surrounding areas in an acoustic/ultrasound image and can be easily detected.

On the other hand, through-transmission mode images are made by recording the ultrasonic energy transmitted through the entire package. Any defects in the sample that block the energy will appear as a dark feature in the image. Thus, it is used mainly in verifying and evaluating packages rather than locating a defect position. Ultrasound inspection can also be used in material characterisation and dimensional measurement by calculating the time of flight (TOF) and the reflection behaviour. Time of flight (TOF) is the time taken for an acoustic pulse to travel a distance through a medium. It is often used to estimate the distance or the depth of the defects if the velocity of the wave is known.

Figure 2.13 shows the basic principle of AMI inspection in flip chip packages. The transducer lens is immersed in de-ionised water, and is positioned where the transducer focus point falls on the desired sample depth or interface. The desired depth can be focused by moving the transducer up and down in the z-direction. The echo of a particular depth reaches its maximum when the particular depth is said to be highly focused. De-ionised water is normally used as a coupling medium to transmit ultrasound but other liquids can be used. The reflected ultrasound signal contains multiple echoes representing different interface layers in a flip chip package sample as shown in Figure 2.13. The acoustic waveform consisting of reflected echoes acquired at a single x-y point is known as an A-scan signal. An A-scan carries arrival time, amplitude and polarity (phase) information of each acoustic echo that forms a foundation to generate images. The x- axis of an A-scan can show the time of flight information or the depth information. The y-axis is the signal amplitude and polarity information. In the waveform shown in Figure 2.13, the first echo is known as the ‘main bang’ caused by the electrical excitation in the transducer. A second echo is the sensed reflection of the sample surface. The third echo and fourth echo is the reflection from the chip-to-bump

interface and bump-to-board interface respectively. Since the PCB material has lower acoustic impedance than the solder material, the polarity of the echo is in opposite direction. In order to construct an image for a particular depth or interface, an electronic gate is applied to select the specific echo and eliminate all others. There are multiple electronic gates available in the Sonoscan AMI system (Sonoscan et.al). Figure 2.14a shows two of them are represented in two green bars and two red bars. Only signals bounded by the gate at the particular x-y plane are used to create an interface scan image. After a gate is set, a 2D scan over the surface plane of interest begins with pulsing and receiving of ultrasound signal thousands of times per second.

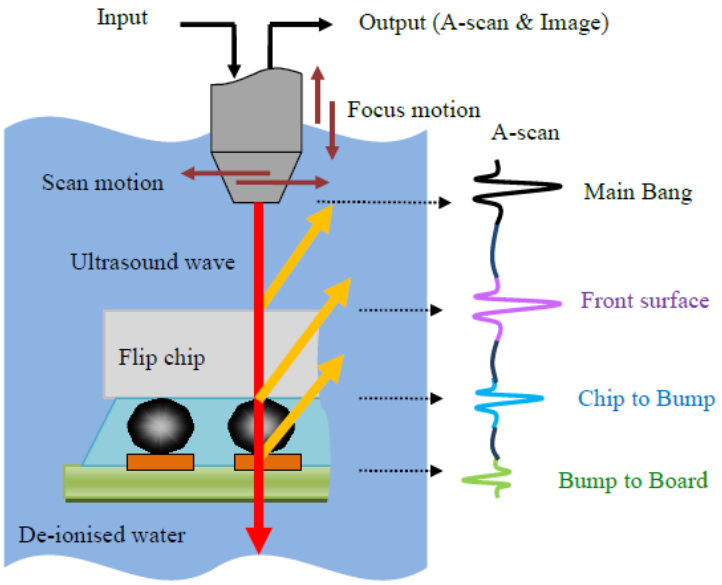


Figure 2.13: Basic principle of ultrasound imaging

AMI scanning involves a mechanical scan by moving the transducer back and forth rapidly in a linear motion. The transducer emits a pulse and receives the reflected signal while in the scanning motion, thus positional accuracy and stability is crucial in order to maintain the coherence of receiving signal with respect to the particular x-y point. The x-, y-, z-dimensions must be accurate and precise in order to obtain the required resolution and maintain the validity of the information. AMI scanning is controlled by a high precision coordinated position control and a null inertia scanning mechanism developed by Sonoscan Inc. (Cichanski, 1988). The null inertia scanning mechanism can eliminate the vibration due to the acceleration of the motion and the weight of the transducer. This mechanism adds a counterweight to neutralise the momentum and

inertia while the transducer is in motion, and thus obtains high positional accuracy and precision.

A typical AMI scan pattern is demonstrated in Figure 2.14b. This enables 2D images of layers of interest to be acquired. This x-y scanning pattern is known as C- scan mode, with an example image shown in Figure 2.14c. C-scan detects the peak value of the gated signal segments. The amplitude differences of the peak values at different x-y points produce a grey scale image.

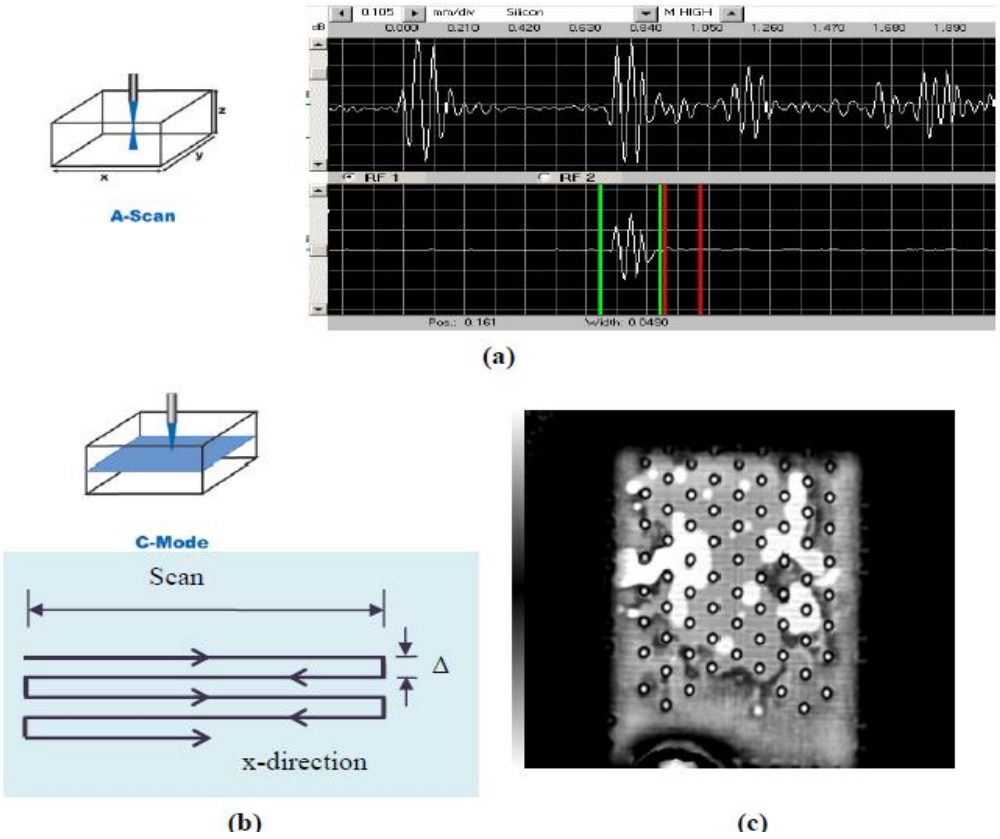


Figure 2.14: Scanning mode, (a) A-scan, (b) Typical C-scan scanning pattern, (c) C-scan image of underfill voids in the flip chip

Pseudo-colour maps are often employed in the image to provide a clearer vision of the defects. C-scan images are helpful in detecting interface delamination, underfill voids and solder joint cracks.

In C-scan mode, the system displays the image as a final output, and discards all other signal information. There is another powerful scanning mode in AMI which records all signal information developed by Sonoscan Inc. known as the Virtual Rescanning Mode

(VRM). This VRM scans the sample at every x, y and z coordinate. It collects A-scan signals at every coordinate which is stored as 3D acoustic data. The digitally stored 3D acoustic data can be recalled and virtually reconstructed using A-scan signals, B-scan and C- scan ultrasound images without the presence of the sample. The data can then be further processed to generate acoustic frequency domain images (FAMI) (Semmens and Kessler, 2002) and acoustic time-frequency domain images (TFDAMI) (Zhang *et al*., 2010b) and 3D AMI (Baishya et. al. 2016). By selecting different frequency ranges or different time-frequency information, images with higher resolutions can be achieved and more information can be unravelled.

2.4.1 AMI Sensitivity and Resolution

Sensitivity is the ability to detect the amplitude of the reflected signal of small discontinuities at a given depth, thus it refers to how small a defect will be detected. On the other hand, resolution refers to the ability of the ultrasound to distinguish two discontinuities that are close together both in the axial and lateral directions. Sensitivity and resolution of AMI inspection are determined by several factors such as the frequency of transducer, focal length, frequency attenuation and fluid path. The beam diameter ΔX of a transducer is given by (Kino, 1987):

$$\Delta X = 1.22N\lambda \qquad \text{Eq. 2-6}$$

Where ΔX is the transducer beam diameter, λ is the wavelength of the ultrasound, N is the depth of focus achieved by the lens, and is determined by the lens diameter, D and its focal length, F (Sonoscan, 2002):

$$N = \frac{F}{D} \qquad \text{Eq. 2-7}$$

N or the depth of focus is used to exhibit the beam focusing characteristic, for instance, if N for two transducers are identical, the transducer will have similar resolution and depth of field if they have the same centre frequency. The depth of field, ΔZ which is the starting and ending points of the focal zone is given by the following:

$$\Delta Z = 7.1 \times (N)^2\lambda \qquad \text{Eq. 2-8}$$

Resolution in an AMI system is known as the ability of the ultrasound to distinguish two objects and interfaces (Semmens, 2000). It can be further divided into two categories: *axial resolution and lateral resolution*.

Axial resolution refers to the ability to separate echoes from two discontinuities close together located at different depths, whereas lateral resolution is the ability to distinguish two points side by side in the direction perpendicular to the ultrasound beam. Axial resolution is crucial to inspection, because if the second echo arrives at the receiver before the first echo dies out sufficiently, the second echo would interfere with the first echo and lead to distorted information. For example, if a low resolution frequency in the range of 10Hz to 50Hz is used in a thin structure, the echo from the defects in a solder joint will overlap with the neighbouring interface echo, hence producing a contaminated image in the C-scan and probably showing false defects during an inspection. The axial resolution is measured by the width of the acoustic pulse. Since frequency is inversely proportional to the wavelength (or pulse width), higher frequencies have a shorter pulse length, thus achieve better axial resolution.

In pulse echo mode, the ultrasound travels until it encounters an object where a portion of the pulse is reflected back to the transducer, the total travelling time observed in the A-scan is twice the distance. If the velocity of sound propagation, v is known, the time difference, t between two echoes is depicted as follows:

$$t = \frac{2d}{v} \qquad \text{Eq. 2-9}$$

where d is the distance between two interfaces and v is the velocity of the ultrasound in a material. The echo time duration, D_t is often equal to three half cycles of a sine wave at the transducer frequency, f and can be expressed as follows:

$$D_t = \frac{3}{2f} \qquad \text{Eq. 2-10}$$

In order to prevent the merging of two echoes, the minimum time separation must not exceed the echo time duration. Therefore, the maximum axial resolution can be

estimated when the time separation between echoes is equal to the pulse time duration ($t = D_t$):

$$d_{axial} = \frac{3v}{4f} \quad \text{Eq. 2-11}$$

Eq. 2-11 shows that the relationship of the distance between two interfaces and transducer frequency is inversely proportional. Therefore the higher the frequency, the shorter the distance between interfaces that can be resolved. However, it should be noted other variables such as transducer design will also affect the resolution.

In contrast to axial resolution, lateral resolution refers to resolution in the x-y direction of the sample plane. Lateral resolution is dependent on the width of the beam and the depth of focus during the inspection. If two objects are separated by less than the beam width, the objects will be detected by one single pulse which causes missing data, as two objects will then appear as one object. According to the Rayleigh Criterion (Kino, 1987), in pulse echo mode two objects are said to be resolved when their separation, $d_{lateral}$ is equal to the following:

$$d_{lateral} = \frac{1}{\sqrt{2}} \times \Delta X \quad \text{Eq. 2-12}$$

where ΔX is the beam diameter given by Eq. 2-6. Hence, the estimated lateral resolution can be re-written as a function of frequency by substituting Eq. 2-6 and Eq. 2-7 into Eq. 2-12.

$$d_{lateral} = \frac{1}{\sqrt{2}} \times 1.22 \times \frac{F}{D} \times \frac{v}{f} \quad \text{Eq. 2-13}$$

Again, as seen from Eq. 2-12, the resolution is inversely proportional to the frequency. Therefore, similarly to axial resolution, higher ultrasound frequencies achieve higher lateral resolution.

Beside the ultrasound resolution capability, the quality of the inspection is also reliant on the image resolution. The image resolution must be able to resolve the defect

dimensions. Hence, the sampling interval must follow the Nyquist theorem, which means the sampling interval should be at least half of the dimension to be resolved. For example, to resolve a defect size of 10μm, the pixel size should be no greater than 5μm. Generally, the minimum number of pixels required can be calculated by dividing the scan size in x-dimension by the transducer spot size, i.e.:

$$Pixel\ density\ = \frac{Scan\ size}{Transducer\ spot\ size} \qquad \text{Eq. 2-13}$$

For example, assume a scan size of 9100μm (x-dimension) is used to scan a flip chip with a transducer spot size of 16μm. The minimum number of pixels required in the x-dimension is 569 pixels. Any number of pixels lower than 569 is considered to be an under-scan which may lead to missing data and blurring of images.

2.4.2 Limitations

AMI inspection has its own limitations. AMI systems today can resolve 10- 15μm in the spatial x-y direction with a ~200MHz transducer for samples no thicker than a millimeter (Zhang *et al*., 2010a; Yang et al. 2012). The resolution of an acoustic image is affected by several factors such as the frequency of the transducer, focal length, fluid path and signal strength (Semmens, 2000). Typically, higher frequencies can achieve higher resolutions but compromise the penetration power. Thus penetrating multiple layers of organic substrate is a challenge due to high attenuation and scattering of ultrasound energy. Another issue in AMI inspection is the edge effect. When an ultrasound signal strikes the edge of a material, the signal is scattered away and causes a drop off of information (Semmens and Lawrence, 1997; Hoh *et al*., 2008). This effect can be reduced by certain transducer design but cannot be eliminated entirely due to the intrinsic properties of ultrasound. Another drawback of AMI inspection is the requirement for a coupling medium, usually deionised water to propagate the acoustic energy (Yang and Ume, 2010). Consequently, there are certain concerns whether this action could damage the test sample and affect the inspection result.

2.5 Summary

This chapter gave a brief idea about the basic concepts and background needed for proper understanding of the project. This included a discussion on area array packages mainly BGAs and flip chips followed by the principles of environmental testing. A brief literature review on all the research work related to vibration testing that has been done till date has also been discussed. It can be concluded that compared to ATC, vibration testing is relatively less researched. The test objects in the literature review were found to have a limited number of solder joints compared to the design proposed in this work. To top that, to my knowledge, very limited research data on real time vibration has been found. This research work is an endeavor to meet that gap. Currently, some research work is slowly moving towards mixed environmental testing although it is still fairly new. Non-destructive reliability inspection techniques like electrical testing, optical testing X-ray and laser ultrasound were also discussed briefly. However, more focus was given on acoustic inspection/AMI as this method has been used in this research work. Hence AMI has been discussed in details in the chapter.

Chapter 3

Experimental Plan

Any research idea needs to be accompanied by an executable research plan for fruition. This chapter discusses, in stages, the various trials and tribulations that led to the development of a sustainable research plan for the proper execution of this project. The first stage is the assessment of the necessary equipment like the vibration test chamber and the scanning acoustic microscope for performing the vibration tests and imaging the test boards respectively and gathering/ designing the requisite components such as test boards and fixtures. The second stage involves defining the parameters of the vibration profile and acoustic imaging for carrying out the test. The third and final stage is performing the test to verify if the test set up is accurate and then process the data using MATLAB to see if the experiment yields informative results.

3.1 Test equipment

3.1.1 Vibration Chamber

Vibration testing, most commonly applied at Delphi is done utilizing a servo controlled electro-dynamic test facility as shown in figures 3.1 and 3.2.

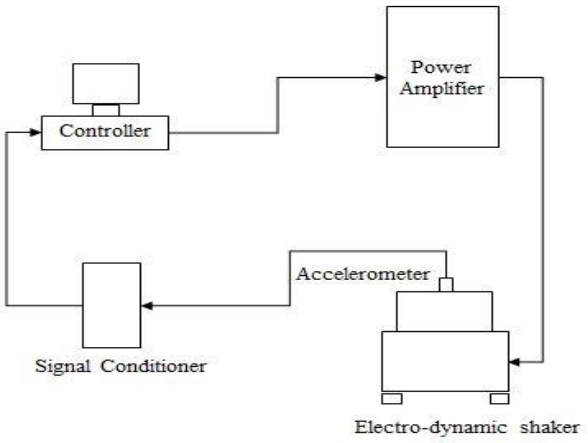


Figure 3.1: Servo controlled electro-dynamic test setup block diagram. (Delphi, Krakow)

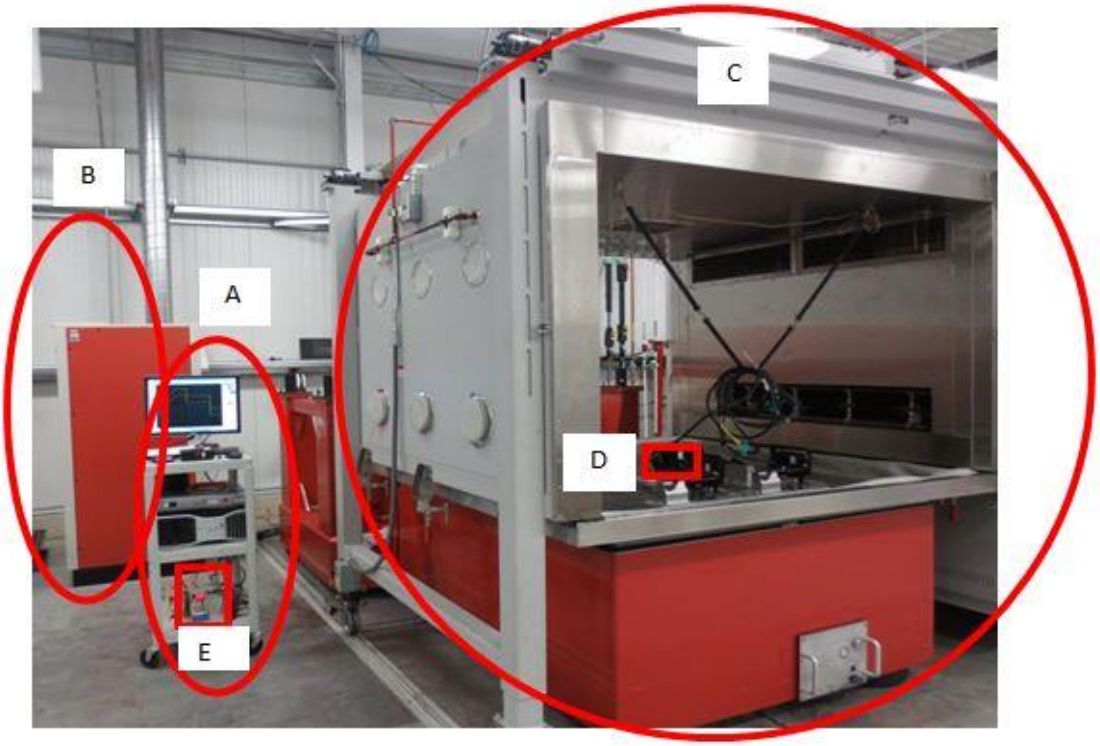


Figure 3.2: Servo controlled electro-dynamic test setup at Delphi, Krakow

A: The servo control system generates and sends the specified test signal to the shaker via a power amplifier. It also receives and analyzes the feedback signal from the accelerometer, adjusting its output to maintain specified test parameters.

B: The power amplifier then provides to the electro-dynamic shaker an amplified control signal to power the moving element via DC power to the field coils.

C: The electro-dynamic shaker is a machine comprising of a moving element to which the test products are attached and DC field coils. The moving element with armature windings is free to respond to an input signal within an electro-magnetic field. The shaker functions much like the voice coil assembly in an audio speaker.

D: The accelerometer is a transducer attached to the moving element which outputs a signal proportional to acceleration, typically in pC/g (pico Coulombs per g of acceleration).

E: The signal conditioner converts the accelerometer signal from pC/g to mv/g (milli volts per g of acceleration).

The experiment for the project was conducted in the vibration chamber in Delphi,

Liverpool following a pre-test that was done in a very similar chamber in Krakow, Poland. The vibration chamber/ shaker in Liverpool is a vibration cum humidity chamber with model no. Thermotron F40-OHMV-705-705, from Thermotron, Holland (USA) and has the following specifications:

Table 3.1: Specifications of the vibration shaker in Delphi, Liverpool, UK

Temperature range	Humidity	Compressors	Cooling	Gas	Controller
-70 to 190^{o}C	20-95% RH	7.5HP 7.5HP	Water	HP80 x10lb R23 x 9lb	4800

3.1.2 Test fixture and test boards

An Aluminium test fixture (figure 3.3) was designed at Delphi, Krakow for the experiment. It can accommodate four test boards at one go with 4-5mm recessed support for each board as shown in figure 3.3.

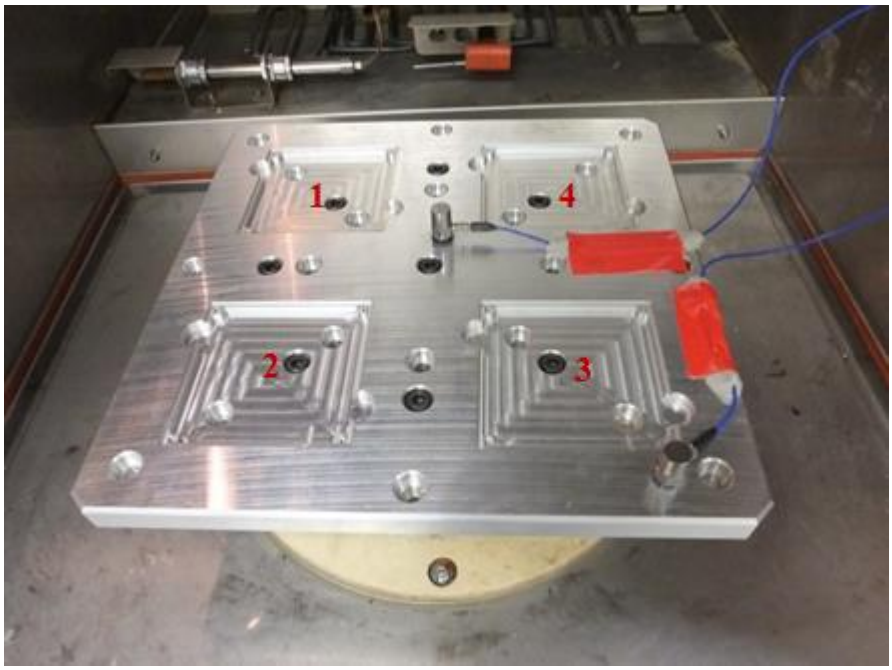


Figure 3.3: Aluminium test fixture with four PCB slots

Printed circuit boards with various area array packages, different surface finish configurations and substrate thickness were designed also at Delphi, Krakow for experiments. Table 3.2 shows the list of all the different types of boards available for the test. Electro less nickel immersion gold (ENIG) and hot air solder (HASL) are types of surface plating used for printed circuit boards.

ENIG consists of an electro less nickel plating covered with a thin layer of immersion gold, which protects the nickel from oxidation (Weiming Li, Reliability Research and Analysis Center, CEPREI, Guangzhou, China).

In HASL, the PCB is typically dipped into a bath of molten solder so that all exposed copper surfaces are covered by solder. Excess solder is removed by passing the PCB between hot air knives.

ENIG reduces the use of lead and emission from flux and fusing oil due to which it is more environment friendly compared to HASL. With anti-lead laws now in place in almost all of Europe, ENIG has almost become the industry standard. (RoHS, 2006)

Table 3.2: Types of board available for the experiment

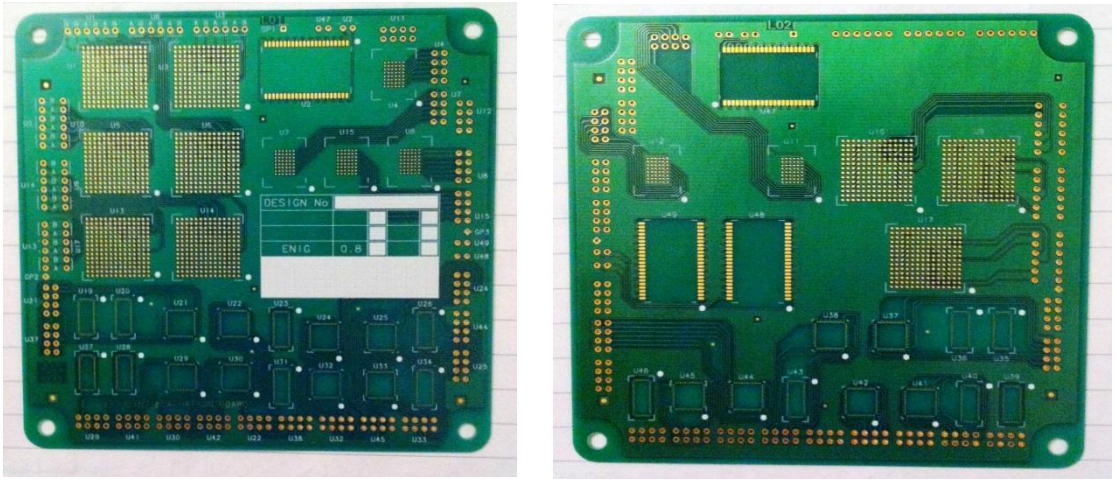
Board No.	Board Thickness	Surface finish
1	0.8mm	HASL
2	0.8mm	ENIG
3	1.6mm	HASL
4	1.6mm	ENIG

All boards are FR-4 which stands for Flame Retardant Class 4. FR-4 is a composite material composed of woven fiberglass cloth with an epoxy resin binder that is flame resistant (self-extinguishing). It is a commonly used printed circuit board material. However, the woven structure of the FR4 scatters most of the ultrasound signal during inspection, thus ultrasound scanning can only be performed from the top of the flip chip as it is nearly impossible to image through the opposite FR4 side. Each of the boards has the same layout as shown in figures 3.4 and 3.5.

For the purpose of this study, initially, focus was given on two components of the board namely:

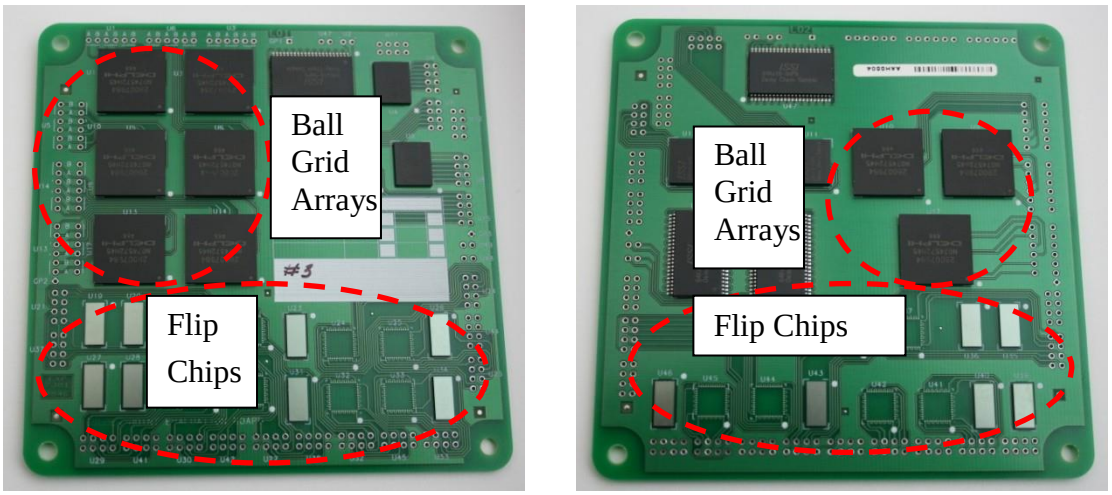
i. Flip chips (FCs)
ii. Ball grid arrays (BGAs)

There are 8 FCs and 6 BGAs on the front of the board and 5 FCs and 3 BGAs on the back of the board. Each FC has 109 Pins and each BGA has 196 pins.



Top view **Bottom view**

Figure 3.4: Bare PCB layout without components



Top view **Bottom view**

Figure 3.5: PCB layout with components

3.1.3 Scanning Acoustic Microscope

The ultrasound C-scan images used in the solder joint through life monitoring were obtained using the Sonoscan Gen6™ C-Mode Scanning Acoustic Microscope machine in the LJMU laboratory as shown in figure 3.6.

Figure 3.6: Sonoscan Gen6™ C-Mode Acoustic Microscopy System (Image courtesy of Sonoscan Inc.)

3.2 Defining the test parameters

In this section, all the parameters of the experiment and how they were derived will be explained in details. This will include the parameters for the vibration test, test board and acoustic micro imaging and vibration testing and AMI scan intervals.

3.2.1 Vibration test parameters

Based on the data collected from the automobile industry with the help of Delphi experts, an agressive random vibration profile was proposed for the project that mimicked the vibration characteristics experienced by current automobiles in real time. Figure 3.7 and table 3.3 below shows the profile and profile parameters respectively. PSD refers to the power spectral density of the profile.

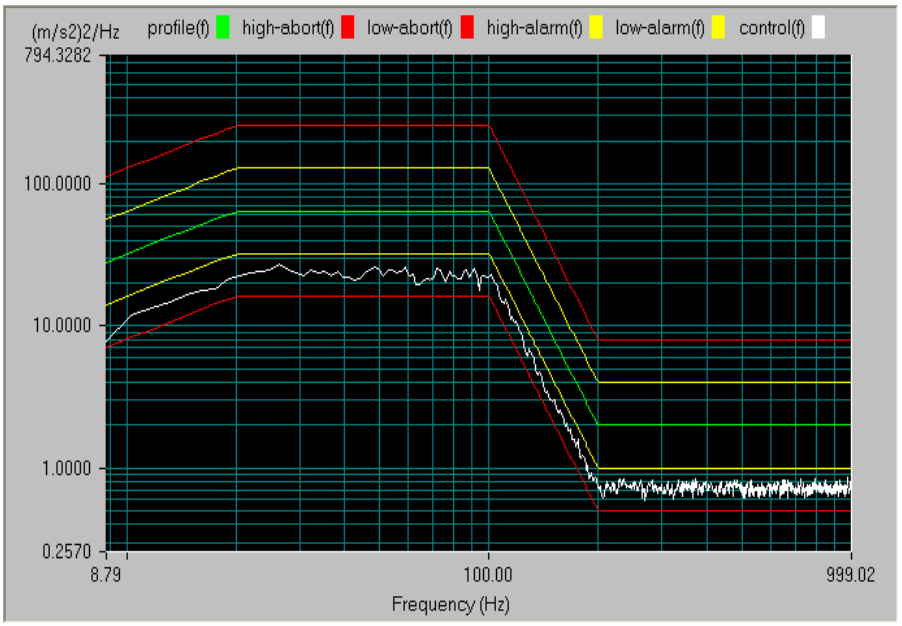


Figure 3.7: Proposed random profile for the experiment (green trace)

Table 3.3: Parameters of the random profile proposed for the experiment

Frequency (Hz)	0	20	50	100	200	300	400	500	750	1000
PSD $((m/s^2)^2/Hz)$	32	64	64	64	2	2	2	2	2	2

In order to assure that the resonant frequency of the test fixture did not interfere with the resonant frequency of the test boards, a resonance sweep was performed first on the test fixture and then on the test boards attached to the test fixture. The sine profile used for the resonance sweep is shown in figure 3.8.

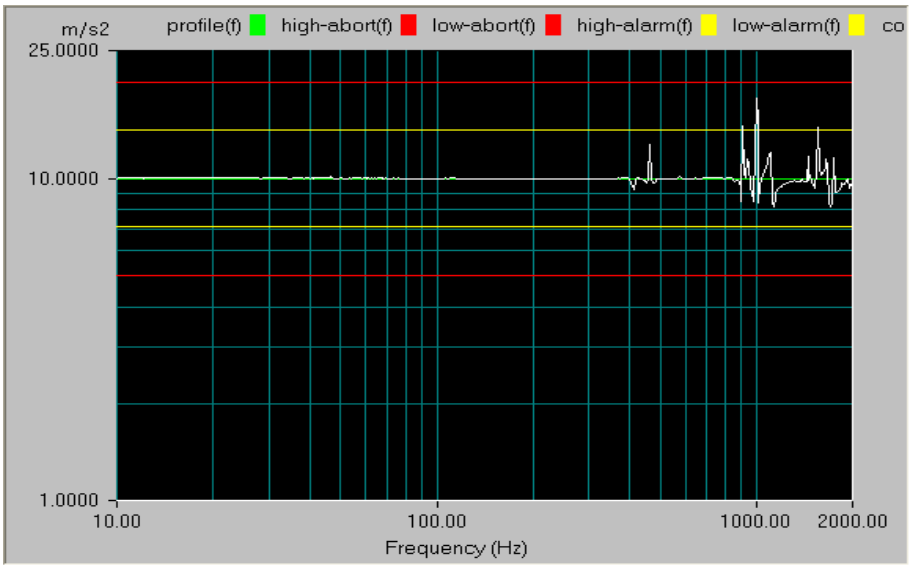


Figure 3.8 Sine profile

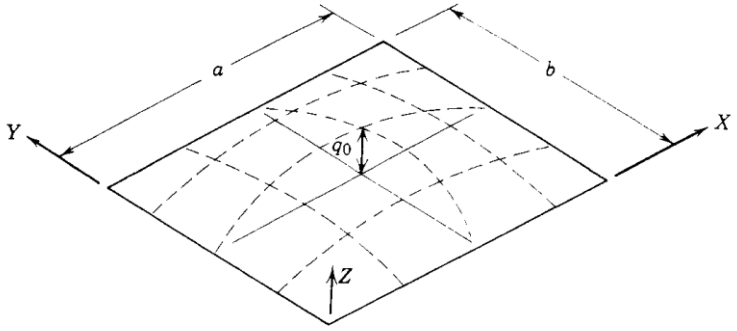


Figure 3.9 Dynamic deflection mode of a circuit board. Source: Chapter 6, Steinberg, 2000

Since the PCBs were fixed to the fixture using four screws at the four corners of the board as shown in figure 3.9, the expected natural resonant frequency of the PCB board was calculated using Steinberg's equation for natural resonant frequency for a PCB with four fixed points at the corners as given in equation 3-1 below:

$$f_n = \frac{\pi}{2}\left(\frac{D}{\rho}\right)^{\frac{1}{2}}\left(\frac{1}{a^2}+\frac{1}{b^2}\right) \qquad \text{Eq. 3-1}$$

Where,

$D = \frac{Eh^3}{12(1-\mu^2)}$ is the plate stiffness factor with modulus of elasticity E, plate thickness h and Poisson's ratio μ.

$\rho = \frac{W}{abg} = \frac{uh}{g}$ is the mass per unit area where W is the weight of the board, u is the

material density, g =9.8 m/s^2 is the acceleration due to gravity and a,b,h are the length, width and thickness of the board respectively.

Maximum board displacement is given by equation 3-2,

$$Z_o = \frac{9.8G_{out}}{f_n^2} \quad \text{Eq. 3-2}$$

Maximum dynamic load intensity at the center of the plate is given by equation 3-3,

$$q_o = \frac{WG_{out}}{ab} \quad \text{Eq. 3-3}$$

Maximum bending moment is given by equation 3-4,

$$M_Y = \frac{q_0\left(\frac{\mu}{a^2} + \frac{1}{b^2}\right)}{\pi^2\left(\frac{1}{a^2} + \frac{1}{b^2}\right)^2} \quad \text{Eq. 3-4}$$

Dynamic bending stress at the center of the plate is given by equation 3-5,

$$S_b = \frac{6K_tM_Y}{h^2} \quad \text{Eq. 3-5}$$

Where,

K_t = 3.0 (theoretical stress-concentration factor for a small hole in the circuit board.

For the experiment, in case of the 0.8mm thickness board, (Braden, 2012)

E=24500N/mm^2

a = b= 9.9cm

h=0.8mm or 1.6mm(for 1.6mm thickness board)

W=19g(0.8mm board) or 38g (1.6mm board) (measured in LJMU Laboratory)

μ=0.15

G_{out} =12, peak vibration output

Using these values in the above equations, the following parameters are calculated,

1. Natural frequency, f_n = 219Hz (0.8mm board) or 450Hz(1.6mm board)
2. Maximum board displacement, $Z_{0=}$ 62.23μm
3. Maximum dynamic load intensity, q_0 = 23.27 kg/m^2
4. Dynamic bending stress, S_b= 18317775 kg/m^2

Experimentally, the natural board frequency for the 0.8mm board was found to be 210 Hz while the rest of the parameters could not be verified.

The torque required to fix the PCB to the fixture is given by equation 3-6,

$$T = 0.2DP \qquad \text{Eq. 3-6}$$

Where,

T = torque

D = outside diameter of thread

P = axial load induced in bolt = Stress area of the bolt x tensile yield strength

0.2 = constant for most bolt and bolt materials

For the bolts used in the experiment,

Tensile yield strength = 33000 lb/in^2 = 23201296 kg/m^2

Stress area of the bolt = 0.0090 in^2 = 5.80644e-6 m^2

Bolt diameter = 0.138in = 0.0035052m

Using the parameters in the torque equation we get,

Torque= 0.9265 Nm~ 1Nm

Accordingly, for the experiment, 1Nm was used to torque the PCB to the fixture.

As per the instructions of Delphi specialists, 20 Nm was used to torque the fixture to the vibration chamber or shaker. These torque values proved sufficient to hold the test fixture and the PCBs in place during the vibration tests.

3.2.2 Test board parameters

Although at the starting of the experiment, the intent was to focus on both FCs and BGAs for through life testing, after the pre-test, it was found that the BGAs cannot be used for further testing, the details of which will be discussed in section 3.5 of this chapter. Hence, in this particular study, the test boards used in vibration tests and AMI monitoring were flip chip on board (FCOB) packages. Table 3.4 details the specifications of the FCs.

Table 3.4: Information about the FCs

Flip chip	
Die X	3948µm
Die Y	8898µm
Die Z	725µm
Poisson's ratio	0.22 to 0.28
CTE flip chip	2.6 ppm/K
UBM material	UBM stack is Al, Ni and Cu with Cu being on the top of stack.
UBM pad size	102µm
Level 1 interconnects (Solder joint)	
Solder bump diameter (middle)	140µm
Solder Bump height	125µm
Solder material	Sn=52.9%, Pb=45.9%, Cu= 1.2%
Substrate	
Material	FR-4
Thickness	0.8mm or 1.6mm
Substrate x dimension	100mm, 5mm radius to corners
Substrate y dimension	100mm, 5mm radius to corners
CTE - PCB (ppm/K)	$z=35x10^{-6}$, $x=11x10^{-6}$, $y=13x10^{-6}$, (in/in/c)
Pad thickness	35 - 42 microns
Pad material	Cu with HASL/ENIG surface finish
Underfill	No underfill

As was discussed in section 3.1.2, each PCB has 14 FCs. All of these FCs were designed with different orientations to test the effects and interactions of placement position and relative placement. Some of them have back to back connections, with or without different offsets while some have been placed single sided on the PCB. Figure 3.10 shows all the FC positions and they are named as U19, U20, U23, U26, U27, U28,U31, U34, U35, U36, U39, U40, U41 and U46.

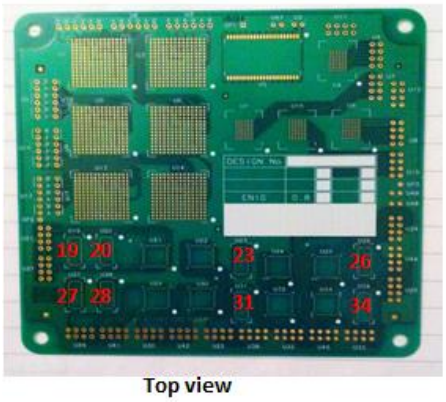
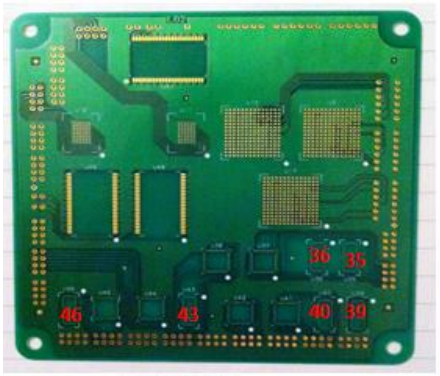
Board Layout	 Top view	 Bottom view

Figure 3.10 Name of all the positions where the FCs are placed in the PCB

U23 and U26 are single sided flip chips with no back to back connections.

U19-U35 and U20-U36 pairs are placed back to back with an offset along the breadth as shown 3.11a.

U27-U39, U28-U40 pairs are placed back to back with an offset along the length as shown 3.11b.

U34-U46, U31-U43 pairs are placed exactly back to back with no offset as shown 3.11c.

The red and blue logos indicate the solder joints of two different flip chips.

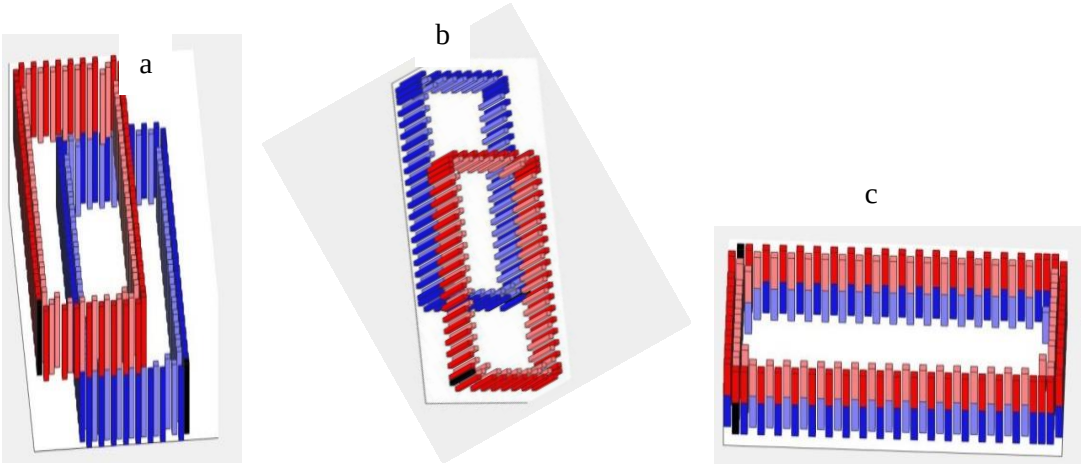


Figure 3.11: Different flip chip orientations in PCBs. a) FC with back to back connection and offset long the breadth. b) FCs with back to back connection with offset along the length c) FCs with back to back connections with no offset

3.2.3 AMI scan parameters

To get the best scans possible for the test the following key points have to be noted:

i) Transducer resolution versus penetration: Higher the frequency of the transducer used, higher the resolution but lower the penetration.

ii) Edge effect (Chean Lee, 2012) is a very common problem in acoustic micro imaging. To prevent this, transducers with higher N values should be used where, N is the transducer's depth of focus. The higher the N, the greater the defect detection near the edges of the inspected samples and hence lower the edge effect.

Hence using a transducer with the highest possible frequency is desirable. The highest frequency transducer available in the LJMU lab was a 230MHz, 0.25" focal length transducer, so was favourable. However, the next important aspect to determine is, if the penetration capability of this transducer is acceptable for the test components viz. the FCs.

To verify this, a preliminary scan of a random FC using the 230 MHz, 0.25" transducer was done. The results and the other test parameters are shown in tables 3.5 and 3.6 respectively.

Table 3.5: Transducer parameters

Frequency	Focal length	Diameter	N	Resolution	Optimum scan area
230 MHz	0.25"	0.125"	2.00	0.011mm	5.759mm

Table 3.6: Scan parameters

Transducer frequency	Focal length	Resolution	Trigger level	Front end gain	Channel gain	Scan size
230 MHz	0.25"	To be set after pretest	0.590	24.5	24.0	Determined by the area of interest

The scan size refers to the size of the test area (mm or inches) and based on this the resolution of the scan in pixels can be determined using the formula:

Resolution in pixels = $\frac{\text{scan size(per axis)}}{\text{spot size}}$

Where scan size is the size of the area being scanned and spot size is = N x λ x 1.22

Where λ(mm) = (velocity of sound in distilled water in mm/μs)/frequency in MHz

Now, velocity of sound in distilled water= 1495m/s=1.495mm/μs

and N = $\frac{\text{focal length}}{\text{diameter}}$ of the transducer.

For example, for a square scan area of 6mm x 6mm, with the aforementioned transducer of 230 MHz, 0.25" focal length and N=2 , λ = 1.495/230 = 0.00598mm

Therefore spot size = N x λ x 1.22 = 2 x .00598mm x1.22 = 0.01459 mm

Hence resolution = 6/0.01459 = 411 pixels in each direction or 411 x 411 pixels.

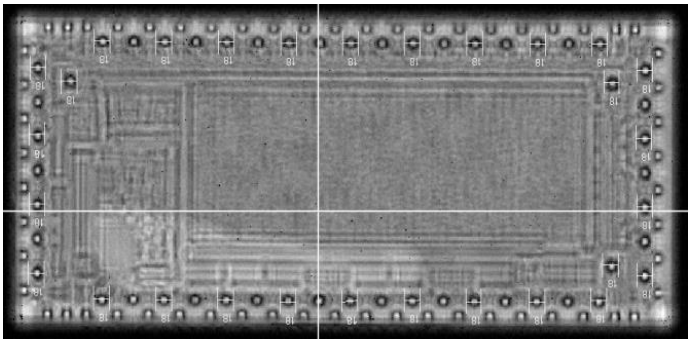


Figure 3.12: C-scan of an FC scanned at 3 micron resolution

As can be seen from the figure 3.12 above, the selected transducer generates a good image of the FC solder joints. Hence penetration will not be an issue. The final scan resolution will be determined after the pretest.

3.2.4 Test cycle and scan duration

Since the random vibration profile proposed for the test has never been used on the test boards before, the duration of the test till all the flip chips fail was unknown. Hence a pre-test was performed using sample test boards to determine the total time for complete failure of all the FCs on the board. This result was then used to inform the AMI scan resolution and test intervals for life time tests. These factors will be discussed in details in section 3.3 of the chapter.

3.3 Pretest

Once all the equipment and parameters for the experiment have been decided, the next step was to perform a preliminary test using all the information in order to:

1. Verify that the theoretical resonance points of the PCBs and torque measurements calculated in section 3.2.1 match the experimental observations. The resonance sweep test was also needed to ensure that the bare fixture does not have any resonance points within the frequency range of the proposed profile. Otherwise, the bare board resonance point would have interfered with the resonance of the PCBs and lead to faulty results.
2. Determine the complete time for failure of all the FCs in the PCBs: Through life monitoring of vibration testing on FCOB assemblies in the presence of other components on board like BGAs, micro BGAs in real time had, to my knowledge, never been attempted before. Hence the time required for complete failure of all the FCs was unknown. So the pretest was done to determine the failure points of all the FCs. This helped in estimating the total time required for the completion of the experiment. Each vibration test cycle was set to take 4 minutes.
3. Determine the scan interval: Once the time for complete failure of all the FCs in the PCBs was determined, the next step was to determine the time intervals at which the FCs need to be acoustically scanned in order to obtain enough data points for through life monitoring and analysis.
4. Determine the scan resolution: Another important aspect to consider for successful completion of the test was the scan resolution of the transducer. Practically, the resolution of the transducer could be set to as low as 1 micron/pixel for scanning the FCs. But completing one scan set for 1 micron/pixel resolution takes an hour. Scanning at 2 micron/ pixel takes 30 minutes per scan and at 3 micron/pixel takes 15 minutes per scan. Keeping that in mind the next thing to take into account was the number of FCs that needed to be scanned at the end of each cycle. Although 1 micron/pixel gives the best resolution, considering the possibility that all the 14 FCs could probably be scanned at the end of each cycle, the total time for completion of 1 complete set of scans for just one PCB takes 14 hours if scanned at 1 micron/pixel. Now if we factor in the fact that time for complete failure of all

the flip chips in one PCB might take, say 100 to 1000s of cycles. Then, the total scanning time will be 1,400 hours to 14,000 hours if scanned at 1 micron/pixel which is approximately 58 to 580 days (about 2 years) just for scanning one board. Initially, the idea was to test all the 4 boards of different configurations as listed in section 3.1.2. So that would have meant almost about 8 years of just scanning, impossible in a PhD timescale. To top that we also have to factor in the time taken for vibration testing the boards in the Delphi facility in Knowsley, UK and then bringing them back to the university for scanning and then again taking them back to the industry for the next cycle. The commute from LJMU to Delphi itself takes about 3 hours. So taking all these factors into consideration, it was decided that the scan resolution would be set to 3 micron/pixel. Nevertheless, any higher resolution than that did not yield good images. An acoustic image is considered to be good if all the solder joints in a flip chip are distinctly visible to the naked eye. Also, at 3 micron/pixel, sufficient pixels were collected across each solder joint, typically over 100 microns in diameter, to validate the solder joint status.

3.3.1 Resonance testing and verification

Initial training for the experiment was done in Delphi, Krakow for a week and then the main experiment was conducted in Delphi, Liverpool.

Before staring the main experiment, the bare fixture was mounted into the shaker (figure 3.13a) as shown in figure 3.13b and a resonance sweep was done using the sine profile as was discussed in section 3.2.1.

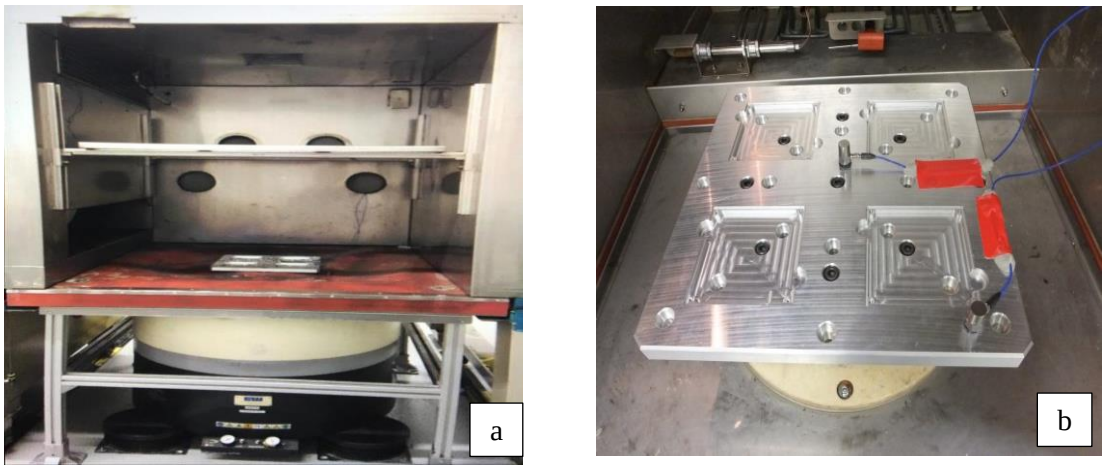


Figure 3.13: a) Vibration chamber in Delphi, Liverpool (UK) (b) Bare fixture mounted on the shaker for resonance sweep

Two tri-axial accelerometers were placed at the center and the corner of the fixture to monitor the results.

It can be clearly seen from figure 3.14 that the bare fixture does not have any resonance point in the proposed frequency range 0-1400Hz of the random profile to be used for the experiment.

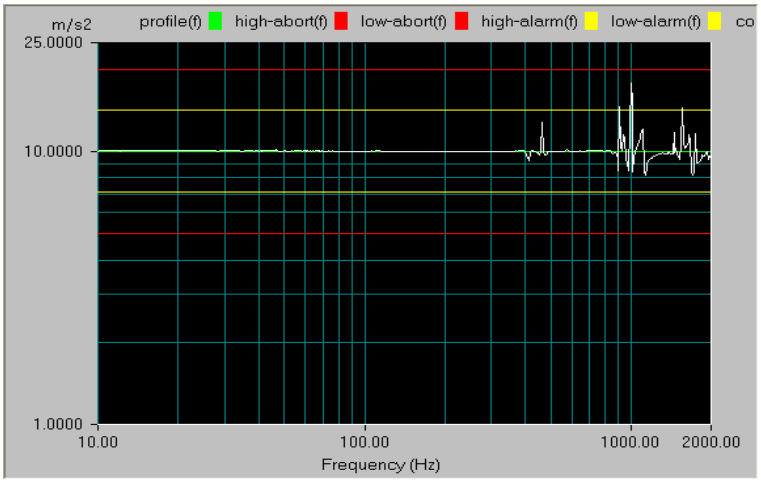


Figure 3.14: Resonance sweep of bare fixture

Thereafter, the 0.8mm ENIG board was torqued down into one of the PCB slots of the fixture as figure 3.15 and a resonance sweep was done to find the resonance point. The test board showed a resonance point of 212 Hz as shown in figure 3.16. Similarly, the resonance points for the 0.8mm HASL, 1.6mm ENIG and 1.6mm HASL boards were found to be 218, 413Hz and 428Hz respectively.

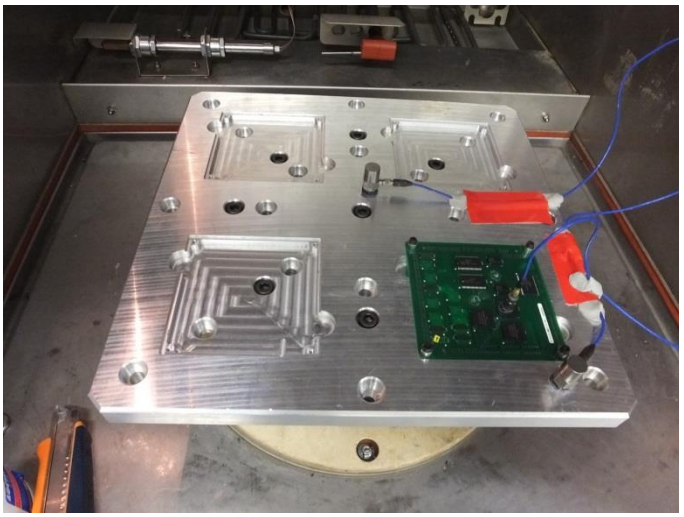


Figure 3.15: 1.6mm ENIG board mounted on to the fixture for resonance sweep

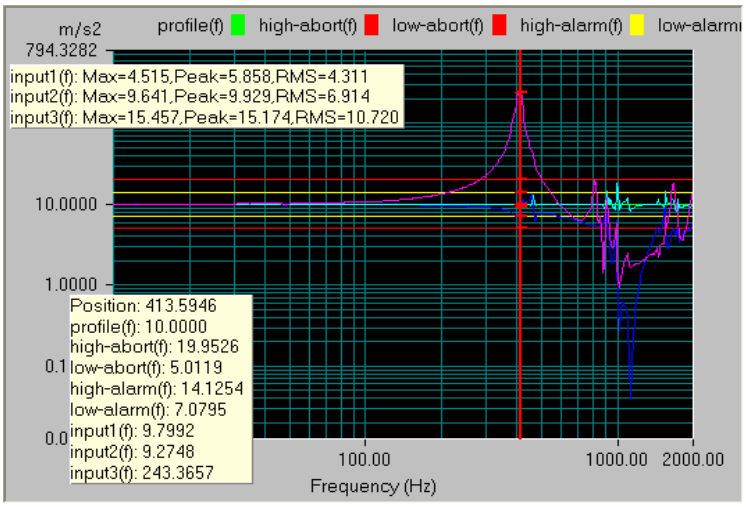


Figure 3.16: Resonance sweep result for 1.6mm ENIG board (purple trace)

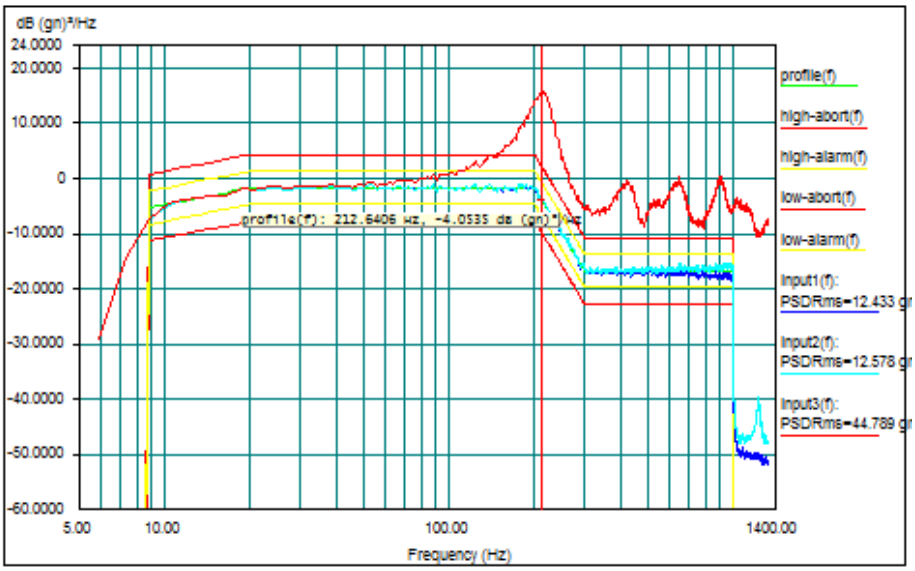


Figure 3.17: Result of the 0.8mm ENIG board subjected to random vibration profile (red trace)

On performing the vibration test with the random profile, the same resonance points were noticed. For example, the 0.8mm ENIG board showed the same resonance point of 212 Hz as shown in figure 3.17.

Based on the test results, it was found that:

1. The torque value of 1Nm that was based on the theoretical calculations as discussed in the section 3.2.1, held the boards perfectly in place. Even a slight change of ± 0.5Nm in the torque changes the resonance points by only 10Hz.
2. Compared to the theoretical resonance points, the experimental resonance points

differed only by a few Hz.

3. The 0.8mm boards have lower resonance points at about half the frequency compared to the 1.6mm boards. Since the total duration needed for the failure of the boards is still unknown, using 0.8mm boards for the pre-test is desirable as they will probably fail faster owing to their lower resonance values. Hence, for the purpose of the experiment, 0.8mm PCBs will be used.
4. In general, ENIG boards were found to have slightly lower resonance values compared to their HASL counterparts.

3.3.2 Determination of test duration for complete failure of the 0.8mm ENIG and 0.8mm HASL boards

The main aim of the pre-test was to determine the time required for complete failure of all the 14 FCs in both the 0.8mm ENIG and 0.8mm HASL boards. Hence, without taking the boards out for scanning, they were vibrated in the vibration chamber and inspected after every test cycle to monitor the failure order of FCs. Each test cycle was equal to 4 mins. Figure 3.18 below shows the PCB placement for the experiment. Since the populated 0.8mm ENIG board and 0.8mm HASL board will have relatively more weight than a bare 0.8mm board, bare 1.6mm boards were introduced to balance out the weight difference in the fixture. All the boards were screwed down to the fixture using 1Nm torque. Table 3.7 shows the failure times and order in which the FCs failed.

Aluminium fixture

0.8mm ENIG populated	1.6mm ENIG bare
1.6mm ENIG bare	0.8mm HASL populated

Figure 3.18: Board placement for the test

Table 3.7: Failure time and order of FCs

0.8ENIG flip chip no.	Cycles to failure	Time to failure in hours (1 cycle= 4 minutes)	0.8HASL flip chip no.	Cycles to failure	Time to failure in hours
U23	3	0.2	U23	4	0.267
U26	14	0.933	U26	27	1.8
U35	21	1.4	U27	51	3.4
U39	23	1.533	U34	57	3.8
U46	24	1.6	U19	101	6.733
U34	29	1.933	U28	103	6.867
U36	34	2.267	U20	122	8.133
U27	45	3	U46	130	8.667
U43	48	3.2	U36	268	17.867
U20	53	3.533	U39	278	18.533
U31	55	3.667	U35	294	19.6
U40	57	3.8	U31	311	20.733
U19	68	4.533	U43	316	21.067
U28	86	5.733	U40	380	25.333

An important fact to be noted here is that, when screwed to the fixture on the vibration chamber, only the top sides of the PCBs are visible, so in order to see if any FC has failed on the bottom side, after every cycle, the PCBs need to be unscrewed and then screwed back again. So, even though one vibration cycle takes only 4 minutes, factoring in the time for unscrewing and screwing the PCBs back into the fixture, each cycle took approximately 20 minutes. Hence the effective total time per cycle is 24minutes. Hence actual time taken for the completion of the pretest is shown in table 3.8.

Table 3.8: Effective failure time of all the FCs

Board type	Total Cycles to complete failure	Effective failure time in hours (1 cycle= 24 minutes=0.4 hour)
0.8mm ENIG	86	34.4
0.8mm HASL	380	152

Taking into consideration, various other factors like the vibration cycling training in Krakow, Poland, getting acquainted with the test equipment in Delphi, Liverpool and unforeseen error resolutions during the test the entire pre-test took about 1 year.

3.3.3 Determination of acoustic scan interval

While coming up with a scanning plan, other than the pre-test time many other factors were needed to be considered. These were:

i. The time taken to scan the FCs in the LJMU laboratory. All the FCs on the 2 PCBs if scanned after every cycle at a scan resolution of 3microns will take 15mins per FC and hence a total of 28 x 15 = 420 mins = 7 hours.

ii. Factoring in the commute time of about 3-4 hours to and from the industry to university, one vibration test cycle time of about a half hour along with the scan time of 7 hours, each complete test cycle almost took 12 hours. So for the ENIG board which took 86 cycles for complete failure and HASL board that took 380 cycles for complete failure, the total test time was 1032 hours (43 days) and 4560 hours (190 days) respectively just for data collection. Analysis of such a huge data set is a whole new challenge.

iii. The scanning machine in LJMU was available for only half the week as other researchers were also carrying out their experiments simultaneously.

iv. Weekends and holidays also needed to be considered.

Taking into consideration all the above factors and the fact that about a year and half had already passed at this point, it was decided only certain FCs and only at certain intervals, the FCs will be scanned for data collection. These FCs were carefully chosen to include all types of orientations and the scanning interval was decided so as to include at least 8 data points for each FC to be scanned to failure. Based on this, the following FCs and scan intervals were chosen as shown in table 3.9.

Table 3.9: Scan intervals for different FCs for 0.8mm ENIG and 0.8mm HASL boards

0.8mm ENIG	Scan interval	0.8mm HASL	Scan interval
U23	1 scan/cycle	U23	1 scan/cycle
U26	1 scan/ 2 cycles	U26	1 scan/ 2 cycles
U27	1 scan/5 cycles	U27	1 scan/5 cycles
U34	1 scan/5 cycles	U34	1 scan/5 cycles
U19	1 scan/5 cycles	U19	1 scan/10 cycles
U28	1 scan/10 cycles	U28	1 scan/10 cycles
U20	1 scan/10 cycles	U20	1 scan/10 cycles
U35	1 scan/5 cycles	U35	1 scan/20 cycles
U40	1 scan/5 cycles	U40	1 scan/20 cycles

Before the commencement of the test all the aforementioned FCs were acoustically scanned to obtain the base ultrasound C-scan images of FCs using the configuration stated in the previous section 3.2. This data set served as the reference point for through life monitoring of the solder joints of the FCs as the experiment progressed and the solder joints started to fail.

3.4 Test failures and limitations

Any experimental idea comes with its fair share of challenges. In this experiment the following problems were encountered:

i. For the pre-test, the 1.6mm PCBs were also tested but it was found that even after 3000 test cycles the FCs had not completely failed. Hence the idea of using them for the main test was discarded due to long test time.

ii. Another problem that occurred was that the 0.8mm HASL board that was used in the main test turned out to be faulty. After just 20 cycles, all the FCs fell off the PCB. That is why, finally only the 0.8 ENIG board came to be used for the main test. On observing the faulty 0.8 HASL board under a Scanning Electron microscope it was found that the under bump metallization was not fully formed during manufacturing that eventually led to the failure of the FCs within 20 test cycles. Figure 3.19 shows the image of the solder joints remnants after their failure.

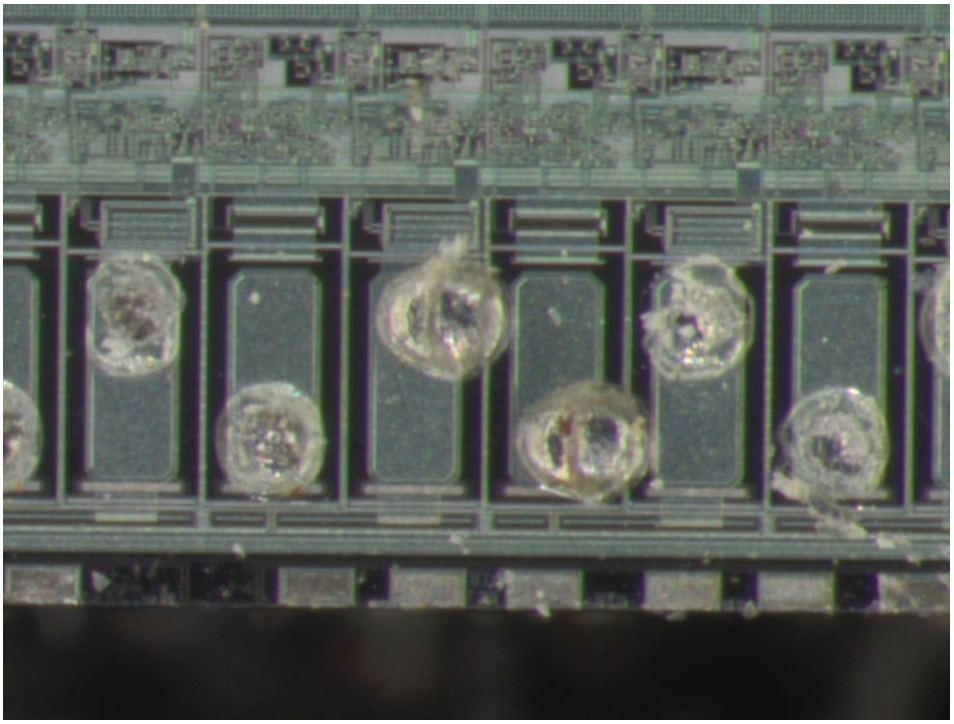


Figure: 3.19: Image of some solder joints residue on a flip chip disconnected from a 0.8mm HASL board after complete failure

iii. Before determining to use AMI and image processing for data analysis, the prospect of resistance spectroscopy was investigated for through life monitoring of the BGAs and FCs. The initial idea was that as the PCBs are subjected to vibration, they start to fail. It can be expected that as the FCs and the BGAs start failing the resistance across the failing points will start to change, and slowly increase because of expected crack formations. So another proposal was to use time domain reflectometry or TDR to measure the resistance of the FC pins and the BGA ball points after each vibration cycle and hence, spot any crack initiation and propagation based on the change in their resistance. TDR

measures impedance discontinuities as discrete peaks with respect to their positions in the circuit and is useful for fault location. But after investigating further, it was found that there are currently no electrical probes available in the market that can monitor the resistance of the BGAs or FCs on a PCB board assembly directly for through life monitoring purposes. Hence these ideas were discarded.

iv. Just like TDR, 3D X-ray was also considered as a novel technique for through life monitoring of the FCs. However, the nearest 3D X-ray machine that was accessible was located in University of Manchester and to use it the cost around £500 per day. Through an application process, this study was able to gain free access to the 3D X-ray facility for a day but found out that one 3D scan of a FC took about 12 hours. Another important constraint was that the maximum sample size that can be scanned in a typical 3D X-ray was about 5cm^2 and hence it was not suitable for the test boards used in this research which have an area of about 100cm^2. Considering all the above factors, this idea also was discarded. However, the initial image of a few flip chips in figure 3.20 shows the potential of 3D X-ray measurement for future studies.

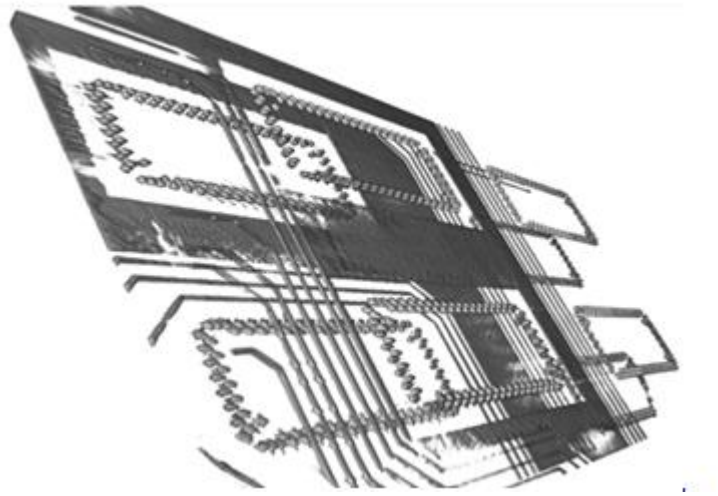


Figure 3.20: 3D X-ray scan of populated PCB taken at the Manchester X-ray Imaging Facility (MXIF), University of Manchester

3.3.4 Data collection and analysis

After each scan, the images were stored in a portable hard drive as well as backed up in the university cloud account. Each image is about 5MB. After collection of the

complete data set obtained on successful completion of the vibration testing, the images were analyzed using image processing techniques in MATLAB. The results obtained are discussed in details in the next chapter.

3.4 Summary

In this chapter, the various highs and lows encountered during the experiment were discussed. Vibration testing is a very expensive and time consuming procedure and adding the through life monitoring requirements, the experiment becomes even more challenging. After thorough research into various types of PCBs and different types of through life monitoring techniques, it was finally decided that the 0.8mm ENIG board will be used for the test and AMI will be used for through life monitoring of the solder joints in the FCs. A resolution of 3 micron/ pixel was established for the scans. Because of time constraints, it was agreed upon that only 9 out of the 14 FCs on the PCB will be monitored. However, these FCs were carefully chosen to include all types of orientations present in the PCB. The different types of difficulties that were encountered during the whole experiment have also been discussed here.

Chapter 4

Experimental Results

Following from the previous chapter, which discussed the experimental plan, this chapter discusses the experimental results. As discussed in Chapter 2, AMI techniques have been widely used in solder joint inspection due to its capability in detecting discontinuities in a material. However, to my knowledge, it has not been used to monitor the solder joint through life performance for vibration cycling. This chapter will therefore deal with the implementation of AMI to through life inspection of solder joints subjected to vibration cycling. The data obtained will then be analyzed using image processing techniques in MATLAB.

Based on the data obtained from vibration cycling, the flip chips were classified into three reliability configurations viz. least reliable, medium reliable and highly reliable. One flip chip from each reliability type was then chosen for further image analysis. For the ease of analysis, all the 109 solder joints of each flip chip were labelled as per a labelling scheme which will be discussed in detail in section 4.1 of this chapter. Initial analysis of the 109 solder joints in all the flip chips revealed that the degradation of all the solder joints follow one of three possible patterns, all of which will be discussed in section 4.2 of this chapter.

4.1.1 Introduction

Due to the large number solder joints in each of the flip chips used in the test board, it is important to label the solder joints so that they can be referenced correctly throughout the experiments. Table 4-1 provides a brief review of the nomenclature of the flip chips in the test board and the labelling scheme of the solder joints is shown in Figure 4.1.

Table 4-1: Nomenclature of the test board

Board Type	Flip chip Identifier	
	Top side (8 Flip chips)	Bottom side (6 Flip chips)
0.8mm ENIG	U19	U35
	U20	U36
	U27	U39
	U28	U40
	U23	U43
	U26	U46
	U31	
	U34	

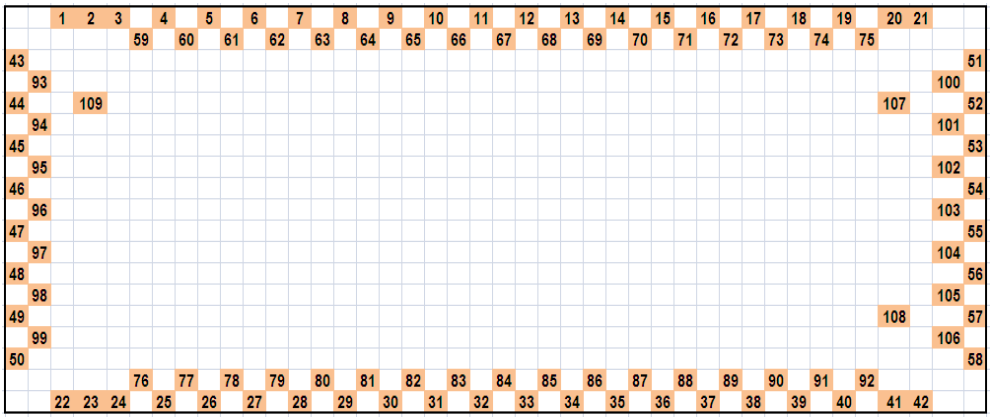


Figure 4.1: Labelling scheme of solder joints

4.2 Failure analysis

In a case study carried out by Zhang *et al*. (2000), it was found that the mean-time-to-failure of flip chip with underfill is about 2000 cycles for accelerated thermal cycling, whereas for flip chips without underfill this decreases dramatically to 100 cycles. Although this data refers to flip chips subjected to accelerated thermal cycling, it does give us a brief idea about what can be expected in case of vibration cycling. Since vibration cycling induces higher stress compared to thermal cycling, it can be expected that the flip chips without underfill will have a lower mean-time-to-failure. This

hypothesis was confirmed with the experimental result where it was found that all the flip chips on the 0.8mm ENIG board failed within 86 vibration test cycles. Table 4.2 shows the failure pattern of the flip chips.

Table 4-2: Flip chip failure pattern

0.8mm ENIG flip chip no.	Cycles to failure 1 cycle = 4 minutes	Failure time in hours
U23	3	0.2
U26	14	0.933
U35	21	1.4
U39	23	1.533
U46	24	1.6
U34	29	1.933
U36	34	2.267
U27	45	3
U43	48	3.2
U20	53	3.533
U31	55	3.667
U40	57	3.8
U19	68	4.533
U28	86	5.733

Upon close observation of the failure table 4.2, one can argue that the flip chips in the PCB can be cassified into 3 categories based on their reliability performance. If we consider 86 cycles as the total expected lifetime of a flip chip, then flip chips with a lifetime of less than 25% of expected lifetime will be considered as the least reliable while those above 50% will be considered as the most reliable while those in between will have medium reliability. In order to visualise this classification colour coding is introduced as explained below in table 4.3 and implemented in figure 4.2a and 4.2b. Figure 4.2a shows the nomenclature of the flip chips while 4.2b shows their respective reliability.

Table 4-3: Reliability based colour coding scheme

Colour code	Criteria (% cycles to failure, say X)
Red: least reliable	X≤25
Yellow: medium reliability	25 <X≤ 50
Blue: most reliable	X>50

Top view Bottom view

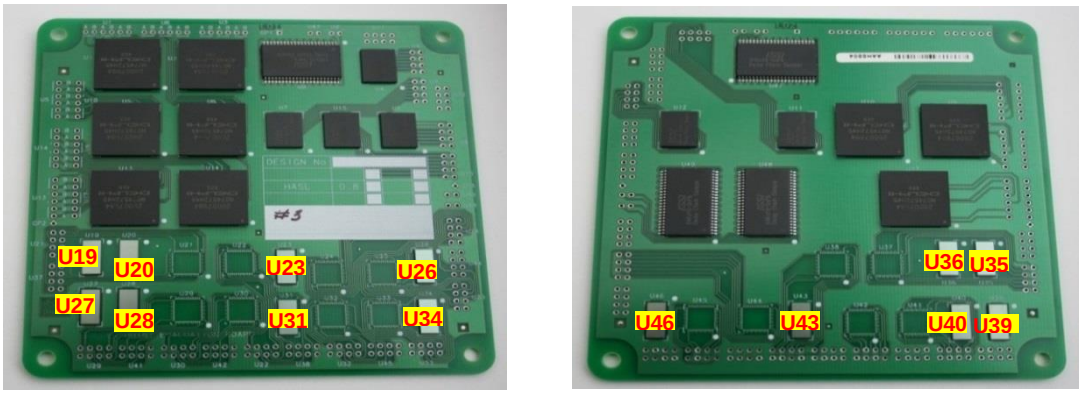


Figure 4.2a: Generic board layout with flip chip numbers

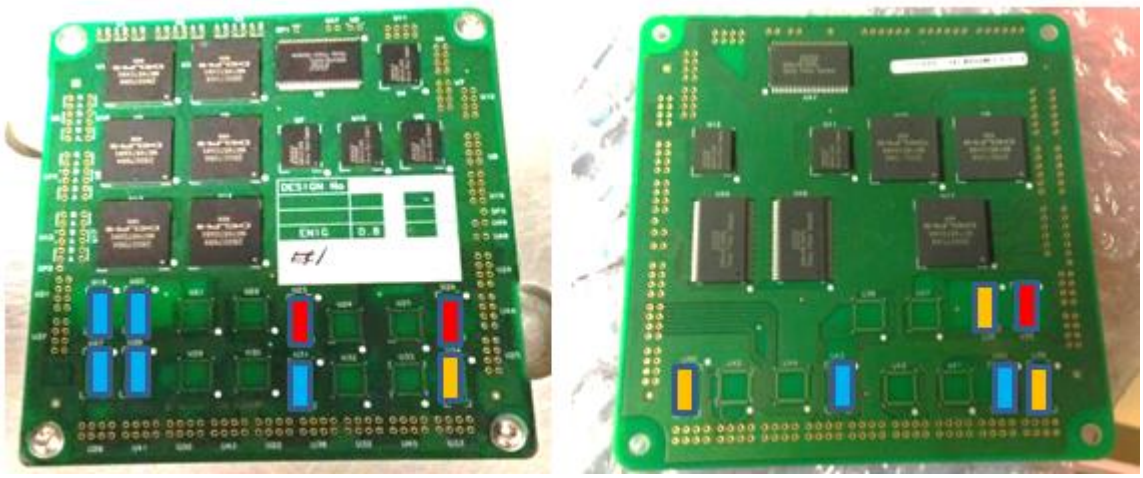


Figure 4.2b: 0.8 ENIG board layout with colour coded flip chip positions based on reliability

Once all the flip chips have been categorized based on the colour coded reliability measurement criteria, the next step was to analyze how the solder joints in each of the three types of flip chips degrade when subjected to vibration cycling. As was already discussed in details in the previous chapter, a few of the flip chips were through-life monitored using acoustic micro imaging. Hence, based on their reliability, three flip chips were selected for detailed failure analysis namely:

U19 – highly reliable

U34- medium reliability

U26- least reliable

Although U23 is the least reliable of all the flip chips, it has not been used for analysis purposes. This is because U23 fails only after 3 cycles. So, there are not enough data points for analysis purposes. Hence U26 was analysed.

The images obtained via through-life monitoring were then subjected to various stages of image processing, each of which will be discussed hereafter.

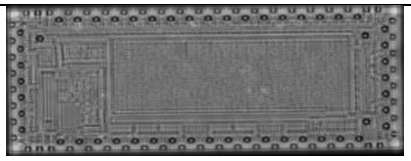
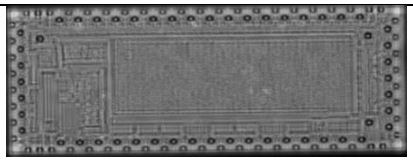
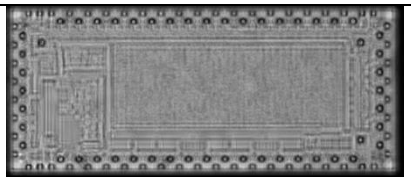
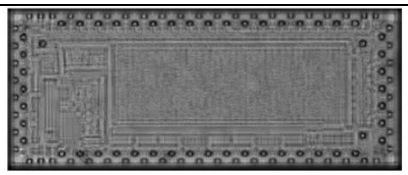
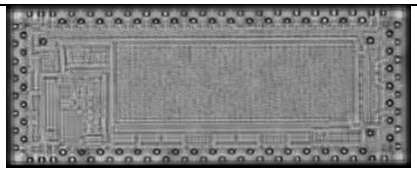
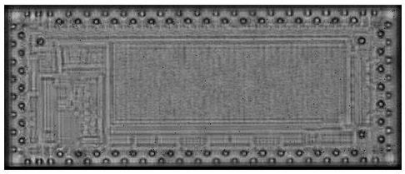
4.2.1 Image intensity equalization

As it will have been near impossible to keep the intensity and gain of the AMI system the same for all the scans that were done over a period of 12 months, image equalization is done. For this purpose, images at cycle 0, for each flip chip were taken as the reference. Then the mean intensities of all the other images were calculated. A scaling between each image with the reference image was determined by the formula**:**

Scaling factor(n) = mean_of_reference / mean_of_each image(n).

All the images were then multiplied with their corresponding individualized scaling to obtain the equalised images. Table 4.4 shows the comparison of the images with and without equalisation.

Table 4-4: Comparison of images with and without equalisation

Flip chip	Without equalisation	With equalisation
U19, cycle 0		
U19, cycle 10		
U19, cycle 65		

In order to ensure that the intensity equalization does not affect the final results, the maximum intensity plots for few of the solder joints of the flip chips were analysed.

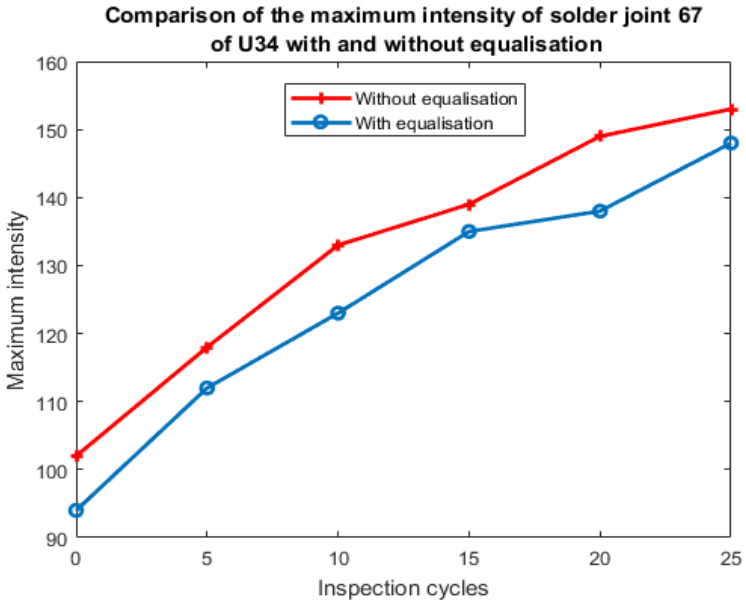


Figure 4.3: Comparison of the maximum intensity of the solder joint 67 of U34 with and without equalization

Figure 4.3 shows a comparison of the effect of equalization on the maximum intensity of a solder joint 67 of flip chip U34. As can be seen from the figure 4.3, as the number of vibration cycles increases, mean intensity equalization does not have any effect on the propagation pattern of the maximum intensity values. Since it does not affect the shape or propagation pattern, it will not have any effect on the results drawn from the data analysis. However, for analysis purposes only the mean intensity and area of the solder joints was used. This is because mean intensity and area are more reliable measures compared to maximum intensity whose values can be directly affected by any mismatches in the gain of the AMI system. Since the image analysis will be based on the area and hence the diameter of solder joints, the error rate in calculating the solder joint diameter was considered. Considering a measurement error of $\pm \mathbf{0.5}$ pixel per pixel in a solder joint, it can be seen from table 4.5 that as the diameter of the joint increases, the overall error rate decreases. Figure 4.4 shows the corresponding error plot.

Table 4-5: Error measurement in terms of area and circumference

Joint diameter, D=2r (in pixels)	Area= πr^2 $(pixel)^2$	Circumference, C=πD (pixels)	Error in C, E (±0.5 pixels)	% error=(E/A) x 100
10	78.5	31.42	15.71	20
20	314.2	62.83	31.42	10
30	706.9	94.25	47.1	6.67
40	1256.6	125.66	62.8	5
50	1963.5	157.08	78.5	4
60	2827.4	188.5	94.25	3

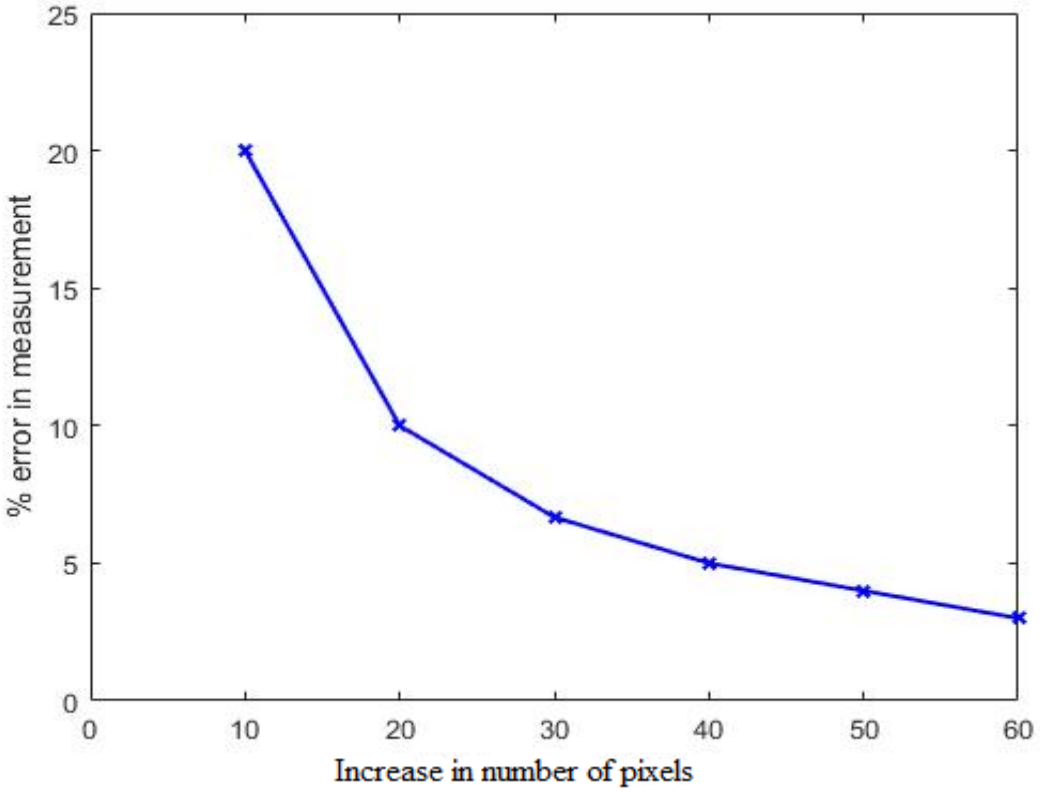


Figure 4.4: Error (%) in measurement of a solder joint area with the increase in the number of pixels

4.2.2 Joint selection and thresholding:

Once the intensity/gain mismatches were corrected as illustrated in section 4.2.1, the next step would be to select individual solder joints for degradation analysis. The joints to be analyzed are individually selected from the flip chips using MATLAB coding. Then further analysis is carried out, the first step of which is thresholding. Thresholding is a simple but effective technique of image segmentation. For most images, in general, the grey levels of pixels belonging to an object are substantially different from the grey level of the background. An appropriate threshold value can be set to differentiate the object and the background. For example, any pixels with values either greater than or less than a threshold value are treated as the main object and the rest are considered as background. The most important parameter in a thresholding technique is the decision of the threshold value. Many features in the image can be used to set the threshold parameter, e.g. histogram (Otsu, 1979; Glasbey, 1993) and gradient information (Henstock and Chelberg, 1996).

Otsu's thresholding technique is one of the most widely used thresholding technique in image processing that is used for converting greyscale images into binary images. Named after its developer, Nobuyuki Otsu, Otsu's method algorithm assumes that the image contains two classes of pixels that follow a bi-modal histogram namely foreground pixels and background pixels. It then calculates the optimum threshold value separating the two classes so that their combined spread (intra-class variance) is minimal, or equivalently (because the sum of pairwise squared distances is constant), so that their inter-class variance is maximal (Nobuyuki Otsu ,1979).

For the threshold that minimizes the intra-class variance (the variance within the class), defined as a
weighted sum of variances of the two classes:

$$\sigma_w^2(t) = \omega_0(t)\sigma_0^2(t) + \omega_1(t)\sigma_1^2(t) \qquad \text{Eq. 4-1}$$

Where,
Weights ω_0 and ω_1 are the probabilities of the two classes separated by a threshold *t*, and σ_0 and σ_1 are variances of these two classes.

The class probability $\omega_{0,1}(t)$ is computed from the bins L of the histogram of the image as

$$\omega_0(t) = \sum_{i=0}^{t-1} p(i) \qquad \text{Eq. 4-2}$$

$$\omega_1(t) = \sum_{i=t}^{L-1} p(i) \qquad \text{Eq. 4-3}$$

Otsu showed that minimizing the intra-class variance is the same as maximizing inter-class variance.

$$\begin{aligned}\sigma_b^2(t) &= \sigma^2 - \sigma_w^2(t) = \omega_0(\mu_0 - \mu_T)^2 + \omega_1(\mu_1 - \mu_T)^2 \\ &= \omega_0(t)\omega_1(t)[\mu_0(t) - \mu_1(t)]^2\end{aligned} \qquad \text{Eq. 4-4}$$

which is expressed in terms of class probabilities ω and class means μ .
while the class mean $\mu_{0,1,T}(t)$ is:

$$\mu_0(t) = \frac{\sum_{i=0}^{t-1} ip(i)}{\omega_0(t)} \quad \text{Eq. 4-5}$$

$$\mu_1(t) = \frac{\sum_{i=t}^{L-1} ip(i)}{\omega_1(t)} \quad \text{Eq. 4-6}$$

$$\mu_T = \sum_{i=0}^{L-1} ip(i) \quad \text{Eq. 4-7}$$

$$\omega_0\mu_0 + \omega_1\mu_1 = \mu_T \quad \text{Eq. 4-8}$$

$$\omega_0 + \omega_1 = 1 \quad \text{Eq. 4-9}$$

The class probabilities and class means can be computed iteratively which yields an effective algorithm as described below:

1. Histogram and probabilities of each intensity level of the image is to be calculated first.
2. Then the initial and $\omega_i(0)$ and $\mu_i(0)$ values are to be set.
3. Thereafter, all possible thresholds, t= 1,… maximum intensity needs to be stepped through by
   a. Updating ω_i and μ_i
   b. Computing $\sigma_b^2(t)$
4. The desired threshold will correspond to the maximum $\sigma_b^2(t)$.

Yang (Yang et. al 2012) in his thesis on the effects of thermal cycling on solder joints found that as the solder joints degraded their intensity increased drastically for fractured joints while there was not much change when it came to healthy joints. In order to verify, if this is also the case with vibration cycle and also to get a rough overview of how the flip chip intensities change with an increase in the number of vibration cycles, the greyscale AMI images are converted to binary images using OTSU's thresholding. The binary images are then masked over the original image to get a thresholded image using MATLAB. Figure 4.5 shows the implementation of Otsu's method and subsequent masking of the original image with Otsu's image. As can be observed from the image, Otsu's thresholding method provides a distinct region of interest for further image analysis.

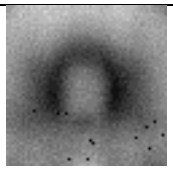
		
Flip chip U19, joint 67, cycle 0	Otsu masked image	Image obtained after placing the Otsu mask over the original image

Figure 4.5: Implementation of Otsu's method and masking

On implementing the Otsu and masking method to solder joint 67 of flip chip U19 over all the images obtained throughout vibration cycling, it can be seen from figure 4.6 that as the vibration cycling progresses, the intensity and area around the centre of the solder joint increases. The same pattern was generally observed with all 109 solder joints in all the flip chips across all the scans (about 100) that were selected for through life monitoring using AMI as was discussed in Chapter 3. This observation proves that just like in thermal cycling, in vibration cycling too, the intensity and area of the solder joints increases with vibration cycling and hence, these parameters can be used to analyze the degradation pattern of the solder joints.

The region of interest is grey region inside the black ring obtained after Otsu's thesholding. Hence the next stage would be to isolate this region of interest for further processing.

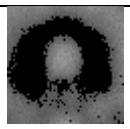
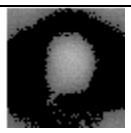
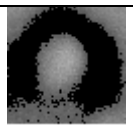
					
Cycle 0	Cycle 10	Cycle 20	Cycle 25	Cycle 30	Cycle 35
					
Cycle 40	Cycle 45	Cycle 50	Cycle 55	Cycle 60	Cycle 65

Figure 4.6: Implementation of Otsu's thresholding and masking on joint 67 of flip chip U19 at different vibration test cycles

4.2.3 Selecting the region of interest using masking:

As discussed in section 4.2.2, the joints to be analysed are individually selected using MATLAB coding. It was found that a rectangular area of 60x60 pixels is enough to isolate one solder joint. An adjustable elliptical mask is then used to separate out the region of interest as shown in figure 4.7. As the region of interest is almost never a circular region, using an adjustable elliptical mask helps in seperating out a more accurate region of interest as illustrated in figure 4.7:

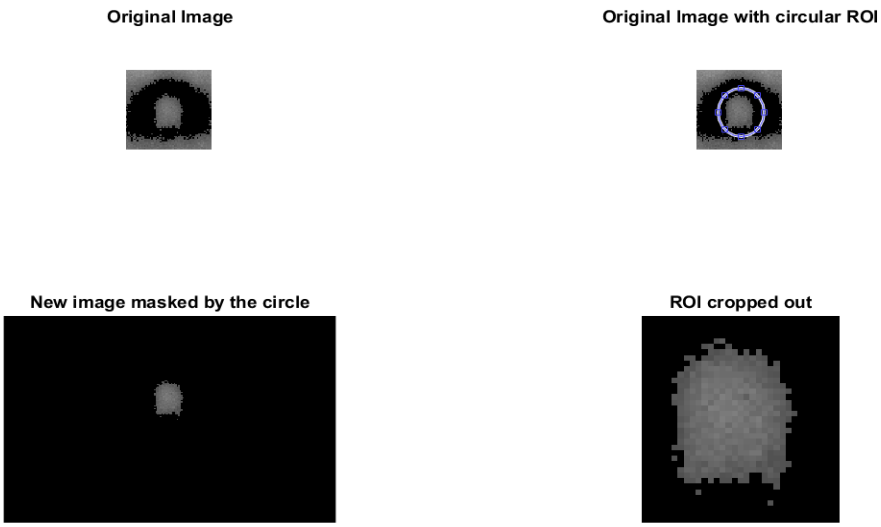


Figure 4.7: Selection of the region of interest(ROI) in a solder joint

As mentioned in section 4.2.2, the grey region inside the black ring obtained after Otsu's thesholding and subsequent masking with the original image of the selected solder joint is the region of interest which is then extracted using elliptical masking. As was discussed in Chapter 2, in AMI, the strength of the reflected echoes provide information about the surface type of the object under test. Hence, in case of solder joints, higher the strength of the refelected echoes from the surface of the solder joint, the higher the intensity of the resultant ultrasound image. The higher the intensity of the resultant image, the greater the chances of crack formation and propagation. This is because, as soon as cracks start forming in the solder joints, the strength of the ultrasonic echoes reflected from the grey region of interest in the solder joints will increase resulting in higher intensity reflections which will further increase as the crack propagates. That is why, it can be concluded that the mean pixel intensities and the histogram of the solder joint images are very important features in determining the degradation pattern of the solder joints. In addition to intensity, the size or area of the

region of interest will also increase as the crack propagates which can be clearly seen from the results of Otsu thresholding shown in figure 4.4 section 4.2.2. Hence area is an important feature to be considered while analysing the degradation of solder joints.

4.2.4 Mean intensity scatter plot and histogram analysis

As was discussed in section 4.1, based on reliability criteria three flip chips were selected for further image processing viz. U19(most reliable), U34(medium reliability) and U26(least reliable). From hereafter, only the results pertaining to U19, U34 and U26 will be discussed in details.

After extracting the region of interest as illustrated in section 4.2.3, the mean intensity of all the solder joints in all the flip chips under consideration were calculated. Figure 4.8 shows a scatter plot for the mean intensity variation of all the solder joints of U19 at cycle 0, before the test and at cycle 65, the last test cycle before complete failure. From the mean intensity calculation of the solder joints, it can be seen that as the vibration cycling progresses and flip chips start to fail, three types of solder joints can be identified.

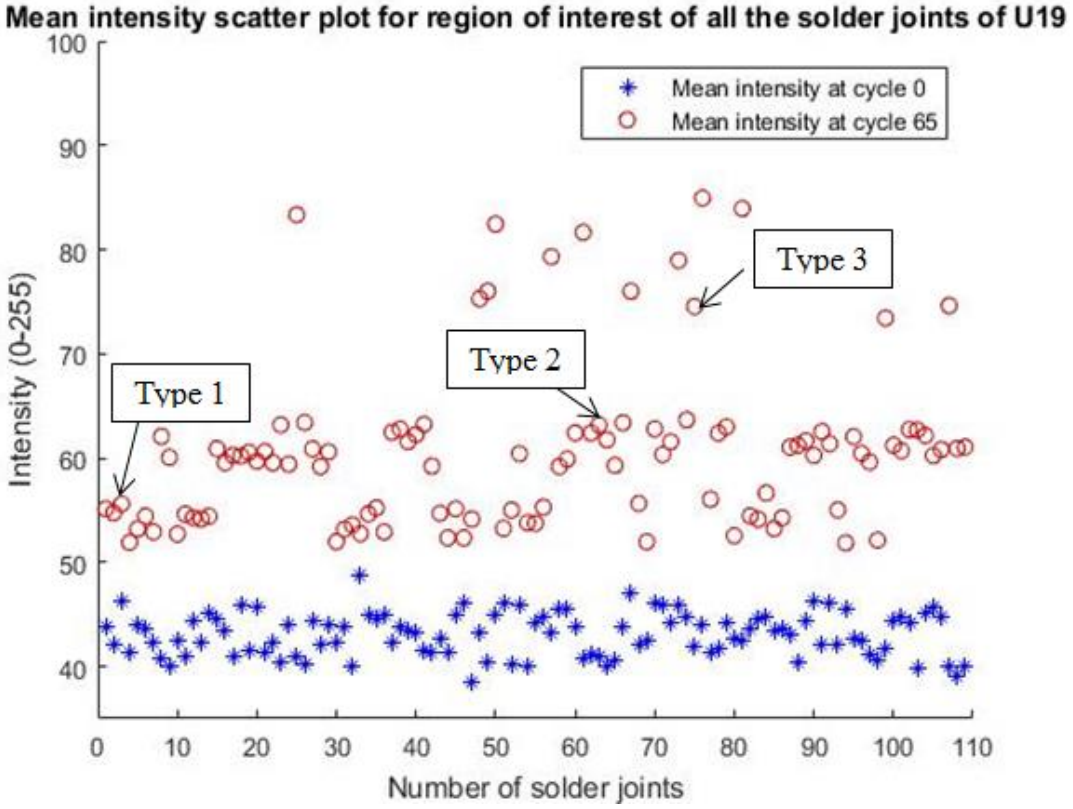


Figure 4.8: Mean intensity scatter pot for all the joints of U19

In order to determine the characteristics of these three types of joints histogram analysis of the solder joints was done at cycle 0 and at the last scan cycle data obtained just before complete failure for U19, U34 and U26. From the analysis three joints have been selected that can clearly define the characteristics of the three types of solder joints formed during cycling. They are joints 67, 84 and 108. Each flip chip and the relative position of the selected joints in the flip chip are shown in figure 4.9. It should be noted the solder joint orientation for all the flip chips is the same.

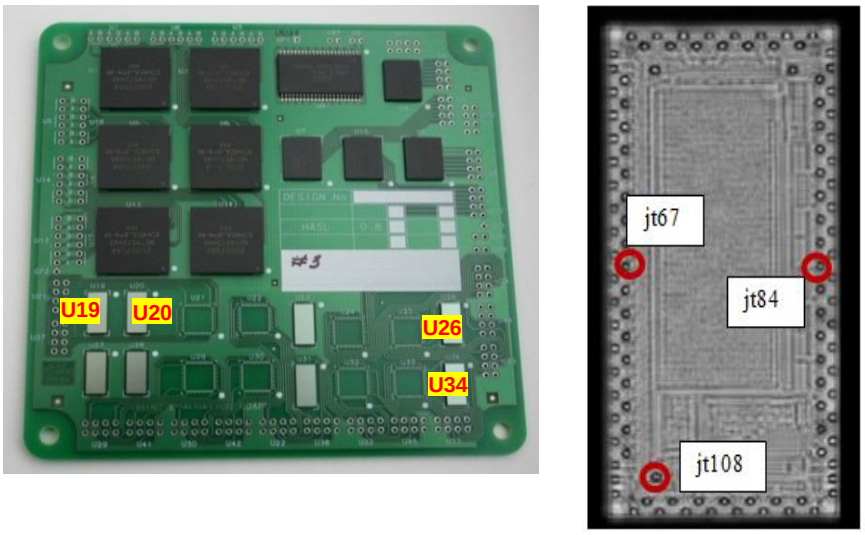
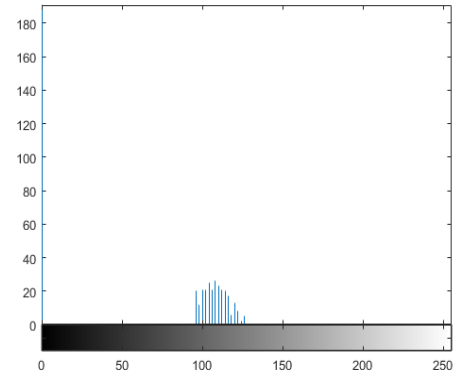
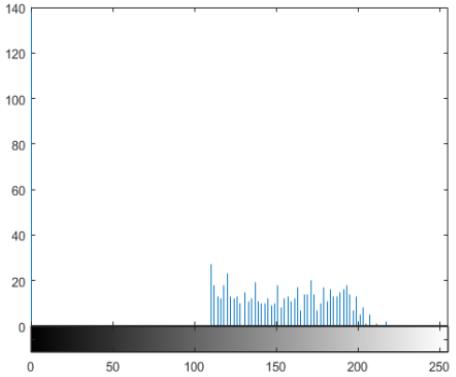
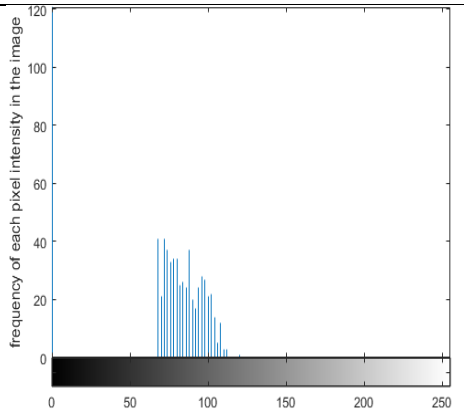
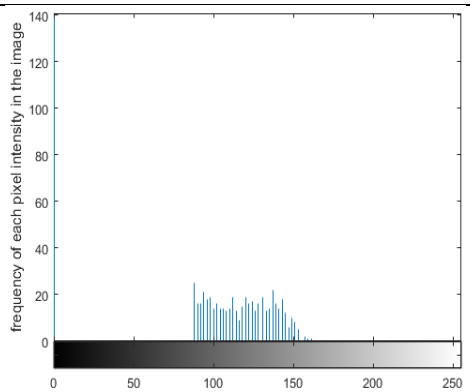
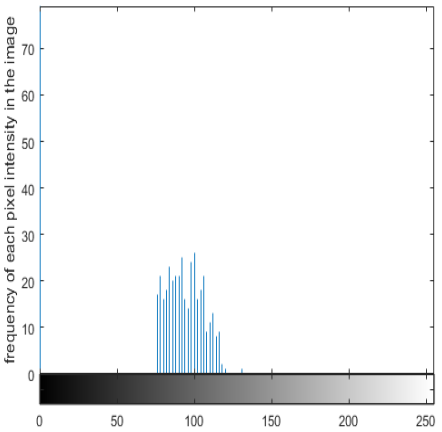
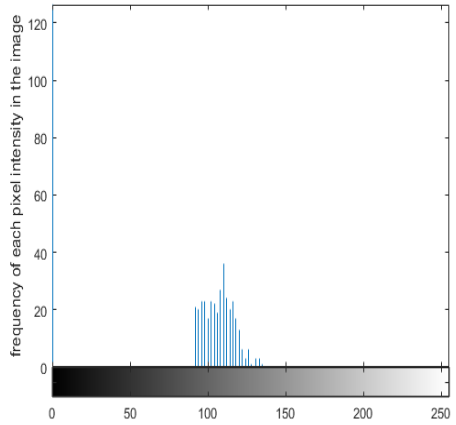


Figure 4.9: Selected flip chips and solder joints for further analysis

The reason for selecting the joints 67, 84 and 108 is that joints 67 and 84 are close to the neutral point of the flip chip which is the point at the centre, but are also placed exactly opposite to each other. As a result depending on the FC position, while one of them is near the edge of PCB the other is at the end away from the PCB edge. Hence analyzing them not only showed the individual degradation pattern of the solder joints but also the degradation pattern with respect to the position of the FC in the PCB. Joint 108 was chosen because it is placed towards the corner of the FC but also is placed far away enough to eliminate any possible 'edge' effects.

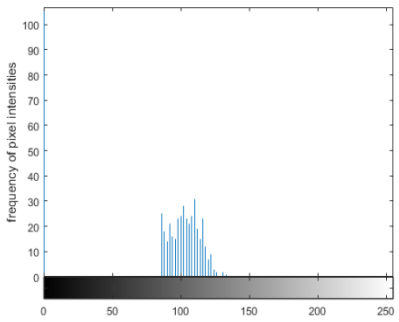
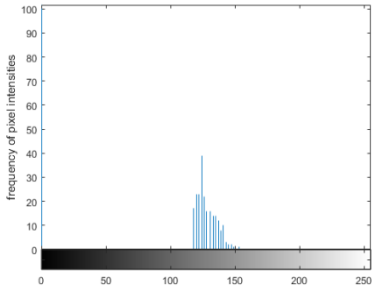
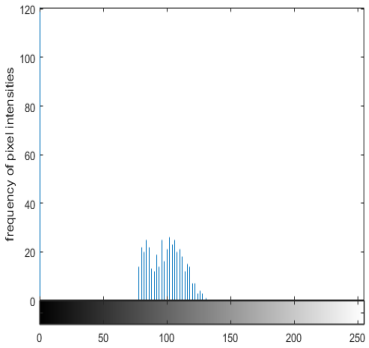
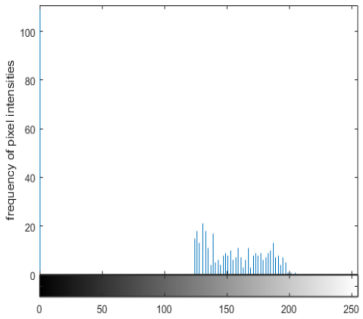
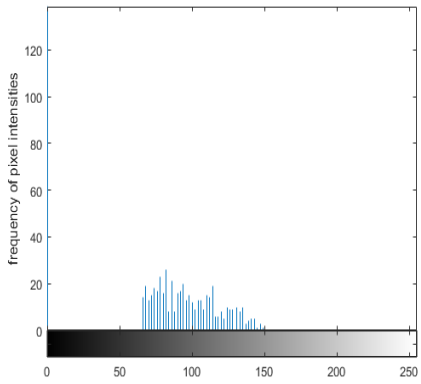
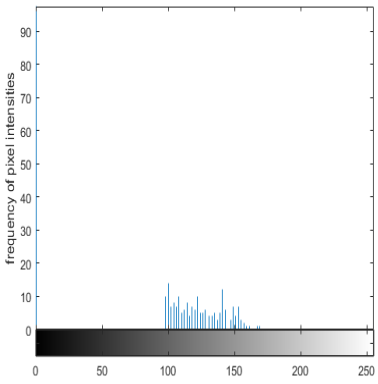
Tables 4-6 to 4-8 shows the results obtained from the histogram analysis of these three joints for each of the flip chips U19, U34 and U26.

Table 4-6 :Histogram analysis for U19 at cycle 0 and cycle 65 (X axis represents pixel intensity and Y axis represents the frequency of each pixel intensity in the image)

Joint no.	Cycle 0	Cycle 65
67		
108		
84		

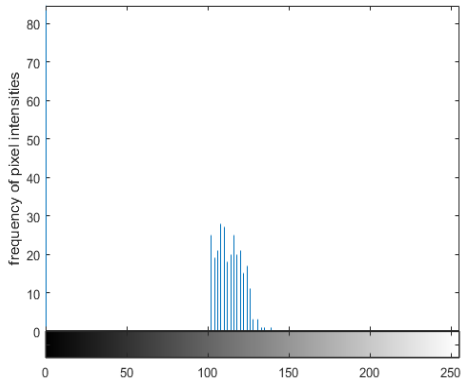
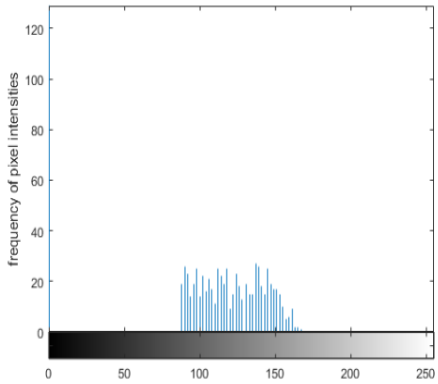
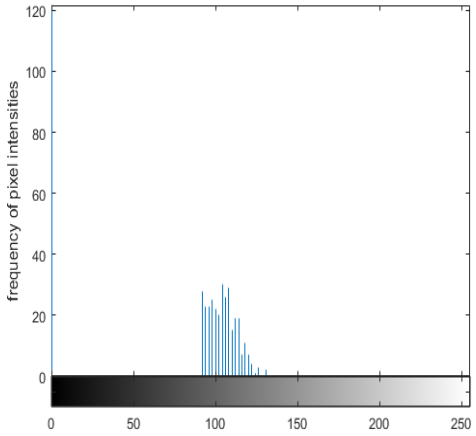
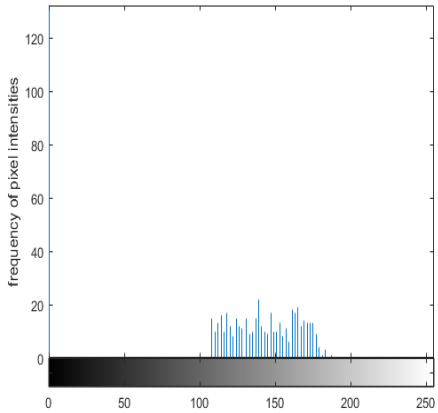
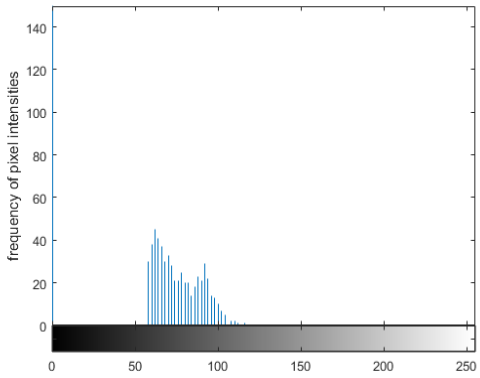
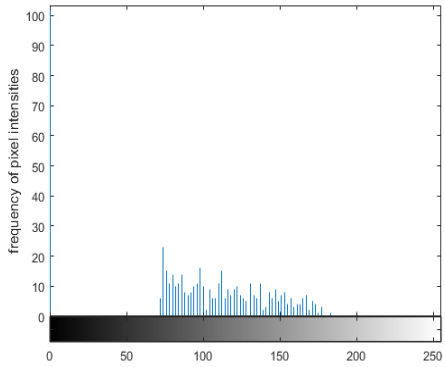
For joint 67, the centre frequency shifts from 112 at 0 cycles to 175 at 65 cycles (56% increase). For joint 108, the centre frequency shifts from 90 at 0 cycles to 125 at 65 cycles (38% increase) and for joint 84, the centre frequency shifts from 95 at 0 cycles to 110 at 65 cycles (15% increase)

Table 4-7 :Histogram analysis for U34 at cycle 0 and cycle 25

Joint no.	Cycle 0	Cycle 25
67		
84		
108		

For joint 67, the centre frequency shifts from 112 at 0 cycles to 130 at 25 cycles (16% increase). For joint 84, the centre frequency shifts from 100 at 0 cycles to 170 at 25 cycles (70% increase) and for joint 108, the centre frequency shifts from 100 at 0 cycles to 125 at 25 cycles (25% increase).

Table 4-8 :Histogram analysis for U26 at cycle 0 and cycle 12

Joint no	Cycle 0	Cycle 12
67		
108		
84		

For solder joint 67, the centre frequency shifts from 112 at 0 cycles to 125 at 12 cycles (11.6% increase). For joint 108, the centre frequency shifts from 105 at 0 cycles to 145 at 12 cycles (38.1% increase) and for joint 84, the centre frequency shifts from 75 at 0 cycles to 130 at 65 cycles (73.33% increase).

From the histogram analysis of the solder joints of the flip chips, three of which has been discussed in detail so far it can be concluded that as vibration cycling progresses, three types of solder joints are indeed formed near the time of complete failure of a flip chip:

a. Type 1: Joints that show 9% -18% increase in intensity with cycling
b. Type 2: Joints that show 25% - 40% increase in intensity with cycling
c. Type 3: Joints that show 55% - 80% increase in intensity with cycling

When the number of type 2 and type 3 joints exceed the number of type 1 joints, a flip chip fails. Based on the research conducted by Yang (2012) it was found that solder joints that showed a very low change in intensity at the end of ATC relative to the intensity calculated before the test were actually healthy joints that survived ATC while those that showed very high change in intensity at the end of ATC were fractured joints. Going by that logic, it can be argued that Type 1 joints, in the case of vibration cycling too, actually represent the healthy joints while type 3 will represent the fractured joints. Type 2 therefore will be used to represent partially fractured joints. Accordingly the following table 4-9 classifies the joints 67,84 and 108 of U19, U34 and U26 into types 1, 2 and 3.

Table 4-9 : Classification of joints into types 1,2,3

Flip chip name	Type 1 joint/healthy	Type 2 joint/ Partially fractured	Type 3 joint/ fractured
U19	84	108	67
U34	67	108	84
U26	67	108	84

An interesting finding was observed from the results in table 4-9. Joint 67 of U19 and joint 84 of U34 and U26 behaved very similarly as they are both positioned near the edge of the PCB which brought about earlier failure compared to the joint 84 of U19 and joint 67 of U34 and U26 that are located at the exact opposite side but away from the PCB edge. This phenomenon will be further discussed in detail in section 4.4 of the chapter.

Now that the types of joints formed during vibration cycling have been classified, the next step would be to see how and when the crack forms and propagates in a particular solder joint. Mean intensity and area analysis of the solder joints gives us that solution.

4.2.5: Mean intensity and area analysis:

As in histogram analysis, the same flip chips U19, U34 and U26 and solder joints 67, 84 and 108 will again be used to illustrate the results for mean intensity and area analysis

Figures 4.10 to 4.15 illustrate the measured mean intensity values of the three solder joints at every vibration cycle up to complete failure.

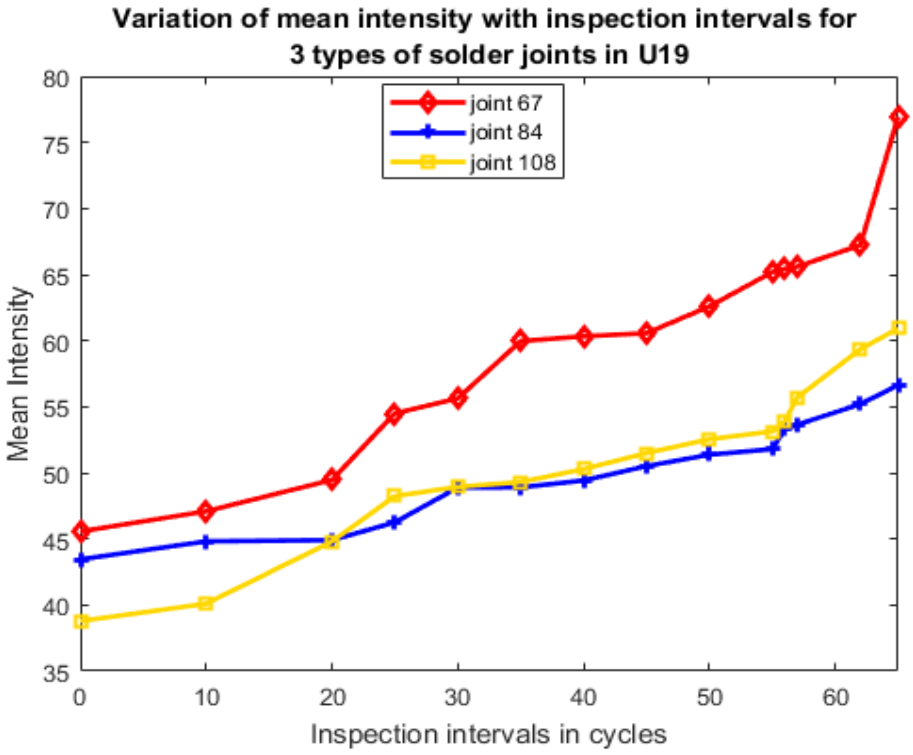


Figure 4.10: Mean intensity plot for joints 67, 84 and 108 of U19

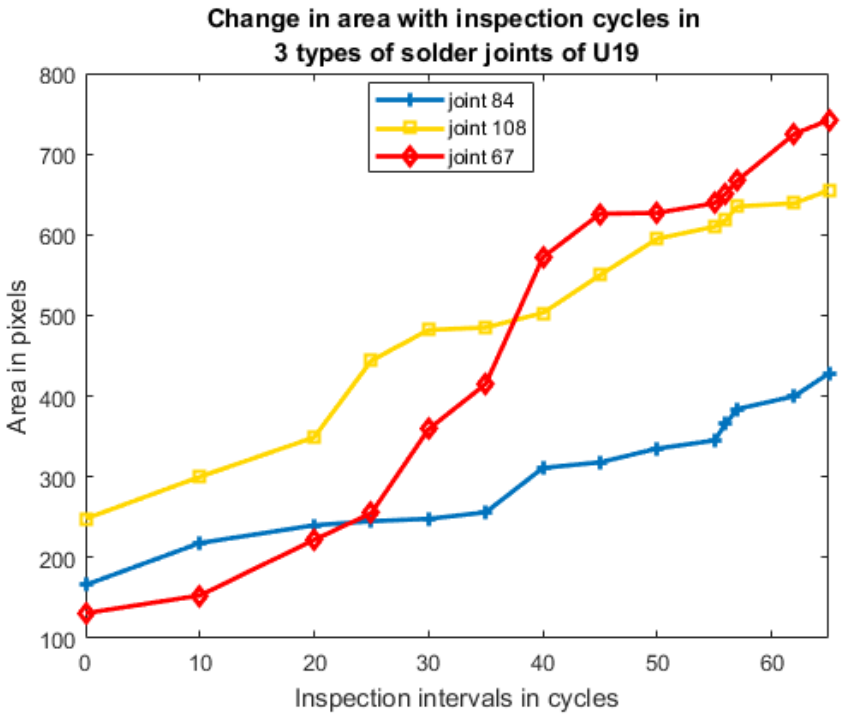


Figure 4.11: Area plot for joints 67, 84 and 108 of U19

From the mean intensity and area plots of U19, it can be clearly seen that the first abrupt change in gradient of mean intensity/area, which will henceforth be referred to

as the first trigger point occurs at 25 cyles (38.5% cycling) while the second abrupt gradient change which will be referred to as the second trigger point occurs at 55 cycles (84.5% cycling) for all the joints 67, 84 and 108.

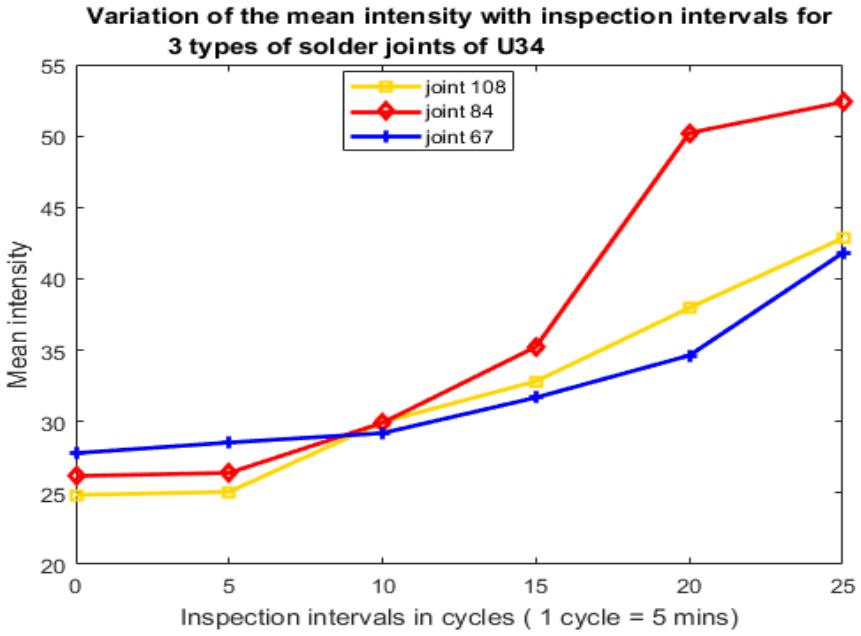


Figure 4.12: Mean intensity plot for joints 67, 84 and 108 of U34

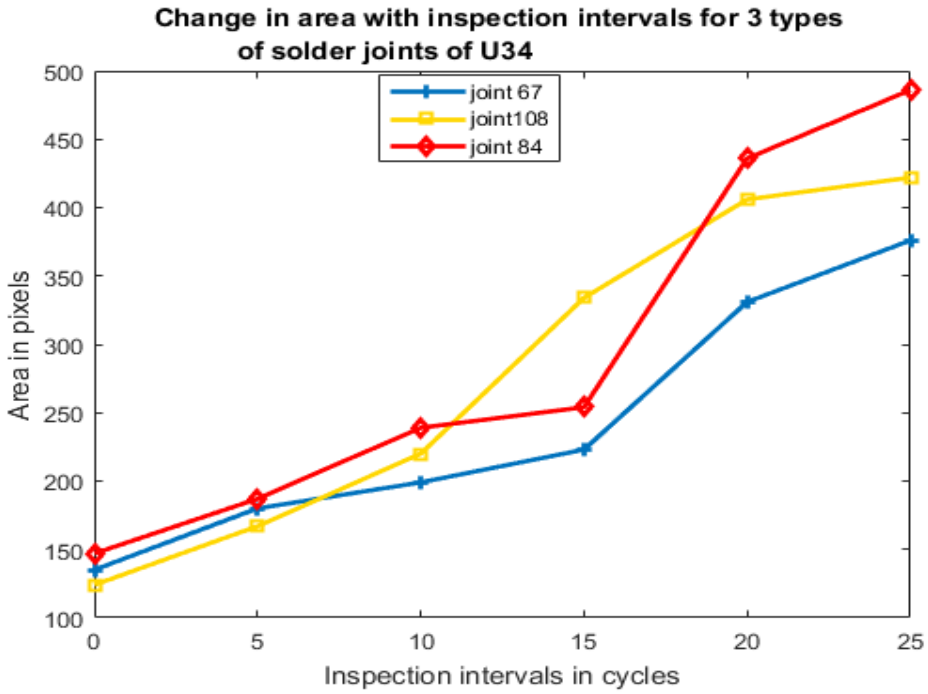


Figure 4.13: Area plot for joints 67, 84 and 108 of U34

For fip chip U34, the first trigger point occurs at 10 cyles (40% cycling) while the second trigger point occurs at 20 cycles (80% cycling).

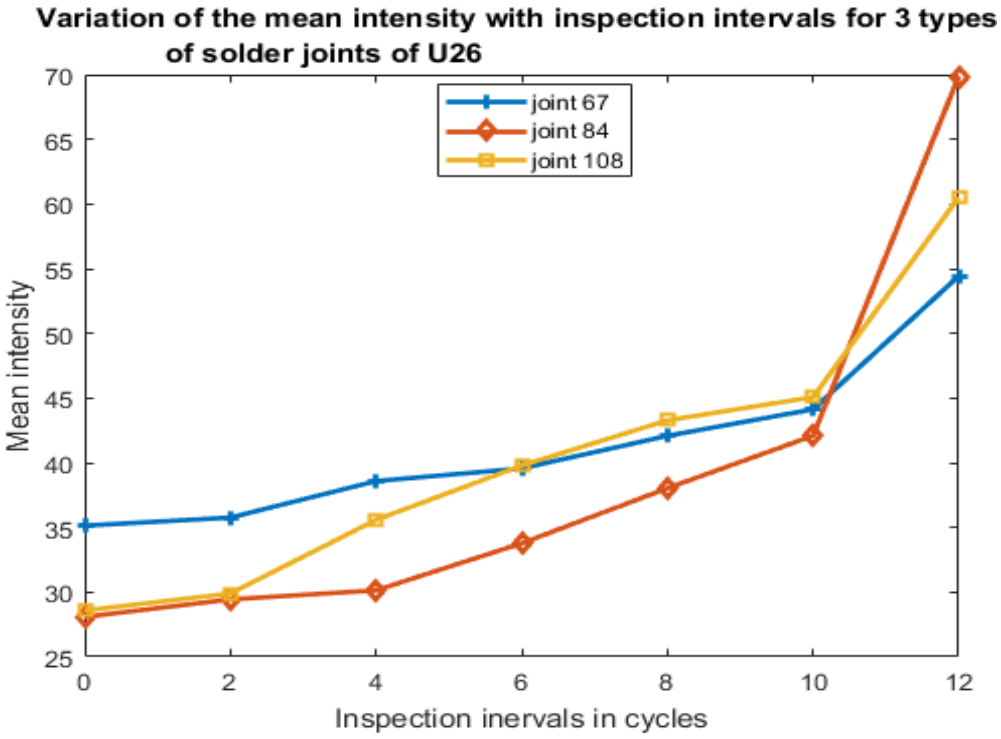


Figure 4.14: Mean intensity plot for joints 67, 84 and 108 of U26

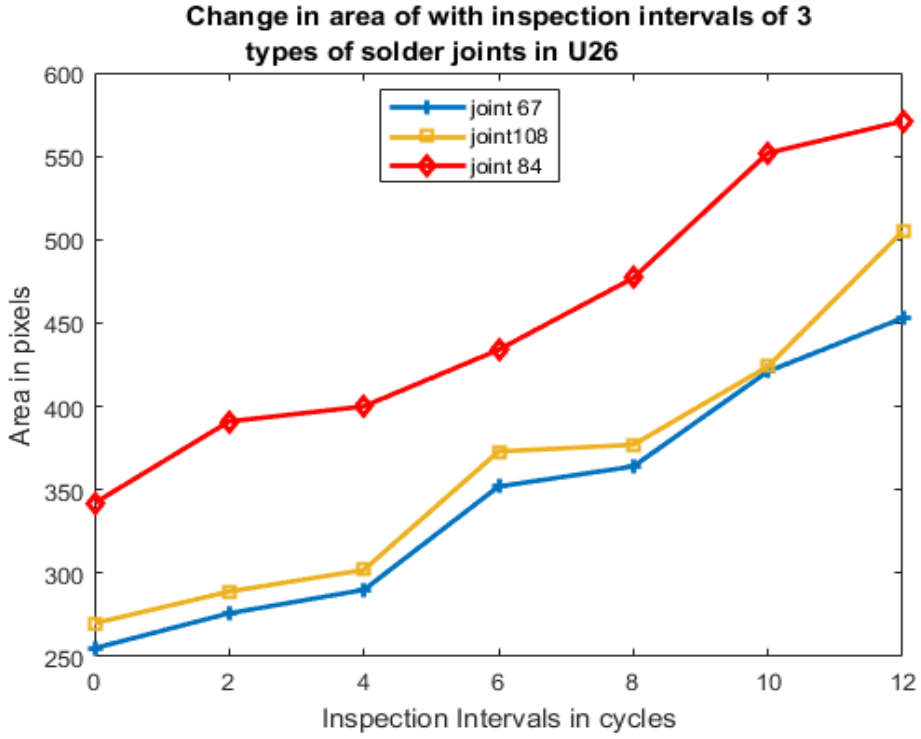


Figure 4.15: Area plot for joints 67, 84 and 108 of U26

For U26, the first trigger point occurs at 4 cyles (33.3% cycling) while the second trigger point occurs at 10 cycles (83.33% cycling).

The abrupt increase in the mean intensity and area with the increase in the number of vibration cycles at the first and second trigger points of all the solder joints, clearly suggests the origin and propagation of cracks. However, depending on the type of solder joint as healthy, partially fractured or fractured, the resultant rise in mean intensity or area varies, which further validates the results obtained from the histogram analysis of the solder joints discussed in the previous section. For all types of joints in a flip chip, the first trigger point occurs at around 35-40% cycling and second change occurs at around 80-85% cycling. Thus the failure pattern of any solder joint can be loosely said to fall into three regions. The region between 0 cycle and first trigger point where the crack initiates, the region between the first and second trigger point where the crack propagates and finally the region after the second trigger point where the crack formed reaches its peak and finally the flip chip fails.

4.3 Statistical analysis

In order to further verify and solidify the results obtained so far, a 3D surface intensity plot was generated for a solder joint at cycle 0 as shown in figure 4.16.

3D pixel intensity plot for joint 84 of flip chip U19, cycle 0

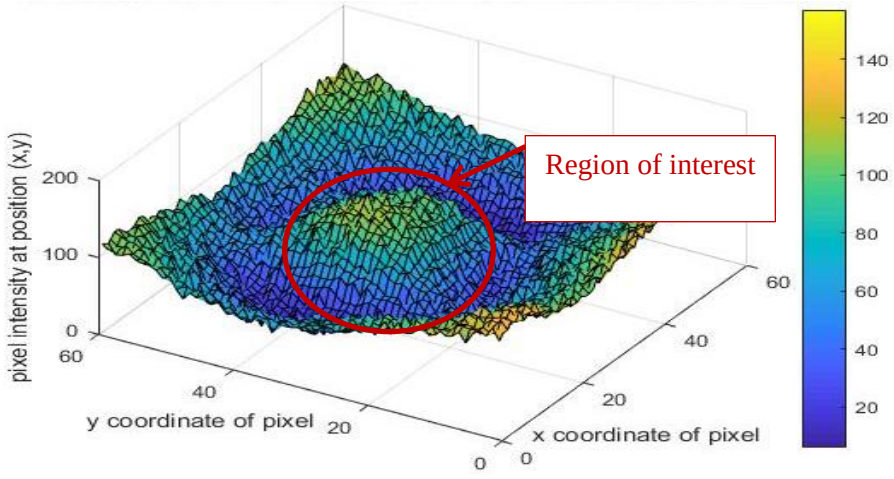


Figure 4.16: 3D pixel intensity plot of solder joint 84 of U19

From the 3D surface intensity plot, it can be seen that just like most natural processes, the intensity distribution of the region of interest also follows a bell shape. Hence it can be approximated by a normal or Gaussian distribution.

The Gaussian (or Normal) distribution is the most commonly encountered continuous distribution in real life processes and is considered to be a reasonable model for many situations. If a (scalar) variable 'x' has a first order Gaussian distribution, then it has a probability density function p(x) given by:

$$p(x) = \frac{1}{\sqrt{2\pi\sigma^2}} exp\left(\frac{-(x-\mu)^2}{2\sigma^2}\right) \quad \text{Eq. 4-10}$$

Where, μ and σ are the mean and standard deviation of the distribution.

Although, data measurements of many properties are often normally distributed, sometimes, with heterogeneous populations, data measurements reflect a mixture or sum of normal distributions (Earl F. Glynn, 2007). For example: Consider a population that is a mixture or sum of two Gaussian distributions. Y = p(x; 3.75, 0.75) + n(x; 6.00, 0.50). Figure 4.17 below shows a graphical representation of y.

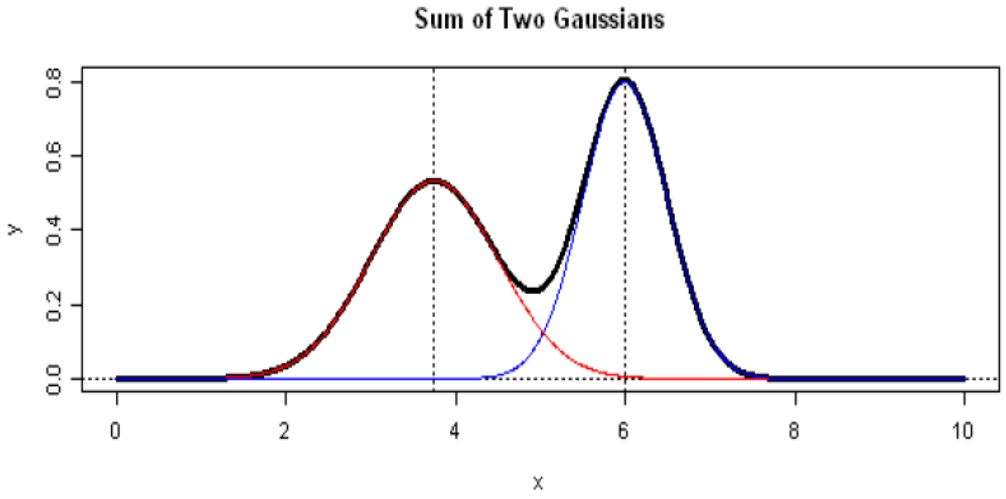


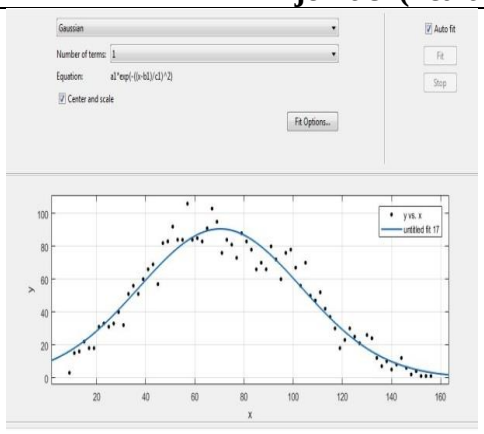
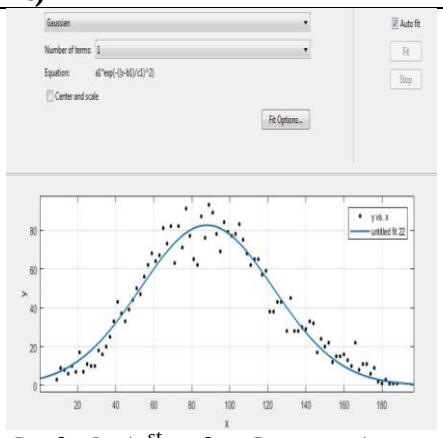
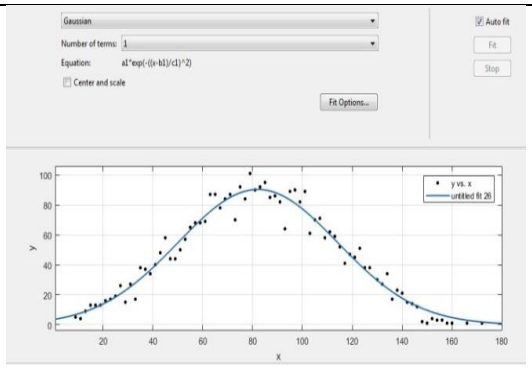
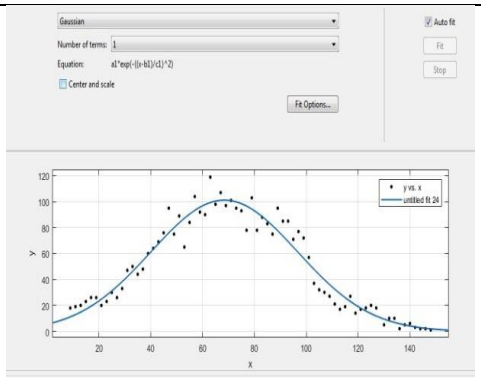
Figure 4.17: Graphical representation of the sum of 2 Gaussian distributions (Earl F. Glynn,2007)

In the experimental analysis, some of the distributions of the solder joints were found to show behaviours of mixed Gaussian distributions.

Now, based on the observations of histogram analysis, three types of solder joints were identified in a flip chip namely; healthy, partially fractured and fractured. A statistical analysis was done on the same three sample joints namely, joint 67, 84 and 108 of flip

chip U19 to observe their statistical behaviour with the increase in vibration cycling. For this purpose, the 'cftool' function of the statistical toolbox of MATLAB was used. Firstly, the probability distribution of each of the solder joints for various vibration cycles was obtained using MATLAB coding and then using 'cftool', the nearest Gaussian fit for the each probability distribution was obtained. Table 4-10, 4-11 and 4-12 shows the approximation results for joints 84, 108 and 67 of U19 respectively. The X-axis represents the intensity values while the Y axis represents the frequency of each intensity value found in the region of interest of the solder joint.

Table 4-10: Statistical approximation of the pixel intensity distribution of solder joint 84(healthy joint)

 Cycle 0(1st order Gaussian)	 Cycle 35(1st order Gaussian)
 Cycle 40(1st order Gaussian)	 Cycle 50(1st order Gaussian)

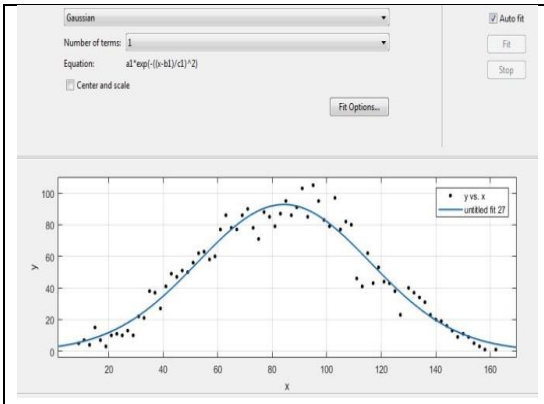
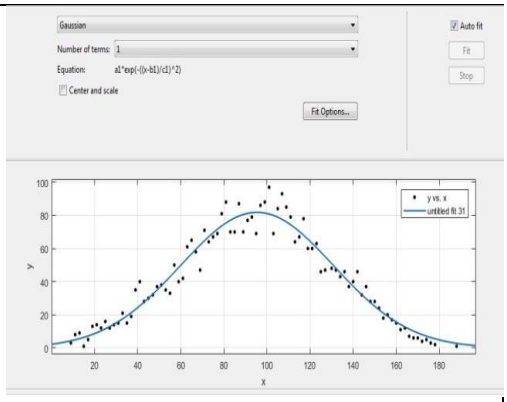
	
Cycle 55(1st order Gaussian)	Cycle 65(1st order Gaussian)

Table 4-11: Statistical approximation of the pixel intensity distribution of solder joint 108 (partially fractured joint)

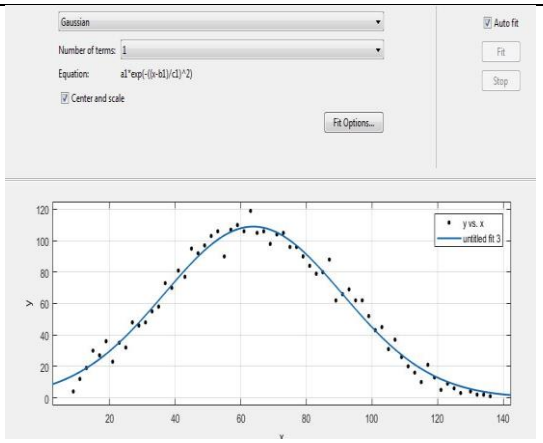
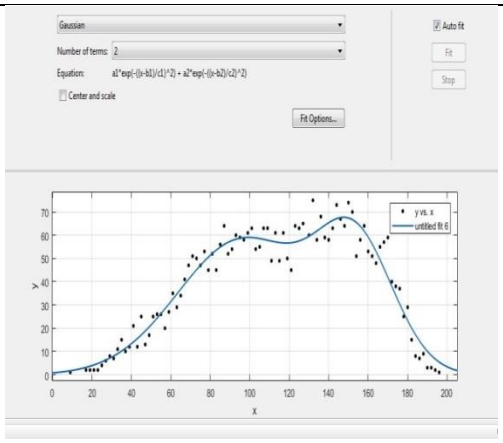
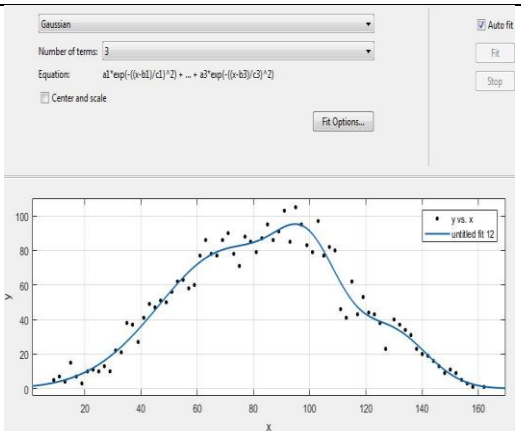
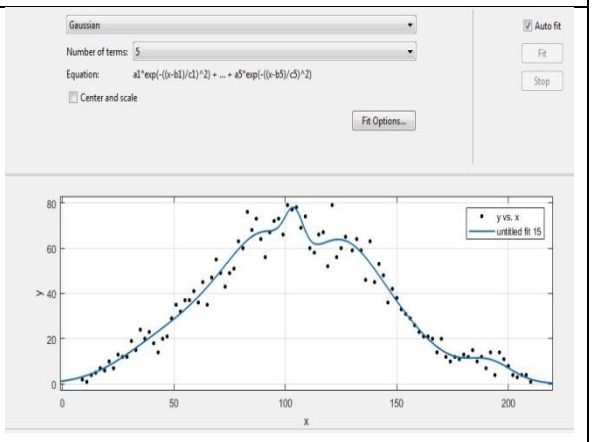
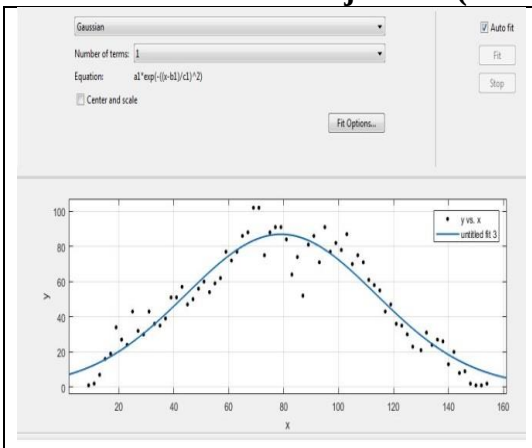
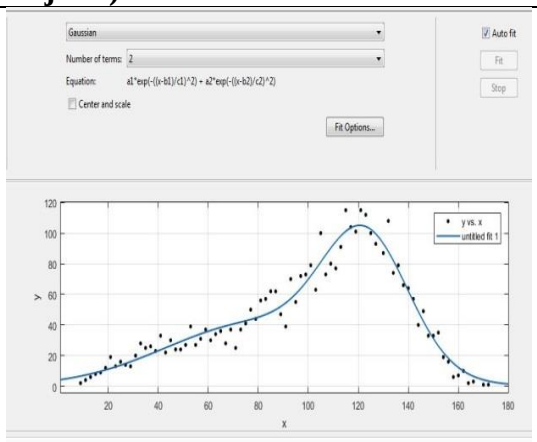
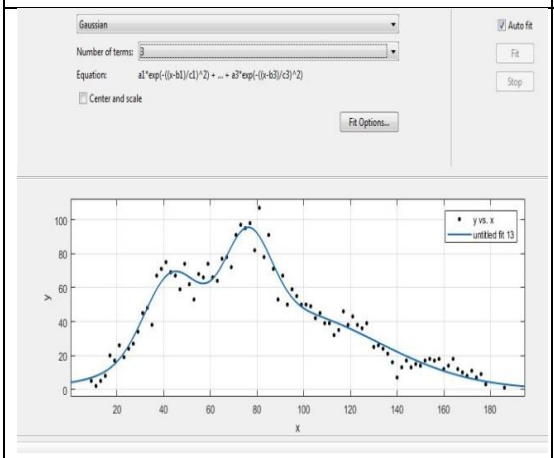
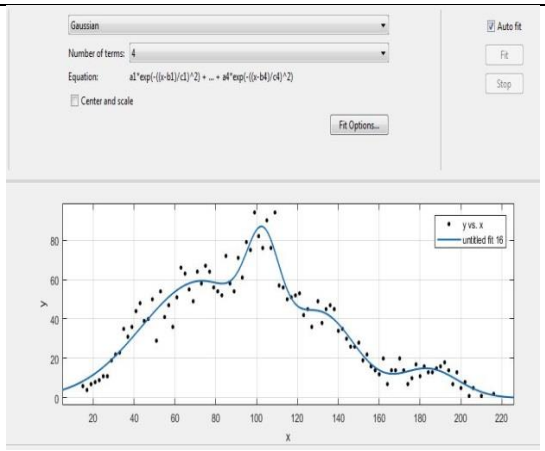
	
Cycle 0(1st order Gaussian)	Cycle 25(Sum of two 1st order Gaussians)
	
Cycle 55(Sum of three1st order Gaussians)	Cycle 65(Sum of five 1st order Gaussians)

Table 4-12: Statistical approximation of the pixel intensity distribution of solder joint 67 (fractured joint)

 Cycle 0(1st order Gaussian)	 Cycle 25(Sum of two 1st order Gaussians)
 Cycle 55(Sum of three 1st order Gaussians)	 Cycle 65(Sum of four 1st order Gaussians)

As was shown in the histogram analysis, in case of U19, joint 84 is a type 1 or healthy joint, joint 108 is a type 2 or partially fractured joint and joint 67 is a type 3 or fractured joint. Again based on mean intensity and area analysis, we found that crack initiation occurs at the first trigger point (35%-40% vibration cycling) and it propagates till the second trigger point (80%-85% cycling) after which it fails. For U19, the first trigger point was noticed at 25 cycles and the second trigger point was noticed at 55 cycles.

From the statistical analysis, it can be seen that for the healthy joint 84, the probability distribution exhibits the behaviour of a first order Gaussian distribution all throughout the test cycles. This is because in the case of a healthy joint the intensity distribution

does not shift a lot when compared to that at cycle 0 as was seen from their histogram plots. But for partially fractured and fractured joints 108 and 67, as the crack propagates, shift in the intensity distribution increases and hence, it loses the properties of a normal Gaussian distribution and can only be represented by a mixture combination of Gaussian distributions. The statistical analysis hence further validates the results obtained from step histogram analysis. Furthermore, with the crack initiation at cycle 25, the intensity distribution also changes for fractured joints 67 and 108 from cycle 25 while it remains the same throughout for healthy joint 84 which validates the findings of mean intensity and area analysis.

4.4 Analysis of solder joints according to their positions and orientations in the PCB

So far in the analysis, focus has been given only on the generic reliability of flip chips and the solder joints irrespective of their positions in the PCB or their orientations. In this section, these factors will be taken into account. As was discussed in details in chapter 3, the PCBs used for the experiment have 14 flip chips each of which are placed in different positions in the PCB and also have different relative orientations. Although only the 0.8mm ENIG board was used for the experiment, a pre-test was done with 0.8mm HASL board as well. However, in case of the 0.8mm HASL board, through life monitoring using AMI was not completed. Still, based only on the results of vibration cycling, very fruitful comparisons can be drawn, that provide interesting insights into the relationship of the reliability of a flip chip with its position in the test board/PCB and also with its relative orientation. Table 4-13 shows a comparison of the time taken for failure of all the flip chips in cases of 0.8 ENIG and 0.8 HASL board. Figures 4.18, 4.19, 4.20 and 4.21 further provide a graphical representation of the failure patterns for each of the boards.

Table 4-13: Comparison of failure times of 0.8mm ENIG and 0.8mm HASL boards

0.8mm ENIG flip chip no.	Cycles to failure	Failure time in hours	0.8mm HASL flip chip no.	Cycles to failure	Failure in hours
U23	3	0.2	U23	4	0.267
U26	14	0.933	U26	27	1.8
U35	21	1.4	U27	51	3.4
U39	23	1.533	U34	57	3.8
U46	24	1.6	U19	101	6.733
U34	29	1.933	U28	103	6.867
U36	34	2.267	U20	122	8.133
U27	45	3	U46	130	8.667
U43	48	3.2	U36	268	17.867
U20	53	3.533	U39	278	18.533
U31	55	3.667	U35	294	19.6
U40	57	3.8	U31	311	20.733
U19	68	4.533	U43	316	21.067
U28	86	5.733	U40	380	25.333

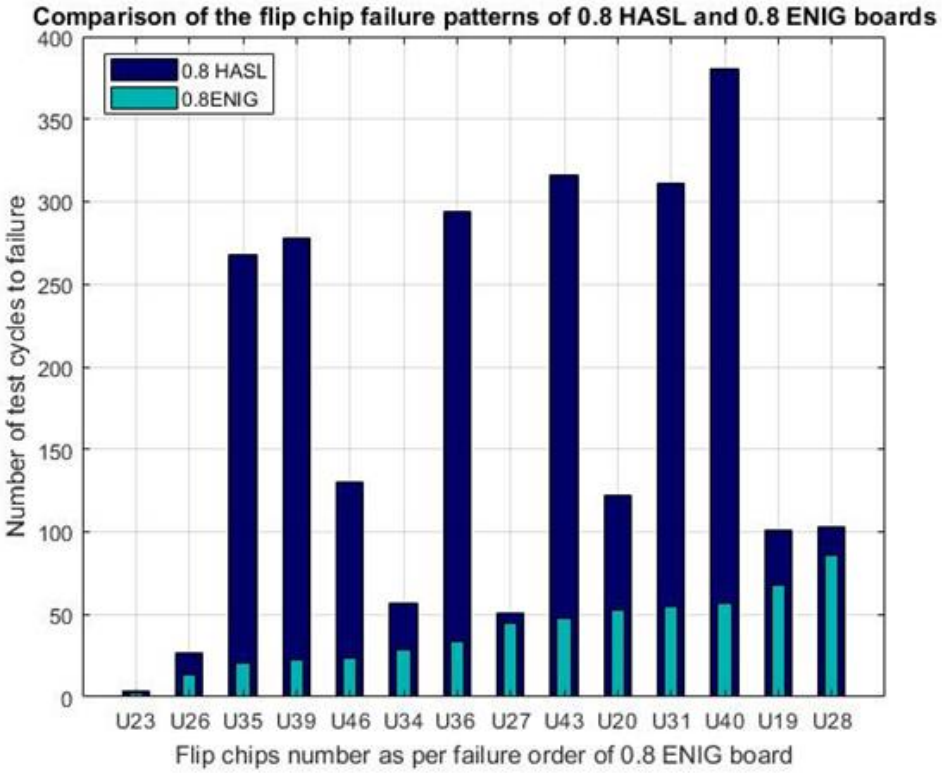


Figure 4.18: Comparison of the failure pattern of flip chips in 0.8 ENIG and 0.8 HASL

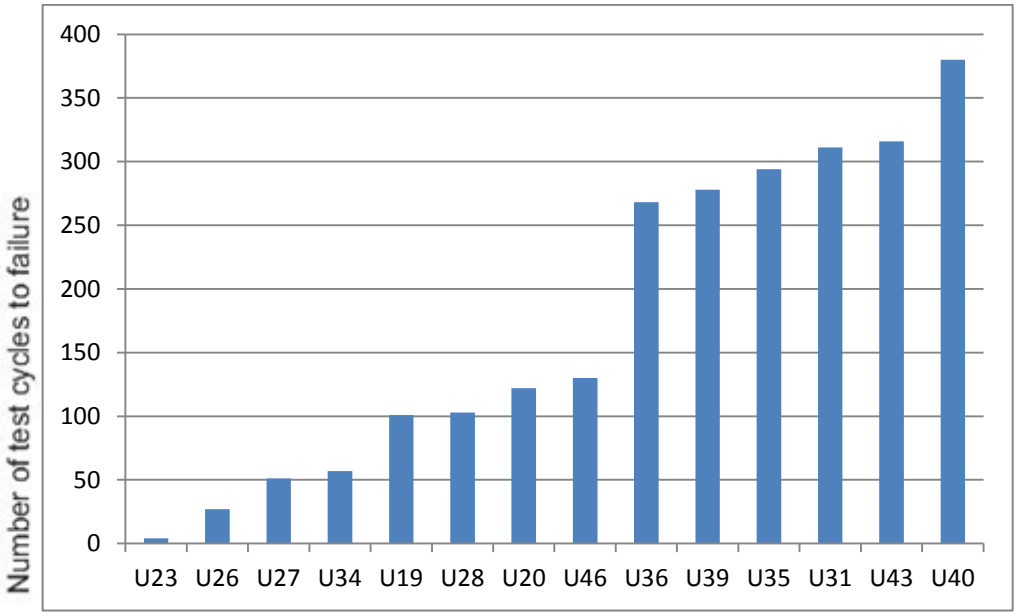


Figure 4.19: Failure order of flip chips for 0.8HASL board

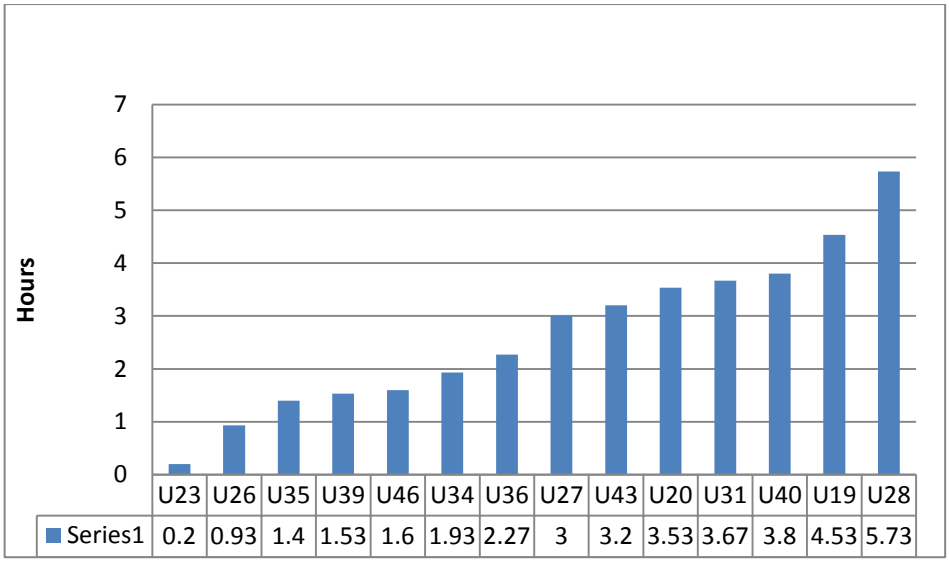


Figure 4.20: Failure time of flip chips in 0.8 ENIG board

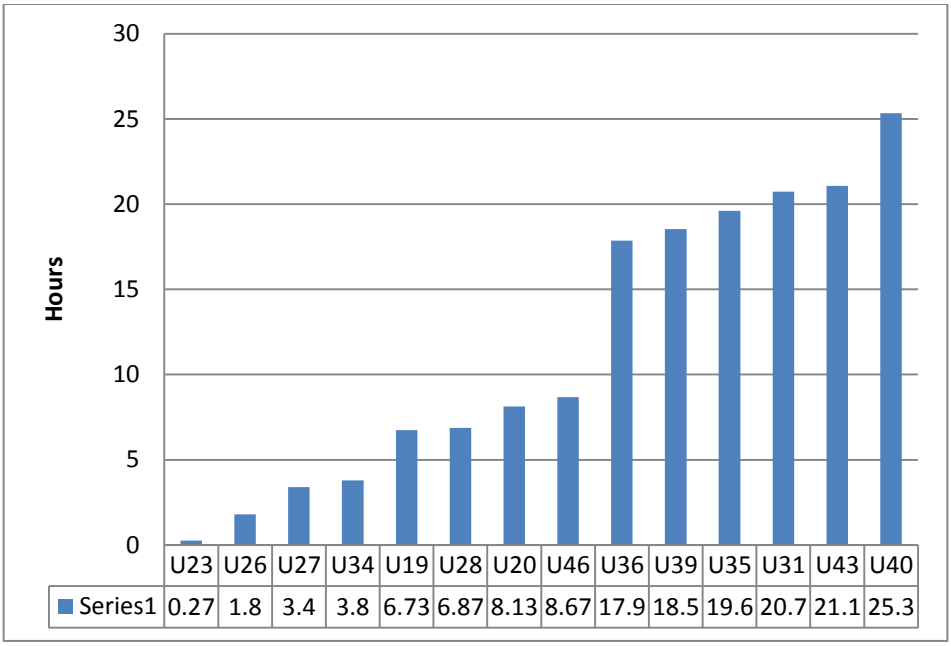
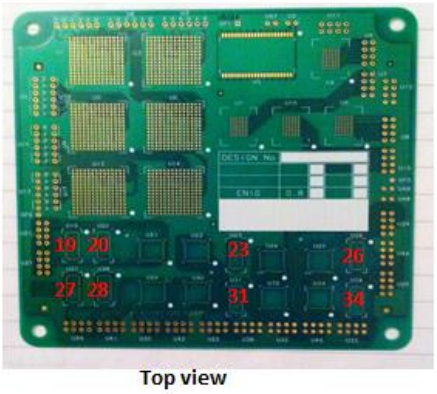
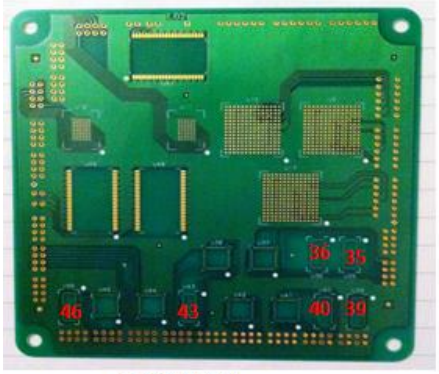
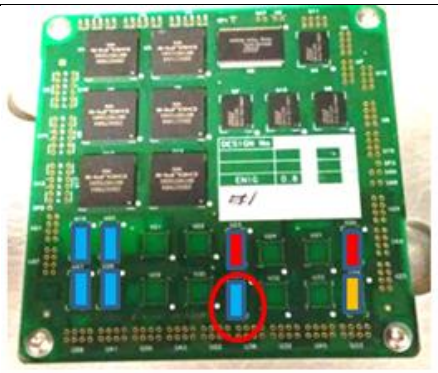
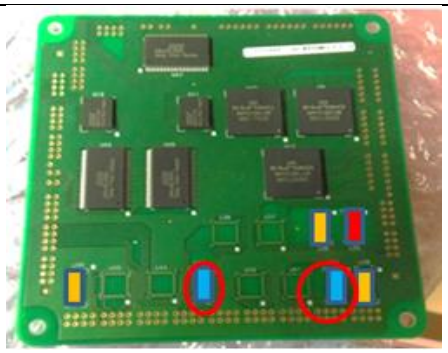
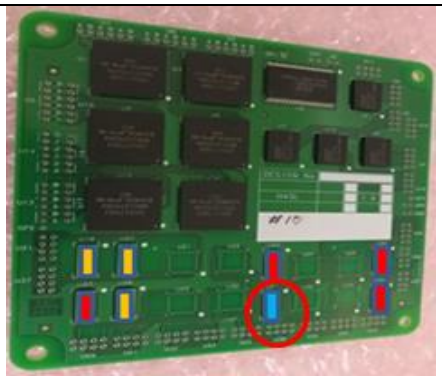
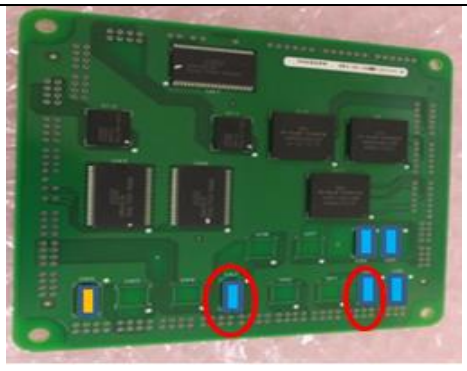


Figure 4.21: Failure time of flip chips in 0.8 HASL board

As can be easily seen from the table 4-13 and figures 4.18 to 4.21, the HASL board took 25.33 hours for complete failure as opposed to 5.73 hours taken by the ENIG board. This clearly shows, that the HASL board is more reliable compared to ENIG. Although the reason for this behaviour is still not clear, it can only be presumed that the reason lies somewhere in the materials used for the PCB finish. However, more focused research needs to be done in this case, to arrive at a more definitive conclusion.

The next more pressing issue to be taken into account is the way the flip chips behave with respect to their positions and relative orientations, normally called the floor plan, irrespective of the PCB finish. To deal with the problem, a comparative table 4-14 has been drawn that categorises the flip chips in both the 0.8 ENIG and 0.8 HASL boards as per the reliability criteria discussed in table 4-3 of section 4.1. Based on those criteria, all the flip chips have been colour coded into red, yellow and blue where red refers to flip chips with least reliability, yellow refers to medium reliability and blue refers to the most reliable flip chips.

Table 4-14: Grouping of flip chips in both ENIG and HASL based on colour coded reliability

Board layout	 Top view	 Bottom view
0.8mm ENIG		
0.8mm HASL		

As was discussed in detail in chapter 3, all the flip chips on the PCBs are arranged in 4 different orientations. Each of the orientations and the corresponding flip chips are explained hereafter.

U23 and U26 are stand-alone flip chips with no back to back connections.

U19-U35 and U20-U36 pairs are placed back to back with an offset along the breath as shown in figure 4.22.

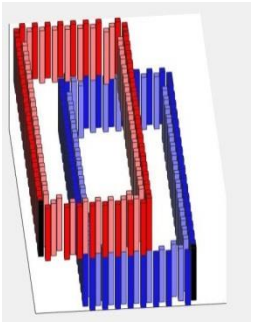


Figure 4.22: Orientation of flip chips U19-U35 and U20-U36

U27-U39, U28-U40 pairs are placed back to back with an offset along the length as shown in figure 4.23.

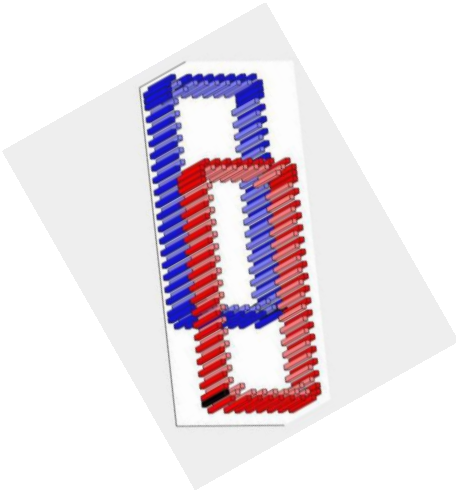


Figure 4.23: Orientation of flip chips U27-U39 and U28-U40

U34-U46, U31-U43 pairs are placed exactly back to back with no offset as shown in figure 4.24.

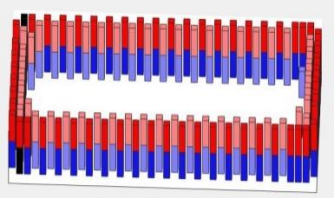


Figure 4.24: Orientation of flip chips U34-U46 and U31-U43

Now from table 4-14, it can be seen that the most reliable positions are those of flip chips U31, U43, U40 marked by red circles. Of these flip chips U31-U43 is a pair with back to back connection and no offset while U40 is back to back connected with offset along the length. On the other hand, the least reliable flip chips are U23 and U26.They were the first two flip chips to fail within first few vibration cycles in both the test boards. Both these flip chips are stand alone and have no back to back connections. Even between them U23 that is placed near the centre of the PCB has lower reliability than U26. Hence it can be safely concluded that in a PCB, flip chips with back to back connections with no offset are the most reliable while standalone flip chips with no back to back connections especially the ones placed near the centre of the PCB are the least reliable in case of vibration cycling.

Going further into the reliability issue, the next step is to determine which of the solder joints fail first depending on the orientations and positions of the flip chip on the board. For this purpose, in-depth analysis was done on all the flip chips U19, U26, U27 and U34 of 0.8mm ENIG board each of which belongs to a specific orientation viz.

U34 - Back to back with no offset, near the board edge at the centre
U19- Back to back with breath offset, near the board edge next to the corner
U27- Back to back with length offset, near the board edge next to the corner
U26- Single sided near the board edge next to the corner
Figure 4.25 shows the flip chip positions in the PCB in red circles. For the purpose of documentation to avoid repetition, only the analysis results for flip chip U34 will be discussed here in detail.

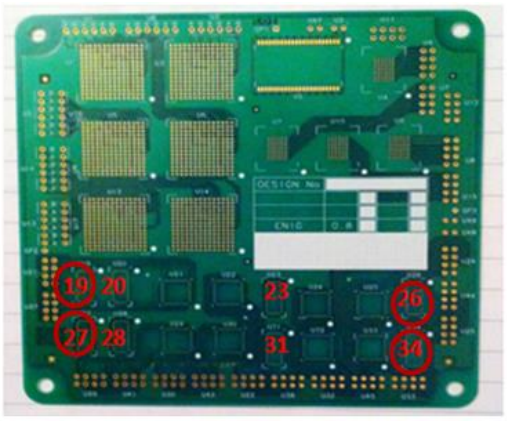


Figure 4.25: Layout of the flip chips selected for inspection on the PCB

In order to witness the behaviour of the solder joints in each of the flip chips based on their orientations and positions, a 3D plot of the mean intensity of the 51 solder joints in the inner region of each of the flip chips was generated. The reason for dealing with only the inner 51 joints is an ultrasound imaging edge effect. Yang (Yang et al 2012) in his thesis concluded that because of the acoustic edge effect witnessed at the imaging of the outer row of solder joints in the flip chips, getting an accurate measure of their image parameters is very difficult. When an ultrasound signal strikes the edge of a material, the signal is scattered away that results in a drop off of information (Semmens and Lawrence, 1997; Hoh *et al*., 2008). This effect can be reduced by certain transducer design but cannot be eliminated entirely due to the intrinsic properties of ultrasound. Hence in order to get a more accurate picture of the behaviour of the solder joints in a vibration environment based on the position and orientations of the flip chips only the inner periphery of 51 solder joints have been analyzed as shown in figure 4.26.

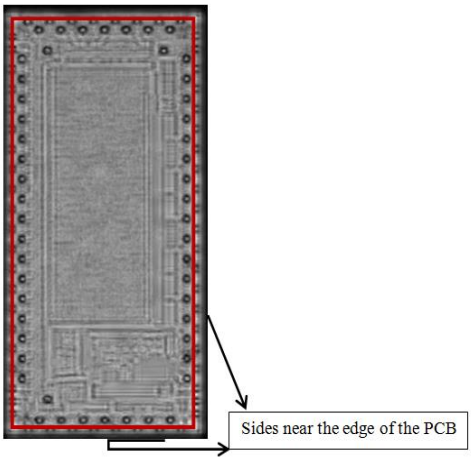


Figure 4.26: C-scan image of U34 showing the solder joints to be examined within the red rectangle

As was shown in section 4.2.5, the first trigger point of change or crack initiation in a solder joints occurs at 35-40% of total cycling time while the second trigger point occurs at 80-85%. For flip chip U34 that has a total vibration cycling time of 29 cycles, the first trigger point of change or crack initiation occurs at around 10 cycles while the second trigger point occurs at around 25 cycles. Hence, the solder joints at scan intervals of 0 cycles, 10 cycles, 20 cycles and 25cycles will be analyzed in detail. The reason for analyzing the scan at 20 cycles is because 20 cycles represents a point between the 1st and 2nd trigger point and hence will provide valuable information on the crack propagation. Figure 4.27 to 4.30 shows the 3D plot of the mean intensity of the solder joints of U34 at cycles 0, 10, 20 and 25 respectively.

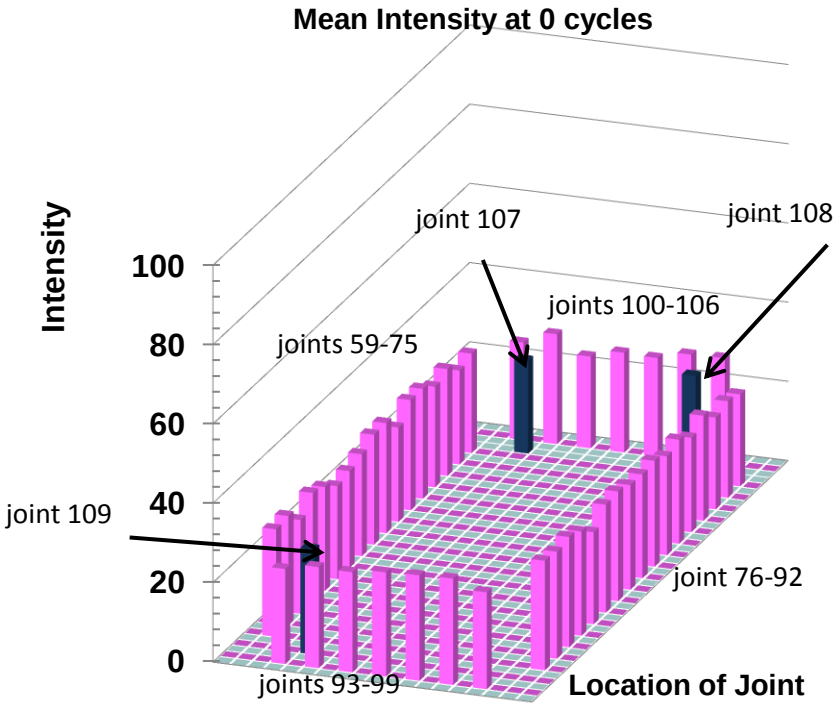


Figure 4.27: 3D plot of the mean intensity of joints 59-109 of U34 at cycle 0

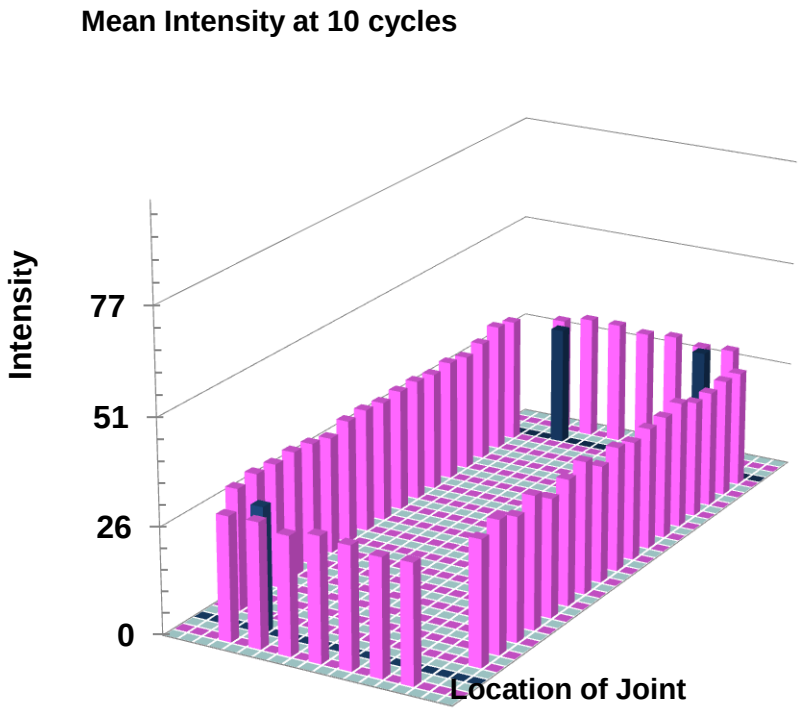


Figure 4.28: 3D plot of the mean intensity of joints 59-109 of U34 at 10 cycles

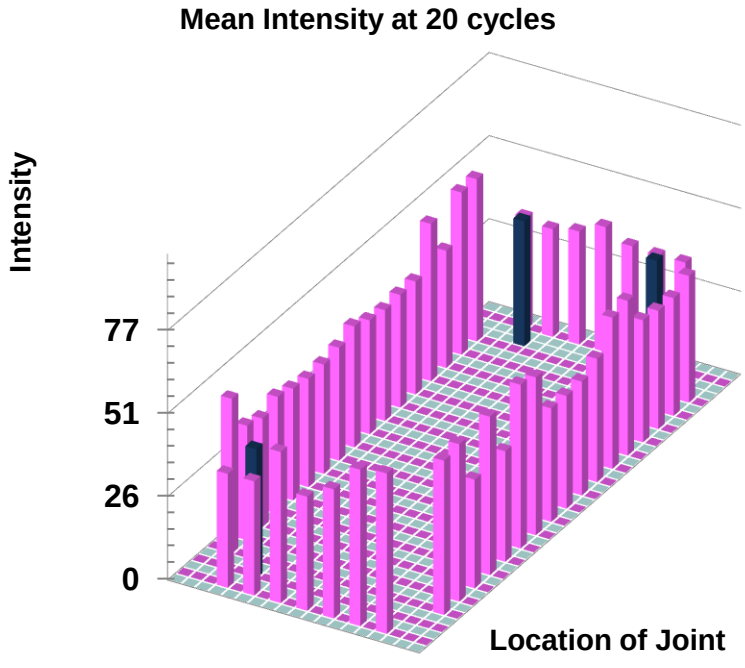


Figure 4.29: 3D plot of the mean intensity of joints 59-109 of U34 at 20 cycles

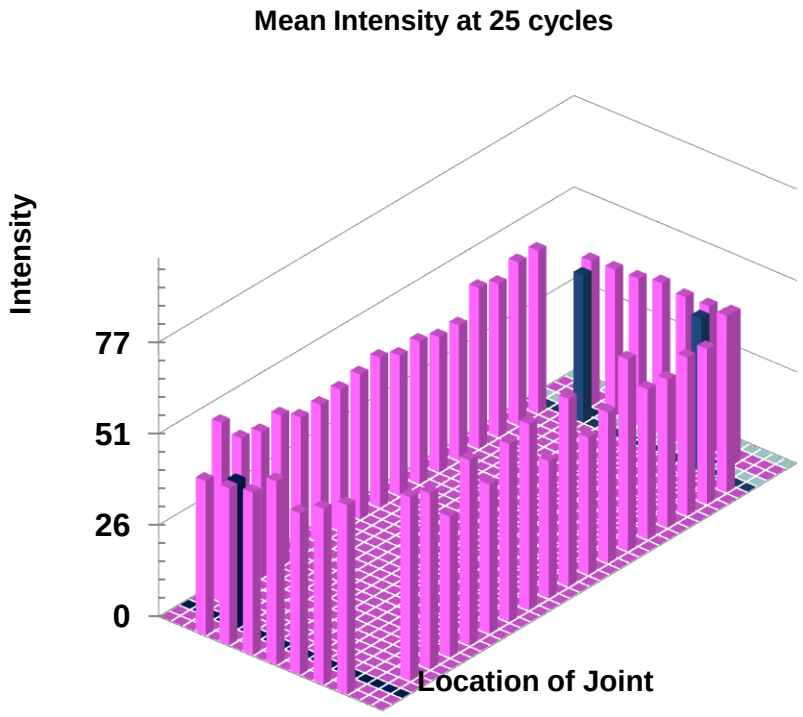


Figure 4.30: 3D plot of the mean intensity of joints 59-109 of U34 at 25 cycles

For a clearer visualization, the graphs in figures 4.31 to 4.35 show the intensity change of all the 51 joints at cycle 25.

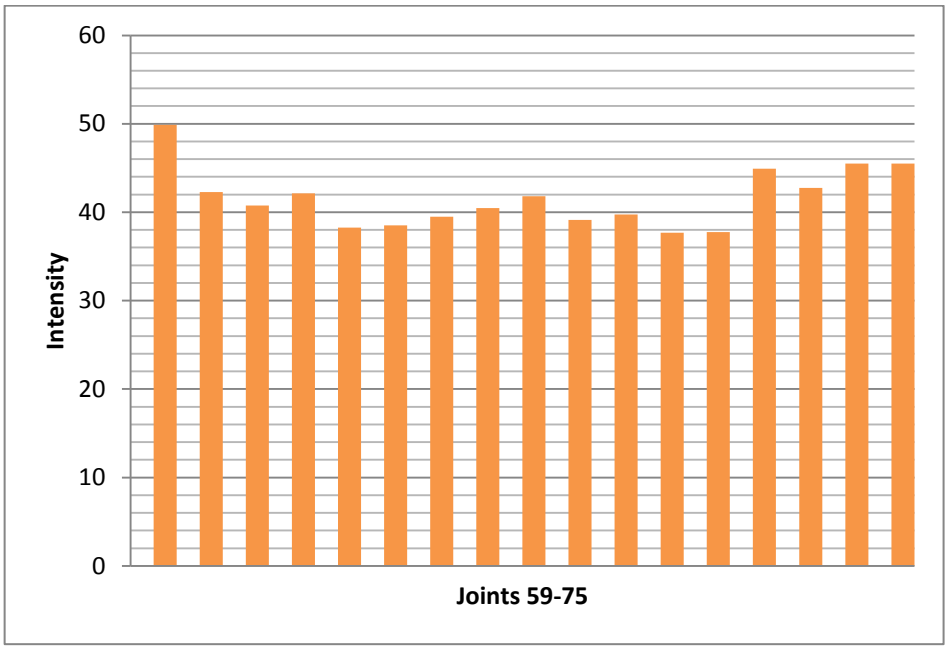


Figure 4.31: Intensity of solder joint 59-75(away from the PCB edge) at cycle 25

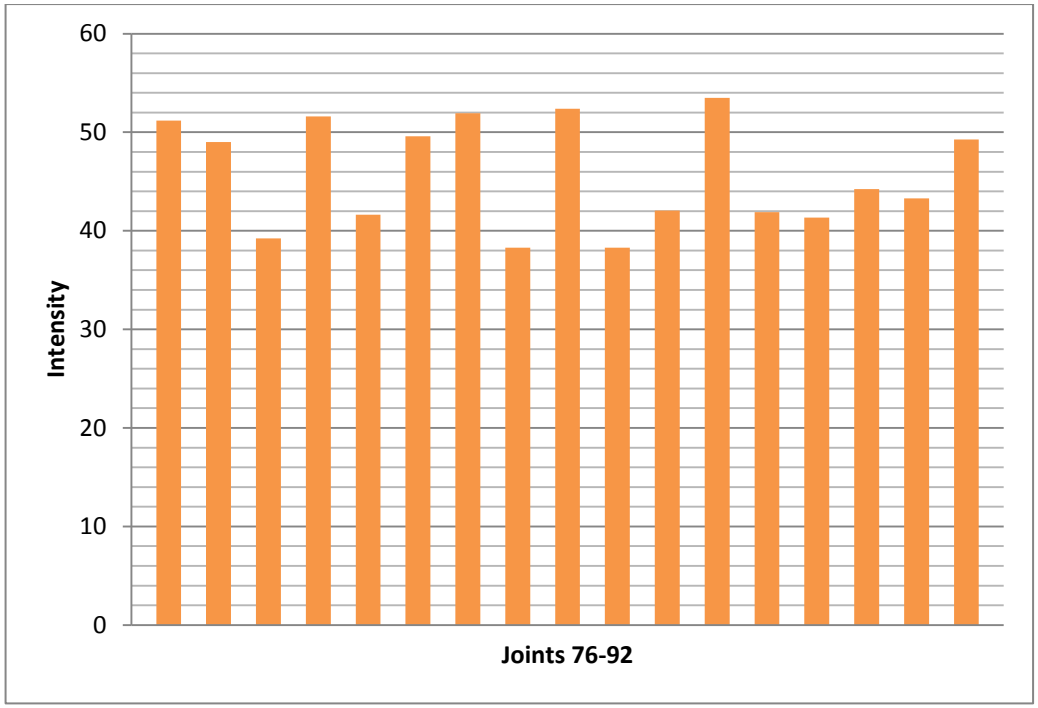


Figure 4.32: Intensity of solder joint 76-92 (near the PCB edge) at cycle 25

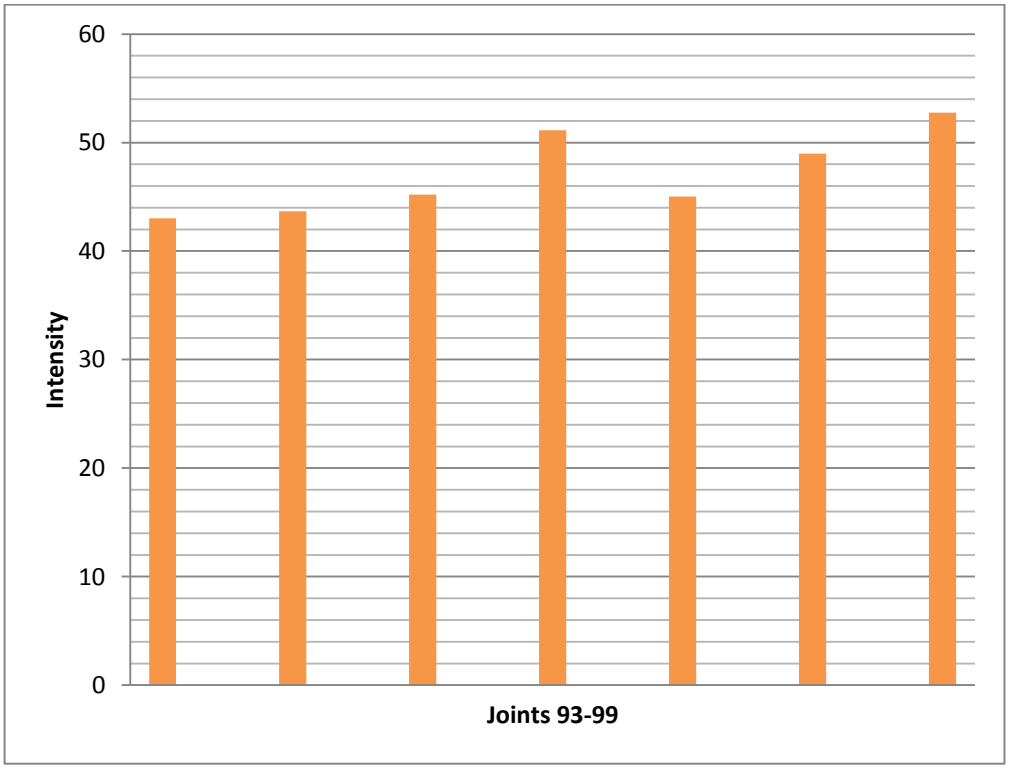


Figure 4.33: Intensity of solder joint 93-99(near the PCB edge) at cycle 25

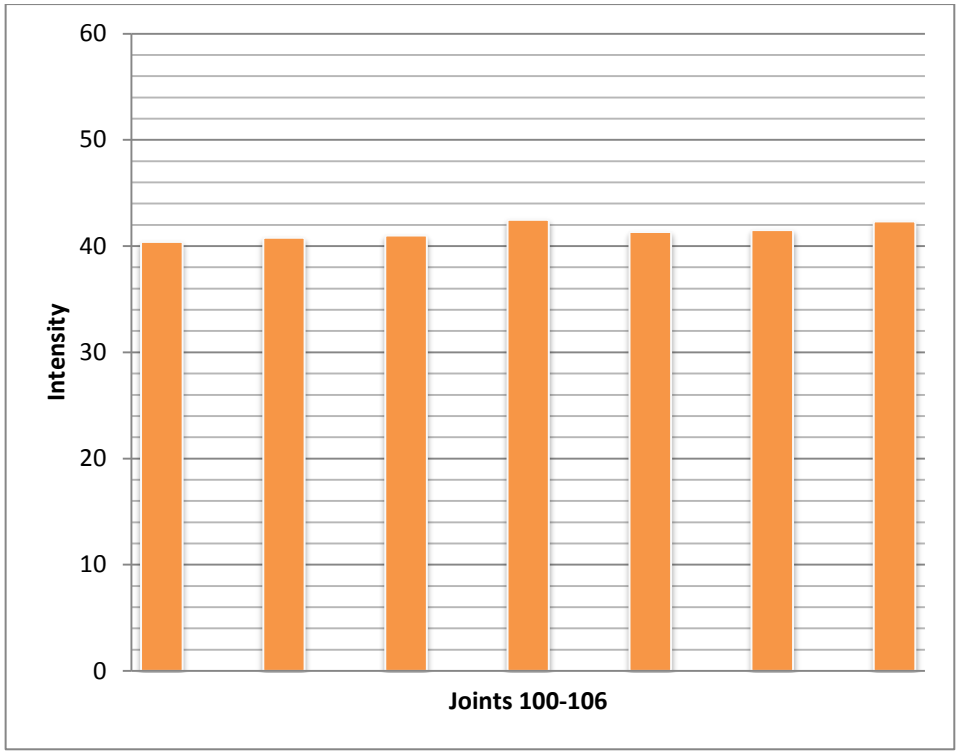


Figure 4.34: Intensity of solder joint 100-106 (away from the PCB edge) at cycle 25

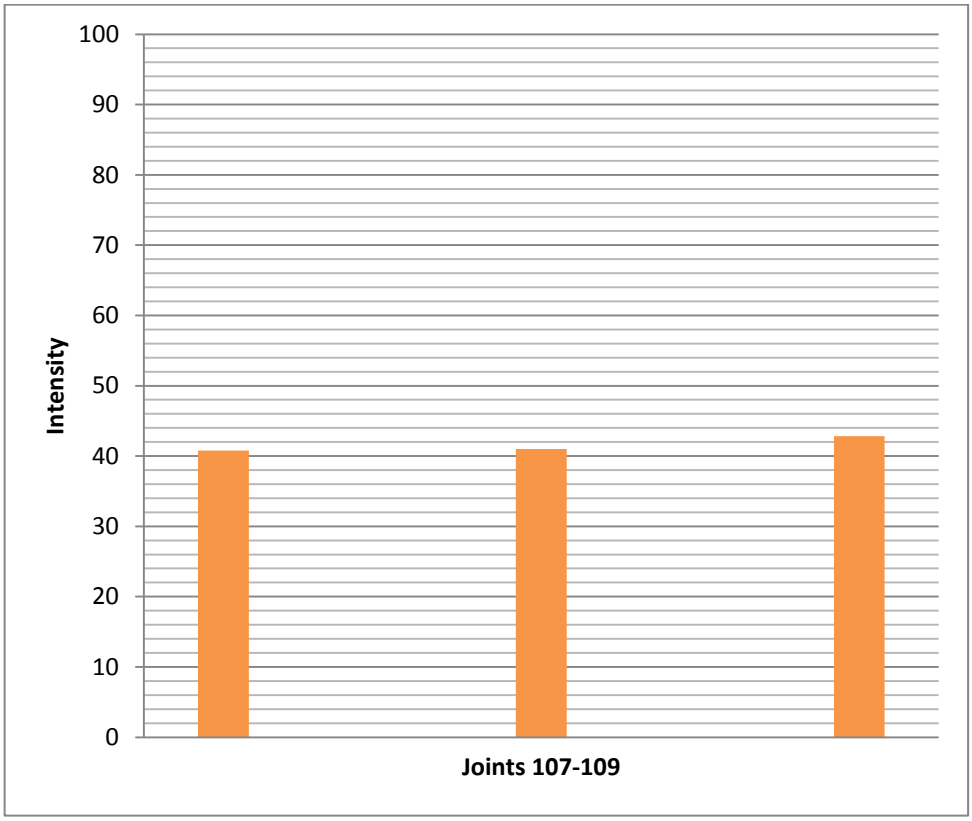


Figure 4.35: Intensity of solder joint 107-109 at cycle 25. (Joint 109 is near the edge)

From the 3D plots it can be clearly seen that at cycle 0, all the solder joints have a mean intensity of around 20 to 25. However as the cycles progress, joints 76-92 that are located near the edge of the board start showing more intensity change compared to the joints 59-75 that are located away from the edge. Joints 93-99 and 100-106 show lesser intensity change but compared to joints 100-106 that are located away from the board edge, joints 93-99 have slightly more intensity change. Joints 107-109 show similar intensity change but the intensity change of joint 109 that is located near the board edge is very slightly more than 107 and 108.

A similar pattern in the behavior of solder joints was observed in the case of the rest of the flip chips as well. In the case of U19, the solder joints near the edge of the board, namely, 59-75 showed more damage compared to the joints at the side away from the edge, namely, 76-92. The overlapping joints 95-99 and 103-106 show average damage but the joints 103- 106 near the board edge have slightly more damage compared to 95-99. In case of U27, the solder joints near the edge of the board, namely, 59-75 show more damage compared to the side away from the edge, namely, 76-92. The overlapping joints 59-67 and 76-84 show average damage but the joints 59-67 near the board edge have slightly more damage compared to 76-84. Solder joints 68-75 have more damage compared to 59-67, 76-92 while 85-92 have more damage than 76-84. Finally, in the case of U26, the solder joints near the edge of the board, namely, 59-75 show more damage compared to the joints at the sides away from the edge, namely, 76-109.

From all the above observations it can be concluded that the solder joints near the board edges start failing first. Thus the farther away from the edge a solder joint is the better the reliability. Solder joints with back to back connections are more reliable than the ones placed in one sided orientation. However solder joints with back to back connections but located near the board edges are less reliable compared to the ones located away from the board edges. Finally, just before failure, about 70-80% of the solder joints had greater than 25% change in intensity, which according to the histogram analysis done in section 4.2 means that they are either partially fractured or fractured. Thus it can be said, that when about 70-80% of the flip chips are either partially fractured or fractured a flip chip is about to fail.

4.5 Comparison of thermal cycling and vibration cycling

This section briefly compares the results of thermal and vibration cycling. Yang (Yang, 2012) conducted through life monitoring of 0.8mm ENIG boards subjected to ATC. This experiment too uses a 0.8mm ENIG board of the exact same configuration. Hence, the results obtained from the ATC tests and analysis done by Yang (Yang, 2012) can be used to draw a rough comparison between the similarities and differences in how the solder joints behave in case of vibration cycling as opposed to ATC.

Figures 4.36 and 4.37 shows a comparison between the mean intensity of solder joints of flip chip U34 before the test and just before failure.

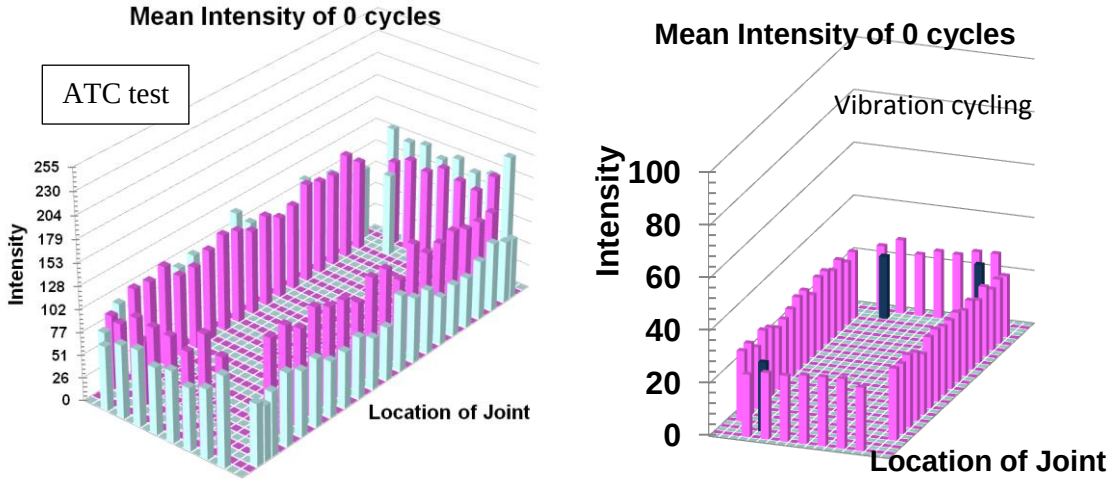


Figure 4.36: Comparison of 3D mean intensity plots of solder joints subjected to ATC and vibration cycling at cycle 0.

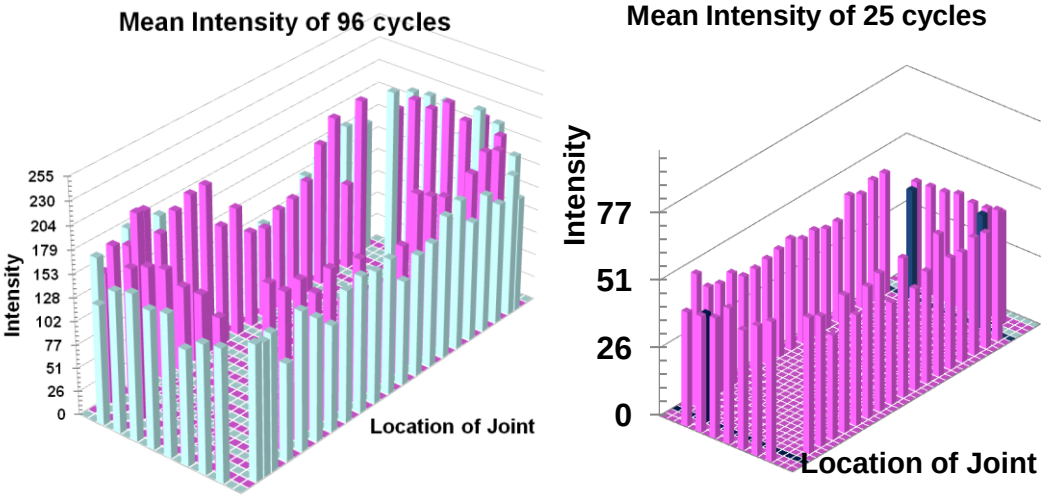


Figure 4.37: Comparison of 3D mean intensity plots of solder joints subjected to ATC and vibration cycling just before failure

From the 3D plots, it can be seen that in thermal cycling, as cycling progresses, the distinction between a good and bad joint is very high whereas with vibration cycling as the cycling progresses almost all joints suffer a similar damage. As a result locating a good and bad joint is challenging in vibration compared to thermal. This is due to the fact that thermal cycling is low stress cycling while vibration represents high stress cycling. Next figure 4.38 shows the comparison between healthy and fractured joints in case of ATC and vibration cycling. As can be seen, solder joints in both thermal and vibration cycling show similar failure characteristics.

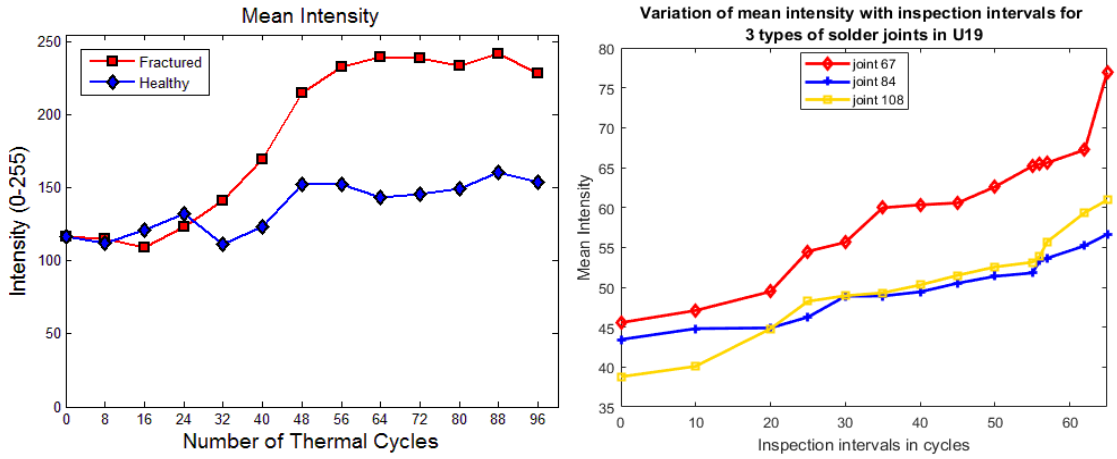


Figure 4.38: Comparison of healthy and fractured joints in case of ATC (left image) and vibration cycling(right image). Joint 84 is a healthy joint while joints 67 and 108 are fractured and partially fractured respectively.

Interestingly, it was found that, back to back with no offset orientation was found to be the least reliable orientation in case of thermal cycling while it was the most reliable orientation in case of vibration cycling. Just like thermal cycling, in case of vibration as well, the reliability of the flip chips increased as they were moved away from the centre of the PCB. However, in case of vibration, the reliability also improves if the flip chips are placed away from the edges of the PCB.

4.6 Design guidelines for flip chip layout and orientations in a PCB subjected to vibration

Based on all the observations of section 4.4, certain design guidelines can be loosely suggested to ensure better reliability of solder joints and flip chips and improve their susceptibility in PCBs in a vibration environment.

1. Single sided flip chip placements should be avoided.
2. Back to back connections should be made where possible.
3. Placement of flip chips at the centre of the PCB should be avoided.
4. Placement of flip chips very close to the edges of the PCB should be avoided.
5. Back to back connection with no offset is the most reliable orientation for flip chips in PCBs subjected to vibration.
6. Back to back connection with length offset is the second most reliable orientation for flip chips in PCBs subjected to vibration.
7. Finally back to back connection with breath offset is the least reliable of the three offsets but it is more reliable than a stand-alone single sided connection.

4.7 Weibull Analysis

The Weibull distribution is one of the most widely used lifetime distributions in reliability engineering. The equation for the probability density function (pdf), f(t) of a Weibull distribution is given by (Reliability Engineering Resources):

$$f(t) = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \qquad \text{Eq. 4-11}$$

Where $f(t) \geq 0, t \geq 0 \; or \; \gamma, \beta > 0, \eta > 0, -\infty < \gamma < \infty$

The parameters β, η and γ control the scale, shape and location of the pdf function. The scale parameter, η, defines where the bulk of the distribution lies. The shape parameter, β, defines the shape of the distribution and the location parameter, γ, defines the location of the distribution in time.

The Weibull distribution can take on the characteristics of other types of distributions, based on the value of its shape parameter, β. The Weibull shape parameter, β, also known as the slope, is equal to the slope of the regressed line in a probability plot. The value of β has a marked effect on the failure rate of the Weibull distribution. Inferences can be drawn about a population's failure characteristics just by considering whether

the value of β is less than, equal to, or greater than one. Populations with β <1 exhibit a failure rate that decreases with time, populations with β =1 have a constant failure rate that is consistent with an exponential distribution and populations with β >1 have a failure rate that increases with time.

Figure 4.39 below shows a comparison of the Weibull probability plots of the 0.8mm ENIG and 0.8mm HASL boards based on the observations of table 4-13.

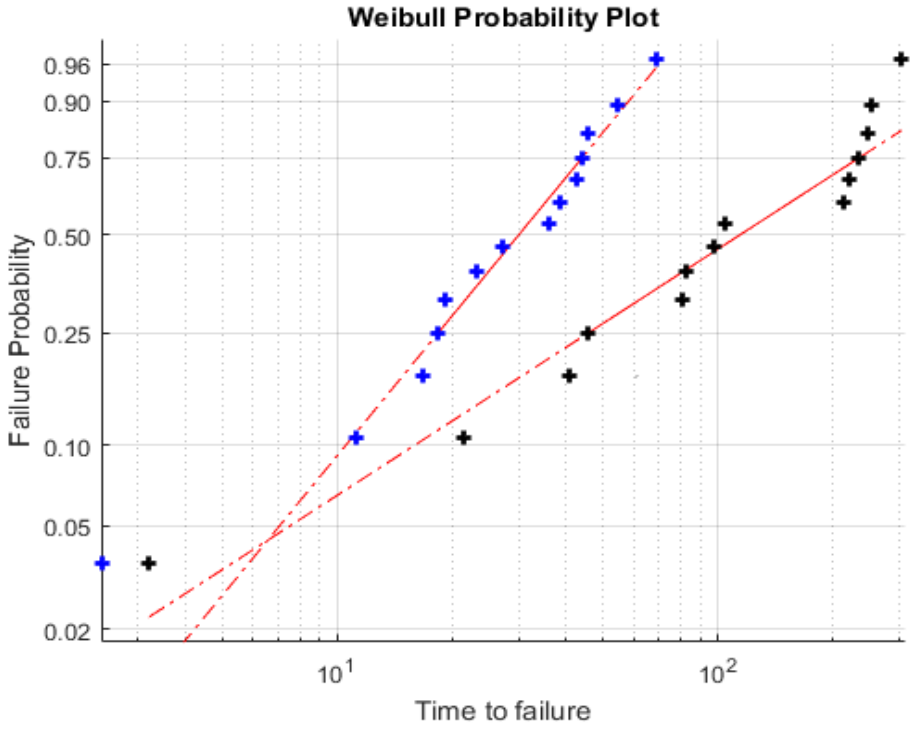


Fig 4.39: Weibull plots for 0.8mm HASL and ENIG whole PCB/board vibration failures (Blue = ENIG, black = HASL)

The two Weibull plots in figure 4.39 show the differing reliability characteristics for ENIG and HASL finished PCBs from vibration testing. A clear difference in the lifetime characteristics can be seen for the two surface finishes on the PCBs. The long-term reliability of HASL is best extending to over 300 cycles, compared to ENIG that only reaches about 70 cycles. The shape parameter, β (Di Mario, 2008) has been calculated to be β = 0.765 for HASL, which being less than 1 indicates that the materials set accumulates more failures initially, with an increase in failure rate at a lower number of cycles. The lower slope of the HASL plot, however indicate a longer overall lifetime. The shape parameter β = 1.297 being greater than 1, indicating that the ENIG material set has a more consistent behaviour with a more constant failure rate. The higher slope of the ENIG plot indicates a reduced overall lifetime.

4.8 Summary

In this chapter, the effects of vibration cycling on the solder joints of flip chips have been discussed in detail. It was found that, in vibration cycling, crack initiation in solder joints occur at around 25-30% of the total lifetime of a flip chip and propagates almost linearly till 80-85% of the lifetime after which it fails completely. Three types of solder joints can be found in a flip chip near failure – healthy, partially fractured and fractured. When 70-80% of the solder joints in a flip chip are partially fractured or fractured a flip chip fails in the next few vibration cycles. The behaviour of solder joints in flip chips placed at different positions and orientations in a PCB in a vibration environment was also discussed in detail. It was found that flip chips placed at the centre and near the edge of the PCB were the least reliable in terms of position in a PCB whereas orientation wise, standalone flip chips are the least reliable. Back to back connection with no offset was found to be the most reliable orientation for flip chips in a PCB subjected to vibration. Based on the results obtained, a few design guidelines were formulated for placing the flip chips in a PCB for vibration environments. A brief comparison between flip chips in ATC and vibration cycling environments was drawn to determine the similarities and differences between the behaviour of solder joints and flip chips in the two cases. Weibull analysis of the reliability of the FCs in the 0.8mm ENIG and 0.8mm HASL PCBs was also investigated. In the next chapter, conclusions and scope for future work will be presented.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

This thesis investigated the reliability of solder joints in area array packages in a real time vibration environment. Focus has been given on identifying the failure pattern of the solder joints starting from the point of crack initiation, propagation and finally failure. For this purpose, through life monitoring of the solder joints has been done using acoustic micro imaging (AMI). Although flip chips and ball grid arrays both represent area array packaging, because of the presence of interposers in ball grid arrays, ultrasound cannot penetrate through them. Hence flip chips have been used as the test vehicle to represent area array packages. Another major aspect covered in the thesis is the effect of the component floor plan layout on the reliability of solder joints. Detailed analysis has been done to show how the relative positions and orientations of the flip chips on the PCB affect their reliability as well as the reliability of the solder joints. A brief comparison of the effects of vibration testing on PCBs of different finishes has been discussed. Finally, a short comparison of the behaviour of solder joints in vibration cycling and accelerated thermal cycling environments has also been presented. Figure 5.1 shows a brief flowchart of the entire analysis process done using MATLAB after acoustic imaging.

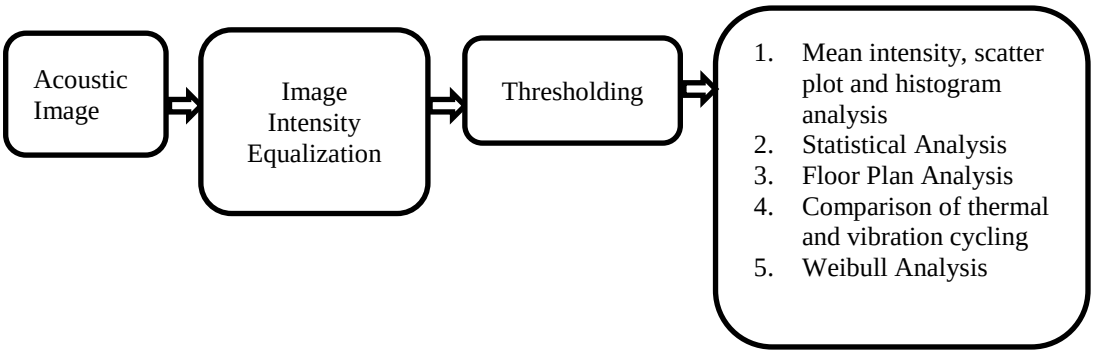


Figure 5.1: MATLAB processing flowchart

From this experimental study and analysis the following conclusions can be made:

- Acoustic micro imaging (AMI) proved to be an effective technique for through life monitoring of the reliability of solder joints non-destructively.
- From the analysis of the ultrasound images obtained from AMI it has been found that the grey region in the middle of the solder joints varied according to the quality of the connection between silicon die and solder joint. The intensity and area of this region for a partially fractured or fractured joint tends to be higher compared to a healthy joint.
- Three types of solder joints have been found to be formed near the time of complete failure of a flip chip:
  a. Type 1 or healthy: Joints that show 9% -18% increase in intensity with cycling
  b. Type 2 or partially farctured: Joints that show 25% - 40% increase in intensity with cycling
  c. Type 3 or fractured: Joints that show 55% - 80% increase in intensity with cycling
- Two trigger points in the lifetime of any solder joint have been identified from the mean intensity and area analysis. The first trigger point suggests crack initiation and occurs at around 35% - 40% cycling and the second trigger point which refers to the path of crack propagation occurs at around 80% - 85% cycling. However, depending on whether the joint is healthy, partially fractured or fractured, the resultant rise in mean intensity or area varies. Hence, the failure pattern of any solder joint can be said to fall under three regions. The region between 0 cycle and first trigger point where the crack initiates, the region between the first and second trigger point where the crack propagates and finally the region after the second trigger point where the crack formed reaches its peak and the flip chip fails.
- From statistical analysis, it has been found that the probability distribution of the mean intensity of a healthy joint exhibits the behaviour of a first order Gaussian distribution all throughout the test cycles. This is because in the case of a healthy joint the intensity distribution does not shift a lot when compared to that at cycle 0. However, for partially fractured and fractured joints, as the crack propagates,

the shift in the intensity distribution increases and hence, they lose the properties of a normal Gaussian distribution and can only be represented by a mixture or combination of Gaussian distributions.

- The HASL finish board has been found to be more reliable compared to ENIG for vibration testing. The reason for this is unclear and needs further focused research.

- The solder joints near the board edges have been found to be the least reliable in a vibration environment. Solder joints with back to back connections have been found to be more reliable than the ones placed in one sided orientation. However solder joints with back to back connections but located near the board edges are less reliable compared to the ones located away from the board edges. Figure 5.2 shows the reliability zones in a PCB. Red represents the least reliable area of a PCB, yellow represents medium reliability and green represents high reliability.

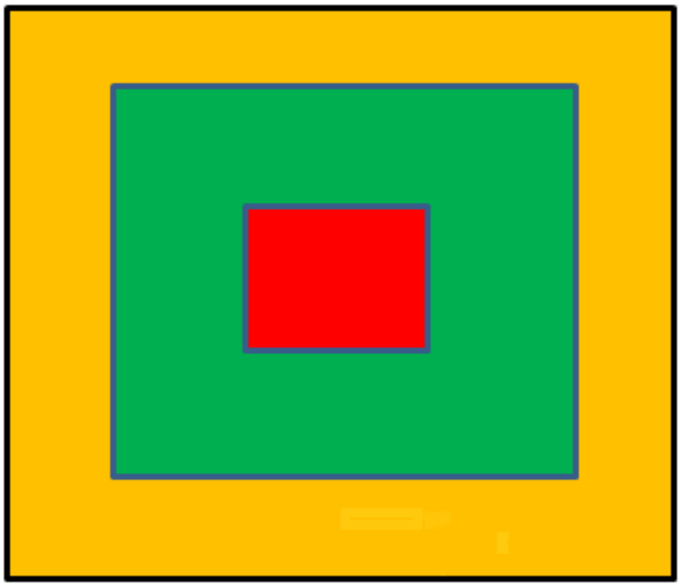


Figure 5.2: Different reliability zones of a PCB for a vibration environment

- When about 70% - 80% of the solder joints in a flip chip are either partially fractured or fractured a flip chip is expected to fail in the next few vibration cycles.
- Based on the analysis, to minimize vibration susceptibility a few design guidelines for flip chip layout and orientations in a PCB have been proposed for:

1. Single sided flip chip placements should be avoided.
2. Back to back flip chip connections should be made where possible.
3. Placement of flip chips at the centre of the PCB should be avoided.
4. Placement of flip chips very close to the edges should also be avoided.
5. Back to back connection with no offset has been found to be the most reliable orientation for flip chips in PCBs in a vibration environment.
6. Back to back connection with length offset has been found to be the second most reliable orientation.
7. Finally back to back connection with breadth offset has been found to be the least reliable of the three offsets but is still more reliable than a stand-alone single sided connection.

- The distinction between a good and bad joint is very clear in the case of thermal cycling as compared to vibration cycling. As a result locating a good and bad joint is a bit challenging in vibration compared to thermal.
- Although back to back with no offset orientation has been found to be the most reliable orientation in the case of vibration cycling, it is the least reliable orientation in case of thermal cycling.
- In the case of both vibration and thermal cycling, the reliability of the flip chips increases as they are moved away from the centre. However, in the case of vibration, the reliability also improves if the flip chips are placed away from the edges of the PCB. This is opposite in case of thermal cycling where the solder joints near the edge were found to be more reliable compared to the ones away from the edge.

5.2 Future Work

Based on the results obtained from this work, many different directions of research can be proposed:

- **Revised floor plan regarding flip chip placement**: All the flip chips in the PCB used in the project have been placed in a similar orientation. However, if the

floor plan layout is changed by placing a few flip chips perpendicular to each other or at different angles to each other, the analysis results could reveal more information regarding the effects of floor plan layout on solder joint reliability.

- **Use different sizes and types of solder joints:** Research can also be done by placing different sizes of solder joints in a PCB or by using different types of solder, material wise such as lead free solders like SAC305 or Sn0.7Cu.
- **Mixed environmental reliability testing:** This thesis only deals with the effects of real time vibration cycling on solder joints and flip chips. The next step would be to use both thermal and vibration simultaneously along with shock and humidity cycling to monitor the failure pattern of solder joints. This can be referred to as mixed environmental reliability testing or MERT.
- **Use other monitoring techniques like 3D X-ray or 3D US for imaging:** Although AMI has been used for the study, a lot of other innovative techniques such as 3D X-ray, 3D AMI and online electrical resistance monitoring can also be investigated for through-life monitoring of the joints. However, the key points to keep in mind while dealing with these methods is firstly the time/data acquisition in the case of 3D X-ray and 3D AMI. A typical 3D X-ray scan of a flip chip can take up to 12 hours and generate half a gigabyte of data while a 3D AMI scan, depending on the resolution can take up to 5 hours and generate up to a gigabyte of data. Secondly, it will be very important to come up with an appropriate set-up that can provide accurate live measurements in an extreme vibration environment in the case of an online electrical resistance monitoring system. Also depending on the size of the solder joints, electrical probes necessary to connect to the joints for resistance measurement might not yet be available in the market.
- **Optimal floor plan layout for MERT:** Further research can also be done to analyse the behaviour of solder joints in a mixed testing environment using thermal cycling, vibration cycling, shock and humidity based on which an optimal floor plan layout can be proposed.

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