AC NBTI of Ge pMOSFETs: Impact of Energy Alternating Defects on Lifetime Prediction

J. Ma [(1)], W. Zhang [(1)], J. F. Zhang[(1)], Z. Ji[(1)], B. Benbakhti[(1)], J. Franco[(2)], J. Mitard[(2)], L. Witters[(2)], N. Collaert [(2)], G. Groeseneken[(2)]
[(1)]School of Engineering, Liverpool John Moores University, Liverpool L3 3AF, UK. [(2)]*IMEC, Leuven B3001, Belgium*

Introduction: Ge pMOSFETs with either HfO_2/SiO_2/Si-cap/Ge or Al_2O_3/GeO_2/Ge gate stacks are strong candidates for next technology nodes due to its high hole mobility [1-3]. Their reliability was studied under DC stress [2-4], but is missing under AC stress. For Si devices, industry predicts AC NBTI lifetime from DC stress after introducing a measurement delay either purposely [5] or implicitly by using a measurement time of 10-100 ms [6] (**Fig.1a**). In this way, AC lifetime predicted by DC stress agrees well with that from AC stress when using effective stress time (**Fig.1b**), because degradation under AC is the same as DC after a delay-induced recovery (**Fig.1c**). *The significance of this work is that, for the first time, we report that AC lifetime for Ge is much longer than DC even after a long measurement delay, and the AC lifetime MUST NOT be predicted from DC stress as used in Si, since overdrive voltage can be underestimated by 0.5V (**Fig.2**). A key advance of this work is the understanding of this important difference between Si and Ge and identifying the responsible defects and mechanism.*

Difference in Si and Ge AC NBTI: Test devices are given in **Table 1**. Unless otherwise specified, tests were carried out at 125 °C and AC stress was at 10 kHz with a duty factor of 0.5. In contrast to Si shown in **Fig.1c**, much less defects are generated under AC stress than DC even after the delay-induced recovery in Si-cap/Ge devices (**Fig.3**). To further study it, an AC-DC-AC stress cycle was carried out. In Si, the DC-enhanced charging is fully recovered during the 2nd AC (**Fig.4a**) and NBTI follows a single kinetics (**Fig.4b**). In Ge, however, defects generated by DC stress cannot be fully discharged (**Fig.5a**), indicating additional DC generation (**Fig.5b**). This can be further supported by the defect energy distribution, where AC stress in Si generates the same defects as DC when discharged under the same Vg_rec (**Fig.6a**). DC stress in Ge, however, generates much more defects after discharging under the same AC Vg_rec (**Fig.6b**).

Different Defects in Si and Ge: It has been shown that defects are different in Ge and Si devices, as there are energy alternating defects (EAD) in Ge, but not in Si devices [4]. As shown in **Fig.7a-c**, following the discharge through which the energy profiles are obtained [7], traps in GeO_2/Ge cannot be recharged until charging energy level (EL) is swept back to ~Ev(Ge) (**Fig.7a**), and the same also occurs in Si-cap/Ge devices (**Fig.7b**). For Si, however, recharge starts as soon as energy level is swept negatively (**Fig.7c**).

The above differences can be well explained by the presence of energy alternating defects (EAD) in Ge, but absent in Si devices. The energy level of EAD alternates with its charge status: shifts above Ev when charged, and back below Ev when neutralized, in both GeO_2/Ge (**Fig.8a**) and Si-Cap/Ge (**Fig.8b**). EADs in fresh Si-cap/Ge are located further below Ge Ev because of the band misalignment [3]. EAD-recharge can only take place when biased below ~Ev, the same as in a fresh device, and does not occur above ~Ev (**Fig.7a&b**). In contrast, the generated defects (GD) in Si have energy levels well above Ev and do not alternate (**Fig.8c**). Since these defects keep their high energy level after neutralized, they recharge readily once above Ef (**Fig.7c**) by electron tunneling to Si conduction band, rather than capturing holes from valence band.

We propose a double-well model for the energy alternation in Ge devices (**Fig.9**) and then use it to explain the additional DC generation. The energy level of the 1st well is relatively shallow and below Ev, and a hole must have sufficient energy to be injected and trapped in it. Only after this trapping, it can proceed to overcome the 2nd barrier by a field-enhanced relaxation process and reach the deep well [8]. The EADs trapped in the 2nd well is proportional to the charge density in the 1st well, N_h. The shallow level of 1st well makes N_h dynamic: it is much less under AC because of short charging time and the discharge at Vg=0V. The smaller AC N_h, in turn leads to less EADs in the 2nd well. Moreover, AC ON time can be too short to complete the relaxation responsible for the EAD generation. This explains the missing 'additional generation' under AC (**Fig.5&6b**). The trapping in the 2nd well is more stable due to its deep energy level. For Si devices, there is no 'additional generation' under DC because of the lack of energy alternation (**Fig.1c&8c**)

To further support the above explanation, several tests have been carried out. The additional EAD generation occurs in both GeO_2/Ge (**Fig.10a**) and Si-cap/Ge devices (**Fig.5**). To demonstrate that EAD generation requires sufficient time and this time reduces for higher stress field strength, Eox, **Fig.10b** shows that at low Eox in Si-cap Ge, the additional EAD generation only occurs after a long DC stress. Under a higher Eox, it occurs at a shorter stress time. Furthermore, for AC stress in Ge, higher Eox leads to the additional EAD generation starting at higher frequency **(Fig.11a)**, supporting that the generation time reduces at higher Eox. At high frequencies, the impact of frequency and Eox becomes negligible, because the small N_h trapped in the 1st well becomes the limiting factor. In contrast, the ratio between AC and DC in Si is independent of Eox (**Fig.11b**), supporting the lack of EADs. Moreover, a higher frequency leads to the additional EAD generation starting at a higher duty factor, so as to provide sufficient generation time (**Fig.12a**). At a high frequency of 10k Hz, the additional EAD generation is independent of Eox at duty factors ≤ 50% (**Fig.12b**), agreeing with Fig.11a. It increases with Eox at a higher DF, where t_{stress} is no longer the limiting factor.

AC lifetime prediction in Ge: For Si device (**Fig.1b, Fig.11b**), the AC lifetime at high frequency is the same as the DC lifetime after a recovery, making it possible to predict the AC lifetime from DC stress after subtracting the discharge. For Ge device, however, as the additional DC generation is absent in AC stress (10 kHz, **Fig.13**), AC lifetime cannot be predicted by performing DC stress, as shown in **Fig.14.** An AC overdrive voltage of 1.92V is obtained for keeping ΔVth within 100 mV for 10 years in Si-cap/Ge, comparing to the 1.42V predicted by DC stress, making an additional 0.5V available for gaining higher speed. Further process optimization is clearly needed before GeO_2/Ge makes its commercial debut.

Conclusions: For the first time, AC lifetime in Ge pMOSFETs is investigated and it must not be predicted by the conventional DC stress method with a measurement delay. This is because the energy alternating defects are generated in Ge but not in Si, which introduces additional generation under DC stress.

Acknowledgement: This work is supported by EPSRC of UK (Grant nos: EP/I012966/1 and EP/L010607/1)

Reference: **[1]** Zhang et al, VLSI, p.161, 2012. **[2]** Groeseneken et al, IEDM, 2014. **[3]** Franco et al, IEDM, p.397, 2013. **[4]** Ma, et al, IEDM, 2014. **[5]** Intel, "Quality System Handbook," p. 19-22, 2009. **[6]** Huard et al, IRPS, p. 40, 2004. **[7]** Ma et al, EDL, p.160, 2014. **[8]** Grasser et al, IRPS, p.33, 2009.

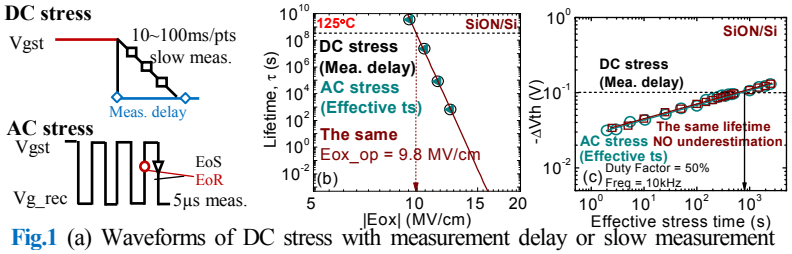


Fig.1 (a) Waveforms of DC stress with measurement delay or slow measurement used for AC NBTI prediction, and AC stress with a measurement time of 5μs taken either from the edge of End of Recovery (EoR) or End of Stress (EoS). (b) The lifetime predicted by DC stress in (a) agrees well with the measured AC one for effective stress time. (c) Degradation under AC stress is the same as DC after a delay-induced recovery.

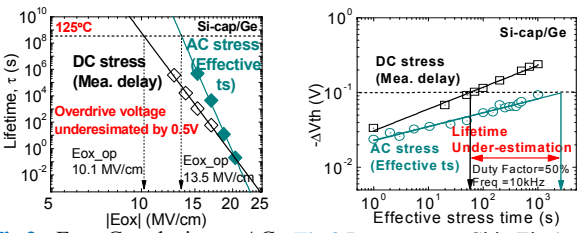


Fig.2 For Ge devices, AC lifetime is much longer than that predicted by DC stress and the overdrive voltage can be underestimated by 0.5V.

Fig.3 In contrast to Si in Fig.1c, Si-cap/Ge has much less defects generated under AC stress than DC even after the recovery induced by a delay in the order of seconds.

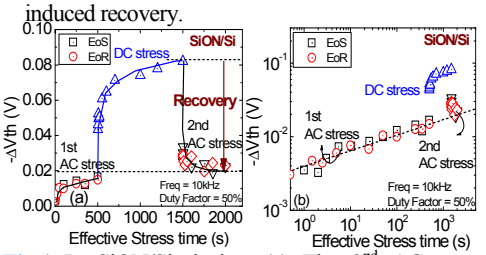


Fig.4 In SiON/Si device, (a) The 2nd AC stress recovered DC-enhanced charging. (b) The AC-DC-AC stress follows the same generation kinetics, suggesting no additional generation by DC stress.

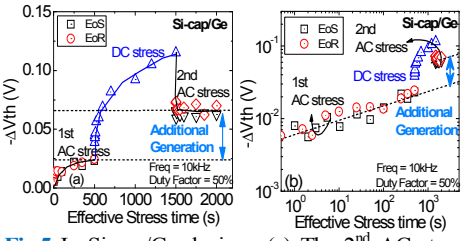


Fig.5 In Si-cap/Ge devices, (a) The 2nd AC stress cannot fully recover the additional defects generated from DC stress (b) AC-DC-AC stress does not follow the same generation kinetics.

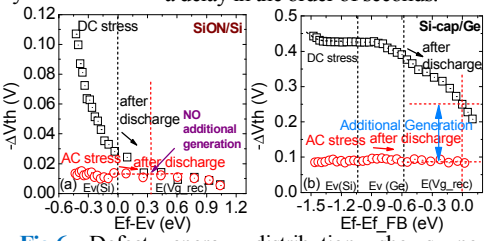


Fig.6 Defect energy distribution shows no additional DC generation in (a) SiON/Si, but additional DC generation in (b) Si-cap/Ge device, when comparing ΔVth after discharge at the same Vg_rec following DC and AC stress.

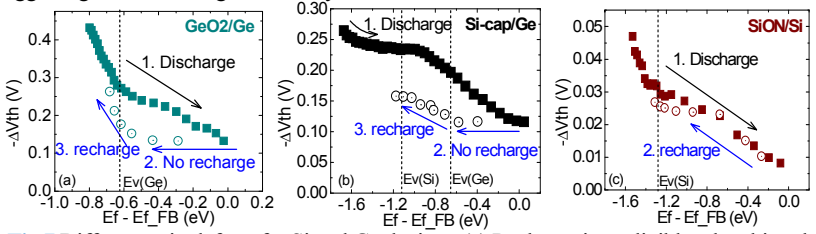


Fig.7 Differences in defects for Si and Ge devices: (a) Recharge is negligible when biased above ~Ev(Ge) for GeO_2/Ge. (b) Also no re-charge above ~Ev(Ge) for Si-Cap/Ge. (c) Recharge occurs as soon as energy sweeping negatively, well above ~Ev(Si) for SiON/Si. This difference is explained in Fig.8a-c.

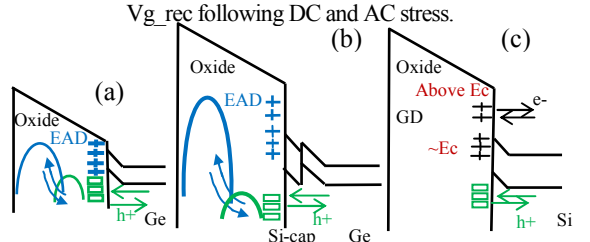


Fig.8 An illustration of energy alternating defects (**EAD**) in (a) GeO_2/Ge and (b) Si-Cap/Ge: their energy level shifts above Ev when charged and back below Ev when neutralized. (c) In SiON, defect energy does not alternate with charge status and recharge takes place by e-tunnelling back to Si conduction band.

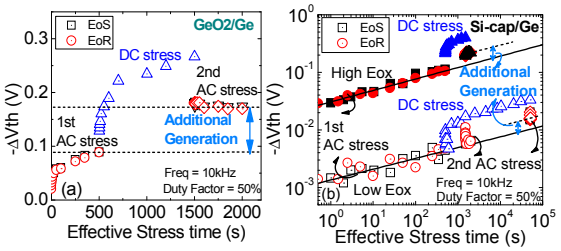


Fig.10 (a) Additional EAD generation is also observed in GeO_2/Ge devices. (b) Long DC stress time is required at low Eox for the additional EAD generation in Si-cap/Ge. At a higher Eox, it occurs at a shorter stress time.

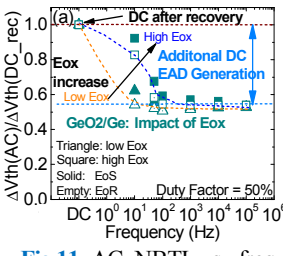
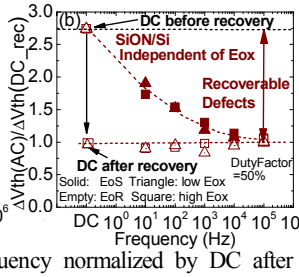


Fig.11 AC NBTI vs. frequency normalized by DC after recovery. (a) In Ge, the additional EAD generation starts at higher frequency under higher Eox. (b) In Si devices, the difference between AC and DC is caused by discharging recoverable defects only, independent of Eox.



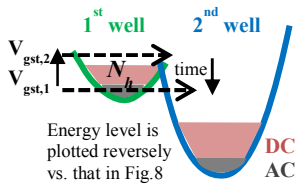


Fig.9 Double-well model in Ge: generation of energy alternating defects in 2nd well with deeper energy level requires holes in 1st well to overcome the 2nd barrier, through a field-enhance relaxation process.

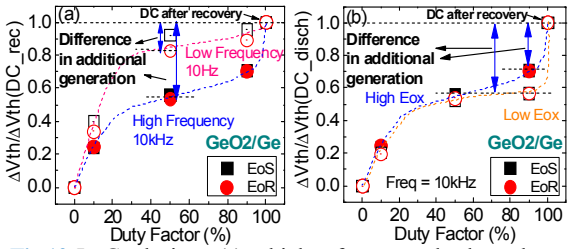


Fig.12 In Ge devices, (a) a higher frequency leads to the additional EAD generation starting at a higher DF. (b) At a high frequency of 10k Hz, the additional generation is enhanced by the high Eox only at a high duty factor. DC data (Duty Factor = 1) were measured after recovery.

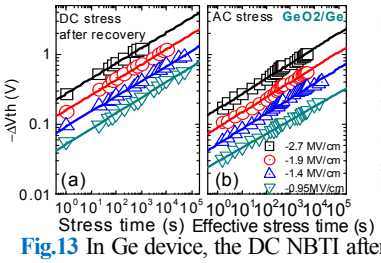


Fig.13 In Ge device, the DC NBTI after recovery (a) is substantially higher than the AC NBTI (10 kHz), due to the 'additional DC generation' (Fig. 5)

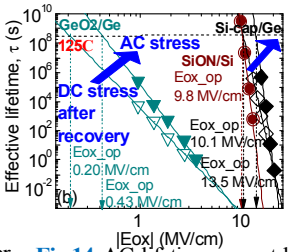


Fig.14 AC lifetime cannot be predicted by DC with recovery at Vg_rec=0V for Ge devices, whilst it can for Si devices since its AC and DC (with recovery) overlapped.

Table 1: Gate stack
a) 2.3nm or 2 nm plasma-N SiON/Si
b) 4nm Al_2O_3/1.2nm GeO_2/Ge
c) 2nmHfO_2/~0.4nmSiO_2/ Si-cap/Ge