NBTI of Ge pMOSFETs: understanding defects and enabling lifetime prediction

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Introduction: Ge pMOSFETs are strong candidates for next technology nodes and record hole mobility has been reported for $Al_2O_3/GeO_2/Ge$ and HfO_2/SiO_2/Si-cap/Ge structures [1-3]. Reliability, however, is still problematic and currently impedes the progress [4-5]. Large NBTI exists in GeO_2/Ge, and little is known about the defects. Si-cap/Ge device has superior reliability, but its lifetime, τ, cannot be predicted by power law extrapolation [3, 4]. *This work demonstrates that the defects are different in Ge and Si devices. For the first time, a method is developed for Ge devices to restore the power law for NBTI kinetics, which enables τ prediction and process optimization* (**Figs.1a-d**).

Current issues: It was reported that NBTI degradation in Si-cap Ge devices by DC measurement cannot be described by power law $\Delta V_{th}=C\cdot V_{ov}^{\gamma}\cdot t^{n}$ [3]. This is also true for GeO_2/Ge devices albeit NBTI is higher [5]. NBTI measured by fast pulse technique is further examined here, and power law is also inapplicable for both Si-cap/Ge (**Fig.1a**) and $Al_2O_3/GeO_2/Ge$ (**Fig.1b**), preventing reliable τ prediction (**Fig.1c**). For Si devices, our latest results show that the power law can be restored for the generated defects (GD), after removing the as-grown hole trapping (AHT) [6]. This Si method works well for Si device, but does not work for Ge (**Fig.2**) and there is a pressing need to develop a new method for Ge to restore power law, enable τ prediction, and assist in process development. *The key advance of this work is to meet this need (**Fig.1d**), based on an understanding of defects in Ge and their differences from Si devices.*

Defect Differences: The devices used are summarized in table 1. **1) Recovery**: Degradation in GeO_2 devices is fully recoverable, but not in Si (**Fig. 3a&4a**); **2) 2nd stress:** After the recovery, 2nd stress in Ge follows the same kinetics as 1st one (**Fig.3b**), indicating all defects returned to fresh states after recovery, while in Si, 2nd stress deviates from 1st one after AHTs are filled (**Fig.4b**); **3) Recharge:** Following discharge through which the energy profiles (**Fig.2a**) are obtained [6], traps in Ge cannot be recharged until charging energy level (EL) is swept back near Ge Ev (**Fig.3c**). For Si, recharge starts once energy level is swept lower than Ec (**Fig.4c**); **4) Temperature (T):** For Ge, no recharge in the upper half of band gap, independent of T (**Fig.3d**). For Si, recharge near Si Ec clearly rises when lowering T (**Fig. 4d**).

Energy Alternating Defects (EAD): The above differences are caused by the presence of EAD in Ge, which is absent in Si devices. As illustrated in **Figs.5a&b**, the energy level of EAD alternates with its charge status: shifts above Ev when charged, and shifts back below Ev when neutralized. In contrast, the generated defects (GD) in Si with energy level well above Ev do not alternate (**Fig.5b**). Since EADs in Ge return to their fresh states once neutralized, 2nd stress in Ge has the same kinetics as 1st one (**Fig.3b**). Recharging EAD can only take place when biased below ~Ev, the same as in a fresh device (**Fig. 3c**), but cannot when biased at ~Ec at either room temperature (RT) or 125 °C (**Fig.3d**). In contrast, since generated defects in Si keep their high energy level after neutralized and do not return to their fresh states, its kinetics during 2nd stress is different from 1st one (**Fig.4b**). The neutralized GDs at high energy level recharge once above Ef (**Fig.4c**). They also recharge when switching from 125 °C to RT as there are less electrons at RT that can reach and neutralize them (**Fig.4d&5b**). The energy alternation with charge status is supported by first-principle calculations (**Fig.6**) [7-9], suggesting that EADs are intrinsic in $Al_2O_3/GeO_2/Ge$. The absence of 'permanent' component in Ge (**Fig.3a**) is because the charged EADs are sufficiently close to Ge Ec and fully neutralized, as the Ec offset at GeO_2/Ge interface is smaller than that at SiON/Si [10].

As-grown hole traps (AHT): All Si AHTs are below Ev and measured by sweeping energy level lower [6]. When this Si method is applied to GeO_2/Ge, it appears that Ge AHTs were also below Ev ('■', **Fig.7a**). This, however, is an artifact and Ge AHTs above Ev (Grey triangle, **Fig.7a**) were not detected by the Si method because of insufficient charging during sweeping due to lower hole density above Ev. By sweeping energy level from low to high, an AHT 'tail' was observed above Ge Ev, which is independent of temperature.

Separating EAD from AHT: To support that Ge AHTs and EADs are two different types of defects, **Fig.7b** shows that EADs increase with stress time, but AHTs do not, since they are 'as-grown'. The initial degradation is dominated by filling AHTs, insensitive to temperature (**Fig.7c**), supporting **Fig.7a**. In contrast, charging EADs is thermally accelerated and does not saturate (**Figs.7b&c**). To separate EADs from AHTs, we obtain the saturation level of AHT for a given stress Eox from **Fig.7a**. EADs is then extracted by subtracting these saturated AHTs from the total ΔVth (**Fig.7d**).

Restore power law and enable lifetime prediction in Ge: When EADs were extracted by evaluating AHTs with Si-method, power-law was restored (**Fig.2b**), but the exponent 'n' varies substantially with Eox ('▲' **Fig.8a**), preventing reliable prediction. In contrast, 'n' is a constant when AHTs were evaluated by the new Ge-method, demonstrating that the AHT-tail above Ev plays a crucial role. This tail does not scale with Eox and impacts more on the raw 'n' at lower Eox. After taking it into account, the variation of lifetime power exponent, m, (**Fig.1c**) disappears, enabling prediction (**Fig.8b**).

Si-cap devices and optimization: **Fig.9a** compares the AHTs in optimized and non-optimized Si-cap Ge devices. The optimized one does not have a tail above Ev, but the non-optimized one does. The non- and optimized Si-cap devices behave like GeO_2/Ge and Si devices, respectively. The AHTs saturate with stress time clearly for both (**Figs.9b&c**). When the Ge-method is applied for the non- and optimized devices, power law was restored (**Figs.10a&b**). The processing temperature for the non-optimized one is higher and Ge can diffuse through Si-cap, making it like GeO_2. **Fig.11** compares the lifetime of different devices/processes. Si-cap Ge is superior to SiON/Si and optimization is clearly needed for GeO_2/Ge, agreeing with ref.[3]. For the optimized Si-cap device, an overdrive voltage of 1.77 V can be used to keep ΔVth within 100 mV for 10 years.

Conclusions: Conventional τ prediction method developed for Si is inapplicable to Ge devices. There are energy alternating defects in Ge, but not in Si devices. The as-grown hole traps have a tail above Ev for Ge, but not Si devices. For the first time, the importance of this tail is demonstrated for restoring power law with constant power exponents. The developed Ge method enables lifetime prediction for Ge devices, which assists in Ge process/device optimization.

Reference: **[1]** Kaczer et al, ME, p.1582, 2009. **[2]** Zhang et al, VLSI, p.161, 2012. **[3]** Franco et al, IEDM, p.397, 2013. **[4]** Groeseneken et al, IRPS, p.41, 2013. **[5]** Ma et al, EDL, p.160, 2014. **[6]** Ji et al, IEDM, p.413, 2013. **[7]** Weber et al, JAP, p.033715, 2011. **[8]** Liu et al, JAP, p.083704, 2013. **[9]** Binder et al, ME, p.1428, 2011. **[10]** Lin et al, APL, p. 242902, 2010.

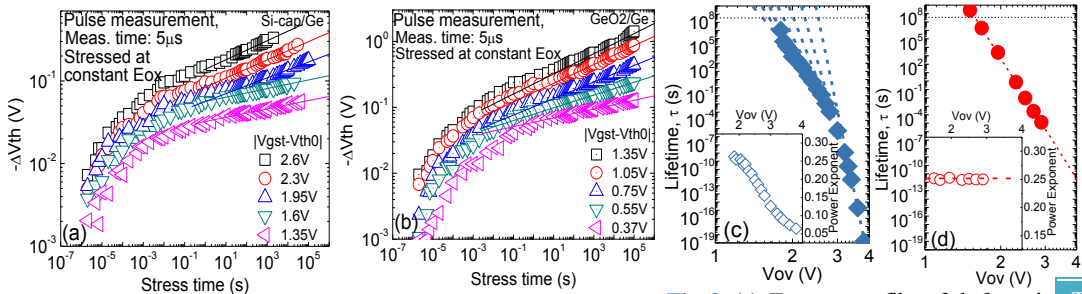

Fig.1 NBTI in (a) Si-cap and (b) GeO_2/Ge devices does not follow a power law. (c) Power law extrapolation failed for Si-cap devices, as the exponent (inset) is not a constant [3]. (d) Power law is restored by the new technique developed in this work with a constant exponent (inset).

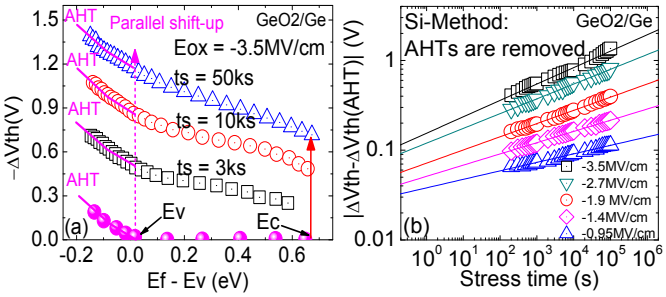

Fig.2 (a) Energy profile of defects in GeO_2/Ge are obtained by discharging defects against energy levels from low-to-high. AHTs, obtained with the Si-method by sweep-charging from high-to-low on fresh device [6], are below Ev and do not increase with stress time. (b) Removing AHT leads to a varying power exponent (slope), preventing reliable extrapolation from high stress Vg to low operation Vg.

Table 1: Gate stack and exponents
a) 2.3nm plasma-N **SiON/Si** (125°C: n=0.20, m=16.1, γ=3.22)
b) 4nm Al_2O_3/1.2nm **GeO_2/Ge** (RT: n=0.20, m=14.4, γ=2.88; 125°C: n=0.24, m=10.9, γ=2.62)
c) 4nmHfO_2/~0.5nmSiO_2/**Si-cap/Ge(non-optimized)** (RT: n=0.19, m=25.3, γ=2.92)
d) 2nmHfO_2/~0.4nmSiO_2/**Si-cap/Ge(optimized)** (thick Si-cap: RT: n=0.25, m=46.0, γ=11.5 ; 125°C: n=0.28, m=34.4, γ= 9.63; thin Si-cap: 125°C: n=0.19, m=34.0, γ=6.46)

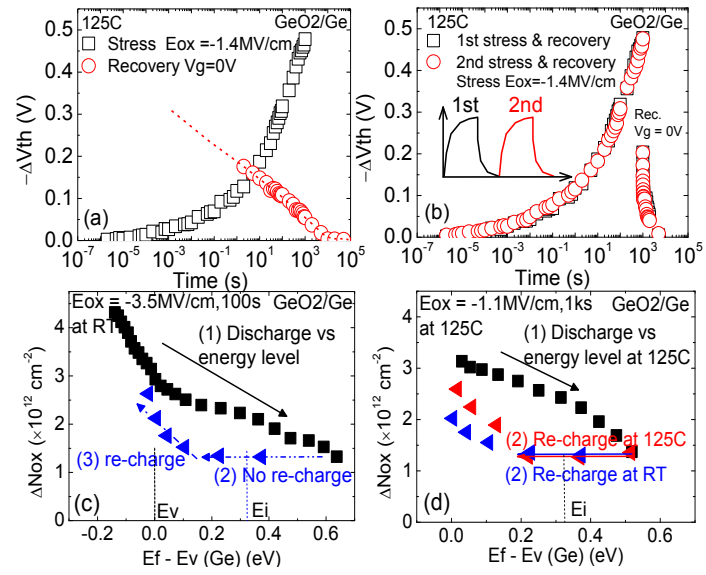

Fig.3 Defects in GeO_2/Ge device: (a) Degradation is fully recoverable without a permanent component. (b) The 2nd stress after recovery follows the same kinetics as the 1st one. All defects returned to their fresh states after recovery. (c) Negligible recharge when biased in the upper half of bandgap. (d) Recharge does not increase when switching from 125°C to room temperature (RT).

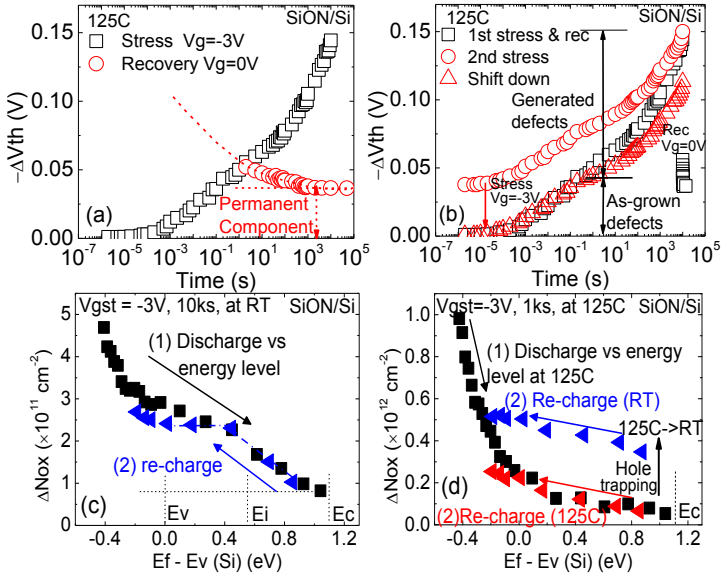

Fig.4 Defects in SiO_2/Si device: (a) NBTI is not fully recovered due to permanent component. (b) 2nd stress after recovery follows the same kinetics for AHTs, but different kinetics for generated defects (GD). '**Δ**' is a parallel downward shift of '**O**'. (c) Recharge occurs in the upper half of band gap. (d) Recharge increases when switching from 125°C and RT. The hole traps neutralized at 125°C at high energy levels are recharged at RT due to lower electron energy at RT.

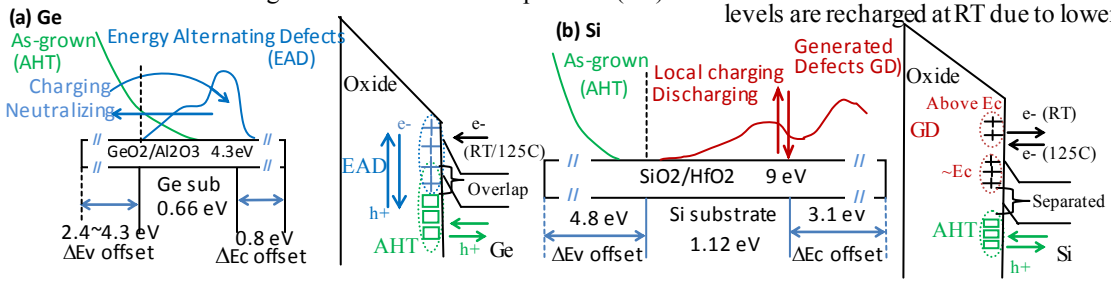

Fig. 5 Illustration of defect differences in Ge and Si devices. (a) GeO_2/Ge: **AHTs**, either charged or neutral, are mainly below Ev with a tail above Ev. **EADs** are below Ev when neutral, shift to above Ev once charged, return to fresh states below Ev after neutralization. (b) SiO_2/Si: **AHTs** are below Ev without the tail. **GDs** are generated and have high energy levels, either charged or neutral. **GDs** above Ec cannot be fully neutralized, leading to the permanent component. **GDs** neutralized at 125°C can be recharged at RT by e-tunneling to Si conduction band. Small Ec offset at oxide/Ge allows full neutralization of **EADs**.

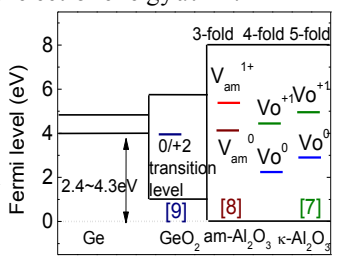

Fig. 6 First principle calculations show intrinsic energy alternating defects in Al_2O_3 [7, 8]. For GeO_2, the charge transition level is reported for hole traps [9].

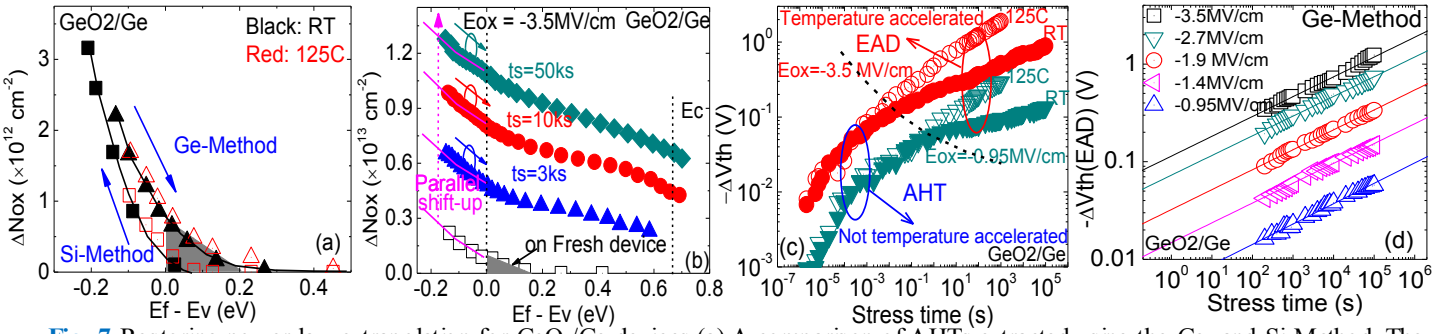

Fig. 7 Restoring power law extrapolation for GeO_2/Ge devices (a) A comparison of AHTs extracted using the Ge- and Si-Method. The Ge method detects a tail above Ev (Grey triangle). (b) AHTs do not increase with stress time, resulting in the marked parallel shift. (c) AHTs are filled first during stress and is temperature independent, whilst EADs is the opposite. (d) Power law is restored after removing AHT extracted with Ge-Method in (a), during which the filling time is kept short enough so that EADs are negligible.

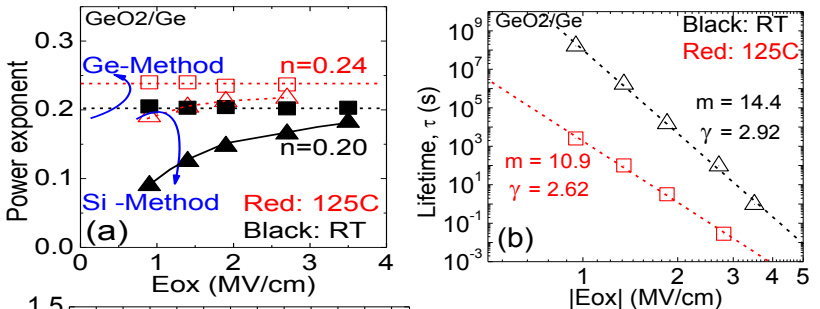

Fig. 8 GeO_2/Ge devices: (a) Constant time power exponents, n, are obtained at both RT and 125C with Ge-Method, but not with Si-Method. The impact of AHT-tail is larger at lower Eox, as it counts to a larger percentage of total degradation. (b) Lifetime prediction are enabled at both RT and 125°C by using the Ge-method, as a constant time-to-failure exponent, m, is restored in both cases. m=γ/n. With T increase, the reliability reduces as suggested by m & γ.

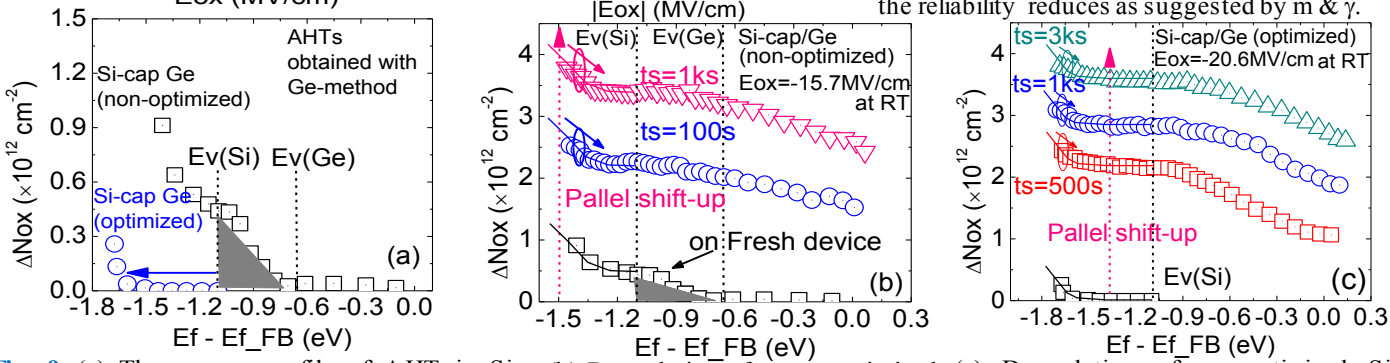

Fig. 9 (a) The energy profile of AHT in Si-cap/Ge (optimized) is further away (~0.4eV) from Ev than Si-cap/Ge (non-optimized). AHT tail is observable in fresh non-optimized device inside Si bandgap, but not in the optimized one. (b) Degradation of a non-optimized Si-cap/Ge device. Like GeO_2/Ge device: AHTs have a tail above Ev(Si) and do not increase with stress time. (c) Degradation of an optimized Si-cap/Ge device. Like SiON/Si device: AHTs do not have a tail above Ev and do not increase with stress time (also in the optimized thin Si-cap/Ge, not shown).

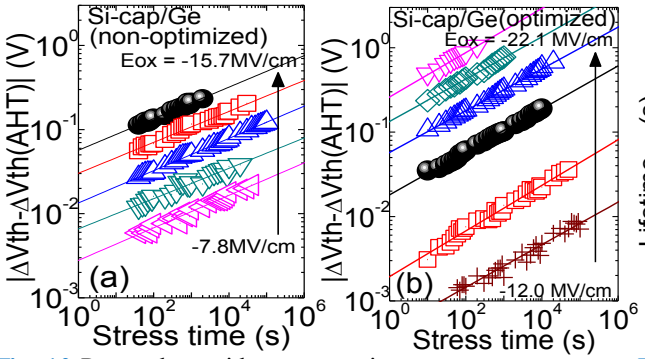

Fig. 10 Power law with constant time power exponent, n, is restored with Ge-Method for Si-cap/Ge (a) non-optimized and (b) optimized device. Both tests are at RT. Constant time-to-failure power exponent, m, is also restored for both cases, as shown in Fig.11, enabling reliable lifetime prediction. Eox of '●' is similar for (a)&(b).

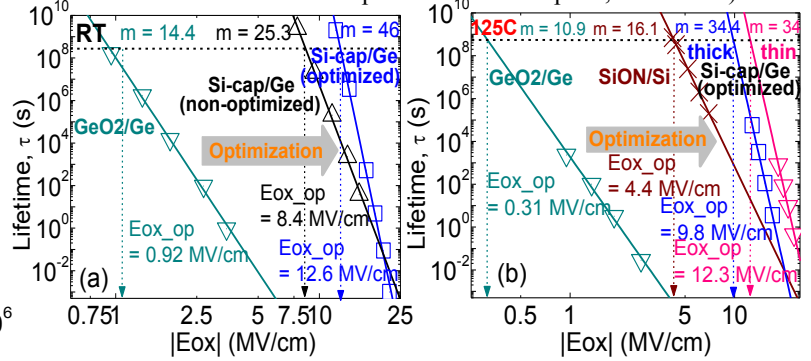

Fig. 11 A comparison of lifetime prediction on different CMOS processes by the new Ge-method developed in this work at (a) RT and (b) 125°C. Si-cap/Ge MOSFETs shows superior reliability. Si-cap/Ge (optimized) show process improvement over the non-optimized one (a). Thick&thin Si-cap (optimized) leads to a larger m & γ (table1) and longer life time/higher maximum operational voltage than Si technology at 125°C (b). Power law is restored in all cases, enabling process evaluation.