Xue, Y, Ren, P, Wu, J, Liu, Z, Wang, S, Li, Y, Wang, Z, Sun, Z, Wang, D, Wen, Y, Xia, S, Zhang, L, Zhang, J, Ji, Z, Luo, J, Deng, H, Wang, R, Yang, L and Huang, R

On the understanding of PMOS NBTI degradation in advance nodes: Characterization, modeling and exploration on the physical origin of defects

On the understanding of PMOS NBTI degradation in advance nodes: Characterization, modelling and exploration on the physical origin of defects

Yongkang Xue, Pengpeng Ren, Junjie Wu, Zhuyou Liu, Shuying Wang, Yu Li, Zirui Wang, Da Wang, Yichen Wen, Shiyu Xia, Lining Zhang, Jianfu Zhang, Zhigang Ji, Junwei Luo, Huixiong Deng, Runsheng Wang, Lianfeng Yang, and Ru Huang

***Abstract*— A complete separation flow for different types of traps, including the separation of energy levels and the separation of charging kinetics, making different traps can be modeled and characterized separately by simple experiments. Industrial-grade 7nm pFinFETs under NBTI stress condition is chosen for the demonstration. Four types of traps are identified, including oxide trap Type-A located in IL layer, oxide trap Type-B (B1 & B2) located in HK layer and interface trap Type-C located at Si/IL interface. Type-A trap belongs to pre-existing trap which can be well described by the two-state non-radiative multi-phonon (NMP) theory and may originate from Vo in SiO_2. Type-B1 and Type-B2 traps originate from Ni and Hi respectively, and can be described by incorporating the activation state into the two-state NMP theory. Type-C located at Si/IL interface and follows the classical power law relationship with the time exponent of 0.17, which may be caused by the breakage of the Si-H bonds due to the reaction with atomic H from either the substrate or the gate. By modelling each type of traps respectively, a unified aging prediction framework was proposed and its long-term predictive capability was experimentally verified under various working conditions. The contribution of each traps to degradation is also discussed, which are helpful to the Design-Technology co-optimization (DTCO) in advanced nodes.**

***Index Terms*— Negative Bias Temperature Instability (NBTI), FinFET, reliability, oxide traps, interface traps, 7nm**

I. Introduction

Negative bias temperature instability (NBTI) continues to be an important reliability issue as the process node scales down [1]. Driven by the low power application requirements, the operating voltage has been reduced low enough[2]–[6]. Limited design margin resulting from lower VDD requires a more precise physical-based ageing model to describe the degradation in the long term. Therefore, clarifying the distributions of the defects and their behavior becomes necessary. Although the underlining physical mechanism is still under debate, it is widely accepted that the traps within the dielectric act as the main root for BTI degradation [7],[8]. The methodologies used to characterize them can be broadly divided into the bottom-up and top-down approaches. The bottom-up approach, such as the random telegraph signal (RTS) [9] or the time-dependent defect spectroscopy (TDDS) technique [10], directly monitors the single defect, including its dynamic behavior. By gathering statistical information on defects from small-area devices [8], the defect-centric model can be established. Such an approach requires a large number of measurements and thus becomes time-consuming. In addition, traps with extreme-long time constants may be missed, resulting in underestimating the device degradation in the longer term. The top-down approach, such as the extended measure-stress-measure (eMSM) [11] or the on-the-fly (OTF) [12], captures the devices' macroscopic degradation, which usually exhibits the overall shift of the threshold voltage in pre-set periods. Such approaches are generally used on large-area devices and rely on mathematical fitting to decompose the contribution of different types of traps, leading to uncontrollable errors in long-term prediction. Recently, Effective Single Defect Decomposition (ESiD) [8], [13] has been proposed to overcome such issue, however, fitting every single defect with physical parameters (E_T, S, x_T) and their weights undoubtedly requires high computation resources.

By trap filling and the following gradual discharging, the discharging-based multi-pulse technique (DMP) [14] has been shown as a powerful tool in understanding oxide traps in transistors with different device structures [15], channel [16], and dielectrics materials [17]. DMP also belongs to the top-down approach and thus does not requires time-consuming measurements. Different traps can be directly separated through measurements rather than curve fitting [16]. Therefore, understanding the dynamics of each type of trap can ensure the model's accuracy, concurring the inaccuracy problem without sacrificing efficiency.

This work presents a comprehensive solution using the DMP technique to establish the defect-centric model for NBTI, with the long-term predictive capability of good accuracy. The paper is organized as follows. The details of devices and experiments are described in Section II. Section III proposes a complete

Yongkang Xue, Pengpeng Ren, Junjie Wu, Shuying Wang, Da Wang, Yichen Wen, Shiyu Xia and Zhigang Ji are with the National Key Laboratory of Science and Technology on Micro/Nano Fabrication, Shanghai Jiaotong University, Shanghai 200240, China (e-mail: zhigangji@sjtu.edu.cn).

Yu Li, Zirui Wang, Lining Zhang, Runsheng Wang and Ru Huang are with the School of Integrated Circuits, Peking University, Beijing 100871, China (e-mail: r.wang@pku.edu.cn).

Zhuyou Liu, Junwei Luo and Huixiong Deng are with Center of Materials Science and Optoelectronics Engineering, UCAS, Beijing 100871, China (e-mail: jwluo@semi.ac.cn).

Lianfeng Yang is from Primarus Technologies, Shanghai, China.

separation flow for different types of traps. In Section IV, we characterize each type of trap separately and establish the corresponding physical-based model. Moreover, a deeper understanding of each trap via qualitative analysis of each trap's physical location, including their vertical locations along the channel and round-Fin locations, is also discussed. In Section V, we introduce an ageing prediction framework and validate its predictive capability under DC & AC & arbitrary conditions. In the end, the article is concluded in Section VI.

II. Device and Experimental

An industrial-grade 7nm pFinFETs with an equivalent oxide thickness of 1.16 nm are used in this work. The channel length and width of devices under test (DUTs) are 240 nm and 1.1μm, respectively. The test pattern of this work based on the discharging-based multi-pulse technique (DMP) is shown in **Fig.1**. After filling under a high voltage bias (V_{stress}), the corresponding traps at each energy level can be stripped layer by layer by gradually lowering the gate voltage. At each discharge voltage (V_{dischN}), a pulse IV within 7.5μs is measured via ultra-fast measure-stress-measure (MSM) sequence using the Keysight B1530A equipped with waveform generator / fast measurement unit (WGFMU). The duration of each discharge voltage lasts 5s [16]. The pulse IV is performed in linear region (I_{dlin}) with V_d = -0.05V, and the threshold voltage is monitored by sensing at a constant drain current of 1 μA × W/L. The testing temperature is 125 °C unless otherwise specified.

III. Separation Method for Different Types of Traps

A. Energy profile of different traps

The separation of different types of traps is based on their energy profiles. Firstly, V_{disch} is converted to the energy level of E_f with respect to E_v at the Si/IL interface, i.e. (E_f-E_v) [18]. It is worth noting that such an energy level is the equivalent energy level that assumes the traps are at the interface between the channel and dielectric. The separation flow of traps is shown in **Fig.2**: When the charging bias ($V_{gstress}$) is low, the energy profiles extracted from discharging after filling at different $V_{gstress}$ overlap well, while they deviate from each other for higher $V_{gstress}$ (Fig.2a), suggesting that there exists two types of

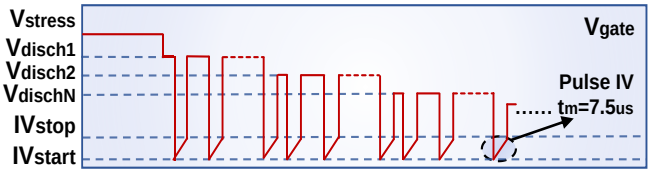


Fig.1. Illustration of the discharging-based multi-pulse (DMP) technique. After trap filling, the traps are discharged gradually

traps in the oxide for such phenomenon. For Type-A traps, if filled at a certain voltage, it can also be released at the same voltage when the bias is lowered. Type-A shows a negligible change in its energy level once captured or discharged. In contrast, Type-B traps need to be released at an energy level lower than where they are filled, suggesting that Type-B may shift energy levels after hole capturing and exhibit the nature of switching traps.

As shown in the inset of **Fig.2b**, Type-A trap can be separated by shifting down the energy profiles under high bias and aligning them with profiles under low bias. The details for such separation can refer to ref. 17. Type-A traps are extracted from multi-DMP measurements with different charging time. As shown in **Fig.2b**, they overlap each other, suggesting the nature of fast saturation.

We then subtract Type-A from the total degradation, as shown in **Fig.2c&d**, the remaining part contains both oxide traps and interface traps. What is worth noting is that even during discharging under different E_f-E_v during DMP test, the threshold voltage (V_{th}) is always sensed at the constant current, which can be approximately considered as the same surface potential. Therefore, the contribution from interface traps in the measured V_{th} shift is the same for different E_f-E_v. Therefore, the impact of interface traps can be removed through the mathematical differentiation with respect to the energy levels. As shown in **Fig.2e**, a clear dual peak can be observed. We label the narrow one as Type-B1 and the wider one as Type-B2. By fitting with two Gaussian distributions and integrating along the energy levels, Type-B can be extracted, as shown in **Fig.2f**. Finally, by subtracting Type-A, Type-B1, and Type-B2 from the total degradation in **Fig.2g**, Type-C can be obtained, exhibiting a constant value against energy level in **Fig.2h**, which seems it is hard be "discharged". However, just as

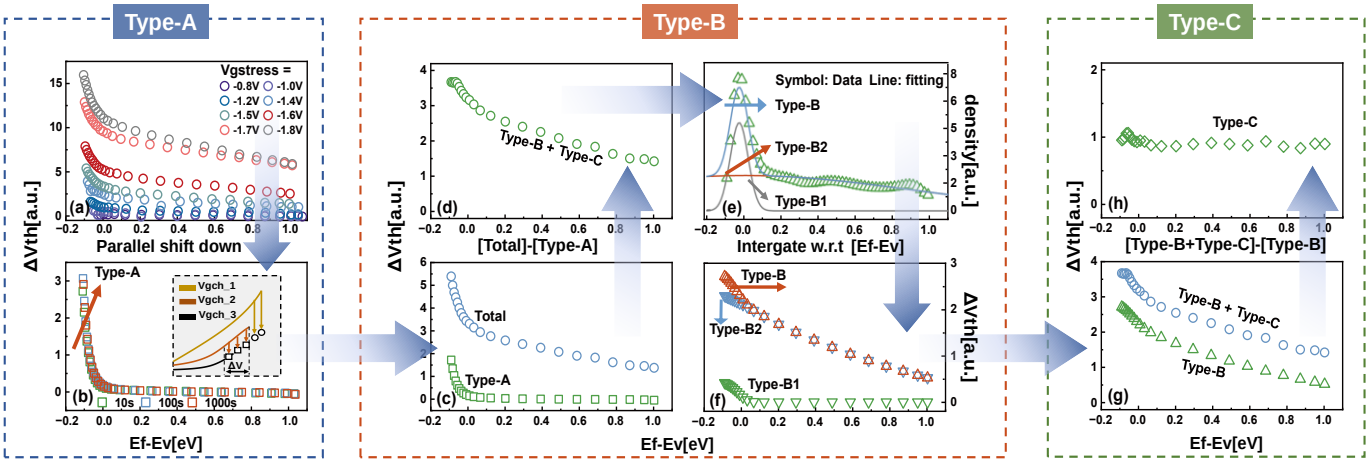


Fig. 2. Proposed procedure to separate different types of traps. Based on DMP technique under different stress biases, three types of traps are clarified and separated. Type-A captures holes without changing energy levels while type-B shifts energy levels after hole capturing. Type-C presents constant energy levels and agree with interface states.

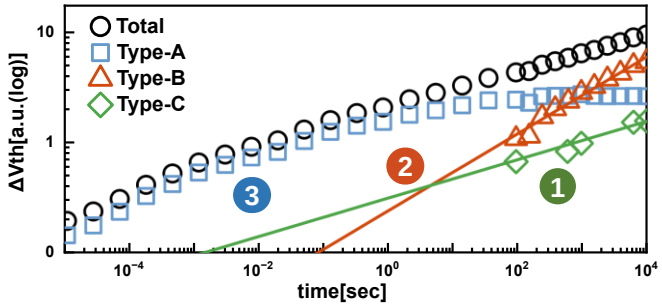


Fig.3. Extraction procedure of charging kinetics of three types of traps under specific stress condition.

mentioned above, its independence of energy level is just because of the same sensing level.

B. Charging kinetics of different traps

Understanding the charging kinetics of each type of trap can be critical for modelling long-term reliability. For this purpose, the measure-stress-measure (MSM) sequence is adopted. Wherein, DMP is performed during the measurement step. The kinetics of Type-C trap (i.e. interface traps) can be extracted as shown as '◇' in **Fig.3**. Since Type-A can quickly saturate (**Fig.2b**), the kinetics of Type-B at longer term can be derived by subtracting Type-C and the saturated Type-A ('Δ' in **Fig.3**). Both Type-B and Type-C traps exhibit a power law relationship. By back-extrapolating Type-B and Type-C and subtracting from the total degradation, the kinetics of the Type-A trap can be obtained ('□' in **Fig.3**). **Fig.3** summarizes the entire extraction procedure. By repeating the procedure, the kinetics of different types of traps under different voltages can be obtained, which is to be used for establishing the physical-based model for ageing kinetics in the next section (**Fig.4**).

IV. Defect Modeling and Physical Origin

A. Physical-based Defect Model

Type-A traps: Type-A traps capture a hole without changing its energy level, suggesting that there is a negligible rearrangement of microscopic structure. This is in coincidence with the properties of structural defects that are widely observed in amorphous system [19],[20]. Therefore, the trapping/de-trapping process of Type-A traps can be modelled with a simple two-state model based on the non-radiative multiphonon theory (NMP). The schematic of the two-state model is shown in **Table.I**, in which energy wells 1 and 2 represent the energy of two states before and after trapping, respectively. ε_{12} and ε_{21} represent the barrier height of the transition between two wells, respectively. Once the negative stress voltage is applied, ε_{12} is lowered, and more holes can jump over the barrier through thermal emission. To account for the distribution, the Gaussian distribution of the trap energy E_T and relaxation energy S is assumed.

Type-B traps: To account for the lattice relaxation process, the behaviors of both Type-B1 and Type-B2 are modelled by a three-state process. During charging, the trap needs to be firstly activated from state 1' to state 1, then the charging process can occur from state 1 to state 2. By fitting the charging kinetics of Type-B (i.e. Type-B1+Type-B2 obtained from **Fig.3**) and the multi-DMP results of Type-B1 and Type-B2 (data from **Fig.2f**), the model parameters can be obtained. As shown in **Fig.4c-e**, the lines from the model can fit well with the experimental results. What is worth noting is that without considering the activation process (1'->1), the kinetics of Type-B traps cannot be fitted, which further confirms its nature of switching type.

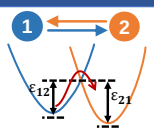
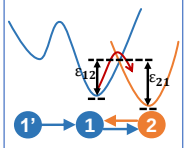
Type-C traps: As shown in **Fig. 4f**, they can be described with the classical power law relationship. The time exponent is found to be 0.16, which is also broadly observed in recent years across multiple technologies by using the delay-corrected DCIV technique [21] or by probing Vth degradations under conditions where hole trapping is minimal. The time exponent has been historically considered the signature of the interface states generation controlled by the Reaction-Diffusion process in which the Si-H bond is assumed to break at the Si/IL interface and diffuse as a hydrogen molecule into the oxide [22]. However, the theoretical study [23] suggests the Si-H bond can be rather stable, putting this R-D process in doubt. Recently, it is proposed that the breakage of the Si-H bonds may be due to the reaction with atomic H from either the substrate [24] or the gate [25], going through the exothermic reaction Si-H + H → Si- + H_2.

B. Discussion on the Physical location

A typical HKMG stack structure contains a silicon oxide based interfacial layer (IL) and a high-k dielectric (HK layer). We extracted the physical thickness of these two layers by measuring the gate leakage current under different temperatures and fitting with *GINESTRA® simulation software* [26]. The extracted values for IL and HK layers are 0.8nm and 1.85nm, respectively. To estimate the traps' location, we evaluate the fitting error between the measured data and the proposed model by assuming these traps distributed uniformly either in the IL or the HK layer. As shown in **Fig.5a**, when Type-A and Type-B traps are in the IL and HK layer respectively, the error becomes minimum.

For further confirmation, we compare the impact of the traps on the corresponding current degradation ($\Delta Id/Id_0$) against the degradation of threshold voltage (ΔV_{th}). As shown in **Fig. 5b**, Type-A and Type-C show similar slope which is larger than Type-B, suggesting Type-A and Type-C has the similar impact on mobility degradation. Since Type-C trap is at the interface, Type-A should also be close to the Si/IL interface, which

TABLE I

	Model		Fitting parameters
Type-A (2 state NMP)		$k_{12} = pv_{th}\sigma\vartheta e^{-\beta\varepsilon_{12}}$ $k_{21} = N_v v_{th}\sigma\vartheta e^{-\beta\varepsilon_{21}}$	$(<E_T>, \sigma_{E_T}, <S>, \sigma_S, \sigma_{ccs}, N_T)$
Type-B (3 state NMP)		$k_{11'} = A * exp(B * E_{ox}) * [1 - exp(-(t/\tau)^{\beta})]$ $k_{12} = pv_{th}\sigma\vartheta e^{-\beta\varepsilon_{12}}$ $k_{21} = N_v v_{th}\sigma\vartheta e^{-\beta\varepsilon_{21}}$	$(<E_T>, \sigma_{E_T}, <S>, \sigma_S, \sigma_{ccs}, N_T, A, B, \tau, \beta)$
Type-C (power-law)	—	$\Delta V_{th} = A * V_g{}^m * t^n$	(A, m, n)

Established Physical-based defect model for three types of traps and their corresponding parameters used for fitting.

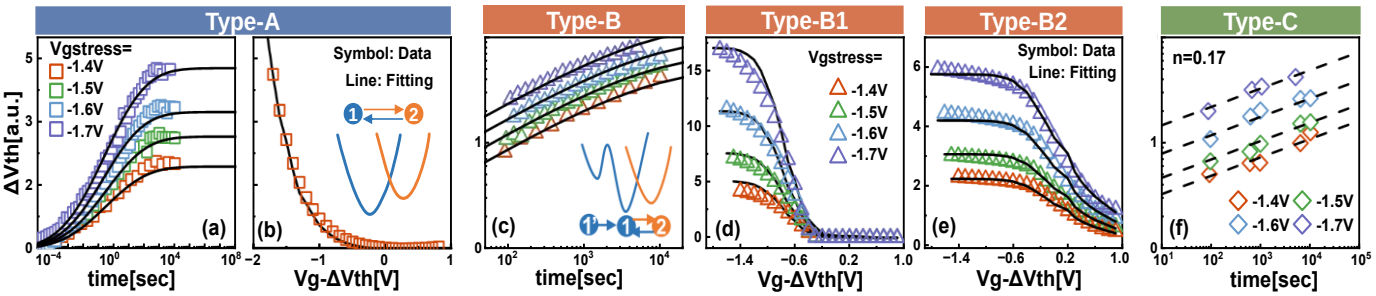


Fig.4. (a) The charging kinetics and (b) energy level distribution of Type-A traps can be well modelled by the two-state non-radiative multi-phonon (NMP) theory. (c) The charging kinetics of Type-B (B1&B2) traps, (d) energy level distribution of Type-B1 traps, and (e) energy level distribution of Type-B2 traps can be modelled by incorporating the activation state into the two-state NMP theory. (f) The charging kinetics of Type-C can be well fitted by power law relationship with the time exponent of 0.17.

supports that Type-A is located in the IL layer. Type-B traps show a less steep slope, suggesting that they are away from the interface. This also agrees that they are in the HK layer.

C. *Discussion on the physical origin*

The energy level (E_T) and relaxation energy (S) can be used as the signature to pursue for the physical origin of the traps. Therefore, we can extract E_T and S by fitting the experimental data with the proposed model and compare with the DFT calculation to explore the potential physical origin of the traps.

To determine E_T and S, the surface potential against gate voltage relationship ($V_s \sim V_g$) is essential, which however, can vary when the traps are at different location in the fin (**Fig.6a**). We calculate the channel surface potential between Fin top and side wall respectively through calibrated TCAD simulation. Under the same V_g, V_s of Fin-top and Fin-side are separated when moving towards strong inversion or accumulation (**Fig.6b**). Therefore, the impact on the E_T and S extraction should be examined first.

As shown in the lower panel in **Fig.7a**, no matter fin top or the fin side, the energy level for Type-A trap can be very deep. The mean value of E_T is around 2.33eV and 2.5eV below the Si midgap for fin side and top, respectively. E_T distributions for Type-B1 and Type-B2 are shown in the lower panel in **Fig.7b**, which is not sensitive to the location. They are located at 1eV and 0.4eV below the Si midgap, respectively. The difference in the location sensitivity can be ascribed to the trap energy location: Type-A has a very deep energy level where $V_s \sim V_g$ is sensitive to the location, while Type-B is relatively shallow in which V_s is not sensitive to V_g. The relaxation energy of different traps by assuming different locations is shown in the lower panel of **Fig.7c&d**. Similarly, the impact is negligible.

For defects in SiO_2, several candidates have been suggested, including the oxygen vacancies (Vo) [27], the hydrogen bridge (HB) and the hydroxyl E' centers (HE) [8]. E_T and S have been systematically calculated in ref.8 calculated. The comparison between the theoretical and the experimental values is shown in **Fig.7a&b**. Both HB and HE defects have a considerable part of components within the Si bandgap. However, Type-A is located below the Si valance band, and the energy level is relatively deep. Therefore, these two types of defects may not be candidates for Type-A. The oxygen vacancy, Vo is the only defect that shows deep energy levels. Although Type-A is slightly shallower than the energy level of Vo, considering that DFT can have a calculation error of 0.5eV [8], we consider there could be a strong correlation between Type-A and Vo. Moreover, the experimental and theoretical S also shows good agreement. Therefore, Type-A can be considered as the pre-existing trap originating from oxygen vacancy. From this point of view, this is consistent with the abovementioned claim that Type-A is the structural defect that is introduced during fabrication due to process imperfectness.

Both Type-B1 and Type-B2 are shallower than Type-A, as shown in the lower panel of **Fig.7c**. We constructed several possible defect structures widely observed in HK layers including the oxygen vacancy (Vo) [28], the interstitial hydrogen (Hi) [29], Nitrogen (Ni) [30] and Oxygen interstitial (Oi) [28]. The HK layer of the amorphous nature is taken into consideration. The calculated results are shown in the upper panels of **Fig.7c&d**. The comparison with the experimental data suggests that Type-B1&B2 may originate from Ni and Hi, respectively. Since the concentration of H can be much larger than N, Type-B2 is far more than Type-B1, which is confirmed by the experimental data (**Fig.3e-f**). Interstitial H could be stabilized as either the hydrogen bridge (HB) or the hydroxyl E', which undergoes a transition to the excited vibronic state after hole capturing. By dissipating the excess energy through the

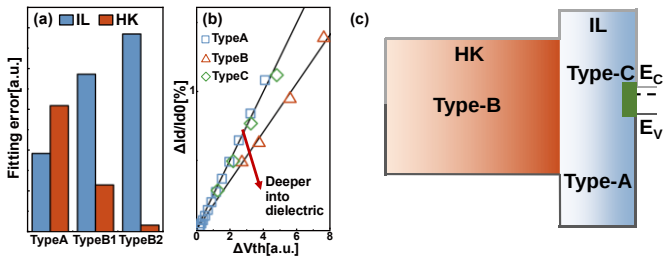


Fig.5. (a) Fitting error comparison when assuming the physical locations of Type-A, Type-B (B1&B2) in IL or HK layer. (b) Current degradation comparison for the three types of traps. (c) Illustration of the determined locations of the three types of traps.

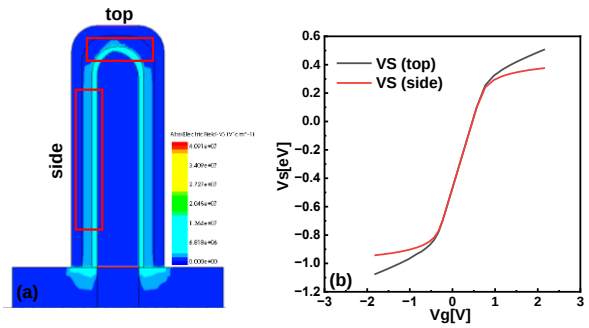


Fig.6. (a) Electric field strength distribution calculation of Fin-top and Fin-side on calibrated TCAD simulation. (b) Surface potential versus gate voltage relationship of Fin-top and Fin-side.

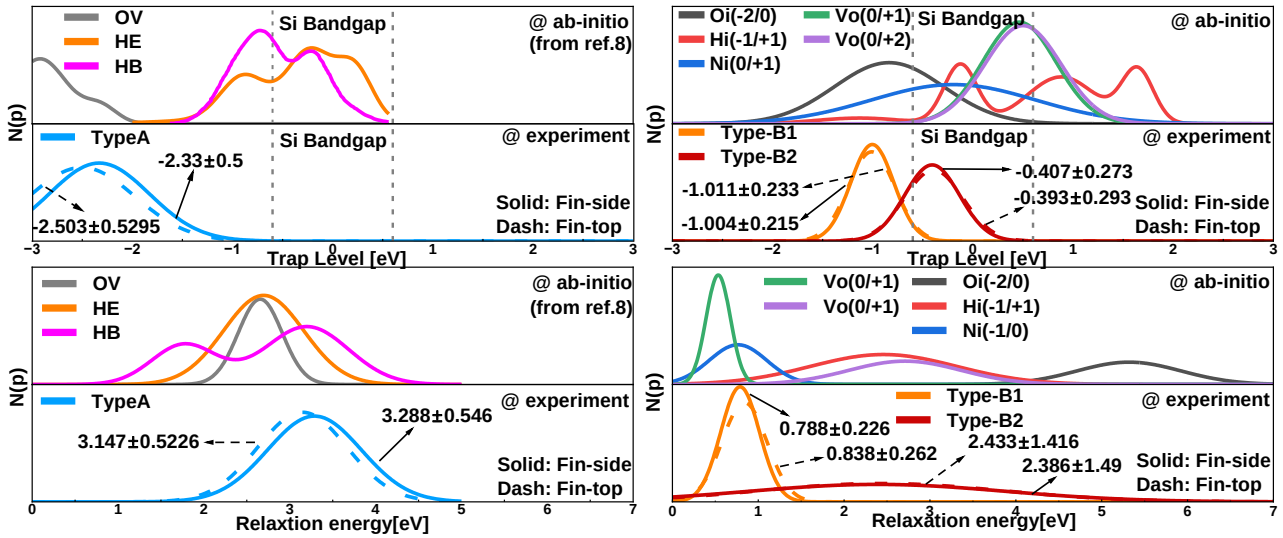


Fig.7. Comparison of the Ab-initio calculation and experiment for (a) energy level and (b) relaxation energy of Type-A in the IL; (c) energy level and (d) relaxation energy of Type-B (B1&B2) in the HK layer.

multi-phonon emission process, they can relax to a lower energy level.

V. MODEL VALIDATION FOR PREDICTIVE CAPABILITY

A. Validation for Predictive Capability

Based on the established models of each trap, the total degradation can be calculated by the ensemble of traps of different types. After determining the filling occupancy of each type of trap based on the corresponding physical process, the averaged degradation can be estimated by multiplying the average trap number of each type with the extracted areal density and summing up.

Here, we validate the predictive capability of our proposed model. we calculate the degradation under AC conditions with different duty factor (**Fig.8a**), and compare with the experiment data. The good agreement between the prediction and the measurement shows that our model can accurately depict the dynamic behavior of traps. The contributions of different traps can be well decomposed as shown in **Fig.8b**. Type-A dominates in a short period, while Type-B2 has a more obvious upward trend compared with others, indicating it may become the major killer for the device's long-term reliability.

Besides, degradation under arbitrary waveform conditions (**Fig.9a**), the long-term frequency (**Fig.9b**) and duty factor (**Fig.9c**) dependences can also be predicted well. What is worth pointing out is that such good agreement is not fitting. All the model parameters are extracted on the data from dc stress and energy profiles. No dynamic information is involved in the fitting process. Good agreement between the prediction and the measured data strongly supports the correctness of the proposed model.

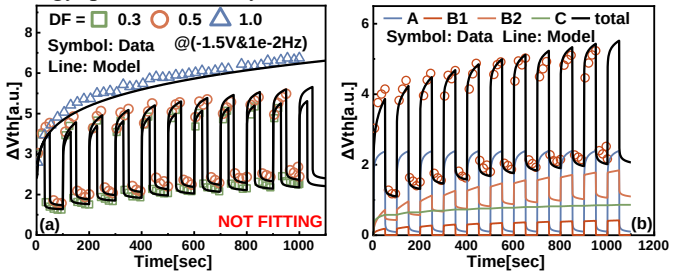


Fig.8. (a) Comparisons of the proposed model and experiment data under DC & AC conditions. (b) The contributions of different traps can be well decomposed.

B. Defect contribution for long-term reliability

Traditionally, long-term reliability can be predicted through extrapolation with simple power law relationship against voltage and time. We compared our model with the traditional method under VDD = -0.75 V, as shown in **Fig.10a.** 10-year degradation predicted by the traditional power-law model is larger than our model by about 50%, suggesting that the traditional method can underestimate the device's lifetime, and leaving a smaller design margin for designers. By decomposing each trap's contribution from total degradation, we find that Type-A trap quickly saturate (about 2mV), while Type-B1 and Type-C trap's degradation is less than 1mV, which can be ignored. Type-B2 trap accounts for most of the total degradation, indicating it is the major killer for the device's long-term reliability. To explore the feasibility of the device under overvoltage application, we also compared the degradation of the device under different VDD voltages (**Fig.10b**). Type-B2 is still dominant, but its proportion decreases with the increase of voltage (**inset of Fig.10b**). The proportion of Type-C increases with the voltage, but it is still too small compared to Type-B2. Therefore, it is concluded that Type-B2 traps can be the most important defect type and should be focused in manufacturing and eliminated by process optimization to improve circuit performance and reliability.

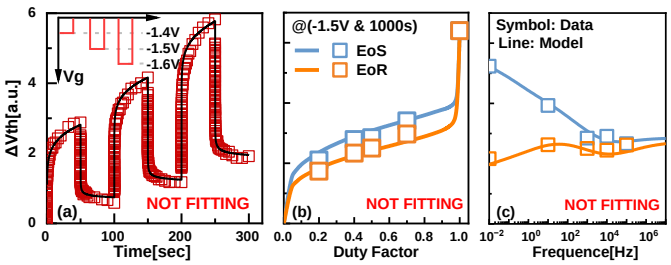


Fig.9. Comparisons of the proposed model and experiment data under (a) Arbitrary waveform conditions and AC conditions with different (b) duty factors and (c) frequencies.

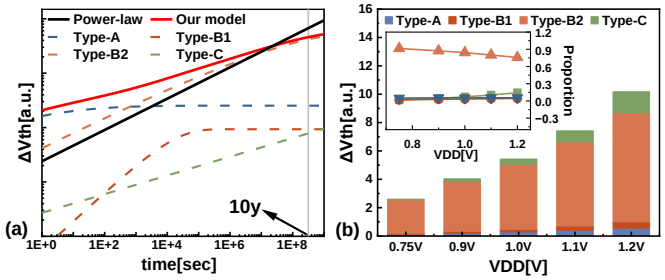


Fig.10. (a) Comparison of our model and traditional power-law model in long-term reliability prediction. (b) Reliability prediction and defect contribution of different types of traps in over-VDD application.

VI. Conclusion

In this paper, a complete separation flow for different types of traps, including the separation of energy levels and the separation of charging kinetics has been proposed and demonstrated on industrial-grade 7nm pFinFETs under NBTI condition. Four types of defects are separated and can be analyzed individually. Wherein, Type-A is oxide traps locating in IL layer. Its energy level is relatively deep and may originate from Vo in SiO_2. Type-B1 and Type-B2 are the oxide traps locating in HK layer, which may originate from Ni and Hi, respectively. Type-C are interface traps locating at Si/IL interface, which may be caused by the breakage of the Si-H bonds due to the reaction with atomic H from the gate. Based on the modelling of each type of traps, the long-term predictive capability under DC conditions, AC conditions with different frequencies, and arbitrary waveform conditions are verified. The contribution of each traps to degradation is also discussed, which are helpful to the Design-Technology co-optimization (DTCO) in advanced nodes.

References

[1] V. Huard, F. Cacho, X. Federspiel, W. Arfaoui, M. Saliva, and D. Angot, "Technology scaling and reliability: Challenges and opportunities," in *2015 IEEE International Electron Devices Meeting (IEDM)*, 2015, no. June 2014, pp. 20.5.1-20.5.6, doi: 10.1109/IEDM.2015.7409743.

[2] J. H. Stathis *et al.*, "Reliability challenges for the 10nm node and beyond," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2015-Febru, no. February, pp. 20.6.1-20.6.4, 2015, doi: 10.1109/IEDM.2014.7047091.

[3] G. Groeseneken, R. Degraeve, B. Kaczer, and K. Martens, "Trends and perspectives for electrical characterization and reliability assessment in advanced CMOS technologies," *2010 Proc. Eur. Solid State Device Res. Conf. ESSDERC 2010*, pp. 64–72, 2010, doi: 10.1109/ESSDERC.2010.5617735.

[4] J. F. Zhang, R. Gao, M. Duan, Z. Ji, W. Zhang, and J. Marsland, "Bias Temperature Instability of MOSFETs: Physical Processes, Models, and Prediction," *Electron.*, vol. 11, no. 9, 2022, doi: 10.3390/electronics11091420.

[5] R. Wang *et al.*, "Too Noisy at the Bottom? - Random Telegraph Noise (RTN) in Advanced Logic Devices and Circuits," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2019, vol. 2018-Decem, pp. 17.2.1-17.2.4, doi: 10.1109/IEDM.2018.8614594.

[6] K. Choi *et al.*, "Reliability on evolutionary FinFET CMOS technology and beyond," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2020-Decem, pp. 9.3.1-9.3.4, 2020, doi: 10.1109/IEDM13553.2020.9371930.

[7] S. W. M. Hatta *et al.*, "Energy distribution of positive charges in gate dielectric: Probing technique and impacts of different defects," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1745–1753, 2013, doi: 10.1109/TED.2013.2255129.

[8] D. Waldhoer *et al.*, "Toward Automated Defect Extraction from Bias Temperature Instability Measurements," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 4057–4063, 2021, doi: 10.1109/TED.2021.3091966.

[9] E. Simoen and C. Claeys, "Random telegraph signal: A local probe for single point defect studies in solid-state devices," *Mater. Sci. Eng. B Solid-State Mater. Adv. Technol.*, vol. 91–92, pp. 136–143, 2002, doi: 10.1016/S0921-5107(01)00963-1.

[10] T. Grasser, H. Reisinger, P. J. Wagner, F. Schanovsky, W. Goes, and B. Kaczer, "The time dependent defect spectroscopy (TDDS) for the characterization of the bias temperature instability," *IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 16–25, 2010, doi: 10.1109/IRPS.2010.5488859.

[11] B. Kaczer *et al.*, "Ubiquitous relaxation in BTI stressing-new evaluation and insights," *IEEE Int. Reliab. Phys. Symp. Proc.*, pp. 20–27, 2008, doi: 10.1109/RELPHY.2008.4558858.

[12] M. Denais *et al.*, "On-the-fly characterization of NBTI in ultra-thin gate oxide PMOSFET's," in *Technical Digest - International Electron Devices Meeting, IEDM*, 2004, pp. 109–112, doi: 10.1109/iedm.2004.1419080.

[13] C. Schleich *et al.*, "Physical Modeling of Charge Trapping in 4H-SiC DMOSFET Technologies," *IEEE Trans. Electron Devices*, vol. 68, no. 8, pp. 4016–4021, 2021, doi: 10.1109/TED.2021.3092295.

[14] Z. Ji *et al.*, "A test-proven As-grown-Generation (A-G) model for predicting NBTI under use-bias," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 2015-Augus, no. 1, pp. T36–T37, 2015, doi: 10.1109/VLSIT.2015.7223693.

[15] L. Zhou *et al.*, "Understanding Frequency Dependence of Trap Generation under AC Negative Bias Temperature Instability Stress in Si p-FinFETs," *IEEE Electron Device Lett.*, vol. 41, no. 7, pp. 965–968, 2020, doi: 10.1109/LED.2020.2992263.

[16] P. Ren *et al.*, "Understanding charge traps for optimizing Si-passivated Ge nMOSFETs," *Dig. Tech. Pap. - Symp. VLSI Technol.*, vol. 2016-Septe, no. 1, pp. 5–6, 2016, doi: 10.1109/VLSIT.2016.7573367.

[17] Z. Ji *et al.*, "An Investigation on Border Traps in III-V MOSFETs With an In0.53Ga0.47As Channel," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3633–3639, 2015, doi: 10.1109/TED.2015.2475604.

[18] R. Gao *et al.*, "A Discharge-Based Pulse Technique for Probing the Energy Distribution of Positive Charges in Gate Dielectric," *IEEE Trans. Semicond. Manuf.*, vol. 28, no. 3, pp. 221–226, 2015, doi: 10.1109/TSM.2015.2407909.

[19] K. R. Farmer and R. A. Buhrman, "Defect dynamics and wear-out in thin silicon oxides," *Semicond. Sci. Technol.*, vol. 4, no. 12, pp. 1084–1105, 1989, doi: 10.1088/0268-1242/4/12/011.

[20] R. Gao, Z. Ji, J. F. Zhang, J. Marsland, and W. D. Zhang, "As-grown-Generation Model for Positive Bias Temperature Instability," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3662–3668, 2018, doi: 10.1109/TED.2018.2857000.

[21] A. Neugroschel, G. Bersuker, and R. Choi, "Applications of DCIV method to NBTI characterization," *Microelectron. Reliab.*, vol. 47, no. 9-11 SPEC. ISS., pp. 1366–1372, 2007, doi: 10.1016/j.microrel.2007.07.037.

[22] S. Mahapatra, P. B. Kumar, and M. A. Alam, "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of p-MOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1371–1379, 2004, doi: 10.1109/TED.2004.833592.

[23] R. Wang *et al.*, "Understanding Hot Carrier Reliability in FinFET Technology from Trap-based Approach," *IEEE Int. Electron Devices Meet.*, pp. 661–664, 2021.

[24] L. Tsetseris, X. J. Zhou, D. M. Fleetwood, R. D. Schrimpf, and S. T. Pantelides, "Physical mechanisms of negative-bias temperature instability," *Appl. Phys. Lett.*, vol. 86, no. 14, p. 142103, Apr. 2005, doi: 10.1063/1.1897075.

[25] T. Grasser *et al.*, "Gate-sided hydrogen release as the origin of 'permanent' NBTI degradation: From single defects to lifetimes," *Tech. Dig. - Int. Electron Devices Meet. IEDM*, vol. 2016-Febru, pp. 20.1.1-20.1.4, 2015, doi: 10.1109/IEDM.2015.7409739.

[26] L. Larcher, A. Padovani, F. M. Puglisi, and P. Pavan, "Extracting Atomic Defect Properties From Leakage Current Temperature Dependence," *IEEE Trans. Electron Devices*, vol. 65, no. 12, pp. 5475–5480, Dec. 2018, doi: 10.1109/TED.2018.2874513.

[27] T. Grasser *et al.*, "On the microscopic structure of hole traps in pMOSFETs," in *2014 IEEE International Electron Devices Meeting*, 2014, vol. 2015-Febru, no. February, pp. 21.1.1-21.1.4, doi: 10.1109/IEDM.2014.7047093.

[28] J. L. Lyons, A. Janotti, and C. G. Van de Walle, "The role of oxygen-related defects and hydrogen impurities in HfO2 and ZrO2," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1452–1456, Jul. 2011, doi: 10.1016/j.mee.2011.03.099.

[29] M. Kaviani, V. V. Afanas'ev, and A. L. Shluger, "Interactions of hydrogen with amorphous hafnium oxide," *Phys. Rev. B*, vol. 95, no. 7, p. 075117, Feb. 2017, doi: 10.1103/PhysRevB.95.075117.

[30] J. L. Gavartin, A. L. Shluger, A. S. Foster, and G. I. Bersuker, "The role of nitrogen-related defects in high- k dielectric oxides: Density-functional studies," *J. Appl. Phys.*, vol. 97, no. 5, 2005, doi: 10.1063/1.1854210.