# System Level Simulation of Quantum-Dot Cellular Automata Computer Circuits

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# Abbreviation

| | |
|---|---|
| 2DEG | Two-Dimensional Electron Gas |
| AFM | Atomic Force Microscopy |
| AI | Artificial Intelligence |
| AlGaAs | Aluminium Gallium Arsenide |
| ALU | Arithmetic Logic Unit |
| AU | Arithmetic Unit |
| CA | Cellular Automata |
| CAD | Computer-Aided Design |
| CMOS | Complementary Metal-Oxide Semiconductor |
| CPU | Central Processing Unit |
| CU | Control Unit |
| DCT | Discrete Cosine Transform |
| D Flip-Flop | Data flip-flop |
| DRC | Design Rule Check |
| DSP | Digital Signal Processing |
| DUT | Design Under Test |
| EBL | Electron-Beam Lithography |
| ECC | Error Correction Codes |
| FCN | Field-Coupled Nanocomputing |
| FET | Field-Effect Transistor |
| FoM | Figure of Merit |
| GaAs | Gallium Arsenide |
| IC | Integrated Circuit |
| IoT | Internet of Things |
| JK flip-flops | Jack Kilby Flip-Flop |
| LU | Logic Unit |
| LVS | Layout Versus Schematic |
| MBE | Molecular Beam Epitaxy |

| | |
|---|---|
| MFM | Magnetic Force Microscopy |
| MOKE | Magneto-Optical Kerr Effect |
| MOSFET | Metal-Oxide Semiconductor Field-Effect Transistor |
| MQCA | Molecular Quantum Cellular Automata |
| MV | Majority Gate Voter |
| NML | Nanomagnetic Logic |
| NoC | Network on Chip |
| QCA | Quantum-Dot Cellular Automata |
| RAM | Random Access Memory |
| RCA | Ripple Carry Adder |
| ROM | Read Only Memory |
| SoC | System on Chip |
| SR Flip-Flop | Set/Reset flip-flop |
| SRAM | Static Random Access Memory |
| T-Flip-Flop | Toggle Flip-Flop |
| TCAD | Technology Computer-Aided Design |
| USE | Unified, Scalable, and Efficient |
| VLSI | Very-Large-Scale Integration |

# Abstract

Quantum-dot cellular automata (QCA) is an emerging transistor-less field-coupled nanocomputing (FCN) approach to ultra-scale nanochip integration, enabling molecular electronics. In QCA, electron tunnelling between quantum dots enables switching, while electrostatic repulsion drives electrons to opposite positions within the four-dot cell, thereby encoding binary configuration. Current QCA circuit designs are either irreversible or logically reversible. This thesis introduces three innovative design methods for building QCA circuits, including logically and physically reversible, partially reversible, and hybrid design methods. The core component of the logically and physically reversible design method, is an innovative reversible majority gate. This method was applied to construct combinational circuits, sequential flip-flops, and more advanced computing circuits, an arithmetic logic unit and multiplexers. Simulation results demonstrate that the logically and physically reversible design method produces functional QCA combinational, sequential, and more sophistecated circuits, with exceptional energy efficiency improvement of up to 97%. The innovative partially reversible majority gate, is the key component of the partially reversible design method. This method was used to build half-adder circuit. Simulation results of the proposed partially reversible half-adder show that the partially reversible design approach enhances speed by up to 67%, reduces circuit cost by up to 77%, compared to the reversible design method, and improves energy efficiency by up to 86% compared to conventional irreversible circuits. The hybrid design method integrates reversible, irreversible, and partially reversible majority gates, offering greater control over the level of circuit reversibility. This approach was utilized to design four distinct QCA half-adder circuits, each employing a specific combination of these three types of majority gates. Simulation results indicate that increasing circuit reversibility tends to increase cost while reducing energy dissipation. Conversely, reducing circuit reversibility can lower costs but results in higher energy dissipation. The present research endeavour has produced six publications in total: five journal articles and one conference paper.

# Declaration

I hereby declare that the work presented in this thesis is my own and has been carried out in accordance with the regulations of Liverpool John Moores University. It has not been submitted for any other degree or qualification at this or any other university or institution.

All sources of information and the work of others have been appropriately acknowledged through citation and referencing in this thesis. Any collaboration, contributions from others, or published material produced during the course of this research has been clearly stated.

I understand that failure to attribute or reference appropriately constitutes an academic offence and confirm that this thesis complies with the university's academic integrity and ethics policies.

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# Dedication

In loving memory of my late father, whose wisdom and encouragement continue to guide me. I hope this work honours your legacy and brings you pride.

I dedicate this thesis to the cherished individuals whose unwavering support has been the foundation of my strength throughout this academic journey.

To my dearest mother, your sacrifices and unwavering faith have made this achievement possible, and this thesis is a testament to the values you've instilled in me.

To my beloved brothers and sisters, thank you for your steadfast support and constant encouragement, which have been a source of immense comfort throughout this journey.

To my beloved wife, your unwavering support and boundless understanding have been my anchor. Your encouragement has fuelled my determination, and your faith in me has been a constant source of inspiration. This accomplishment is as much yours as it is mine.

To my dear sons, Khaled, Mohanad, Muaid, and Ammar, your smiles, laughter, and love have brightened even the darkest days. You are the greatest blessing in my life.

With profound gratitude and love, I dedicate this work to you all.

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All praise and thanks are due to Allah, the Most Gracious and Most Merciful, for granting me the patience, health, strength, and knowledge to persevere and successfully complete this PhD journey.

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I would also like to extend my heartfelt thanks to my co-supervisor, Dr. Richard Stocker, for his invaluable advice and perceptive feedback. His expertise and thoughtful guidance have played a crucial role in refining this work and greatly enhancing its overall quality.

Finally, I would like to acknowledge all my friends who checked in on me and offered their unwavering encouragement throughout this research. Your collective support exemplifies the true power of friendship and solidarity in helping to overcome challenges.

Thank you.

# Chapter 1

# 1. Introduction

## 1.1. Introduction to Nanocomputing

Nanocomputing refers to the use of computing systems and processes that operate at the nanoscale [1]. This entails the use of components and devices that are a few nanometres in size to build an integrated circuit (IC). Conventional ICs that use transistor-based complementary metal-oxide semiconductor (CMOS) technology encode binary information at two separate voltage levels [2]. A high voltage level represents logic 1, and a low voltage level represents logic 0. CMOS circuits utilise complementary and symmetrical pairs of p-type and n-type metal-oxide-semiconductor field-effect transistors (MOSFETs) to ensure that only one transistor conducts at a time, hence reducing power consumption [3].

In 1965, Gordon Moore predicted that the density of transistors on a single chip would increase twofold every 18 months [4]. The doubled number of transistors results in improved computing efficiency because it enables devices to operate at higher speeds, use less area, and consume less energy. For more than fifty years, Moore's Law has been a fundamental principle driving technological advancement. In recent years, there has been increasing doubt regarding the future sustainability of Moore's Law. The advancement of CMOS technology and the continuous scaling down of transistor feature sizes at the nanoscale have led to growing concern about its associated negative aspects, including high resistances, charge quantisation, inadequate switching levels, subthreshold voltage, gate leakage current, and heat dissipation [5-8]. Additionally, the escalating insatiable demand for increasing the number of devices on the CMOS system on a chip (SoC), already at a count of billions, exacerbates the issue of excessive power dissipation [9] – the chip will melt.

Field-coupled nanocomputing (FCN) is one of the most promising computational techniques for addressing the CMOS scalability challenges [10]. FCN is an innovative approach that allows for the construction of digital nanocomputing circuits without

requiring conventional transistors and the associated charge transport with accompanying Ohmic losses. Instead, FCN relies on the local field interactions among nanoscale components arranged in specific patterns [11].

### 1.2. Introduction to Quantum-Dot Cellular Automata (QCA)

This study examines one of the most promising FCN paradigms, which is QCA technology. QCA is an emerging nanocomputing paradigm that relies on FCN and has successfully 'put to use' the physics of quantum mechanical tunnelling and electrostatic interactions to execute both combinational and sequential digital logic circuits [12-14], according to the cell layout. Circuits utilising QCA cells demonstrate the capacity to achieve higher speed and lower size compared with conventional microelectronic devices [15]. Moreover, they possess the capacity to operate with significantly reduced power consumption in comparison to current technologies [16, 17]. For computation, QCA uses nanoscale bistable devices [18]. The QCA approach was inspired by advances in quantum dot technology, harnesses inter- and intra-cell dot Coulomb interactions, and expands upon Landauer's insights into limits on digital device implementations and energy dissipation considerations [19].

Heat dissipation is one of the most critical issues in the construction of electronic devices [20]. Conventional computation technologies mainly rely on irreversible operations [21]. For instance, the AND gate transforms two input bits into a single output bit; thus, it loses one bit of information. Rolf Landauer asserted that irreversible computational methods cause information loss as a form of heat dissipation of $k_B T \ln 2$ per bit erased, with $k_B$ being the Boltzmann constant and $T$ being the system temperature [21, 22]. The energy dissipation caused by information losses was considered negligible for many years [23]. The miniaturization of computational devices and the improvement in material quality and fabrication processes have led to the transformation of the energy dissipation levels of modern circuits and systems to values close to the Landauer bound [24]. Thus, new paradigms of computation that can perform logic operations, without losing information are required to continue reducing energy consumption below the Landauer energy limit ($k_B T \ln 2$).

Reversible computing is an emerging computational paradigm, with the main aim to overcome the heat dissipation problem [25]. In reversible operations, the computation circuits utilise reversible logic gates where the numbers of input and output pins are the same. In 1973, Bennett proved that circuit energy dissipation is theoretically eliminated if computational operations are performed without information loss [25]. Therefore, to overcome the limitations of energy dissipation, computation operations must be carried out reversibly [26]. Thus, computer technologies that employ underlying reversible operations could eventually allow for ultraefficient computing. However, reversible computing is an effective low-power technique, only if reversibility is sustained down to the physical level [27]. QCA is a transistor-less nanoscale methodology that can overcome the limitations of current CMOS-based very-large-scale integration (VLSI) technology [11]. QCA is a suitable nanoelectronics approach for performing digital logic operations that are both logically and physically reversible, allowing for the realisation of ultralow-energy dissipation computing [28].

The design phase is critical to the advancement of emerging technologies, as it directly influences their feasibility, performance, and scalability [29]. Also, it directly impacts the performance, efficiency, reliability, and manufacturability of the final product [30]. This study introduces three innovative design methods for building QCA digital computing systems. First, an innovative logically and physically reversible, time-synchronised design technique for ultra-energy-efficient QCA circuits is introduced. Second, a novel partially reversible design approach is proposed to balance chip power consumption, speed, and area. Finally, a hybrid design method is presented to provide more control over circuit characteristics in terms of power consumption, delay time, and area occupied.

These design methodologies can optimise the circuit's features by making trade-offs in terms of speed, area, and power consumption. Thus, the circuit's ultimate goal, determines the most effective design method to use. The novel, logically and physically reversible, time-synchronised design approach can lead to extremely low energy dissipation. The logically and physically reversible design method's core component is an innovative reversible majority gate. This method was used for designing and simulating novel logically and physically reversible, time-synchronised combinational and sequential QCA circuits that dissipate less energy than the Landauer limit of $k_B T \ln 2$ per bit erased

[31, 32] (see Chapters 3 and 4). The logically and physically reversible design method was then used for designing more sophisticated QCA computing circuits, including a 4:1 multiplexer, an 8:1 multiplexer, and an arithmetic logic unit (ALU) [33, 34] (see Chapter 5). If more characteristics need to be considered besides achieving high energy efficiency, then the partially reversible design technique can be used [35] (see Chapter 6). The partially reversible design approach improves the speed, decreases the circuit cost in comparison with the reversible design method, and still optimises energy efficiency compared to the irreversible QCA circuits. The key ingredient of the partially reversible design method is the introduction of a partially reversible majority gate element building block. Customised systems require circuits with specified specs in terms of power, speed, and area. The hybrid design method allows the designer to have more control over the circuit characteristics to meet different system needs [36] (see Chapter 7). The hybrid design method employs a combination of reversible, irreversible, and partially reversible majority gates.

### 1.3. QCA Background

In the 1980s, there were notable improvements in epitaxial growth techniques, particularly in molecular beam epitaxy (MBE) [37]. This enabled the fabrication of gallium arsenide (GaAs) and aluminium gallium arsenide (AlGaAs) semiconductor heterostructures with extremely smooth interfaces [38]. When the atoms in crystalline semiconductors are carefully controlled, a two-dimensional electron gas (2DEG) can form in the lateral plane, perpendicular where AlGaAs and GaAs meet [39]. This 2DEG is very conductive at low temperatures [40]. By placing lithographically defined metal gates on the semiconductor surface, the 2DEG can be further manipulated by defining a further potential acting on the plane of confined electrons [41]. Applying a negative potential to these gates depletes the 2DEG beneath them [42]. In 1988, two research groups measured the conductance through a constriction connecting two 2DEG regions and found that it was quantized [43, 44]. This phenomenon was convincingly explained by the quantum-mechanical behaviour of the electrons passing through the constriction [44]. Solving the Schrödinger equation in two dimensions, using the effective mass approximation, and

applying the Landauer approach for quantum transport as a waveguide like transmission problem, explained much of this layer's behaviour [45].

The ability to manipulate electrons' effective wavefunctions has shown considerable potential for future device applications [46]. There were several proposals for device designs that were based on waves [47, 48]. These designs are frequently compared to microwave devices and use quantum interference phenomena as their main operational mechanism. Compelling experimental demonstrations have verified the genuineness of these quantum mechanical processes and their capacity for device performance [49]. Moreover, it became possible to generate quantum dots by restricting the two-dimensional electron gas (2DEG) in both horizontal dimensions, while the third dimension is already restricted by the heterostructure potential [42]. These quantum dots can be considered synthetic atoms [50, 51], and high-Q resonators for ballistic electron transport [52, 53].

During that period, the phenomenon of Coulomb blockade in tiny structures was only beginning to emerge and show potential [10]. Electrons, when they tunnel onto tiny metal islands, can raise the island's potential by $e^2/C$, where $C$ represents the island's entire capacitance [54]. In microscale structures, the magnitude of this charging energy can be considerable in relation to thermal energy and must be properly considered [55]. The conventional theories of Coulomb blockade explain the island's transport behaviour in terms of macroscopic island capacitance [55]. While this method is appropriate for metal structures that have a sea of free electrons, tiny semiconductors necessitate a many bodies theory approach. This model computes the effective capacitance by considering the influence of Coulomb effects and quantum mechanical principles rather than relying on a classical capacitance [56].

The QCA idea was derived from the classic cellular automata (CA) paradigm [57]. CA systems are mathematical models that simulate the process of evolution, progressing from one generation to the next based on predetermined principles [58]. The adjacent cells of the preceding generation determine the condition of each cell. The inherently suitable coupling between neighbouring nanodevices for ultra-device scale integration, results from the expectation that a single minuscule device will influence its adjacent devices while exerting negligible influence on devices further away [59]. CA systems offer an alternative approach to computing that diverges from the current-switch model of

transistors. CA systems are versatile mathematical models that can function with any given set of evolutionary rules [58]. The investigation into device design encompassed not only the computational behaviour that local CA rules could generate, but also the rules representing actual physics of cellular interaction [60].

Through a series of seminal publications, Lent *et al.* introduced the concept of QCA technology in the early 1990s. In 1992, a research study observed a very nonlinear threshold behaviour for single-electron transfer in two-electron systems subject to bias comprising of two tunnel-coupled quantum wells [61]. A multi-electron Hamiltonian was used, and the Schrödinger equation was directly solved employing the finite element method. The nonlinearity was a direct result of the process of quantizing charge. When high barriers surround a region of space, the average value of the contained charge tends to be a whole number multiple of the basic charge. This work was extended by using a Hubbard model to describe the QCA cell, containing hopping between cell sites and intra- and inter-cell electrostatic interactions [62]. This model avoided the difficulties associated with resolving exchange and correlation effects by using a direct Schrödinger equation solving approach. The simulation results showed that bistability was a fundamental characteristic of QCA. While the idea of exploring a multi-state QCA cell and multi-state logic may seem attractive, it is important to note that only a bistable system may fully achieve saturation in both logic stages. An intermediate state is inherently susceptible to transitioning between stages.

Lent *et al.* (1993) employed the cell charge configuration of the QCA paradigm to encode binary information [19]. A series of QCA cells functioned as a binary wire, and the convergence of two or three wires could establish a majority logic gate with majority voting behaviour [18]. A specialised cell arrangement at the junction, by fixing the internal biassing to either state 1 or 0, for one of the input cells functions as an ‘OR’ or ‘AND’ gate [19]. Cellular interactions between cells placed along diagonal axes create logic inverters [63]. Thus, any logical or arithmetical function using these fundamental components can be constructed. The specified cell layout and utilising the cell-cell electrostatic interactions determine the logic operations, and many researchers have adopted QCA as a prospective computing paradigm [18, 64, 65]. QCA is a FCN technology where information is encoded in the form of the polarisation of each cell [11].

The coulombic electrostatic force subsequently propagates the information to neighbouring cells. This leads to low energy dissipation because there is no current flow but rather electrons tunnelling between sites in a QCA cell [11].

Lent *et al.* (1994) demonstrated how small metal islands, when connected by tunnel junctions, can function as dots and create QCA cells [66]. An important benefit of metal-dot structures is their ability to direct electric field lines from one dot to affect adjacent dots, whereas with semiconductor depletion dots, the field disperses in all directions. Within a molecular electronics viewpoint, molecular versions of QCA can be envisioned, in which a portion of the molecule can localise charge and serve as the equivalent of a quantum dot [67]. A QCA demonstration magnetic model was constructed utilising three-inch magnets embedded in Lucite blocks capable of rotating on low-friction jewelled pivots [19]. These magnetic cells were employed to illustrate QCA wires and gates.

Thus, we find that the QCA philosophy revolves around four fundamental principles. First, the ability to position quantum dots to contain charge. Second, Landauer's compelling argument that any functional device must demonstrate bistable saturation in its information transfer function. Third, charge quantization is responsible for the inherent nonlinearity of charge tunnelling between these dots. Fourth, there is the instantiation of locally connected architecture resembling cellular automata through the Coulombic interaction between charges, with an inverse square force decay.

Many researchers have addressed the QCA paradigm as a promising future computer technology because of the specific circuit structure and electrostatic interactions among neighbouring cells that allow logic functions to be executed [68-70].

### 1.4. QCA Circuit Architecture

QCA cells are the key elements in QCA technology [19]. A typical QCA cell consists of four quantum dots, arranged at the four corners of a square. Each cell has a pair of electrons that can undergo quantum tunnelling between the four quantum dots. Due to their electrostatic interactions, the two electrons tend to be located on opposite diagonals in a square, representing two binary configurations. The dots within a QCA cell are sequentially numbered in a clockwise manner, starting from the dot positioned at the top

right corner. Thus, the polarisation $P$ within a cell can be measured as the extent of electrical charge dispersion among the four dots:

$$P = \frac{(\rho_1 + \rho_3) - (\rho_2 + \rho_4)}{\rho_1 + \rho_2 + \rho_3 + \rho_4} \tag{1.1}$$

where $\rho_i$ denotes the electronic charge in each dot of a four-dot QCA cell at site $i$. Because coulombic repulsion is present, the two possible polarisation states of QCA cells saturate at P = -1 and P = +1, which correspond to the binary digits 0 and 1, respectively (see Figure 1.1).

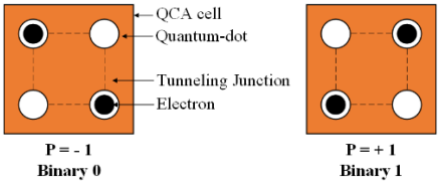



**Figure 1.1 QCA cell polarization.**

Electrostatic forces interact between adjacent cells, inducing a quadrupole moment in neighbouring cells due to the nonuniform distribution of cell charge. These perturbative fields create a dependence of each cell's state on the polarization of other cells. Figure 1.2 illustrates the highly nonlinear intercellular interaction function. This cell–cell response function is essential to QCA operation as a universal computer and provides a noise margin and signal restoration along lengthy arrays.

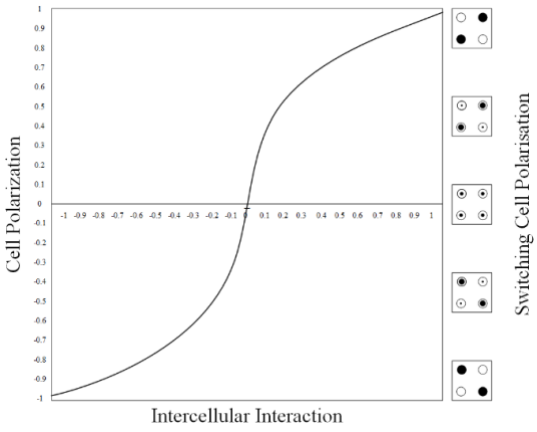



**Figure 1.2 Nonlinear intercellular interaction function [71].**

Under optimal conditions, where the system doesn't get stuck in a metastable state, the system's 'direction of travel' is an inclination towards the lowest energy state that

encompasses computation. QCA computing is commonly known as ground-state computation. The electrostatic interaction between electrons in neighbouring cells tends to align their polarisation. This feature enables the transmission of information across a cellular wire. Typically, the process of designing QCA circuits entails the use of three elementary building blocks, which compromise arrays of QCA cells:

- QCA binary wire.
- QCA inverter.
- QCA majority gate voter (MV).

A useful QCA computer circuit consists of wiring up QCA inverters and majority gates to provide the overall digital circuit's required logic truth table.

### 1.4.1. QCA Binary Wire

The intrinsic bistability of each QCA cell, combined with the Coulomb interaction between cells, guarantees that a linear array of cells will align with the same polarization. The linear array's alignment enables it to function as a binary wire, allowing for the transmission of information from the driven end to the free end. The QCA wire worked well across the whole parameter space of the model Hamiltonian as long as the energy of the Coulomb interaction dominates over the kinetic energy [19]. The bistability of individual cells inside the wire can provide resistance to changes in shape and other oscillations in cell parameters [19]. In order to prevent signal degradation, a binary wire is commonly partitioned into many clock zones, as signals have a tendency to deteriorate due to thermal smearing effects, when there is a lengthy sequence of cells in the same clocking zone [72].

Figure 1.3 displays an example of a QCA wire layout. The driver cell is on the left-hand side, which can maintain a fixed polarisation of either -1, which equals binary 0, or +1, which equals binary 1. The other cells in the array are free to react to this polarization. The output cell is located on the right-hand side.

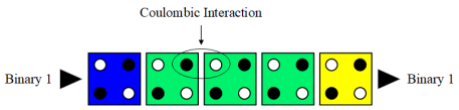



**Figure 1.3 QCA wire layout (The blue colour indicates the input cell, the yellow colour indicates the output cell, and the green colour indicates the internal cells).**

### 1.4.2. QCA Inverter

The inverter is another critical component in the construction of QCA digital circuits. Two distinct configurations for QCA inverters are described in the literature: the single-branch inverter shown in Figure 1.4a, and the double-branch inverter depicted in Figure 1.4b. The single-branch layout is based on a single diagonal Coulombic interaction. In the single-branch inverter, the symmetric diagonal contact with neutral molecules enables the inversion process [73]. On the other hand, the double-branch interaction aims to enhance the symmetry of the inverter layout, thereby promoting the stability of the inversion operation to manufacturing flaws [73]. The double-branch structure typically encourages information inversion. However, the crosstalk effect hinders the ability to conduct inversion using the double-branch inverter. Thus, the choice between single-branch and double-branch inverters depends on numerous factors, such as size constraints, the desired computational speed, sensitivity to noise, stability needs, the complexity of the overall system, and the technology used [73].


(a) (b)

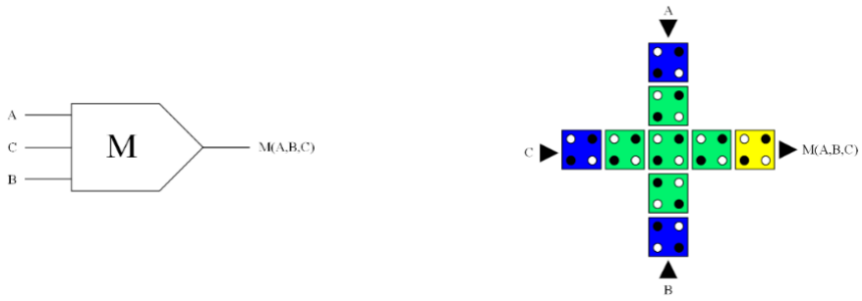
**Figure 1.4 (a) Single-branch inverter and (b) double-branch inverter (The blue colour indicates the input cell, the yellow colour indicates the output cell, and the green colour indicates the internal cells).**

### 1.4.3. QCA Majority Gate

The cell arrangement enables the QCA technology to form logic gates. The majority gate is the fundamental logic gate used in QCA circuits. The conventional QCA majority gate consists of three inputs and one output. It determines the majority value among its three inputs, i.e., it exhibits majority voting behaviour. It is mathematically represented in Equation 1.2.

$$M(A,B,C) = AB + AC + BC \tag{1.2}$$

Figure 1.5 presents the conventional QCA majority. The symbol of the conventional three-input QCA majority gate is presented in Figure 1.5a, whereas Figure 1.5b displays the QCA layout.



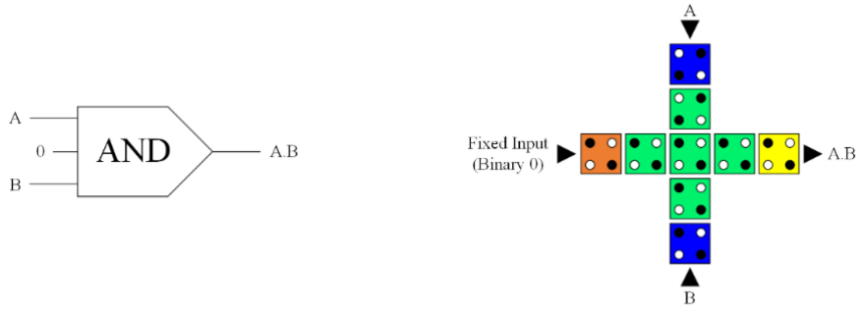

(a) (b)

**Figure 1.5 (a) The symbol of the conventional three-input majority gate and (b) the physical QCA layout of the conventional QCA three-input majority gate (the blue colour denotes the input cells, the yellow colour denotes the output cell, and the green colour denotes).**

The majority gate is programmed to produce an 'AND' gate or an 'OR' gate by setting a binary value of '0' or '1' to one of its inputs. Thus, fixing input C in Equation 1.2 to the value of '0', can produce an 'AND' gate with the Boolean expression given in Equation 1.3.

$$M(A, B, 0) = A.B \tag{1.3}$$

Figure 1.6 presents the produced QCA 'AND' gate. The symbol of the produced QCA 'AND' gate is presented in Figure 1.6a, whereas Figure 1.6b displays the QCA layout.



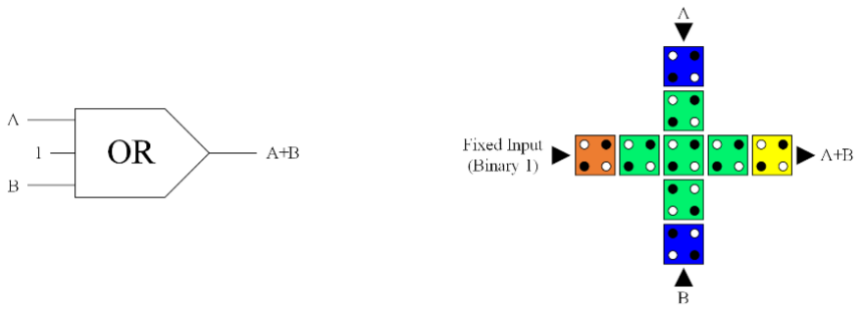

(a) (b)

**Figure 1.6 (a) The symbol of the produced AND gate and (b) the physical layout of the produced AND gate (the blue colour denotes the input cells, the yellow colour denotes the output cell, the green colour denotes the internal cells, and the orange cell with two electrons in upper left and bottom right denotes the cell with a fixed value of '0').**

On the other hand, fixing input C in Equation 1.2 to the value of '1', results in the generation of an ‘OR’ gate with the Boolean expression given in Equation 1.4.

$$M(A, B, 1) = A + B \tag{1.4}$$

Figure 1.7a presents the symbol of the produced QCA ‘OR’ gate, while Figure 1.7b shows its QCA layout.




(a) (b)

**Figure 1.7 (a) The symbol of the produced OR gate and (b) the physical layout of the produced OR gate (the blue colour denotes the input cells, the yellow colour denotes the output cell, the green colour denotes the internal cells, and the orange cell with two electrons in the upper left and bottom right denotes the cell with a fixed value of ‘1’).**

The inclusion of QCA wires, QCA majority gates, and QCA inverters is crucial in QCA circuit design because their combination allows for the implementation of all possible Boolean functions, i.e., they form a full set of universal logic gates. The ability to construct complex logic functions using combinations of majority gates, inverters, and wires makes QCA a promising technology for future computing architectures, particularly in areas where minimising power consumption and maximising speed are critical.

### 1.5. QCA Clocking Algorithms

To ensure proper data transfer and operation in VLSI logic circuits, clocking control plays a vital role in coordinating data flow [74]. Unlike circuits based on field-effect transistors (FETs), QCA circuits do not have a predetermined direction for the flow of current or electrons; instead, information can propagate in multiple directions [19]. Therefore, clocking is crucial for synchronizing and directing the flow of information in a specific direction. To alter the tunnelling barrier strength between the QCA cells and

achieve clocking control, QCA requires an external clock [75]. Researchers have proposed various timing and clocking methods to regulate information transmission via QCA circuits.

In 1997, Lent and Tougaw devised adiabatic switching as a way to control the timing, deal with metastability problems, and facilitate pipeline creation for QCA circuits [76]. This clocking method divides the QCA array into clusters of cells known as clock zones, providing the advantages of multiphase clocking and pipelining. A clock zone structure facilitates the execution of a computation by a set of QCA cells, allowing them to stabilise their states and subsequently transmit the results to the next clock zone as inputs. Allowing the QCA wire length to grow can increase the risk that cells will not switch accurately due to thermodynamic constraints. Therefore, dividing the wire into zones is analogous to breaking it into several smaller wires [77].

The adiabatic switching clocking scheme is implemented through underlying circuitry that generates an electric field to modulate the tunnelling barriers between quantum dots in QCA cells. This clocking system uses buried conducting metal wires to produce signals that achieve four clock phases, with each phase shifted by 90-degrees. The four 90-degree-shifted clock phases consistently adhere to a pattern of four states: switch, hold, release, and relax. Figure 1.8 depicts these four phases of the adiabatic pipelining cycle in simplified form. Each outlined box represents a multicellular clock phase. Each cell in a clock phase uses the same gate to control inter-dot barriers. In each box, the cell on the left depicts the state of the cells at the commencement of this clock phase, while the cell on the right depicts the state of the cells at the end of this clock phase. The single cells depicted can represent a subarray of QCA cells.

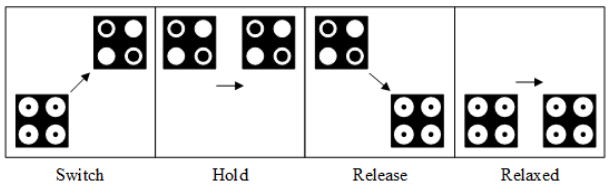



**Figure 1.8 Adiabatic pipelining phases.**

The QCA chip is divided into four clock zones, labelled Clock 0, Clock 1, Clock 2, and Clock 3, which are colour coded in the QCA-Designer tool, as shown in Figure 1.9. A unique clock signal controls each zone, directing the cells to perform specific

computations. Data can only flow between QCA cells managed by consecutively numbered clocks, such as from Clock 0 to Clock 1, Clock 1 to Clock 2, Clock 2 to Clock 3, and Clock 3 back to Clock 0.

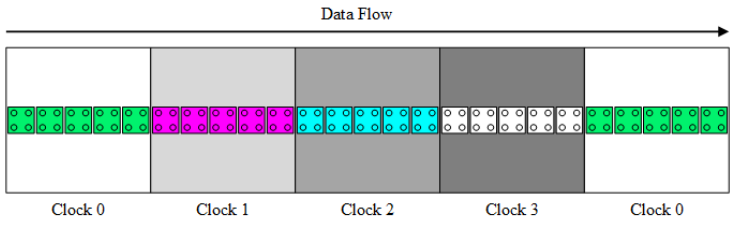



**Figure 1.9 QCA data flow.**

The four clocking zones correspond to the four clock signals, forming a complete QCA clock cycle. Figure 1.10 shows the clocking phase barrier height when switching between the different clock zones. At the beginning of the first phase, referred to as the switch phase, the cells are unpolarized and have low barriers. However, as this phase progresses and computation is performed, the barriers increase, and the cells become polarised to correspond with the computation function. This phase ends with substantial barriers that prohibit tunnelling and fixed cell states. The second phase is termed the hold phase, where the barriers remain at their current height. The third phase is the release phase, where the barriers are lowered and the cells become depolarized. The relax phase is the fourth and final phase of the clock. This phase maintains the unpolarized nature of the cells by keeping cell barriers low. After the fourth phase, the clock system repolarizes and reverts to the first phase, beginning a new cycle.

In the adiabatic switching method, the input states are switched gradually, while the interdot barriers of the cells are changed, at the same time, across the whole array. This keeps the system in an instantaneous ground state. In addition, the synchronisation of data can prevent a signal from reaching and propagating through a logic gate before any further inputs are received. Having these features guarantees that QCA circuits will function properly. However, the implementation of this one-dimensional adiabatic switching scheme faces several obstacles. These obstacles include the difference in the lengths of the wires, in the clock zone capacities, and in the number of cells between the different clock zones, which may preclude the construction of feedback paths and produce an unused area [78].

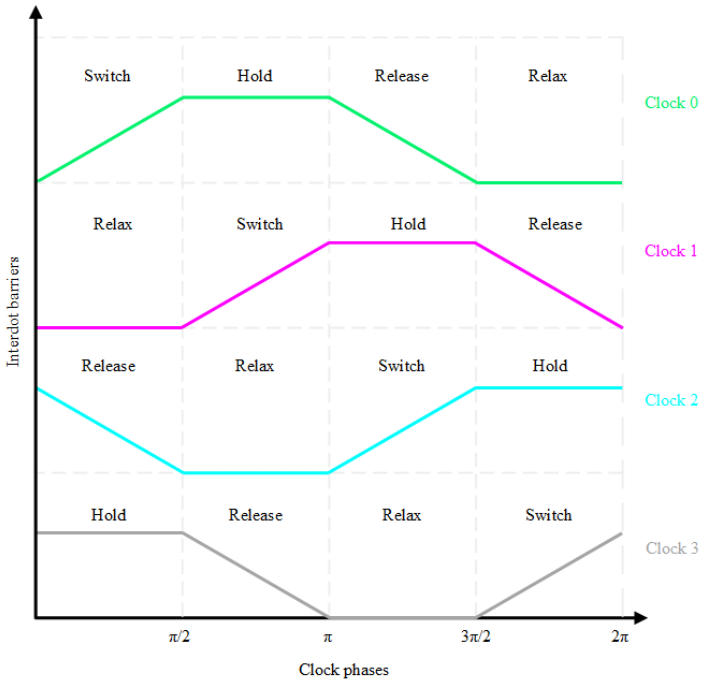



**Figure 1.10 QCA clocking phases in different clock zones.**

Vankamamidi *et al.* (2007) proposed a two-dimensional QCA timing method [79]. The two-dimensional QCA clocking method can achieve higher performance and lower power consumption than the one-dimensional QCA clocking method by exploiting the spatial and temporal parallelism of QCA circuits. This clocking scheme takes zone size into account and comprises a grid of square zones that are equal in size, thus preventing thermodynamic effects on QCA circuits. The overhead of feedback channels, however, remains a major challenge [78]. In advanced QCA circuits, long lines between timing zones have a negative effect, leading to higher delays and sensitivity to thermal fluctuations [78].

Campos *et al.* (2016) developed the unified, scalable, and efficient (USE) timing method [78]. The adaptability of the USE timing method enables it to satisfy the requirements of QCA circuits, which include the implementation of feedback channels with small or large loops, the standardisation of cell libraries, and the facilitation of routing simplicity. Figure 1.11 shows the USE clocking system, which consists of four time zones numbered from 1 to 4. These four time zones constitute one complete clock cycle. Data flows between the QCA cells in neighbouring clock zones, shown here as squares. Each square contains a cluster of five-by-five QCA cells representing a distinct time zone.

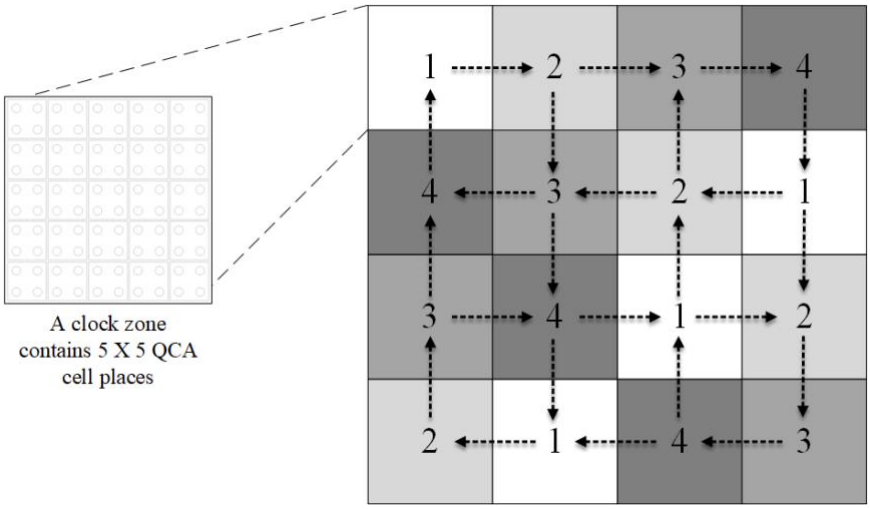



**Figure 1.11 The USE timing mechanism (the squares are used to represent time zones and the arrows are used to represent data flow).**

To balance the speed of data transmission and the arrival time of data, for each logic gate in the circuit, clock synchronization is essential [80]. The differentiation between local and global synchronization must be carefully considered when evaluating QCA circuits. Local synchronization necessitates that data transmission be restricted only between cells in clock zones with consecutive numbers. Global synchronization ensures that new data is transmitted to the inputs of the circuit during every clock cycle; thus, the inputs of all gates are synchronized for at least one clock cycle prior to the arrival of new data. Most researchers emphasize that local synchronization is a crucial requirement to include when developing QCA circuits [80-83]. However, the conclusion for global synchronization research is contradictory. In spite of numerous assertions highlighting the importance of global synchronization [81, 82], some studies argue that global synchronization is not a necessary requirement for QCA circuits [83].

Clocking is vital for the design of QCA circuits as it facilitate the physical implementation of QCA circuits. Either the pipeline-style [79] or the dynamic-style [78, 83] can be used to include the real clocking concept into the QCA clocking system. For complex circuits based on five-input majority gates, the real clocking strategy, with efficient clustering and placement, has been recently developed [84]. Generally, QCA circuits utilizing majority gates with more than three inputs benefit significantly from the real clocking technique [84].

## 1.6. QCA Wire Crossing Methods

One of the most frequently encountered issues in systematic VLSI design practice is wire crossings [85]. Dealing with wire junctions is one of the greatest challenges in the development of QCA digital logic circuits [86]. Wire crossing in QCA is critical for designing complex circuits where multiple data paths intersect. Unlike traditional electronic circuits, where wires can simply overlap, QCA requires careful management of electron positions and interactions to avoid interference and ensure reliable data transmission [71]. In QCA circuits, there are currently two wire crossing techniques available:

- Coplanar wire crossing [87].
- Multilayer wire crossing [72].

### 1.6.1. Coplanar Wire Crossing

Applying a 45-degree rotation to a QCA cell can result in a rotated QCA cell that possesses the same features as the standard QCA cell [67]. The rotated cell aligns its dots both vertically and horizontally. Thus, the cell can be in one of two distinct forms that can represent the binary logic values 0 and 1. Figure 1.12 shows a schematic representation of these two rotated QCA forms.

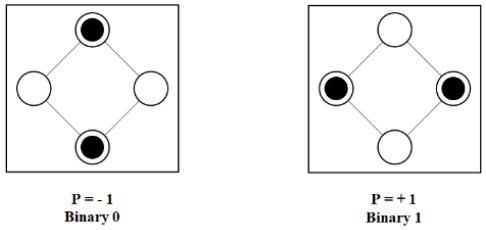



**Figure 1.12 A 45-degree rotated QCA cell.**

QCA circuits that rely on a 4-phase clocking system often use the coplanar crossover technique for transmitting signals across wire junctions. The coplanar approach relies on 45-degree rotated QCA cells. Under certain circumstances, the coplanar crossover can transfer signals across a single planar layer using specific symmetries between rotated and unrotated cells. Proper construction of these cells demonstrates that they will not interfere

when placed adjacent to each other, as shown in Figure 1.13. The lengths of the rotated wire and the unrotated wire are precisely equal, hence enabling identical coulombic interactions among electrons within each cell. As a result, when the wires cross, the signals on each wire remain unchanged [67].

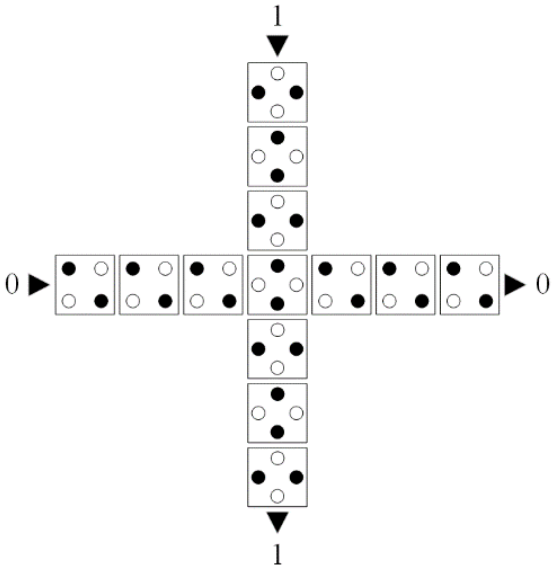



**Figure 1.13 Coplanar crossover method.**

However, fabricating cells with two different orientations presents challenges, and the weak coupling in the cells increases the likelihood of interference or crosstalk [88]. Because of their weak coupling, the cells are susceptible to many physical and environmental factors, such as temperature [89]. Ottavi *et al.* (2006) introduced a new architectural design to address the challenges associated with weak coupling, particularly temperature issues, by developing a more thermally resilient architecture [89]. They devised three designs based on the cell orientation, majority gate voting, and cell interaction. Although these suggested methods addressed certain design problems, they incurred additional costs [87]. Rajeswari *et al.* (2010) attempted to reduce the additional space required by complicated design processes and produced the first clocking-based wire crossings using only one kind of cell [87]. Despite achieving success in executing their recommended methods, there were limited limits in terms of timing. They suggested using a personalised clocking system with eight zones, resulting in a decrease in processing performance.

### 1.6.2. Multilayer Wire Crossing

The multilayer method is another solution for crossing wires. This approach employs a tripartite structure to address the problem of wire junctions by separating crossed wires vertically. A vertical connection and hierarchical cell stacking could transmit the signal to the next layer and then direct it horizontally, thereby preventing crosstalk and interference [90]. The two crossing wires use clocking techniques, resulting in identical delay times for both wire outputs [91]. Figure 1.14 illustrates the multilayer crossover style. The top and bottom layers represent the intersecting wires, while the middle layer serves as an intermediary layer to prevent any potential interference between the two interconnections. The coulombic interaction between stacked cells forces the cells in between to tend to the opposite polarisation of the layers above and below.

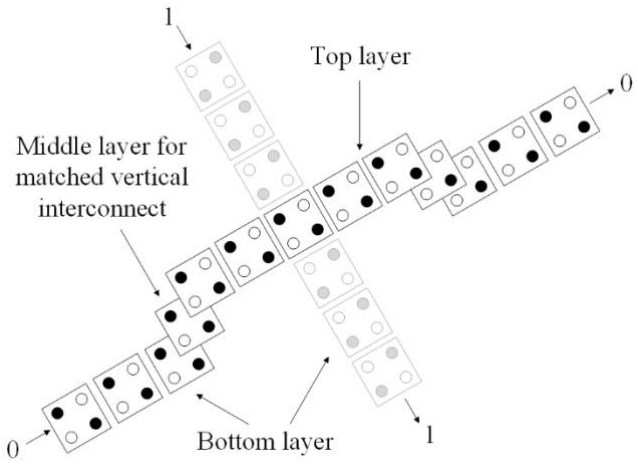



**Figure 1.14 multilayer crossover method.**

The additional layers of QCA multilayer circuits function identically to the underlying base layer. This approach is distinct from conventional CMOS integrated circuits, which use multi-metal layers to interconnect circuit components that are not running together but incapable of performing logical processes. The QCA cells in the additional layers are subject to the same Coulombic interactions as those in the base layer [92]. Hence, additional layers possess the capability to include computational circuit components rather than only wires. Compared to the coplanar circuit, the multilayer crossover method has the potential to significantly reduce the space demands of multilayer QCA circuits [90].

Nevertheless, producing multiple layers with precise alignment and reliable interconnections is technologically challenging and requires sophisticated equipment [90]. The heightened intricacy and exacting specifications augment the expense of fabrication. In addition, managing heat dissipation in multilayer systems can be challenging, as multiple active layers have the potential to dissipate additional amounts of heat [91].

Although most QCA designs use the coplanar method, which is traditionally considered advantageous in the QCA paradigm, research has shown that the coplanar crossover experiences rapid performance deterioration due to significant crosstalk between the two interconnects [92]. The multilayer crossover method, on the other hand, has a higher displacement tolerance than the coplanar crossover. Thus, it can provide more robust QCA circuits with reliable data transmission [92].

### 1.7. Energy Dissipation Analysis of QCA Cells

A QCA cell starts each clock cycle in a depolarized state [93]. Energy needs to be supplied by the clock to reach a polarised state [94]. Most of this energy goes back to the clock and other cells when the cell depolarizes again at the end of the clock cycle [94]. However, some energy is dissipated into the environment [94]. To study the energy loss of QCA cells in detail, a microscopic quantum mechanical model of QCA cell behaviour needs to be applied [95-97].

Presently, there exist two technology computer-aided design (TCAD) tools, namely *QCAPro* [95] and *QCADesigner-E* [96], that enable the modelling of energy dissipation in QCA circuits. The *QCAPro* simulation tool, developed in 2009, cannot provide precise estimates, due to the assumption of a perfect clock slope. Consequently, it permits only the determination of an upper limit for energy dissipation. On the other hand, *QCADesigner-E* can compute the actual energy dissipation values. It calculates the energy transmission to and from the clock ($E_{clk}$), the neighbouring cells ($E_{IO}$), and the environment ($E_{env}$) by calculating the corresponding integral equations for these quantities. The *QCADesigner-E* TCAD tool is an enhancement of the well-known QCA TCAD package, *QCADesigner* [71].

*QCADesigner-E* incorporates a coherence vector simulation engine (CVSE). The CVSE utilises an advanced quantum mechanical density matrix-based treatment, as

described in the literature [93, 95, 96], to simulate the behaviour of QCA cells, including energy dissipation. It uses a computational method in which a transient analysis is performed for the quantum mechanical density matrix-based microscopic description of the intracell dynamics, while the cell–cell electrostatic interactions are incorporated within the Hartree approximation [71]. During each iteration, the CVSE calculates updated values for the coherence vector components, given the time-dependent tunnelling energy determined by the clock. The coherence vector formalism uses the Pauli spin matrices to form the basis for the coherence vector. By solving the matrix differential equations that reflect the evolution of the quantum mechanical density matrix, the coherence vector is determined. This is accomplished using an iterative fixed-timestep technique [96]. To minimise simulation errors and obtain accurate outcomes, the timestep ($T_{step}$) must be sufficiently small.

Going into further detail, the microscopic quantum mechanical model represents the state of a QCA cell using two three-dimensional vectors: the coherence vector and the energy vector. The coherence vector $\vec{\lambda} = (\lambda_x, \lambda_y, \lambda_z)$ represents the current state of the cell, where parameter $\lambda_z$ corresponds to the negative of its polarisation [96]. The energy vector $\vec{\Gamma} = \frac{1}{\hbar}[-2\gamma, 0, \phi]$, where $\hbar$ is the reduced Planck constant, describes the steady-state of the cell, which indicates how the cell will behave in the future based on its current tunnelling behaviour ($\gamma$) and the Coulomb force exerted by neighbouring cells (given by $\phi$ when expressed as a potential energy).

The kink energy between two cells *i* and *j* measures the energy cost of those cells having opposite polarisations. The polarisation of a cell is determined by the positions of the two excess electrons in the four quantum dots that form the cell [19]. The polarisation of a cell can be influenced by the polarisation of its neighbouring cells through Coulomb interactions, as follows:

$$\phi = \sum_{j \in N(i)} E_{kink}^{i,j} P_j \tag{1.5}$$

To calculate the current energy E of a QCA cell, the formula $E = T_r(\hat{H}.\hat{\rho})$ is used, where $T_r$ is the trace operator, $\hat{H}$ is the Hamiltonian of the cell, and $\hat{\rho}$ is the density matrix of the cell. The Hamiltonian contains terms representing the Coulomb interaction between

electrons in the current cell and its nearest neighbours and the tunnelling between the quantum dots within the cell. The density matrix $\hat{\rho}$ represents the statistical state of the cell, such as the probability of finding an electron in a certain quantum dot. By taking the expectation value of $\hat{H}$ with respect to $\hat{\rho}$, we can obtain the average energy of the cell at any given time. By exploiting the linearity of the $T_r$ operator and using $\hat{H} = -\gamma\sigma_x + \phi\sigma_z$, we can calculate the energy dissipation of a QCA cell as a function of time:

$$E(t) = \frac{\hbar}{2}\vec{\Gamma}(t) \cdot \vec{\lambda}(t) \tag{1.6}$$

where the function $E(t)$ denotes the current energy of the cell at time $t$ and is essentially given by the scalar product of the two energy vectors at that point in time.

To calculate the instantaneous power P of a QCA cell, the following expression can be used:

$$P = \frac{d}{dt}E(t) = \frac{d}{dt}\left(\frac{\hbar}{2}\vec{\Gamma}(t) \cdot \vec{\lambda}(t)\right) \tag{1.7}$$

Consequently, the total energy dissipation $E_{total}$ of a QCA cell during a complete clock cycle, with period $T_{clk}$ is given as the integral of $E(t)$ over one cycle:

$$E_{total} = \int_{t_0}^{t_0+T_{clk}} P dt' = \frac{\hbar}{2}\int_{t_0}^{t_0+T_{clk}} \left(\frac{d}{dt}\vec{\Gamma} \cdot \vec{\lambda} + \frac{d}{dt}\vec{\lambda} \cdot \vec{\Gamma}\right) dt' \tag{1.8}$$

The integrand of Equation 1.7 is the scalar product of the derivative of the energy vector $\vec{\Gamma}$ and the coherence vector $\vec{\lambda}$ of the cell. This expression describes the amounts of energy transmitted within the clock $E_{clk}$ and the neighbouring cells $E_{IO}$ during a clock cycle [93, 95, 96], which can be calculated as follows:

$$E_{clk} + E_{IO} = \frac{\hbar}{2}\int_{t_0}^{t_0+T_{clk}} \left(\frac{d}{dt}\vec{\Gamma} \cdot \vec{\lambda}\right) dt' \tag{1.9}$$

$$\mathrm{E}_{clk} = \frac{1}{2}\int_{\mathrm{t_0}}^{\mathrm{t_0+T_{clk}}} \left(\frac{\mathrm{d}}{\mathrm{dt}}(-2\gamma)\cdot\lambda_{\mathrm{x}}\right) dt' \tag{1.10}$$

$$\mathrm{E}_{IO} = \frac{1}{2}\int_{\mathrm{t_0}}^{\mathrm{t_0+T_{clk}}} \left(\frac{\mathrm{d}}{\mathrm{dt}}\phi\cdot\lambda_{\mathrm{z}}\right) dt' \tag{1.11}$$

Moreover, it captures the energy transferred to the environment $\mathrm{E}_{env}$ within a clock cycle [93, 95, 96]. $\mathrm{E}_{env}$ represent the energy dissipated by a QCA cell during a clock cycle and can be calculated as follows:

$$\mathrm{E}_{env} = \frac{\hbar}{2}\int_{\mathrm{t_0}}^{\mathrm{t_0+T_{clk}}} \left(\frac{\mathrm{d}}{\mathrm{dt}}\vec{\lambda}\cdot\vec{\Gamma}\right) dt' = -\frac{\hbar}{2\tau}\int_{\mathrm{t_0}}^{\mathrm{t_0+T_{clk}}} \left[\left(\vec{\Gamma}\cdot\vec{\lambda} + \left|\vec{\Gamma}\right|\tanh\eta_{th}\right)\right] dt' \tag{1.12}$$

where $\tau$ is a technology-dependent relaxation time parameter and $\eta_{th}$ denotes the thermal ratio and can be calculated as follows:

$$\eta_{th} = \hbar\left|\vec{\Gamma}\right|.(2k_B T)^{-1} \tag{1.13}$$

As indicated in [93, 98], the system relaxes towards the thermal steady-state, and to ensure the precision of the calculations, energy conservation must hold numerically, meaning that the total energy must be zero, i.e.,

$$\mathrm{E}_{total} = \mathrm{E}_{env} + \mathrm{E}_{clk} + \mathrm{E}_{IO} = 0 \tag{1.14}$$

### 1.8. QCA Circuits Cost Calculation

The delay, number of logic gates, and number of crossovers are essential metrics to measure the performance, complexity, power dissipation, and fabrication difficulties of QCA circuits [71]. The delay is used to measure the speed of QCA circuits; the number of employed majority gates is associated with irreversible power dissipation, whereas the number of crossovers correlates with fabrication complexity. To compare and evaluate QCA circuits, a cost function may be derived as a figure-of-merit (FOM) [99, 100]. Two cost functions have been presented previously in the literature. The first one evaluates

designs based on three-input majority gates [99], and the other on five-input majority gates [15]. The design methods proposed in this study employ three-input majority gates. Accordingly, the first cost function [99] has been utilised to evaluate the cost of the designed circuits. This cost function is defined by Equation 1.15.

$$\text{Cost}_{QCA} = (M^k + I + C^l) \times T^p, \qquad k, l, p \geq 1 \tag{1.15}$$

where *M* is the number of three-input majority gates, *I* is the number of inverters, *C* is the number of crossovers, *T* is the delay time of the circuit in terms of numbers of clock phases, and *k*, *l*, *p* are the exponential weightings for majority gate count, crossover count and delay time, respectively. The number of inverters is always given a weight of 1, as their presence has a limited impact on the complexity of QCA circuits.

According to the weighting *k*, *l*, and *p* values, the cost function prioritizes various metrics. For example, if speed is a primary concern, more weight can be given to the delay metric, i.e., a higher value of *p*. If fabrication cost is more important, the value of *l* should be higher than that of *p* and *k* and so on. Therefore, the weight values can be adjusted depending on the overall design optimization goal [99]. However, in the most general cases, a double weighting is given to the number of majority gates M (i.e., $k = 2$) and the number of crossovers *C* (i.e., $l = 2$) [99]. Therefore, in the most general case, the following cost function can be applied:

$$\text{Cost}_{QCA} = (M^2 + I + C^2) \times T \tag{1.16}$$

### 1.9. Experimental Implementations for QCA

Experimental implementations are essential for advancing QCA technology from theoretical speculations to practical applications. Experimental implementations can validate theoretical concepts, drive advancements in fabrication techniques, demonstrate practical applications, address technical challenges, guide future research, and pave the way for industry adoption. These experiments are essential for realising the full potential of QCA technology in creating more efficient, powerful, and scalable computing systems. The implementation of the QCA paradigm has been proposed utilising many technologies, such as solid-state metallic island dots, magnetic implementations, and molecular

electronic methods [101-106], with a particularly promising approach with atomic silicon quantum dots based on a silicon dangling bond on a hydrogen-terminated silicon surface [107].

### 1.9.1. Solid State Dots

Orlov *et al.* (1997) demonstrated, for the first time, an experimental implementation of a QCA cell using metal-island dots [101, 108]. This experimental work proposes a QCA cell using aluminium islands with aluminium oxide tunnel junctions, fabricated on an oxidised silicon wafer. Tunnel junctions and capacitors interconnected four metallic dots to form the QCA device under examination. The manufacturing process included standard electron-beam lithography (EBL) and shadow evaporation deposition techniques for developing the islands and tunnel connections. The experimental results demonstrated the transfer of a single electron from input dots to output dots, controlled by the switching of a single electron. This showcased a nonlinear and bistable response. However, the metal-island structures necessitated operation in cryogenic conditions at extremely low temperatures, less than 50 mK [101], and encountered challenges in achieving accurate electron placement and control [109].

### 1.9.2. Nanomagnetic Logic (NML)

Later, studies have presented experimental implementations of QCA circuits using NML [104, 106]. Varga *et al.* (2013) demonstrated an experimental implementation of a nanomagnet full-adder circuit using slanted-edge magnets [104]. The researchers developed stand-alone NML majority gates and wires and integrated these elements into a NML full-adder circuit that operates properly for all input combinations. The fabrication processes involved ferromagnetic materials and utilised EBL to pattern the nanomagnets, followed by deposition and etching, to achieve the required shapes and configurations. Furthermore, they employed the techniques magneto-optical Kerr effect (MOKE) microscopy and magnetic force microscopy (MFM) to observe and measure the magnetic states of the nanomagnets. The results demonstrated full-adder functionality, where the magnetic states of the output magnets correctly represent the sum and carry-out for all possible combinations of inputs ($A$, $B$, and $C_{in}$). They also measured the time required for

the nanomagnets to switch states, which indicates the operational speed of the full-adder circuit. They also examined the energy required to trigger state transitions in the nanomagnets, underscoring the low-power characteristics of NML.

However, NML faces some challenges, such as the need for precise manipulation of the shape, size, and positioning of nanomagnets, to ensure their reliable functionality. Another challenge is ensuring that the magnetic states remain stable at higher temperatures used during operation. Additionally, the process entails integrating the nanomagnetic full-adder circuit with other logic components in order to construct larger and more intricate circuits. Thus, further investigation and advancement in this field have the potential to completely transform energy-efficient computing and enhance the functionalities of nanoscale devices [106].

### 1.9.3. Molecular FCN

Another promising technology for implementing QCA circuits is the Molecular FCN, which exploits molecules to create very small and dense logic devices [73, 110]. Theoretical studies have extensively investigated the current cutting-edge molecular FCN to examine the potential for encoding information in molecules [111]. At the same time, the generic QCA paradigm is utilised to create arithmetic circuits that have the potential to be built at the molecular level [67, 112].

The literature has proposed several species of molecules, including neutral [113], oxidised [105], and zwitterionic [114]. The *neutral molecule* exhibits the lowest crosstalk effect and streamlines the inversion process, which may be achieved with a single-branch interaction. Nevertheless, the neutral molecule lacks net positive charges on the logical dots. As a result, changing the switching characteristics is necessary to reconfigure the neutral molecule. The *oxidised molecule* has an associated external electric field that has the capacity to displace the entire positive charge, hence enhancing the clocking functionality. However, the molecules that have undergone oxidation, exhibit the most severe interference, making it challenging to create even basic circuits. Additionally, the oxidised molecular cell exhibits a strong repulsive force, rendering the inversion process impossible with a single-branch interaction. The *zwitterionic molecule* exhibits an intermediary behaviour that lies between that of neutral molecules and oxidised

molecules. The presence of a positive net charge on the logic dots allows for the molecular cell to be reset by adding a negative clock field, while the molecule's neutrality helps to minimise crosstalk. It is crucial to observe that the location of the counterion has a significant impact on the behaviour of the device. When the counterion is in close proximity to the logical dots, the zwitterionic molecule mimics the behaviour of a neutral molecule. However, when the counterion is far away, it exhibits similarities to oxidised molecules.

Molecular FCN employs molecules to fabricate QCA cells; the locations of electrons within a molecule represent binary states. Molecular FCN used chemical synthesis processes to create these molecular structures [105, 110]. Molecular FCN stores information in the polarisation of molecules and sends it from molecule to molecule using electrostatic interaction. There is no charge transport involved in the information transfer, which greatly reduces the power dissipation [93]. Moreover, molecular FCN is anticipated to offer QCA circuits with extremely high frequencies and high device density [115, 116]. The implementation of molecular QCA cells demonstrates the possibility of operating at room temperature [110]. Nevertheless, the stability and control of molecular QCA devices, along with the meticulous arrangement of molecules, pose substantial challenges.

The molecular FCN fabrication process requires exceptionally high resolution, necessitating tremendous technical improvement. Currently, researchers are using a predominantly computer simulation approach to understand the technology's key features. Potential molecular structures are being investigated that can be easier to construct by lowering resolution demands, as suggested by the concept of big structures [117]. Researchers have conducted multiple studies on the examination of individual molecules using experimental deposition and characterization [113, 118]. Regarding the arrangement of molecular devices, achieving high accuracy and resolution is necessary, which poses challenges in the existing implementation of these devices.

However, there are other methods that show outstanding potential for creating patterned self-assembly monolayers with nanometric precision. These include nanoshaving, hydrogen de-passivation lithography, and scanning tunnelling microscopy [119, 120]. A recent study introduced a computational method that addresses the problem of nanopatterning by performing computations directly on a consistent self-assembly

monolayer [121]. Several strategies show promise for creating extremely thin nanowires [122-124], and they are also promising for the development of write-in or clocking systems [125-127].

To sum up, by leveraging the unique properties of quantum dots and electron positioning, QCA cells offer a novel approach to computation that promises high density, low power consumption, and potentially faster processing speeds. However, challenges such as operating temperature, fabrication precision, and integration with existing technology remain. Continued research and development are essential to overcome these hurdles and realise the full potential of QCA in future computing applications. The implementation of a functional QCA cell is a significant milestone in the development of QCA technology. Overcoming challenges related to operating temperatures, fabrication precision, and reliable readout mechanisms will be crucial for advancing QCA technology in practical applications in future computing systems. Table 1.1 demonstrates a comparison of QCA with other quantum computing technologies, highlighting the specific advantages and limitations of each technology, as well as the reasons for selecting QCA.

**Table 1.1 QCA versus other quantum computing technologies.**

| Technology | Advantages | Limitations | Reason for QCA selection in Comparison to Weaknesses of other Quantum Technologies |
|---|---|---|---|
| **QCA** | - High-density integration<br>- Ultralow power consumption<br>- High switching frequency<br>- Universality<br>- Scalability and robustness | - Fabrication challenges<br>- Measurement challenges<br>- Integration with existing technologies challenges<br>- Lack of standard design tools and methods | QCA offers nanoscale computing circuits with high density, frequency, and energy efficiency, making it suitable for digital circuit design and reversible computing. |
| **Quantum Gate-based Systems** (e.g., Superconducting Qubits, Trapped Ions) | - True quantum computation leveraging superposition and entanglement<br>- Rapid progress with platforms like IBM Quantum and Google Sycamore | - Requires cryogenic cooling<br>- High error rates and decoherence<br>- Scalability challenges due to qubit limitations | Although there is a need for fault tolerant design with QCA, by typically doubling up the number of cells in a gate, this is much simpler than the required complex quantum computing error correction protocols. |
| **Quantum Annealing** (e.g., D-Wave Systems) | - Effective for solving combinatorial optimisation problems.<br>- Operates with relatively low cooling complexity<br>- Commercially available with thousands of qubits.<br>- suitable for logistics, optimisation, and materials science applications. | - Not suitable for general-purpose quantum computing<br>- Requires cryogenic cooling<br>- Lower precision due to stochastic nature | QCA supports general digital circuit designs beyond optimisation problems |
| **Photonic Quantum Computing** | - Operates at room temperature<br>- Ultra-fast communication with minimal loss<br>- Integrates well with existing optical networks | - Scalability challenges in entangled photon production<br>- Susceptible to photon loss | QCA offers scalability in digital circuits with broader applicability beyond optical communication |

# Chapter 2

# 2. Reversible Design Methodology

## 2.1. Reversible computing

Conventional digital circuits and computer systems typically entail the use of irreversible logic gates like AND, OR, NAND, and NOR, which have two input signals and one output signal [128, 129]. This leads to the loss of information and the associated dissipation of heat energy into the surrounding environment [130].

Information loss in computing circuits is a critical issue that has a significant impact on modern computational systems' energy efficiency, performance, and thermal management [131]. Landauer's principle articulates a fundamental relationship between this issue and the principles of thermodynamics and information theory [21]. According to Landauer's principle, erasing a bit of information in a computational process results in a minimum energy dissipation of $k_B T \ln 2$, where $k_B$ is the Boltzmann constant and $T$ is the temperature [21]. This principle highlights the intrinsic energy dissipation associated with information loss in irreversible computing processes. Claude Shannon's research on information entropy and its relationship to thermodynamics provided fundamental principles for understanding the energy expenditures associated with information processing [132]. Shannon's information theory quantifies the amount of information in a communication signal and its transmission efficiency [132].

The amount of energy dissipation due to information loss was long believed to be negligible, although it is significantly higher than Landauer's lower bound [23]. As nanoelectronics circuits and systems decrease in size and become more efficient, their energy dissipation levels approach Landauer’s bound. Therefore, to continue the trend of reducing power consumption and to reach Landauer’s lower bound, novel computation methods that allow for logic operations without information loss are needed [26].

Reversible computing is a computational paradigm that ensures the ’conservation’ of the number of input and output channels, thereby preserving information and reducing energy loss [133]. This property is essential for avoiding the increase in physical entropy

and the associated energy dissipation that occurs when information is erased irreversibly. Theoretically, reversible computations can avoid information loss and achieve zero energy dissipation [25]. As a result, to achieve computing operations with extremely low energy dissipation, it is essential to incorporate reversible computational circuits [26]. The technologies that carry out reversible operations could eventually allow for ultraefficient computing. Reversible computing relies on reversible logic gates, which are the building blocks of reversible circuits [134]. Unlike conventional logic gates, reversible gates have a one-to-one correspondence between the number of input and output signals, ensuring no information is lost. However, for the reversible computing paradigm to effectively function as a low-power strategy, it is essential to maintain reversibility from the logical level down to the physical level [27]. Consequently, both the logical operations and the physical implementation of the circuit must possess reversibility to avoid energy dissipation.

### 2.2. Reversible QCA circuits background

QCA is a very promising nanotechnology for performing computing operations that are both logically and physically reversible, thus allowing for the realisation of ultralow-energy-dissipation computing [133]. Reversible QCA computing circuits combine the principles of reversible computation with QCA's distinctive characteristics to offer ultra-energy-efficient computer systems [135].

Although there have been numerous studies on reversible QCA designs conducted recently [136-138], these studies have tended to address reversibility only at the logical level and have not treated information loss at the physical level. These studies used either the well-known logically reversible gates, such as the 3 × 3 Fredkin gate [139], the 3 × 3 Toffoli gate [140], the 2 × 2 Feynman gate [130], or newly suggested logically reversible gates. However, the equal number of input and output pins in these circuits' netlist is insufficient to make the circuit physically reversible and achieve energy dissipation lower than the Landauer limit. This is because the internal majority gates used in building these digital logic circuits are not reversible, i.e., the number of input and output pins for each internal majority voter gate is not equal.

Torres *et al.* (2019), for the first time, devised logically and physically reversible QCA circuits by designing reversible primitive logic gates and then created a half-adder based on those reversible primitive logic gates [141]. The results confirmed that basic logically and physically reversible QCA building blocks, including wires, single-logic gates, and reversible QCA half-adder circuits, can indeed operate in a logically and physically reversible fashion, resulting in energy dissipation levels lower than ($k_BT\ln 2$) per operation.

However, the design of this half-adder, shown in Figure 2.1, did not consider clock synchronization of the internal logic signals. This affects circuit output reliability, leading to inaccurate computations. The logically reversible QCA half-adder, proposed by Torres *et al.* (2019), consists of three AND gates and one OR gate. The sum operation has two input signals, A and B, that have diverging arrival times. The reversible OR gate inputs arrive after 9 and 13 clock zones, respectively, which means that input 1 arrives before input 2 by four clock zones, representing a complete clock cycle. Hence, input 1 must not change for an additional clock cycle to achieve time synchronization and consequently achieve correct operation.

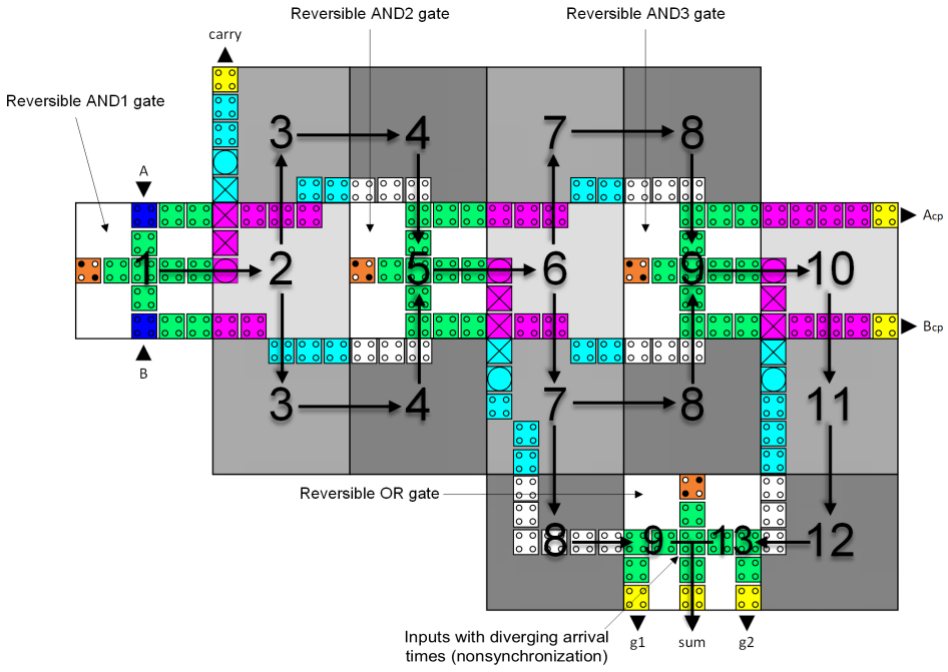



**Figure 2.1 Torres *et al.* [141] Reversible half-adder circuit.**

The present study offers a novel approach for developing QCA computing circuits that are both logically and physically reversible, as well as time-synchronised. This approach uses logically and physically reversible logic gates to construct logically and physically reversible QCA computing circuits. To achieve time synchronisation, this innovative method enables temporal synchronisation by possessing a circuit layout that is intrinsically more symmetrical. This new logical and physically reversible approach, incorporating a time-synchronised design and employing symmetric circuit layouts, can provide QCA circuits with ultra-low energy dissipation and guarantee precise computational outcomes. In Chapter 3, Section 3.1.3, Torres *et al.*'s logically and physically reversible, non-synchronised half-adder [141] was redesigned using the innovative, logically and physically reversible, time-synchronised design methodology.

## 2.3. Reversible, time-synchronised design method

This section provides a comprehensive description of the proposed logically and physically reversible, time-synchronised design method. This design method is implemented by forming each circuit from an arrangement of reversible QCA primitive logic gates connected by QCA wires. Information arrives at every input of a logic gate at each level in the design simultaneously, that is, with a similar delay. Thus, synchronised "signals" are transferred to the subsequent logic gate level in the circuit, up to the final outputs.

### 2.3.1. Logical and physical reversibility characteristic

Designing logically and physically reversible QCA circuits is challenging, as it requires sophisticated techniques to maintain reversibility consistently across both the logical and physical levels of the design. The term "logically reversible" is used to describe a netlist with an equal number of input and output pins. However, this doesn't always mean that the internal logic gates are also reversible and have the same number of input and output pins [141, 142]. "Physically reversible" means that every internal logic gate component in the circuit must have an equal number of input and output pins. As a result, there is no loss of information, and no associated energy dissipates into the environment.

Maintaining reversibility, down to the physical layout level, is the only way to realise ultralow-energy computing circuits [143].

### 2.3.2. Time-synchronisation characteristic

In computing circuit designs, clock synchronisation is essential for all the logic gates that compose the circuit, starting from the first logic gate to the final output [144]. Clock synchronisation is necessary to ensure the balance of the data propagation speed and guarantee that the data arrival time is correct for the next stage in the circuit [145]. The absence of the clock synchronisation characteristic can lead to the generation of inaccurate bits in the next stage, resulting in incorrect data transmission [144]. Thus, designing QCA digital circuits that are logically and physically reversible can ensure that the energy dissipated is less than ($k_BT\ln 2$) per operation. However, time synchronisation is required to ensure accurate data propagation at every stage of the circuit and guarantee the reliability of the circuit's output results.

In QCA circuits, the primary synchronised information applied to the input pins does not necessarily produce a similar arrival time for the inputs of all logic gates that comprise the circuit [146]. Moreover, input signal paths leading to a particular logic gate can come from different clock zones [75]. To assure time synchronisation and preserve the circuit functionality, it should be enforced that each logic gate inputs data during the same clock cycle, i.e., within four clock zones, before inputting new data. The key to achieving time synchronisation is to use an inherently more symmetric geometry in the design, which allows for symmetric data propagation. Symmetric geometry design can be achieved by utilising additional clock zones that can guarantee information arrival within the same clock cycle.

In addition, the proposed design strategy, which is both logically and physically reversible as well as time-synchronised, has been integrated with the USE clocking scheme detailed previously in Section 1.5 and illustrated in Figure 1.11. Current design workflows have seamlessly incorporated this integration, which is critical for automating the design process. The USE clocking scheme can facilitate the incorporation of feedback loops and simplify QCA-based circuit routing [78]. Additionally, it significantly improves

the creation of standard cell libraries and design tools for this technology while also preventing thermodynamic issues.

### 2.3.3. Reversible QCA fundamental logic gates

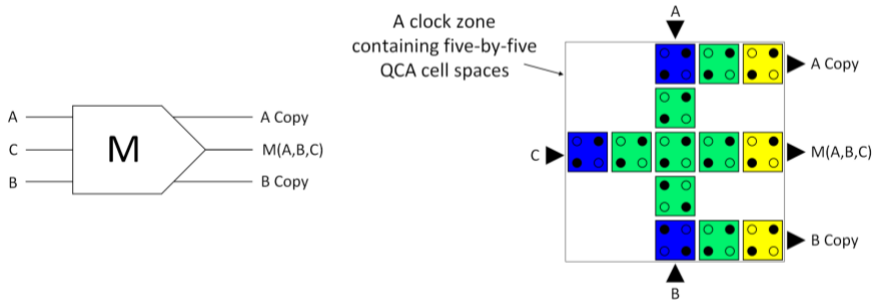
The process of designing QCA circuits typically entails the use of QCA majority voter gates and QCA inverters [67]. In QCA circuit design, the inclusion of these two types of logic gates is critical because their combination allows for the implementation of Boolean functions. The ability to construct complex logic functions using combinations of majority voter gates and inverters makes QCA a promising technology for future computing architectures, particularly in areas where minimising power consumption and maximising speed are critical [147].

The QCA inverter is inherently reversible because it possesses a one-to-one relationship between the input and output signals, as shown previously in Figure 1.4. Conversely, the conventional majority voter gate is inherently irreversible due to its configuration of three input pins and a single output pin, as depicted earlier in Figure 1.5. The conventional majority voter gate is considered the main source of energy dissipation in QCA circuits [148]. The absence of two output pins leads to a loss of information.

Therefore, the initial focus was on developing a majority voter gate with three inputs and three outputs, as demonstrated in Figure 2.2. This fully reversible three-input-three-output majority voter gate has been developed using QCA cells to achieve both logical and physical reversibility. The three-input-three-output majority gate replicates the data for two inputs, labelled A and B, into two outputs, labelled A Copy and B Copy, resulting in an overall situation with equal numbers of binary inputs and outputs. Figure 2.2a illustrates the sybmol of this majority gate, while Figure 2.2b shows its QCA layout. The reversible three-input-three-output majority voter gate can be mathematically expressed through Equation 1.2, which is also used with the standard irreversible three-input-one-output majority voter gate.

Subsequently, the reversible three-input-three-output majority voter gate was used to generate fully reversible 'AND' and 'OR' gates, which recycle two input bits. The recycling of two input bits can make the QCA 'AND' and 'OR' gates reversible [149]. The input label C determines the functionality of the reversible three-input-three-output majority

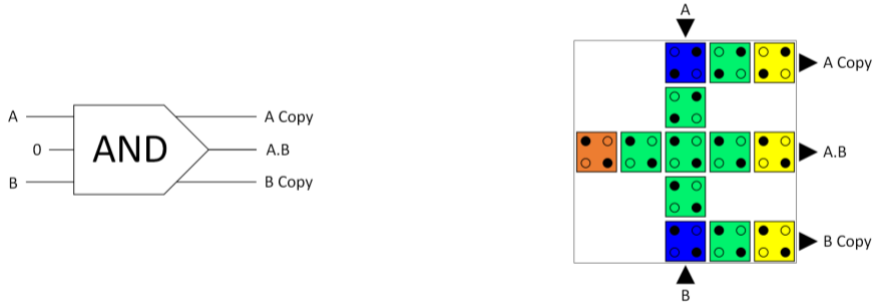
voter gate. The reversible three-input majority gate is programmed to produce an ‘AND’ gate or an ‘OR’ gate by setting a binary value of ‘0’ or ‘1’ to input C.




(a) (b)

**Figure 2.2 (a) The symbol of the three-input-three-output majority gate and (b) a USE clock zone containing the physical layout of the QCA three-input-three-output majority gate (the blue colour denotes the input cells, the yellow colour denotes the output cells, and the green colour denotes the internal cells).**

Assigning input C to ‘0’ can produce a reversible three-input-three-output ‘AND’ gate, as shown in Figure 2.3. Figure 2.3a illustrates the symbol of this logic gate, while Figure 2.3b shows its physical QCA layout. Equation 1.3 presents the mathematical representation of the reversible three-input-three-output ‘AND’ gate, which is the same as the conventional irreversible three-input-one-output ‘AND’ gate.

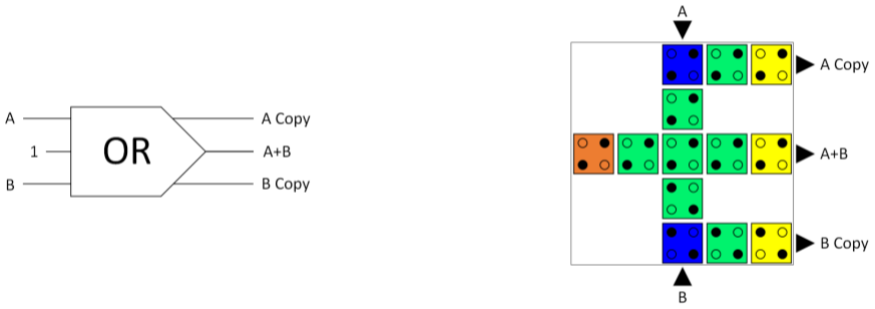



(a) (b)

**Figure 2.3 (a) The symbol of the reversible AND gate and (b) a USE clock zone containing the physical layout of the reversible QCA AND gate (the blue colour denotes the input cells, the yellow colour denotes the output cell, the green colour denotes the internal cells, and the orange cell with two electrons in upper left and bottom right denotes the cell with a fixed value of ‘0’).**

On the other hand, assigning input C to ‘1’ can produce a reversible three-input-three-output ‘OR’ gate, as shown in Figure 2.4. Figure 2.4a illustrates the symbol of this logic gate, while Figure 2.4b shows its physical QCA layout. Equation 1.4 presents the

mathematical representation of the reversible three-input-three-output ‘OR’ gate, which is the same as the conventional irreversible three-input-one-output ‘OR’ gate.




(a) (b)

**Figure 2.4 (a) The symbol of the reversible OR gate and (b) a USE clock zone containing the physical layout of the reversible QCA OR gate (the blue colour denotes the input cells, the yellow colour denotes the output cell, the green colour denotes the internal cells, and the orange cell with two electrons in the upper left and bottom right denotes the cell with a fixed value of ‘1’).**

The logically and physically reversible three-input-three-output ‘AND’ and ‘OR’ gates are the main building ‘blocks’ in the development of logically and physically reversible, time-synchronised QCA digital computing circuits.

### 2.3.4. Designing reversible, time-synchronised QCA circuits

This study uses a two-stage design methodology to develop logically and physically reversible, time-synchronised QCA computing circuits. As shown in Figure 2.5, the first stage is to build the circuit reversibly at the logical level (synthesis), and the second stage is to create the circuit reversibly at the physical level (layout) using QCA-interconnected devices.

The logical level consists of structural and behavioural descriptions. The first step is the structural description, which entails defining and generating the circuit's gate-level netlist. The following step provides a behavioural description of the circuit, which outlines the input and output relations. After that, simulations are employed to validate the circuit synthesis. At this stage, the *Logisim 2.7.1* software is used to develop circuit synthesis and conduct behavioural simulations. If the simulation produces unexpected results, the output is considered a ‘Fail’ result. In this case, the circuit netlist must be modified, and the circuit's input/output relations examined again. When the simulation produces accurate results, it validates the correctness of the circuit synthesis and deems the output a ‘Pass’

result, enabling a move to the second stage, which is designing the circuit's physical QCA layout.

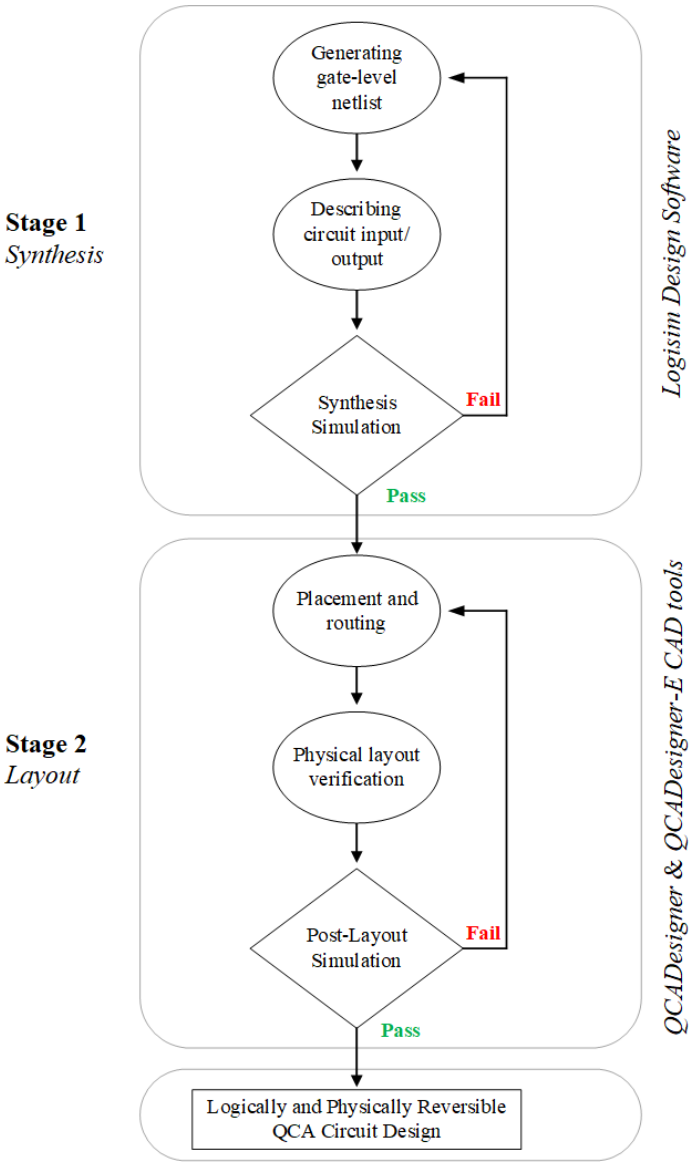



**Figure 2.5 The hierarchical structure of designing logically and physically reversible QCA circuits (*Logisim* is used for the synthesis stage while *QCADesigner* and *QCADesigner – E* are employed for the layout stage).**

The physical level represents the circuit's transition from synthesis to a QCA layout. The QCA layout includes a geometric representation of the circuit elements and their connections in the form of QCA cells and layers that define the circuit's physical structure. This process typically begins with identifying the locations of the 'pins,' followed by gate placement and routing. Layout design tools help create the physical layout of the QCA

circuit. This study employed the widely used QCA technology-based computer-aided design (TCAD) tool *QCADesigner 2.0.3* [71] for this purpose. QCADesigner implements the coherence vector simulation engine (CVSE), which incorporates quantum-level microscopic physical modelling of the performance of QCA cells [150]. Table 2.1 details the technological specifications used for the physical implementation of the logically and physically reversible, time-synchronised design method.

**Table 2.1 The adopted technological parameters.**

| Parameter | Description | Value |
|---|---|---|
| QD size | Quantum-dot size | 5 nm |
| Cell area | Dimensions of each cell | 18 x 18 nm |
| Cell distance | Distance between two cells | 2 nm |
| Layer separation | Distance between QCA layers in multilayer crossing | 11.5 nm |
| Clock high | Max. saturation energy of clock signal | 9.8E-22 J |
| Clock low | Min. saturation energy of clock signal | 3.8E-23 J |
| Relative permittivity | Relative permittivity of QCA materials (GaAs & AlGaAs) | 12.9 |
| Radius of effect | Maximum interaction distance between cells | 80 nm |

Subsequently, layout verification procedures, including layout versus schematic (LVS) and design rule checking (DRC), are implemented. LVS is a crucial verification step in the IC design process. It ensures that the physical layout of the circuit matches the original design intent captured in the schematic. LVS verification helps to identify discrepancies between the designed circuitry and its physical implementation, ensuring that the IC chip will function as intended once fabricated. DRC is another critical verification step in the IC design process. Generally, DRC verification ensures that the physical layout of the circuit adheres to the specified manufacturing process rules. For QCA circuits, DRC is used to ensure that the layout complies with all the necessary geometric, connectivity rules, and technology requirements. Due to the lack of tools integrated with QCA technology to automate DRC and LVS verification processes, this study performs manual verification for QCA layouts. Although manual verification is feasible for basic and small circuit designs, it becomes increasingly complex and challenging with advanced VLSI designs.

Finally, post-layout simulation is performed to validate both the circuit performance and reliability, as well as evaluate the energy dissipation values. To simulate the circuit

performance, the *QCADesigner 2.0.3* can also be used. The output is regarded as a 'Fail' if the simulation produces unexpected outcomes. In this case, we must go over gate placement, the pins' locations, routing, and layout verification. When the layout simulation produces a correct output, or 'Pass' results, it signifies successful completion of the circuit design, paving the way for the energy dissipation simulation.

### 2.3.5. Energy dissipation simulation

This study used the TCAD tool *QCADesigner-E 2.2* [96] to simulate the energy dissipation of the designed logically and physically reversible, time-synchronised computing circuits. The QCADesigner-E is an enhancement tool of the well-known QCA TCAD package, QCADesigner. The QCADesigner-E package adds an energy dissipation extension treatment to the CVSE model of the QCADesigner design package. It also treats QCA cells using quantum mechanics, which is a rigorous microscopic approach. In the present research, the timestep ($T_{step}$) used was $0.1\ \tau = 0.1$ fs, where $\tau$ denotes the relaxation time for the dissipation. A small enough timestep is essential to reduce simulation errors and obtain accurate results (see Section 1.7). When using this time step, we can achieve less than 5% simulation errors for numerical energy conservation violations, which is considered acceptable [96]. Table 2.2 outlines all the simulation parameters that were utilised in this study.

**Table 2.2 The employed simulation parameters.**

| Parameter | Description | Value |
|---|---|---|
| $\tau$ | Relaxation time | 1E-15 s |
| $T_{\gamma}$ | Period of the clock signal | 1E-9 s |
| $T_{in}$ | Period of the input signals | 1E-9 s |
| $T_{step}$ | Time interval of each iteration step | 1E-16 s |
| $T_{sim}$ | Total simulation time | 8E-9 s |
| $\gamma_{shape}$ | Shape of clock signal slopes | Gaussian |
| $\gamma_{slope}$ | Rise and fall time of the clock signal slopes | 1E-10 s |

### 2.3.6. Wire junctions' issue

Handling wire junctions is one of the most significant challenges in developing digital logic circuits. The proposed logically and physically reversible, time-synchronised design method addresses this issue by using the multilayer technique for QCA computing circuit

design. This approach employs three distinct layers to resolve the wire crossing issue, as illustrated in Figure 1.14 (see Section 1.6.2). Compared to other wire-crossing techniques for QCA circuits, the multilayer method's primary advantage lies in its ability to produce more reliable circuits [92].

### 2.3.7. Simulation testbench

In the IC design process, using a testbench is a common approach to characterising designs because it provides a controlled environment to simulate the gates' performance and energy dissipation under various conditions [151]. Typically, designers develop the QCA testbench to facilitate a comprehensive simulation of QCA gates, focussing on aspects such as energy dissipation and functionality [152]. The testbench includes input signals that stimulate the QCA gates. To thoroughly test the gates' performance, these signals cover a wide range of operating conditions and input combinations.

To conduct a realistic energy analysis, the logically and physically time-synchronised design method employed a testbench similar to one previously detailed in the literature [96]. This testbench places buffer cells between the stimulated inputs and the actual inputs of the design under test (DUT), as illustrated in Figure 2.6. These buffer cells help simulate the signal propagation and delay effects that would occur in a real QCA circuit. The DUT consists of the QCA gates being characterised. The testbench is configured to measure the performance of these gates under various input conditions, providing data on energy dissipation, switching behaviour, and other key parameters. The testbench then runs a series of simulations, applying various input signals to the DUT. These simulations are designed to test the gates under different operating conditions. The analysis identifies potential improvements to the gate design. These improvements aim to enhance the energy efficiency, reliability, and overall performance of the QCA gates. Note that the overall energy analysis excludes the buffer cells used to emulate interactions with neighbouring QCA structures. This exclusion ensures that the characterisation focusses solely on the DUT and provides accurate data on the gates' intrinsic performance.

The QCA logic gate characterisation testbench is a critical tool for evaluating and improving the performance of QCA circuits. By simulating realistic operating conditions,

the testbench helps to identify and address potential issues in QCA gate design, leading to more efficient and reliable QCA circuits.

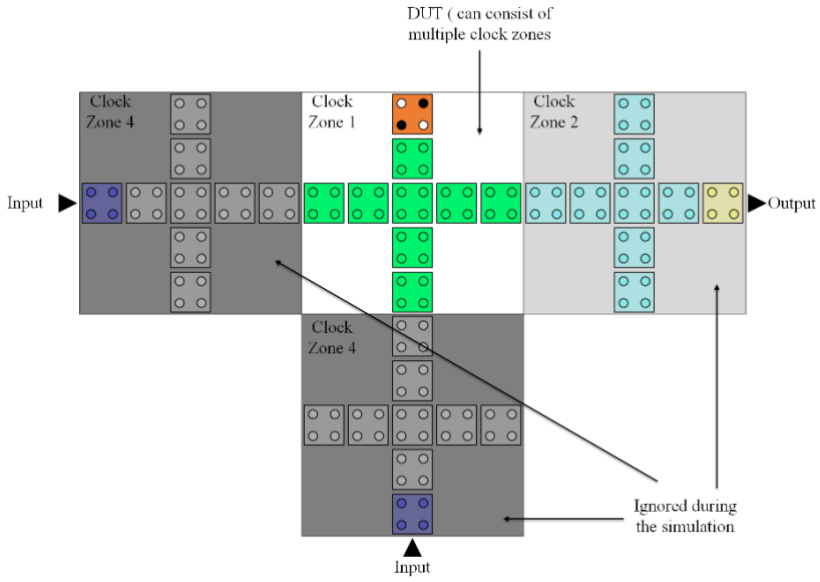



**Figure 2.6 Simulation testbench [96].**

# Chapter 3

# 3. Reversible QCA Combinational Digital Circuits

## 3.1. Designing reversible and time-synchronised QCA combinational circuits

This section employs the innovative design methodology from Chapter 2 to create eight novel, reversible, time-synchronised QCA combinational digital circuits. These circuits were designed to achieve ultralow energy dissipation, thereby pushing the boundaries of efficiency and performance in QCA technology. The designed circuits include exclusive OR (XOR), exclusive NOR (XNOR), half-adder, half-subtractor, multiplexer, demultiplexer, comparator, and decoder. The simulation is performed to validate the effectiveness of the logically and physically reversible, time-synchronised design method in creating ultralow-energy-dissipation QCA combinational circuits. The goal is to achieve energy dissipation values below the Landauer limit of 0.06 meV at 1 K while ensuring reliable computational outcomes.

### 3.1.1. Reversible QCA XOR design

The first QCA-based design developed using the reversible, time-synchronised methodology is a reversible, time-synchronised XOR gate. Digital circuits frequently use the XOR gate for tasks like parity checking and generation, arithmetic operations, and digital signal processing [153]. The proposed reversible, time-synchronized QCA XOR gates consist of two reversible OR gates and one reversible AND gate, each with three binary inputs and three binary outputs (see Figure 3.1). Figure 3.1a provides an overview of the design synthesis, detailing the logical structure and flow of the circuit. Figure 3.1b displays the corresponding QCA cell layout, which shows how the circuit works physically within the QCA framework. The layout is critical for visualizing how the design's theoretical components translate into practical and spatial configurations [30].

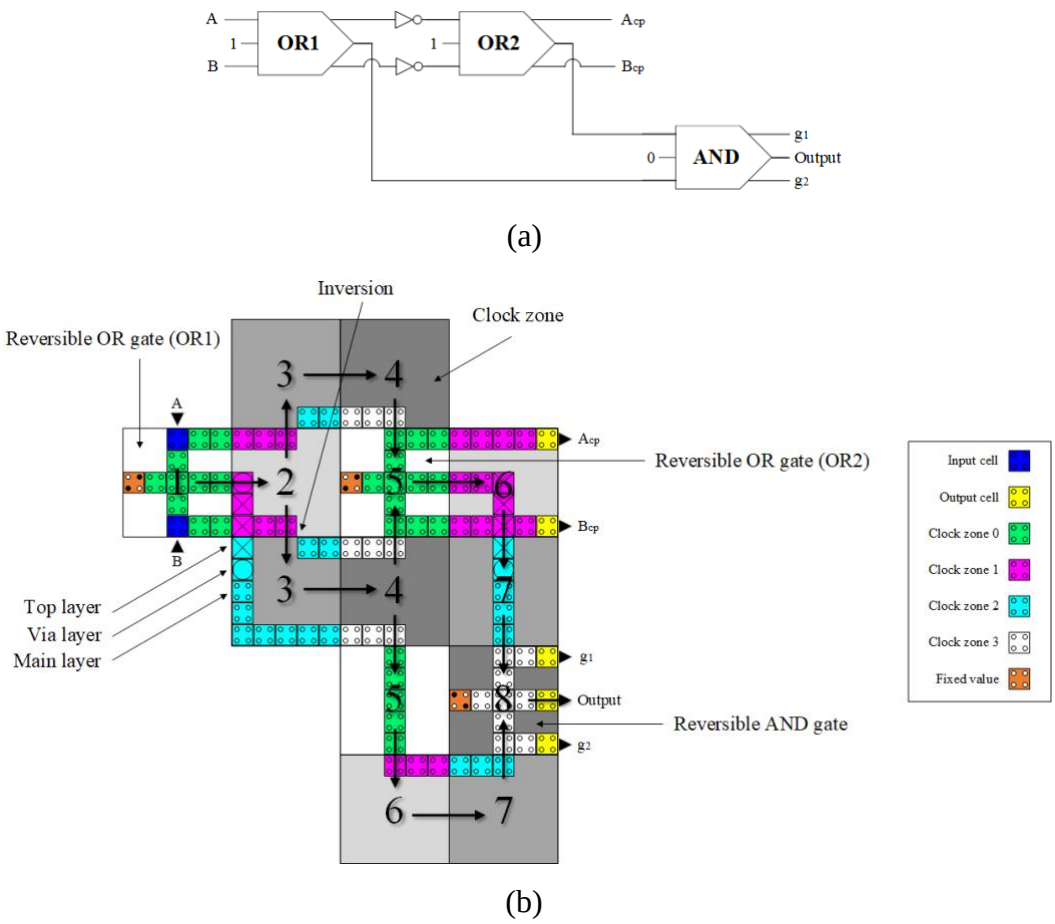



**Figure 3.1 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA XOR ($A_{cp}$ and $B_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs).**

The crucial aspect of time synchronisation lies in the design geometry, which enables symmetric data propagation. The inherently symmetric configuration of the logically and physically reversible, time-synchronized XOR circuit is detailed here. The first reversible OR gate (OR1) initially receives the two binary inputs, *A* and *B*. The lower AND gate receives the output from OR1, which it then routes to the output pin "Out" through eight clock zones. The second reversible OR gate (OR2) simultaneously receives inverted copies of the input data, with a time delay of four clock zones. The output from OR2 is then transferred to the lower AND gate and subsequently to the output pin labelled "Output" through an additional four clock zones. Thus, the outputs of both reversible OR gates are simultaneously transferred to the lower AND gate and then to the output pin labelled "Output" through eight clock zones. The arrival time for the bit information copies of OR2 labelled "$A_{cp}$" and "$B_{cp}$" outputs at the end of the circuit corresponds to six

clock zones. The other QCA combinational circuits also employed the symmetric design strategy to accomplish time-synchronisation along with logical and physical reversibility. Thus, the proposed designs ensure that there is a balance between the data propagation speed, at all the circuit stages, to achieve time synchronisation.

The XOR gate is a digital logic gate that only outputs true or 1 when the number of true inputs is odd. Specifically, for two inputs, A and B, the XOR gate will output true (1) if either A or B is true, but not both. If both inputs are false (0) or both are true (1), the output will be false (0). Equation 3.1 provides the standard Boolean expression for the output of the proposed XOR logic gate. Table 3.1 presents the output responses for different input combinations of the XOR.

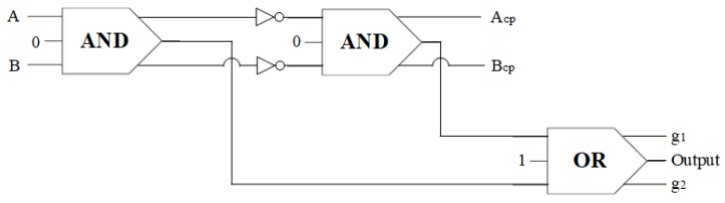
$$Output = (A + B).(\bar{A} + \bar{B}) \tag{3.1}$$

**Table 3.1 Truth table for XOR gate shown in Figure 3.1.**

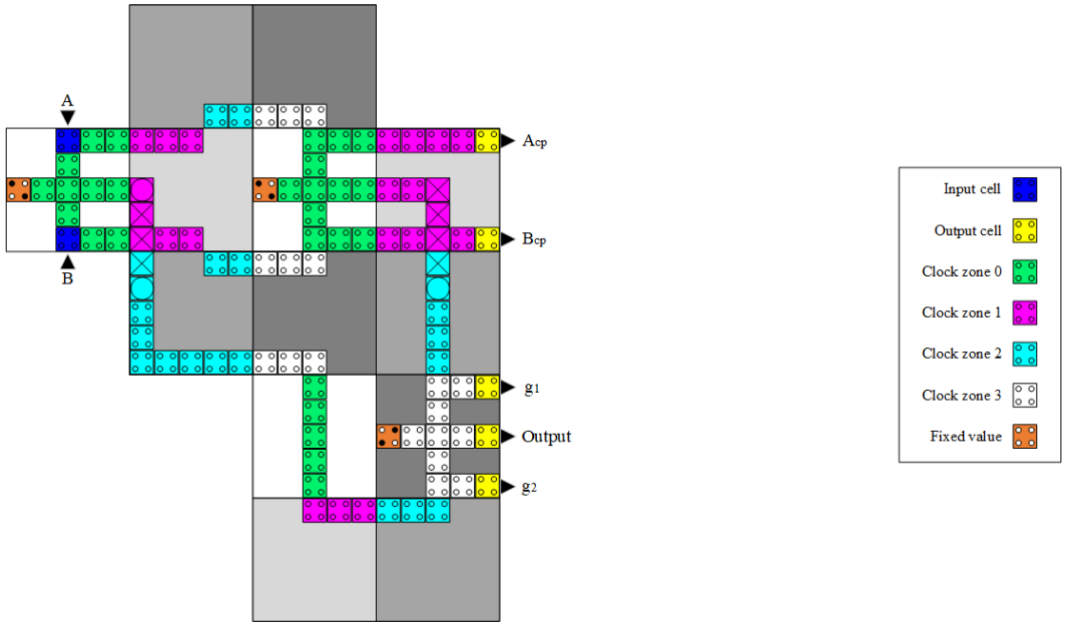
| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

### 3.1.2. Reversible QCA XNOR design

The second combinational circuit introduced is the reversible, time-synchronised XNOR gate. The XNOR gate is useful in digital circuits for equality comparison, error detection, and correction systems, where the output indicates whether two binary values are identical [153]. The proposed reversible, time-synchronised QCA XNOR gate contains two reversible AND gates and a single reversible OR gate. This circuit's design ensures logical and physical reversibility, as well as time synchronisation. Figure 3.2a shows the design synthesis, and Figure 3.2b illustrates the corresponding QCA cell layout.




(a)




(b)

**Figure 3.2 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA XNOR circuit ($A_{cp}$ and $B_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs).**

The XNOR gate is a digital logic gate that only outputs true or 1 when the number of true inputs is even. Essentially, it is the XOR gate's complement. For two inputs, A and B, the XNOR gate will output true (1) if both inputs are the same, either both true (1) or both false (0). If the inputs differ, the output will be false (0). Equation 3.2 provides the standard Boolean expression for the output of the proposed XNOR logic circuit, while Table 3.2 shows the output responses for various input combinations.

$$Output = (A.B) + (\bar{A}.\bar{B}) \tag{3.2}$$

**Table 3.2 Truth table for XNOR gate shown in Figure 3.2.**

| A | B | Output |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

### 3.1.3. Reversible QCA half-adder design

In arithmetic operations, the half-adder serves as a fundamental digital circuit, specifically for adding two single-bit binary numbers [153]. It produces two outputs: the sum and the carry. The sum represents the least significant bit of the result, while the carry represents the overflow bit, which may need to be added to the next significant bit in multi-bit addition. Figure 3.3 shows a reversible time-synchronised QCA half-adder circuit consisting of three AND gates and one OR gate. Figure 3.3a shows the design synthesis, and Figure 3.3b illustrates the corresponding QCA cell layout. This design applies the proposed reversible time-synchronised design paradigm to the previously established reversible non-synchronised half-adder design by Torres *et al.* [141]. In this new design, the OR gate was repositioned, and an additional clock zone was introduced to ensure that all signal paths have equal lengths. This adjustment means that, unlike the original Torres *et al.* design [141], the sum operation in this new version benefits from inputs that arrive at the same time. After 12 clock zones, the inputs to the reversible OR gate reach it simultaneously. This synchronisation ensures that the proposed reversible half-adder circuit achieves precise time synchronisation, which is crucial for maintaining accurate computation throughout the circuit.

The truth table for this circuit is presented in Table 3.3, while its Boolean expressions are described in Equation 3.3 as follows:

$$\begin{aligned} Sum &= (A.\bar{B}) + (\bar{A}.B) \\ Carry &= (A.B) \end{aligned} \tag{3.3}$$

**Table 3.3 Truth table for half-adder circuit shown in Figure 3.3.**

| A | B | Sum | Carry |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

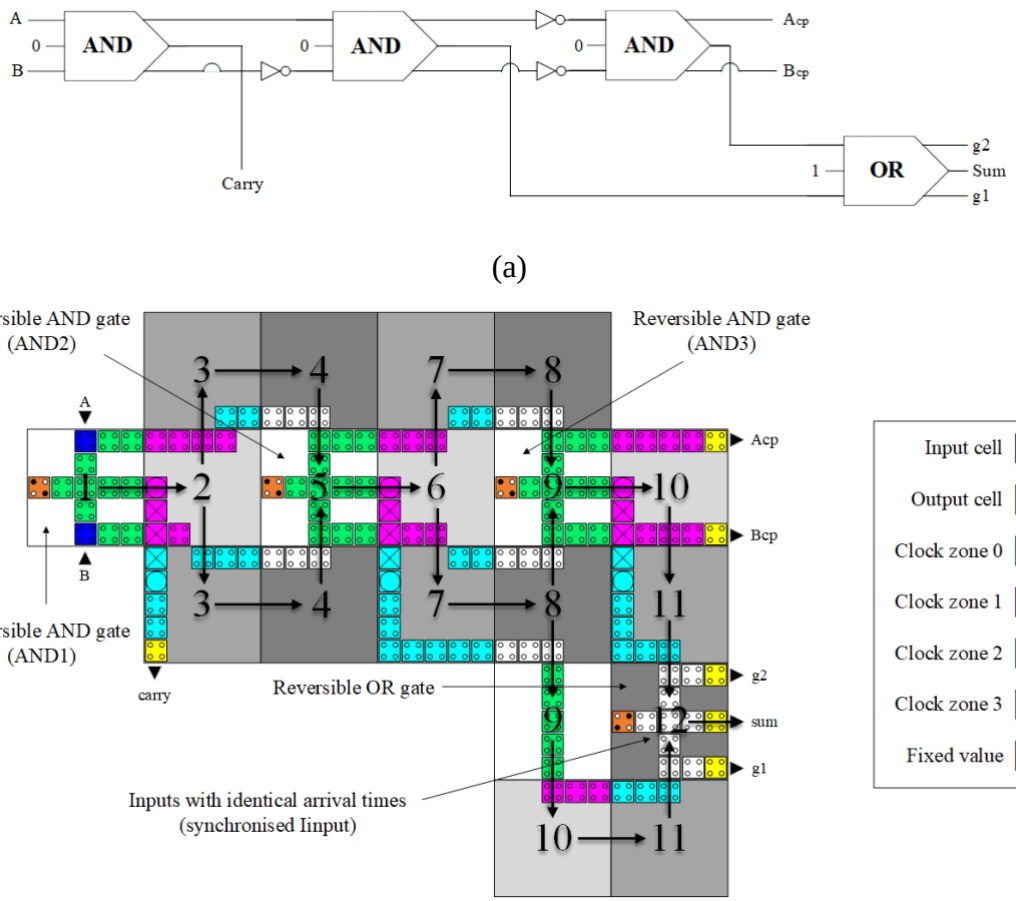


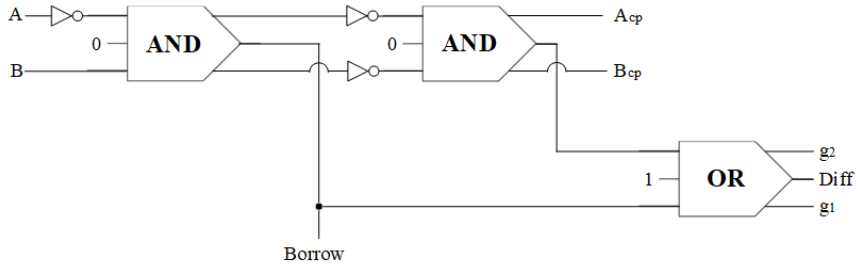

**Figure 3.3 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA half-adder circuit ($A_{cp}$ and $B_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs).**

Chapter 6, Section 6.2 presents a comprehensive comparative analysis for this novel logically and physically reversible, time-synchronised half-adder design. This analysis is conducted in comparison with Torres *et al.*'s logically and physically reversible, non-synchronised half-adder [141], the partially reversible half-adder proposed in Chapter 6, Section 6.1, and the most efficient irreversible and logically reversible circuits documented in the literature.

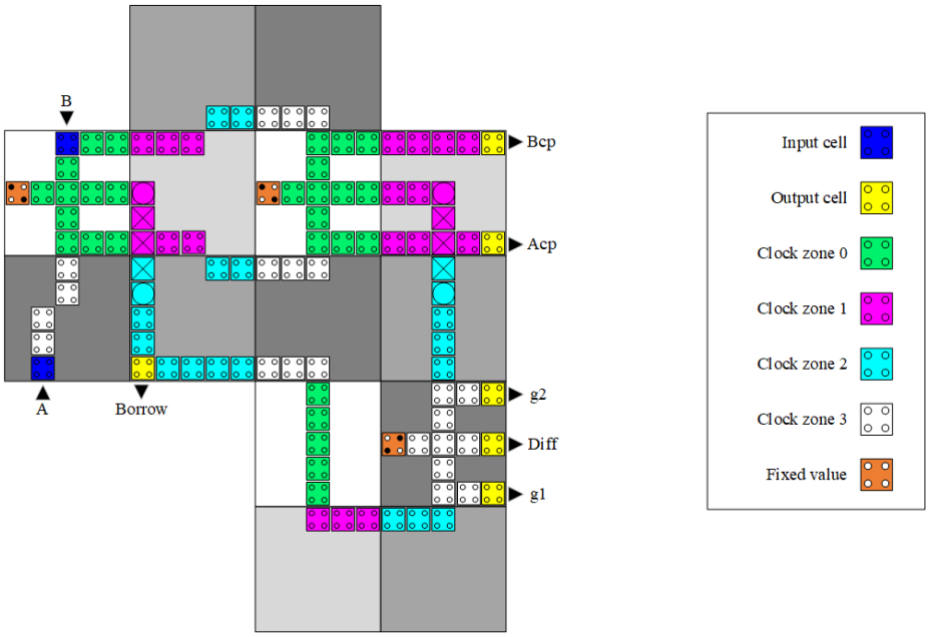
### 3.1.4. Reversible QCA half-subtractor design

The half-subtractor is a digital circuit that subtracts two single-bit binary numbers [153]. It generates two outputs: the difference and the borrow. The difference output shows the outcome of the subtraction, and the borrow output indicates whether a 'borrow'

from the next higher bit is required. Binary subtraction operations use half-subtractors as building blocks for full subtractors, which can handle borrow inputs and subtract multi-bit binary numbers. Figure 3.4 illustrates the proposed reversible, time-synchronised QCA half-subtractor. Two reversible AND gates and one reversible OR gate make up the circuit. Figure 3.4a provides a comprehensive explanation of the design synthesis, whereas Figure 3.4b represents the corresponding QCA cell architecture.




(a)




(b)

**Figure 3.4 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA half-subtractor circuit ($A_{cp}$ and $B_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs).**

Equation 3.4 defines the Boolean equations for the half-subtractor outputs, while Table 3.4 shows the half-subtractor output responses for the various combination inputs.

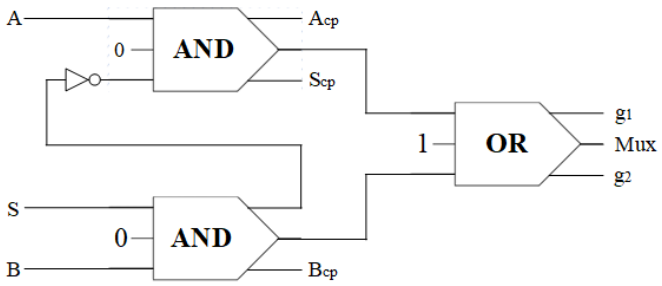
$$Diff = (\bar{A}.B) + (A.\bar{B})$$
$$Borrow = (\bar{A}.B) \quad (3.4)$$

**Table 3.4 Truth table for half-subtractor circuit shown in Figure 3.4.**

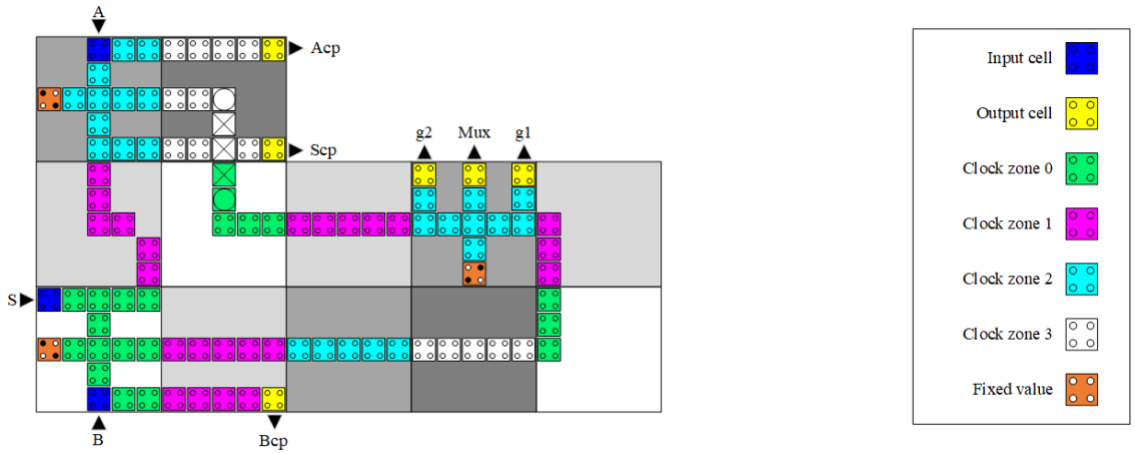
| A | B | Diff | Borrow |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |

### 3.1.5. Reversible QCA 2:1 multiplexer design

The 2:1 multiplexer circuit is a digital switch, enabling the selection and transmission of one of two input signals to the output [153]. A control signal, also referred to as the selector or select input, determines this selection. The 2:1 multiplexer effectively routes one of the two data inputs to the output, depending on the value of the select input. Digital systems like processors, communication systems, and data routing devices frequently use the 2:1 multiplexer, which is crucial for designing more complex multiplexer circuits [154]. Figure 3.5 demonstrates the proposed reversible, time-synchronised QCA 2:1 multiplexer. Figure 3.5a gives the design synthesis of the logic circuit, whereas Figure 3.5b represents the corresponding QCA cell architecture. This circuit comprises two reversible AND gates and one reversible OR gate. It functions by selecting one of two input signals, A or B, based on a selector input, S, and outputs the selected signal as MUX.




(a)




(b)

**Figure 3.5 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA 2:1 multiplexer circuit ($A_{cp}$, $B_{cp}$ and $S_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs).**

Equation 3.5 provides the Boolean expression of the proposed reversible, time-synchronised QCA 2:1 multiplexer and outlines the logical relationship between the inputs and the output. Table 3.5 contains the truth table for the multiplexer, illustrating how different input combinations affect the circuit's output, ensuring that the design operates correctly under various conditions.

$$Mux = (A.\bar{S}) + (B.S) \tag{3.5}$$

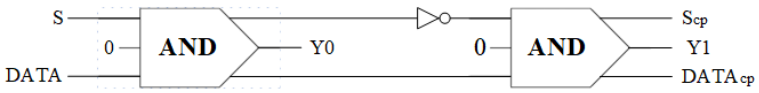
**Table 3.5 Truth table for 2:1 multiplexer circuit shown in Figure 3.5.**

| S | A | B | Mux |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

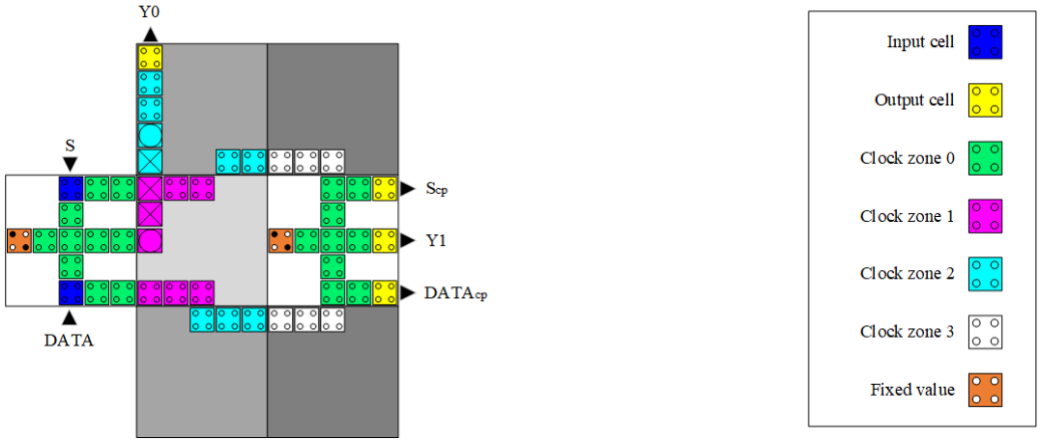
### 3.1.6. Reversible QCA 1:2 demultiplexer design

The 1:2 demultiplexer is a digital circuit that takes a single input signal and directs it to one of two possible output lines based on a select signal [153]. It effectively channels

the input data to one of the outputs, depending on the value of the selected input. Digital systems commonly use demultiplexers to route data from a single source to multiple destinations based on control signals. Demultiplexers are essential in applications such as data distribution, communication systems, and circuit design, where selective data routing is required [154]. Figure 3.6 illustrates the proposed reversible time-synchronised QCA 2:1 demultiplexer. Figure 3.6a gives the design synthesis of the logic circuit, while Figure 3.6b represents the corresponding QCA cell architecture. The design contains only two AND gates.




(a)




(b)

**Figure 3.6 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA 1:2 demultiplexer circuit ($S_{cp}$ and $DATA_{cp}$ indicate copies of the inputs).**

Equation 3.6 defines the Boolean functions for the outputs of the proposed reversible, time-synchronised QCA 2:1 demultiplexer, wherein S and DATA are the two inputs and Y0 and Y1 are the two outputs of the circuit. Table 3.6 provides the truth table for this circuit.

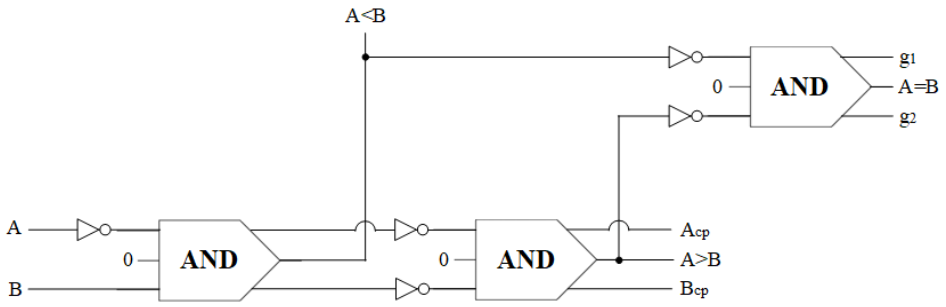
$$Y0 = (S.DATA)$$
$$Y1 = (\bar{S}.DATA) \tag{3.6}$$

**Table 3.6 Truth table for 1:2 demultiplexer circuit shown in Figure 3.6.**

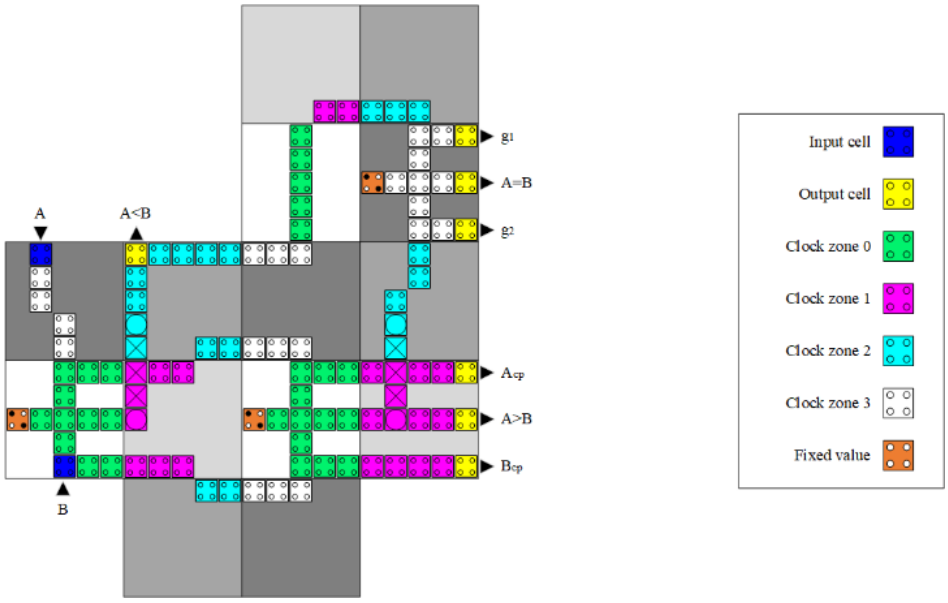
| S | DATA | Y0 | Y1 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 |

### 3.1.7. Reversible QCA 1-bit comparator design

The comparator circuit is an electronic device that compares two input binary numbers and outputs a signal indicating the comparison's result [153]. In digital electronics, a comparator typically compares two binary numbers and determines if one number is greater than, less than, or equal to the other. This functionality is crucial in many applications, including digital signal processing, sorting algorithms, and control systems [154]. A digital comparator circuit can be built using basic logic gates like AND, OR, XOR, and NOT gates. The number of bits compared determines the circuit's complexity. The proposed reversible time-synchronised QCA 1-bit comparator combines three AND gates, as shown in Figure 3.7. Figure 3.7a gives the design synthesis of the logic circuit, while Figure 3.7b represents the corresponding QCA cell layout. This 1-bit comparator has two single-bit inputs, A and B, and three outputs indicating whether A is greater than, less than, or equal to B.




(a)




(b)

**Figure 3.7 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA comparator circuit ($A_{cp}$ and $B_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs).**

Equation 3.7 presents the logic expressions for this logically and physically reversible, time-synchronised QCA 1-bit comparator circuit, outlining the conditions for determining if one input is greater than, less than, or equal to the other. Table 3.7 systematically lists the various possible input combinations and their respective output responses. This table provides a clear representation of how the circuit processes different inputs to produce accurate comparison results, highlighting the comparator's functionality in differentiating between the input values.

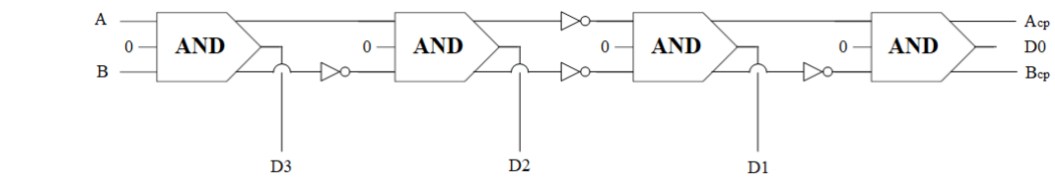
$$\begin{aligned} (A < B) &= (\bar{A}.B) \\ (A > B) &= (A.\bar{B}) \\ (A = B) &= (\bar{A}.B).(A.\bar{B}) \end{aligned} \tag{3.7}$$

**Table 3.7 Truth table for comparator circuit shown in Figure 3.7.**

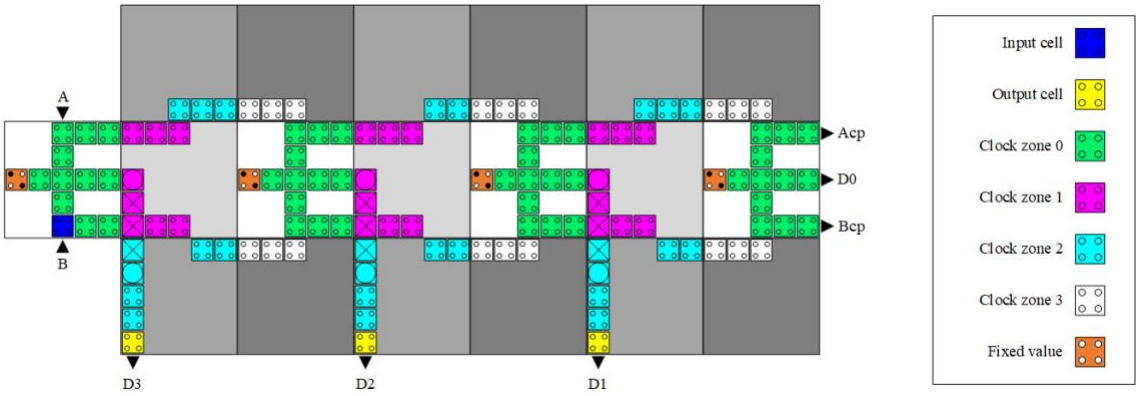
| A | B | A<B | A>B | A=B |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |

### 3.1.8. Reversible QCA 2:4 decoder design

The decoder circuit is a digital circuit that converts an n-bit binary input signal into a corresponding unique output signal [153]. Typically, it activates one of many output lines based on the binary input. Decoders are fundamental components in digital systems, such as microprocessors, memory address decoding, and data routing [154]. A decoder takes a binary input and sets only one of the output lines to active, typically binary 1, while the rest remain inactive, binary 0. This functionality guarantees the activation of only one specific output line for each unique binary input. Figure 3.8 illustrates the proposed reversible, time-synchronised QCA 2:4 decoder. This decoder consists of four AND gates, each responsible for activating one of the four output bits corresponding to the 2-bit input values within the integer range. Figure 3.8a gives the logic synthesis of the circuit, whereas Figure 3.8b depicts the corresponding QCA cell architecture.




(a)




(b)

**Figure 3.8 (a) Logical synthesis and (b) physical QCA layout of the reversible time-synchronised QCA 2:4 decoder ($A_{cp}$ and $B_{cp}$ indicate copies of the inputs).**

Equation 3.8 outlines the logic expressions for the proposed logically and physically reversible, time-synchronised QCA 2:4 decoder circuit, where A and B represent the two binary inputs, as well as D0, D1, D2, and D3 represent the four output lines. Each output

corresponds to a unique combination of the input values, as determined by the logic AND gates within the circuit. Table 3.8 displays the truth table for this decoder circuit, which details the output states for every possible combination of the input signals, illustrating the circuit's selection of the appropriate output line based on the inputs.

$$\begin{aligned} D0 &= (\bar{A}.\bar{B}) \\ D1 &= (\bar{A}.B) \\ D2 &= (A.\bar{B}) \\ D3 &= (A.B) \end{aligned} \tag{3.8}$$

**Table 3.8 Truth table for 2:4 decoder circuit shown in Figure 3.8.**

| A | B | D0 | D1 | D2 | D3 |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

### 3.2. Reliability simulation

The input and output responses for the eight proposed reversible, time-synchronised QCA combinational circuits, detailed in Section 3.1, were simulated using *QCADesigner 2.0.3*. For each circuit, the simulation calculates the results and then displays waveforms representing the computational outputs and delay times. The delay time of the proposed, logically and physically reversible, time-synchronised QCA combinational circuits was calculated by counting the clock zones along the critical path within the circuit. The critical path is defined as the longest route from an input pin to an output pin. Each clock zone corresponds to a delay of one-quarter of a clock cycle, indicating that four clock zones make up one complete clock cycle. Also, the simulation results showed the circuit's respective costs in terms of the area occupied, the number of QCA cells utilised, and the number of USE clocking tiles employed, with each tile consisting of a grid of 5 × 5 QCA cells. Table 3.9 presents these simulation results, based on the technology and simulation parameters specified earlier in Table 2.1 and Table 2.2, respectively.

### 3.2.1. Reversible QCA XOR simulation

Figure 3.9 displays the simulation results for the efficiently designed reversible, time-synchronised XOR gate presented in Figure 3.1. The waveform output results correspond to the truth table values listed in Table 3.1. Moreover, the XOR output value arrived after eight clock zones, a total delay time of two clock cycles. Furthermore, the circuit occupied an area of 0.15 $\mu m^2$, used 101 QCA cells, and used 13 USE clocking tiles.

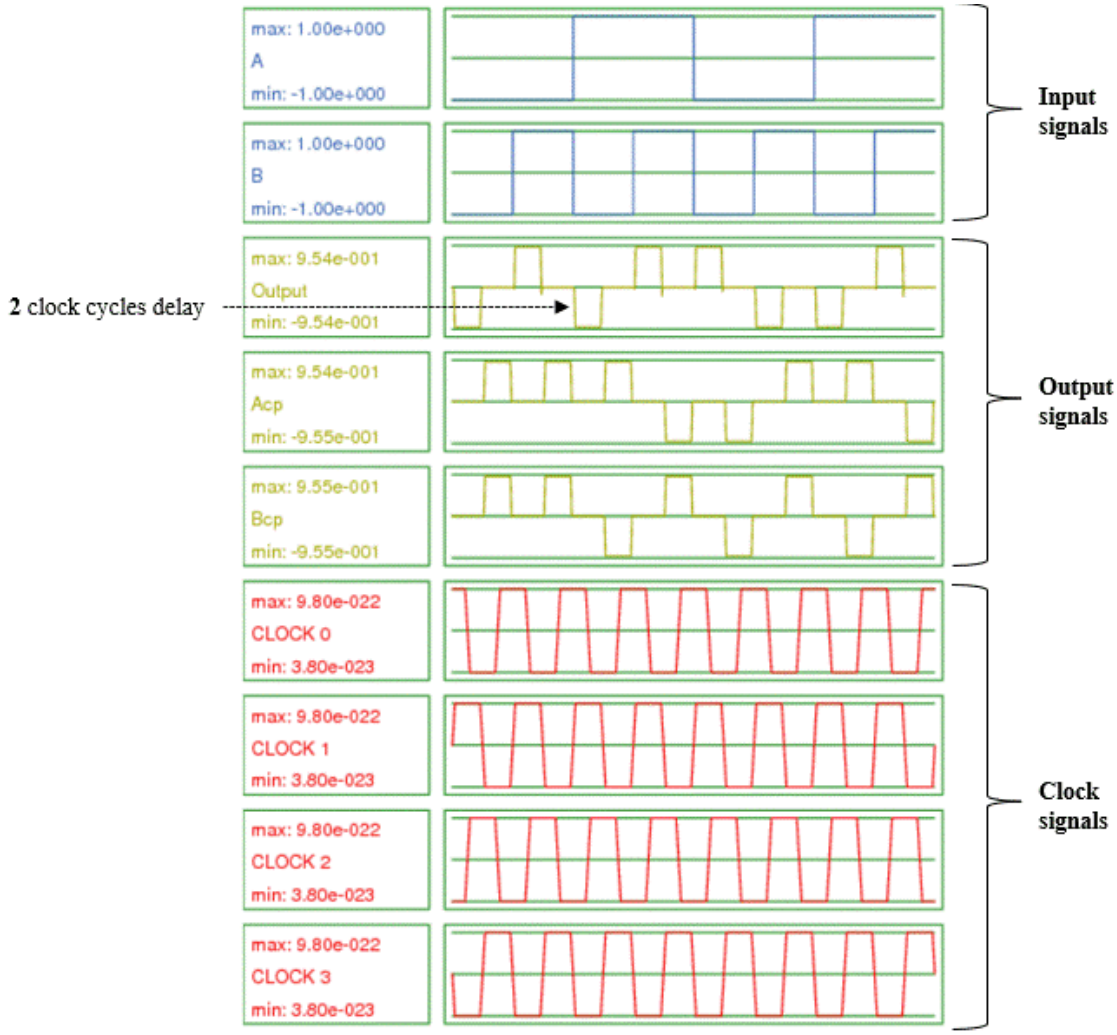



**Figure 3.9 Simulation waveforms of the proposed reversible time synchronised XOR design.**

### 3.2.2. Reversible QCA XNOR simulation

Figure 3.10 presents the simulated waveforms for the proposed reversible, time-synchronised XNOR gate, as presented in Figure 3.2. The polarisation output correctly

corresponds to the truth table values given in Table 3.2, thus confirming the soundness of the proposed reversible time-synchronised XNOR design. The circuit design has a circuit latency of eight clock zones (two clock cycles), which is consistent with the simulation results in Figure 3.10. The design had an area of 0.15 $\mu m^2$ and used 101 QCA cells and 13 USE clocking tiles.

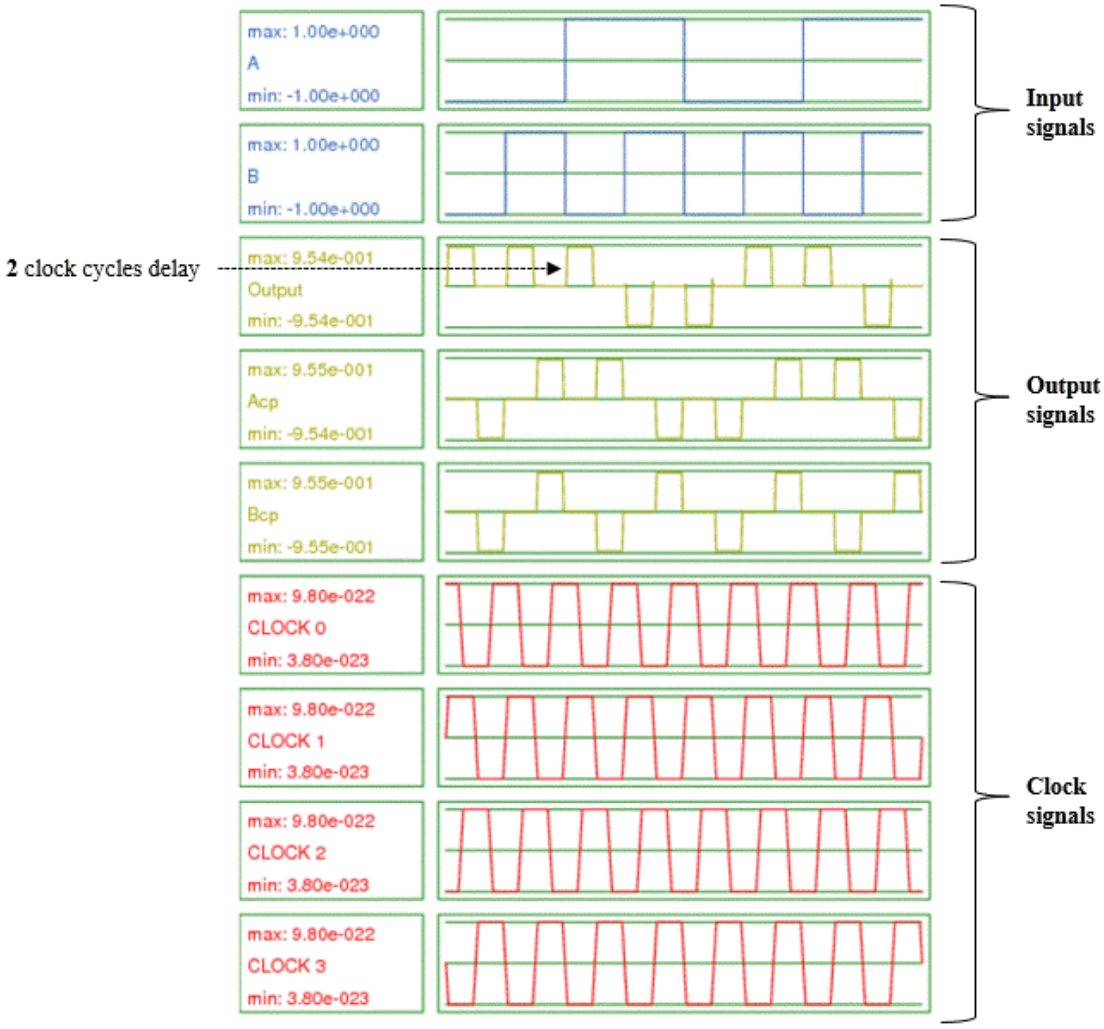



**Figure 3.10 Simulation waveforms of the proposed reversible time synchronised XNOR design.**

### 3.2.3. Reversible QCA half-adder simulation

The simulation results for the proposed reversible, time-synchronised half-adder circuit, depicted in Figure 3.3, are shown in Figure 3.11. The numerical outcomes verify that the design is consistent with its truth table, as detailed in Table 3.3. The reversible time-synchronised half-adder circuit produces the carry output after three clock zones

(0.75 clock cycles) and the sum output after 12 clock zones (three clock cycles), resulting in a total circuit latency of three clock cycles. The design occupies an area of 0.21 μm², employs 101 QCA cells, and utilises 19 USE clocking tiles.

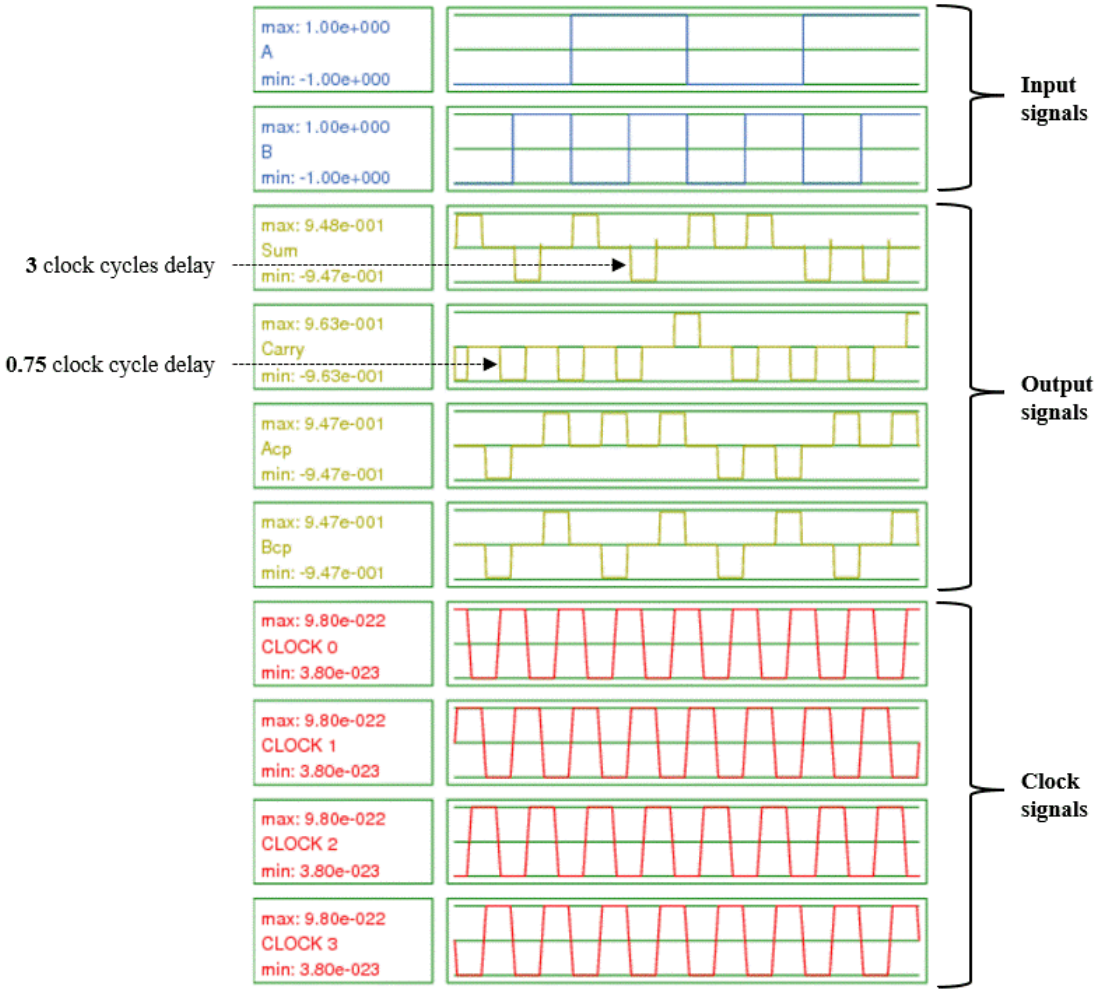



**Figure 3.11 Simulation waveforms of the proposed reversible time synchronised half-adder design.**

### 3.2.4. Reversible QCA half-subtractor simulation

Figure 3.12 presents the simulation results for the proposed reversible, time-synchronised half-subtractor, as described in Figure 3.4. The numerical input/output results validate that the circuit's operation aligns with the truth table provided in Table 3.4. The delay for the borrow output is three clock zones (0.75 clock cycles), while the delay for the difference value is eight clock zones (two clock cycles). Additionally, the design occupies an area of 0.15 μm², utilises 106 QCA cells, and employs 14 USE clocking tiles.

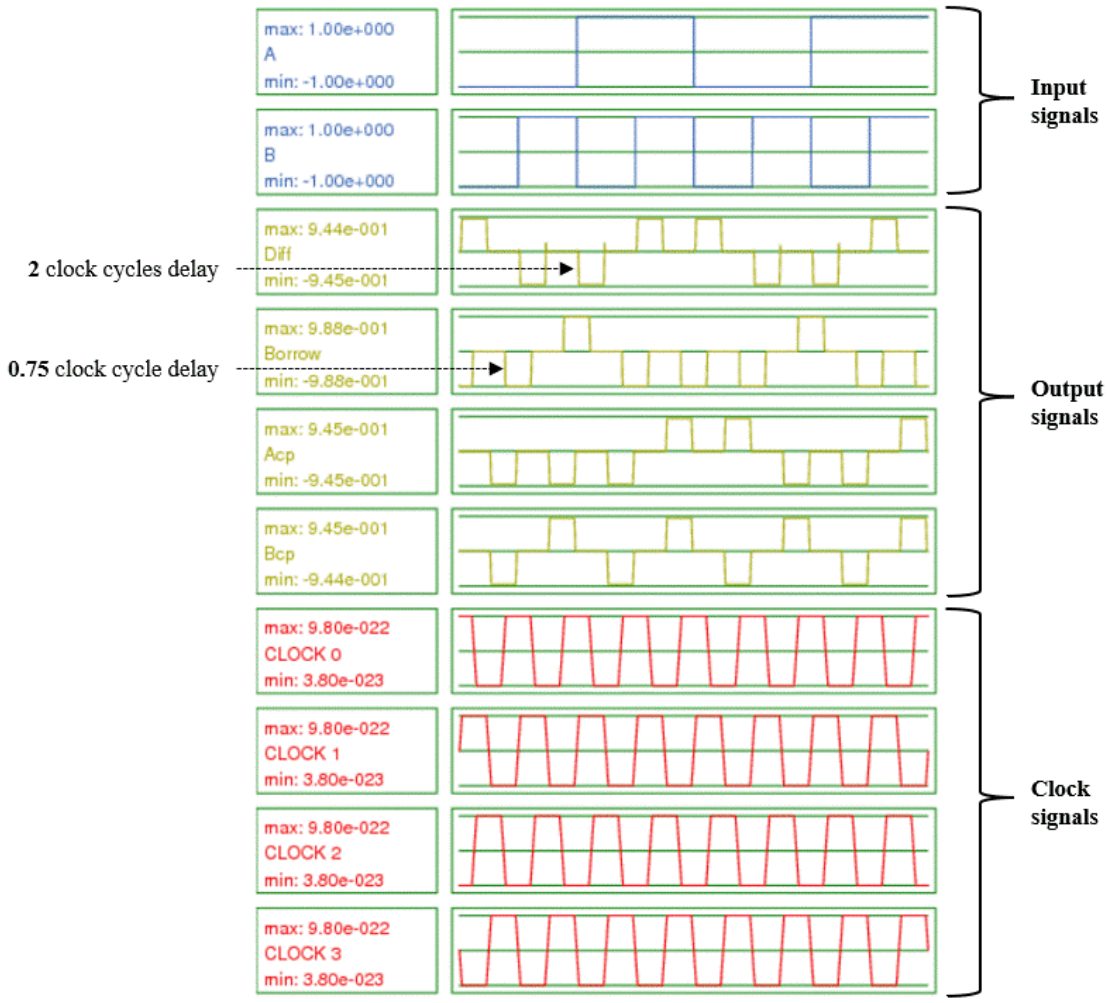



**Figure 3.12 Simulation waveforms of the proposed reversible time synchronised half-subtractor design.**

### 3.2.5. Reversible QCA 2:1 multiplexer simulation

Figure 3.13 displays the simulation waveforms for the proposed reversible, time-synchronised 2:1 multiplexer circuit, as shown in Figure 3.5. The numerical input/output response corresponds to the truth table values in Table 3.5, thus confirming the reliability of the design. The circuit latency is seven clock zones (1.75 clock cycles), aligning with the 2:1 multiplexer QCA layout design illustrated in Figure 3.5a. Additionally, the design requires an area of 0.14 $\mu m^2$, utilises 96 QCA cells, and employs 12 USE clocking tiles.

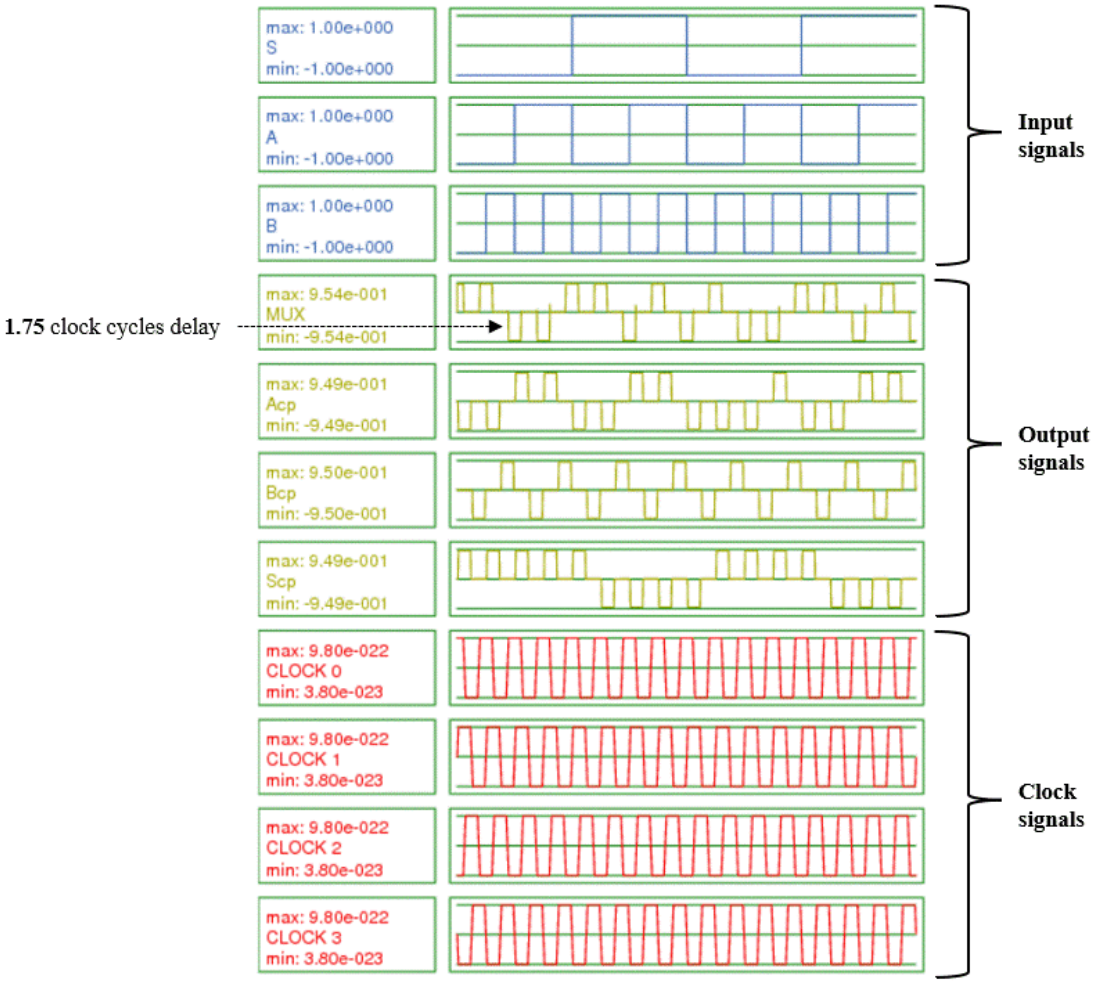



**Figure 3.13 Simulation waveforms of the proposed reversible time synchronised 2:1 multiplexer design.**

### 3.2.6. Reversible QCA 1:2 demultiplexer simulation

Figure 3.14 shows the simulation waveforms for the proposed reversible, time-synchronised 1:2 demultiplexer, whose design is given in Figure 3.6. The input/output simulation results validate the desired circuit computation, and the response agrees with Table 3.6. The output Y0 experiences a delay of three clock zones (0.75 clock cycles), whereas Y1 experiences a latency of five clock zones (1.25 clock cycles). Additionally, the design requires an area of 0.09 µm², utilises 51 QCA cells, and employs 7 USE clocking tiles.

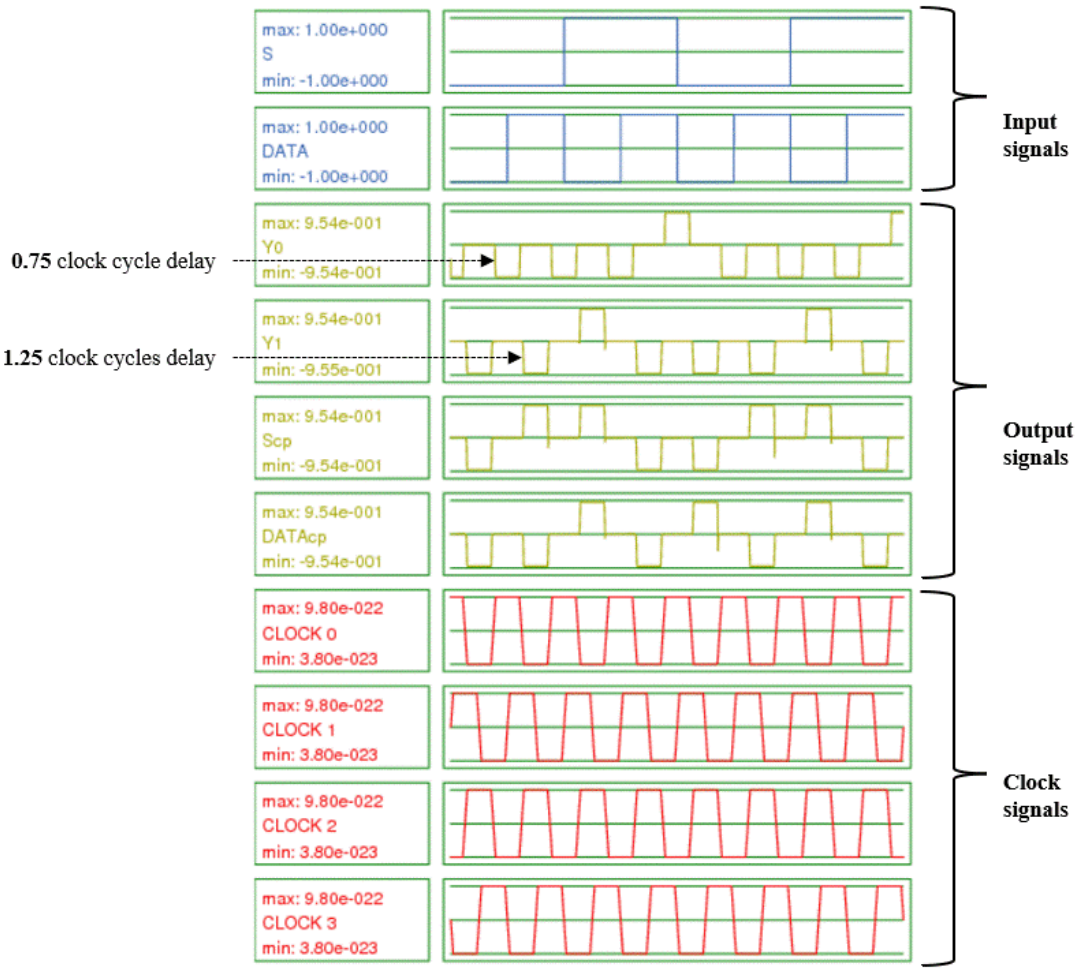



**Figure 3.14 Simulation waveforms of the proposed reversible time synchronised 1:2 demultiplexer design.**

### 3.2.7. Reversible QCA 1-bit comparator simulation

Figure 3.15 shows the simulation waveforms of the proposed reversible, time-synchronised comparator, as given in Figure 3.7. The input/output results confirm the circuit functionality. Moreover, the simulation results align with the truth table values illustrated in Table 3.7. This circuit takes two binary inputs, A and B. If the output A is less than B, the circuit takes three clock zones (0.75 clock cycles). In cases where A is greater than B, the circuit takes six clock zones (1.5 clock cycles). Finally, when A equals B, the circuit is delayed by eight clock zones (2 clock cycles). Furthermore, the design requires an area of 0.15 µm², utilises 107 QCA cells, and employs 14 USE clocking tiles.

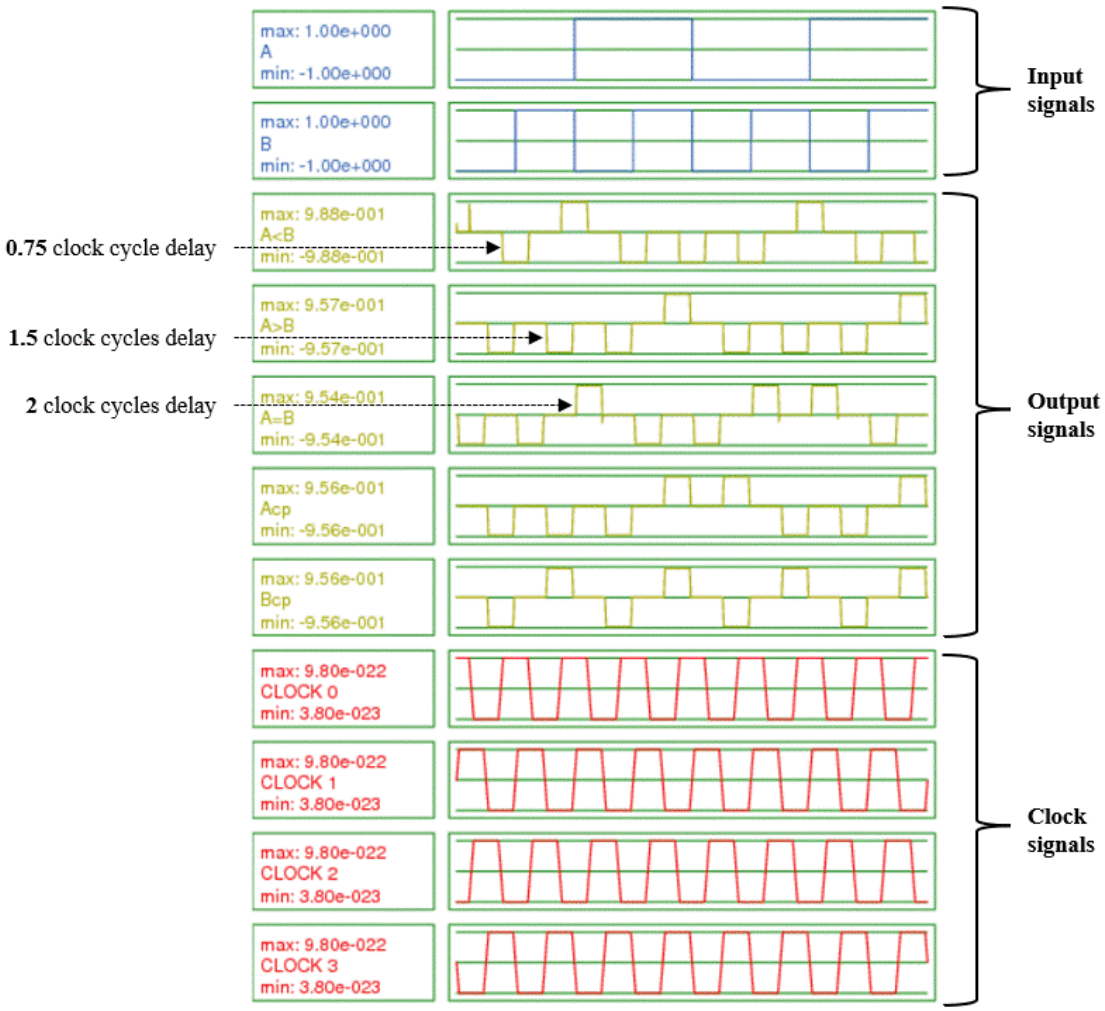



**Figure 3.15 Simulation waveforms of the proposed reversible time synchronised comparator design.**

### 3.2.8. Reversible QCA 2:4 decoder simulation

Figure 3.16 demonstrates the simulation results for the proposed reversible, time-synchronised QCA 2:4 decoder circuit showen in Figure 3.8. The input/output waveforms obtained show that the circuit works as expected and that the simulation results exhibit the correct logical behaviour, as shown in Table 2.1. This circuit takes two input numbers, A and B, in binary form, and gives output D3 after three clock zones (0.75 clock cycles), D2 after seven clock zones (1.75 clock cycles), D1 after 11 clock zones (2.75 clock cycles), and D0 after 13 clock zones (3.25 clock cycles). Furthermore, the design requires an area of 0.18 $\mu m^2$, utilises 126 QCA cells, and employs 19 USE clocking tiles.

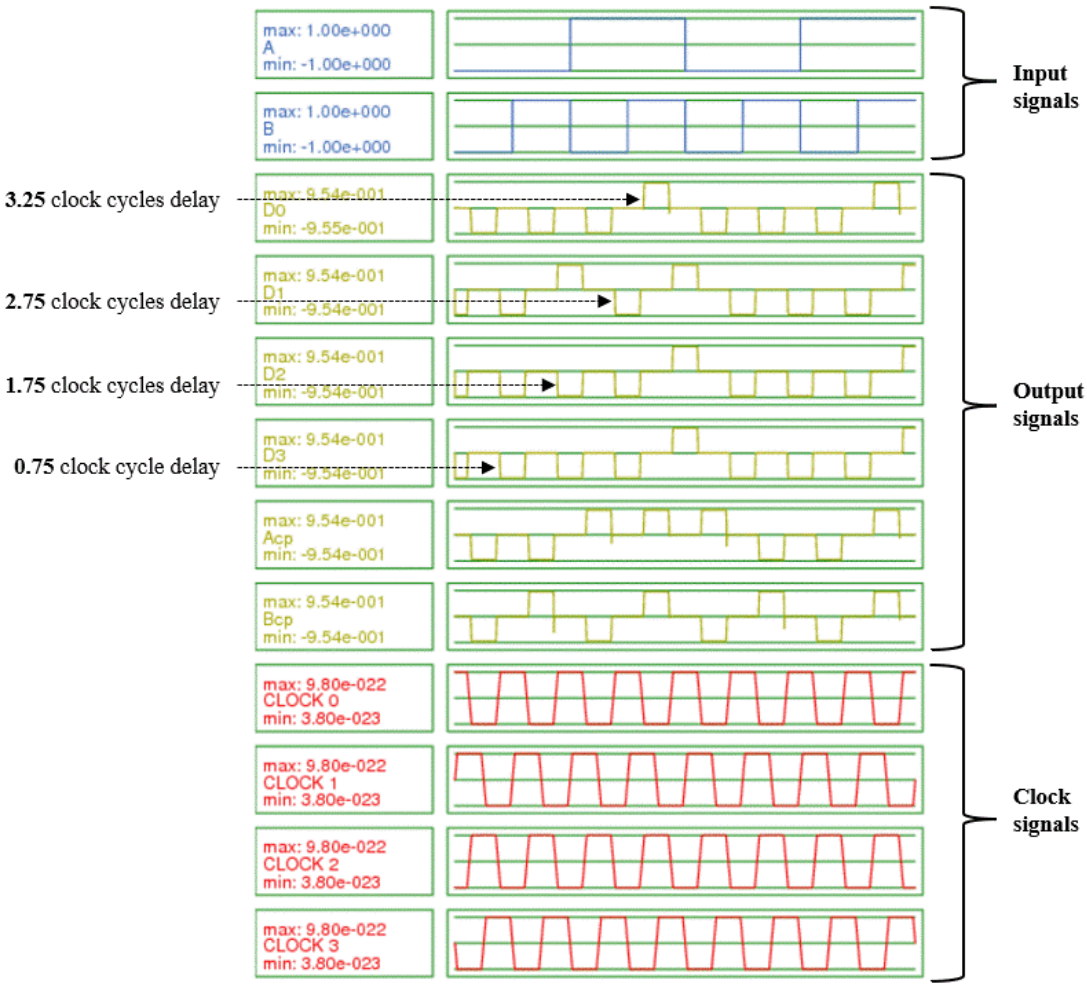



**Figure 3.16 Simulation waveforms of the proposed reversible time synchronised 2:4 decoder design.**

### 3.2.9. Summary of the reliability simulation of the circuits

The demonstrated input/output response waveforms for the eight proposed logically and physically reversible time-synchronised QCA circuits demonstrate that the time-synchronization feature plays a crucial role in guaranteeing the precision and correctness of the circuit's output values. By aligning operations within predefined clocking zones, this synchronisation ensures that signal transitions occur at the intended moments, mitigating timing-related errors and preventing information loss. This precise coordination across different stages of the circuit not only enhances operational accuracy but also optimises performance, by ensuring that all components function coherently, in a synchronised manner. As a result, the proposed designs maintain reliable output behaviour across a variety of input combinations, underscoring the robustness and stability of the

circuits. Furthermore, the time-synchronisation capability supports scalability, making these circuits suitable for integration into more complex QCA-based architectures, where precise timing is essential.

### 3.3. Area cost and delay time evaluation

Table 3.9 provides a detailed breakdown of the area cost and delay time for the proposed reversible, time-synchronised QCA circuits discussed in Section 3.1. The simulation results reveal that the largest circuit, the reversible time-synchronised QCA half-adder, requires an area of 0.21 μm². On the other hand, the smallest circuit, the demultiplexer, has an area cost of just 0.09 μm². Additionally, the results showed that the demultiplexer, the circuit with the least delay, is delaying only five clock zones, equivalent to 1.25 clock cycles. On the other hand, the decoder, the most delayed circuit, is delayed by 13 clock zones, equivalent to 3.25 clock cycles.

**Table 3.9 Area cost and delay time for the proposed reversible and synchronous QCA designs.**

| Proposed reversible and synchronous QCA circuit | Area cost | | | Delay [clock zones] |
|---|---|---|---|---|
| | QCA cells | USE tiles[1] | Area space (μm²) | |
| XOR | 101 | 13 | 0.15 | 8 |
| XNOR | 101 | 13 | 0.15 | 8 |
| Half-adder | 139 | 19 | 0.21 | 12 |
| Half-subtractor | 106 | 14 | 0.15 | 8 |
| 2:1 multiplexer | 96 | 12 | 0.14 | 7 |
| 1:2 demultiplexer | 51 | 7 | 0.09 | 5 |
| Comparator | 107 | 14 | 0.15 | 9 |
| 2:4 decoder | 126 | 19 | 0.18 | 13 |

1 Each tile contains 5 × 5 QCA cells measuring 18 × 18 nm; the spacing between the cells equals 2 nm.

The demonstrated results show that implementing the logically and physically reversible, time-synchronized design method yields highly efficient QCA combinatorial circuits.

### 3.4. Energy dissipation simulation

Table 3.10 outlines the energy dissipation values for the eight proposed reversible, time-synchronised QCA combinational logic circuits. The energy dissipation values for

each binary input signal combination are expressed in millielectronvolts (meV). The *QCADesigner-E 2.2* [96] TCAD tool was used to evaluate the energy dissipation for the circuits employing the technology and simulation parameters detailed earlier in Table 2.1 and Table 2.2, respectively.

**Table 3.10 Energy dissipation values for the proposed reversible and synchronous QCA designs.**

| Proposed reversible and synchronous QCA circuit | Energy Dissipation for input signal combinations [meV] | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **000** | **001** | **010** | **011** | **100** | **101** | **110** | **111** |
| XOR | 0.014 | 0.014 | 0.013 | 0.013 | | | | |
| XNOR | 0.014 | 0.013 | 0.014 | 0.014 | | | | |
| Half-adder | 0.027 | 0.018 | 0.027 | 0.027 | | | | |
| Half-subtractor | 0.014 | 0.021 | 0.014 | 0.014 | | | | |
| 2:1 multiplexer | 0.014 | 0.014 | 0.014 | 0.014 | 0.014 | 0.014 | 0.014 | 0.014 |
| 1:2 demultiplexer | 0.006 | 0.006 | 0.006 | 0.006 | | | | |
| Comparator | 0.014 | 0.024 | 0.015 | 0.015 | | | | |
| 2:4 decoder | 0.015 | 0.024 | 0.024 | 0.024 | | | | |

The simulation results indicate that, across all input signal combinations, energy dissipation consistently remains below the Landauer energy limit of 0.06 meV at a temperature of 1 K. This low dissipation level highlights the efficiency of the logical and physical reversibility feature in enabling QCA combinational circuits to achieve near-zero energy consumption

### 3.5. Conclusion

This chapter has presented logically and physically reversible, time-synchronised designs for eight combinational digital circuits using QCA technology. The USE clocking scheme was implemented, with simulations performed using the *QCADesigner 2.0.3* and *QCADesigner-E 2.2* TCAD tools. QCADesigner was used to simulate the polarisation input/output waveform responses, while QCADesigner-E was employed to extend the analysis by incorporating energy dissipation for the same QCA designs. Both tools utilise a microscopic quantum mechanical model of the QCA cell, with QCADesigner-E featuring an additional relaxation to equilibrium theoretical density matrix treatment, in the mathematical model, to account for energy dissipation.

The proposed logically and physically reversible QCA combinational digital circuit designs, which exhibit intrinsic time-synchronisation, include XOR and XNOR gates, as well as a half-adder, a half-subtractor, a 2:1 multiplexer, a 1:2 demultiplexer, a 1-bit comparator, and a 2:4 decoder. These designs exploit the inherent advantages of QCA technology to ensure coordinated operations across all circuit stages, enhancing both performance and reliability.

The simulation results confirm the feasibility of designing sophisticated QCA circuits that are both logically and physically reversible, while maintaining precise time synchronisation. The proposed circuits demonstrate ultralow energy dissipation, with levels consistently below the Landauer limit of 0.06 meV, at a temperature of 1 K. This minimal energy dissipation highlights the efficiency of the logically and physically reversible feature in minimising power consumption, making these circuits ideal for applications where energy efficiency is critical. Moreover, the combination of logical and physical reversibility with synchronised operation ensures the reliability of the circuit outputs. This reliability supports scalability, enabling seamless integration into more complex QCA-based systems.

### 3.6. Contribution

This chapter highlights innovative advancements in the design and simulation of time-synchronised, reversible combinational logic circuits, with exceptionally low energy dissipation. The findings presented in this chapter have the potential to make a significant contribution to ongoing research in power-efficient QCA-based combinational digital circuits, paving the way for future developments in low-energy nanoscale computing systems.

A peer-reviewed article titled “Design and Simulation of Reversible Time-Synchronised Quantum-Dot Cellular Automata Combinational Logic Circuits with Ultralow Energy Dissipation” was published based on the research findings presented in this chapter [32]. It appeared in the September 2022 edition of The *International Transaction Journal of Engineering, Management, & Applied Sciences & Technologies* (see Figure 3.17).



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# Design and Simulation of Reversible Time-Synchronized Quantum-Dot Cellular Automata Combinational Logic Circuits with Ultralow Energy Dissipation

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## Abstract

The quantum-dot cellular automata (QCA) represent emerging nanotechnology that is poised to supersede the current complementary metal-oxide-semiconductor digital integrated circuit technology. QCA constitutes an extremely promising transistor-less paradigm that can be downscaled to the molecular level, thereby facilitating tera-scale device integration and extremely low energy dissipation. Reversible QCA circuits, which have reversibility sustained down from the logical level to the physical level, can execute computing operations dissipating less energy than the Landauer energy limit (kBTln2). Time synchronization of logic gates is an essential additional requirement, especially in cases involving complex circuits, for ensuring accurate computational results. This paper reports the design and simulation of eight new both logically and physically reversible time-synchronized QCA combinational logic circuits. The new circuit design presented here mitigates the clock delay problems, which are caused by the non-synchronization of logic gate information, via the use of an inherently more symmetric circuit configuration. The simulation results confirm the behaviour of the proposed reversible time-synchronized QCA combinational logic circuits which exhibit ultralow energy dissipation and simultaneously provide accurate computational results.

**Discipline**: Electrical Engineering



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**Figure 3.17 Article paper: Design and simulation of reversible time-synchronized QCA combinational logic circuits with ultralow energy dissipation**

# Chapter 4

## 4. Reversible QCA Sequential Flip-Flop Circuits

Flip-flop circuits are crucial components in digital electronics, functioning as fundamental memory elements and essential parts of sequential digital circuits [154]. The flip-flop output is dependent on instantaneous input and feedback [154]. The feedback characteristic allows flip-fop circuits to store binary data [154]. The progression of flip-flop designs is from the fundamental SR (Set-Reset) flip-flop to the more sophisticated forms, such as D (Data), T (Toggle), and JK (Jack Kilby) flip-flops [155, 156]. Applications for these flip-flop circuits include data storage, computing, synchronisation, and data transfer [154]. Conventional flip-flop circuits often use CMOS technology [30]. The industry favours CMOS technology due to its low power consumption and high reliability [3]. However, as technology scales down, CMOS-based systems encounter constraints, particularly in terms of power dissipation and switching speed [157].

This chapter uses the innovative logically and physically reversible, time-synchronised design approach from Chapter 2 to develop novel ultra-energy-efficient QCA sequential flip-flop circuits. These circuits include the most common types of flip-flops, including the SR, D, T, and JK flip-flops. In addition, novel ultra-cost-efficient irreversible QCA designs for the same flip-flop circuits have also been developed to enable a meaningful comparison. The same design rules are applied to both the reversible and irreversible circuits, ensuring the reliability and consistency of the comparison. The tile-based design concept's [158] principles guide the implementation of the designs. Several studies have used this concept to support automated QCA design integration [159, 160]. The USE clocking scheme, in conjunction with the tile-based design concept, is employed to manage the timing of the circuits. The wire crossing issue, which causes crosstalk interference between intersecting wires, is addressed by implementing the multilayer crossing approach [72]. The crossing points necessitate the use of three distinct layers.

Although reversible sequential QCA flip-flop circuits consume less energy than the Landauer limit, irreversible QCA flip-flop circuits sometimes require less area and time. This chapter comprehensively explores the trade-offs between reversible and irreversible sequential QCA flip-fops in terms of energy loss, area used, delay time, and overall cost.

## 4.1. Designing sequential QCA flip-flop circuits

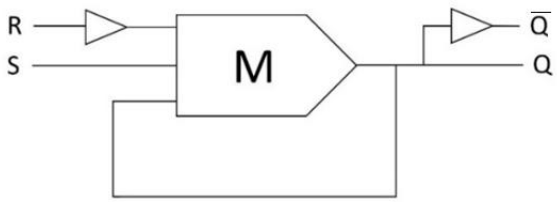
### 4.1.1. Designing QCA SR flip-flop circuits

The SR flip-flop circuit is a single-bit data storage device that can store one binary digit (either 0 or 1) and operates in active-high mode. It detects that the output is SET when $S = 1$ and $R = 0$, or RESET when $R = 1$ and $S = 0$. Equation 4.1 presents an identical Boolean expression for both the reversible and irreversible configurations of the QCA SR flip-flop circuit.

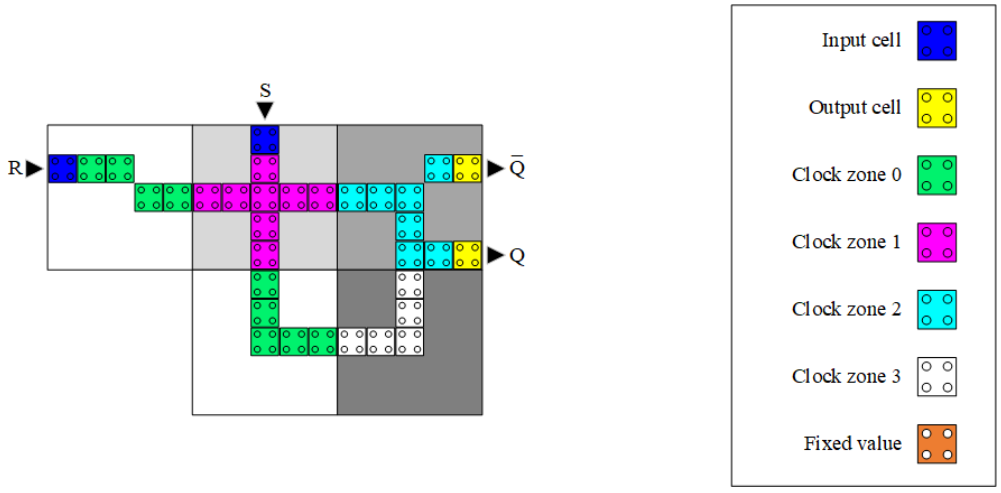
$$Q_{(t)} = M\left(S, \bar{R}, Q_{(t-1)}\right) = S.\bar{R} + S.Q_{(t-1)} + \bar{R}.Q_{(t-1)} \tag{4.1}$$

#### 4.1.1.1. Irreversible QCA SR flip-flop design

The proposed irreversible QCA SR flip-flop uses a single irreversible majority gate and two inverters. Figure 4.1a shows the design's synthesis, while Figure 4.1b shows the circuit layout together with the colour-coded USE clocking scheme. This irreversible QCA SR flip-flop features two inputs: *S*, which triggers the SET function, and *R*, which triggers the RESET function. The output labelled $Q$ stores the current bit, while $\bar{Q}$ ($Q$ complement) displays the binary inverse of $Q$. The circuit operates with a delay of three clock zones, equivalent to 0.75 clock cycles. Using the standard technological parameters presented in Table 2.1, the design is remarkably area-efficient, requiring only an area of 0.06 µm², utilising 33 QCA cells, and employing 5 USE tiles.




(a)




(b)

**Figure 4.1 (a) Logical synthesis design and (b) physical QCA layout of the proposed irreversible QCA SR flip-flop.**

Table 4.1 presents the truth table for the irreversible QCA SR flip-flop which has the standard Input/Output form for a SR flip-flop. This table maps the various input conditions, SET and RESET, to their corresponding outputs, $Q$ and $\bar{Q}$, illustrating the irreversible QCA SR flip-flop's behaviour under various scenarios.

**Table 4.1 Truth table for irreversible SR flip-flop circuit shown in Figure 4.1.**

| Input | | Output | | Description |
|---|---|---|---|---|
| $S$ | $R$ | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | |
| 0 | 0 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | Hold state |
| 0 | 1 | 0 | 1 | Reset |
| 1 | 0 | 1 | 0 | Set |
| 1 | 1 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | Hold state |

#### 4.1.1.2. Reversible QCA SR flip-flop design

The innovative reversible QCA SR flip-flop circuit design utilises only a single reversible majority gate and two inverters to store a bit of data. Figure 4.2a presents the design synthesis, while Figure 4.2b illustrates the circuit QCA layout, implemented using the USE clocking scheme. In the design diagrams of the reversible QCA SR flip-flop, the output labels marked "cp" represent copies of the input data. The reversible QCA SR flip-flop shares similar delay characteristics with its irreversible counterpart, presented in

Section 4.1.1.1, operating with a delay of three clock zones (0.75 clock cycles). Additionally, the design occupies the same 0.06 μm² area and employs five USE clocking tiles. However, it requires a slightly higher number of QCA cells, utilising 37 in total.

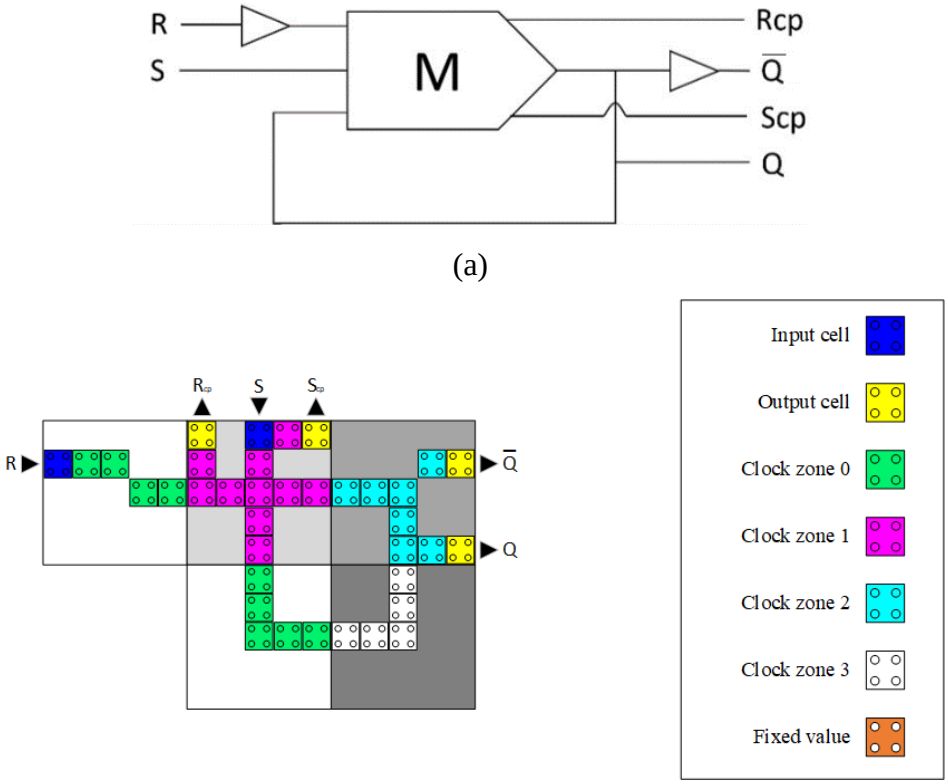



**Figure 4.2 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA SR flip-flop ($S_{cp}$ and $R_{cp}$ indicate copies of the inputs).**

Table 4.2 presents the truth table for the innovative reversible QCA SR flip-flop. This table maps the various input conditions, SET and RESET, to their corresponding outputs, $Q$ and $\bar{Q}$, illustrating the reversible QCA SR flip-flop's behaviour under various scenarios.

**Table 4.2 Truth table for reversible SR flip-flop circuit shown in Figure 4.2 with copies of the two inputs passed to the two additional outputs.**

| Input | | Output | | | | Description |
|---|---|---|---|---|---|---|
| $S$ | $R$ | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | $S_{cp}$ | $R_{cp}$ | |
| 0 | 0 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | 0 | 0 | Hold state |
| 0 | 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 0 | 1 | 0 | 1 | 0 | Set |
| 1 | 1 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | 1 | 1 | Hold state |

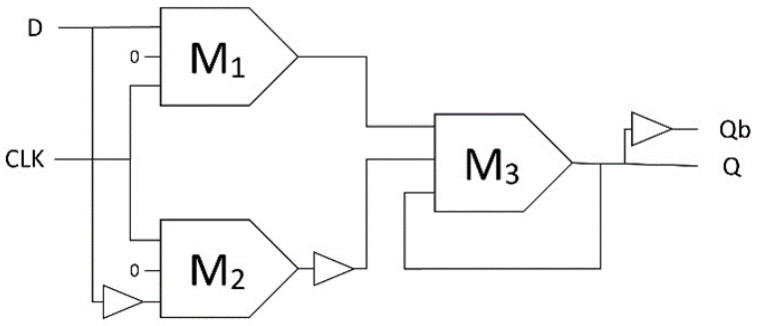
### 4.1.2. Designing QCA D flip-flop circuits

The QCA D flip-flop, where *D* represents the data input, is controlled by a clock signal *CLK*. By combining the two input signals, *S* and *R*, of the SR flip-flop and incorporating an inverter, we can set and reset the flip-flop using only one input, as *S* and *R* are complementary. This complementary configuration avoids the forbidden state of the SR flip-flop, when *S* and *R* both equal to 1 at the same time. Equation 4.2 provides the Boolean expression for the QCA D flip-flop, where *D* represents the input data, *CLK* is the clock signal, and *Q* is the output that stores the data.

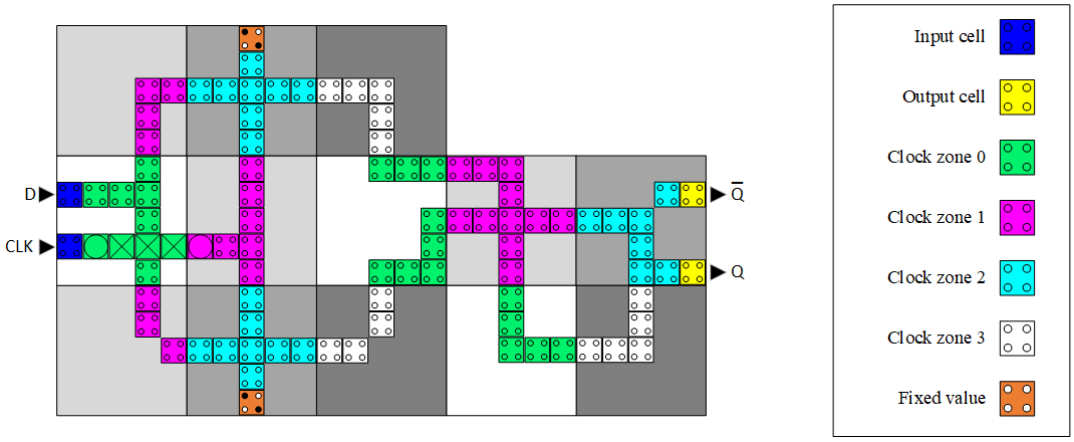
$$\begin{aligned} M_1 &= M(D, CLK, 0) \\ M_2 &= M(\overline{D}, CLK, 0) \\ M_3 &= M\left(M_1, \overline{M_2}, Q_{(t-1)}\right) \\ Q_{(t)} &= M\left(M\,(D, CLK, 0), \overline{M\left(\overline{D}, CLK, 0\right)}, Q_{(t-1)}\right) = D.CLK + \overline{CLK}.Q_{(t-1)} \end{aligned} \tag{4.2}$$

#### 4.1.2.1. Irreversible QCA D flip-flop design

The proposed irreversible QCA D flip-fop circuit is designed using three irreversible majority gates and three inverters to store a single binary digit. Accordingly, the output is SET when *CLK* = 1 and *D* = 1, RESET when *CLK* = 1 and *D* = 0, and HOLD data (no change) when *CLK* = 0. Figure 4.3a demonstrates the synthesis of the proposed irreversible QCA D flip-fop design, and Figure 4.3b shows the circuit QCA layout. The circuit delay is seven clock zones (1.75 clock cycle). Furthermore, this irreversible QCA D flip-fop circuit requires an area of 0.17 μm², utilises 91 QCA cells, and employs 13 USE clocking tiles.




(a)




(b)

**Figure 4.3 (a) Logical synthesis design and (b) physical QCA layout of the proposed irreversible QCA D flip-flop.**

Table 4.3 presents the truth table for the novel irreversible QCA D flip-flop, giving details for the circuit's logical behaviour under various combinations of clock and data inputs. The table clearly illustrates the response of the output *Q*, which sets when both the clock *CLK* and data *D* inputs are high, resets when the clock is high, and the data input is low and maintains its previous state, when the clock input is low. This truth table is crucial for understanding the operational dynamics and verifying the correct functionality of the irreversible QCA D flip-flop, within a digital circuit.

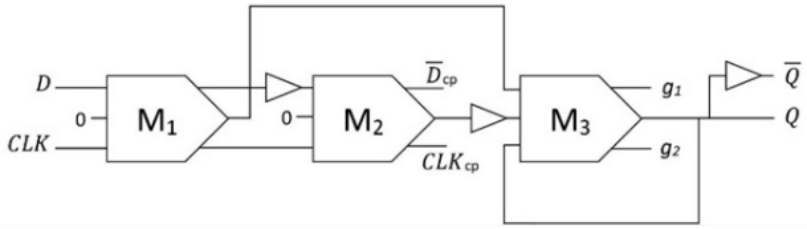
**Table 4.3 Truth table for irreversible D flip-flop circuit shown in Figure 4.3.**

| **Input** | | **Output** | | **Description** |
|---|---|---|---|---|
| ***CLK*** | ***D*** | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | |
| 0 | 0 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | Hold |
| 0 | 1 | | | |
| 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 1 | 0 | Set |

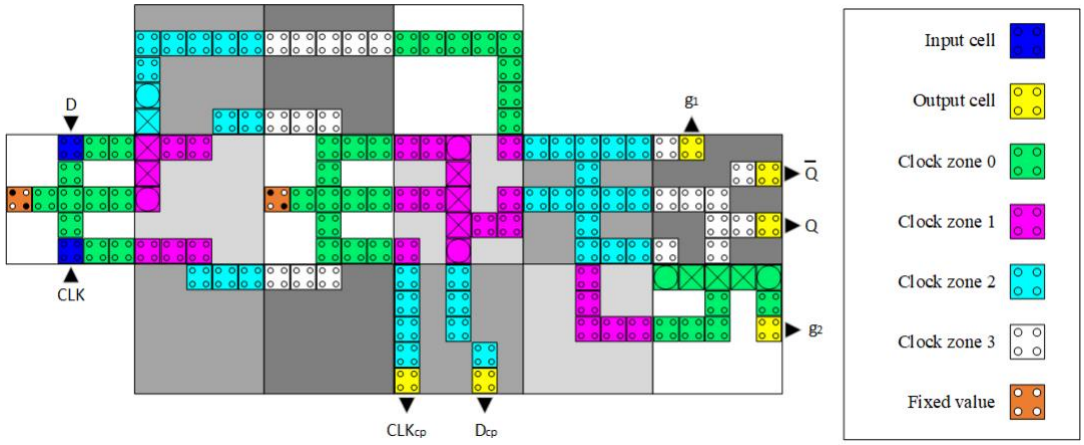
#### 4.1.2.2. Reversible QCA D flip-flop design

The innovative reversible QCA D flip-flop circuit uses three reversible majority gates and three inverters to store data. Figure 4.4a presents the design synthesis, while Figure 4.4b illustrates the circuit QCA layout, implemented using the USE clocking scheme. In the design diagrams of the reversible QCA D flip-flop, the output labels marked "cp" represent copies of the input data, while "g" denotes the so-called garbage outputs. The

reversible QCA D flip-flop operates with a delay of eight clock zones (2 clock cycles). Additionally, the design occupies an area of 0.19 µm² area, requires 136 QCA cells, and employs 14 USE clocking tiles.




(a)




(b)

**Figure 4.4 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA D flip-flop ($D_{cp}$ and $CLK_{cp}$ indicate copies of the inputs, while $g_1$ and $g_2$ are so-called garbage outputs)**

Table 4.4 presents the truth table for the novel reversible QCA D flip-flop, providing a comprehensive overview of the circuit's logical behaviour under various input conditions.

**Table 4.4 Truth table for reversible D flip-flop circuit shown in Figure 4.4.**

| Input | | Output | | | | Description |
|---|---|---|---|---|---|---|
| $CLK$ | $D$ | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | $CLK_{cp}$ | $D_{cp}$ | |
| 0 | 0 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | 0 | 0 | Hold |
| 0 | 1 | | | 0 | 1 | |
| 1 | 0 | 0 | 1 | 1 | 0 | Reset |
| 1 | 1 | 1 | 0 | 1 | 1 | Set |

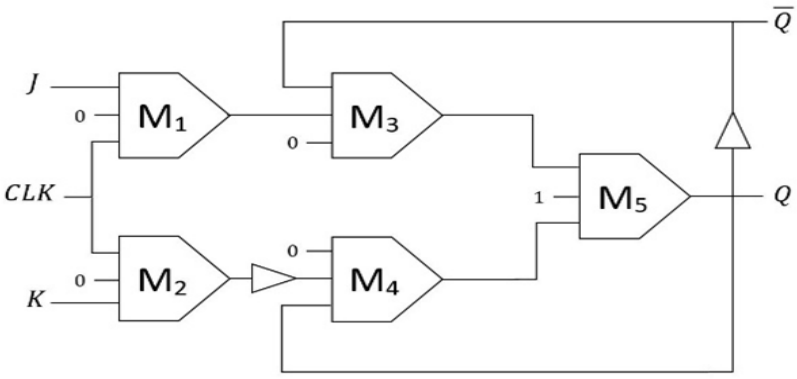
### 4.1.3. Designing QCA JK flip-flop circuits

The JK flip-flop behaves similarly to the SR flip-flop, where *J* is corresponds to the *S* input and *K* corresponds to the *R* input. A control clock signal supplements the JK flip-flop, producing a toggle output value when *CLK* = 1, *J* = 1, and *K* = 1. Accordingly, the output is SET when *CLK* = 1, *J* = 1, and *K* = 0, RESET when *CLK* = 1, *J* = 0, and *K* = 1, and hold data (no change) when *CLK* = 0, or when *J* = 0 and *K* = 0, even if *CLK* = 1. Equation 4.3 provides the Boolean expression for the QCA JK flip-flop designs, where *J* and *K* represent the input data, *CLK* represents the clock data, and *Q* represents the stored bit.

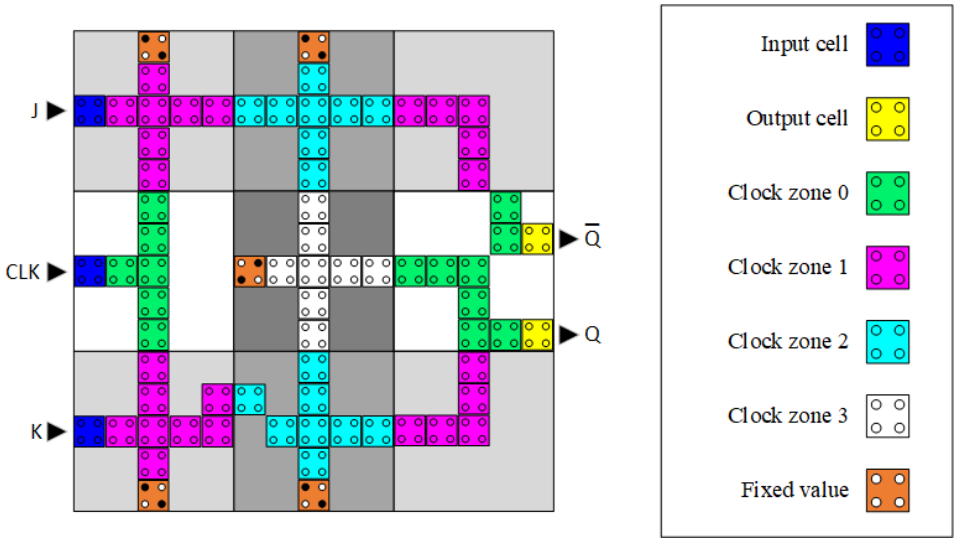
$$\begin{gathered} M_1 = M(J, 0, KLC) \\ M_2 = M(\ K, 0, CLK) \\ M_3 = M\ (M_1, 0, \overline{Q}_{(t\text{-}1)}) \\ M_4 = M\ (\overline{M}_2, 0, Q_{(t\text{-}1)}) \\ M_5 = M\ (M_3, 1, M_4) \\ Q(t) = M\ (M\ (M\ (J, 0, CLK), 0, \overline{Q}_{(t-1)}), 1, M\ (\overline{M\ (K, 0, CLK)}, 0, Q_{(t-1)})) \\ = J.CLK.\overline{Q}_{(t-1)} + (\overline{K.CLK}).Q_{(t-1)} \end{gathered} \tag{4.3}$$

#### 4.1.3.1. Irreversible QCA JK flip-flop design

The proposed irreversible QCA JK flip-fop circuit is designed using five irreversible majority gates and two inverters to store a single bit of data. Figure 4.5a demonstrates the synthesis design of the developed irreversible QCA JK flip-flop circuit, and Figure 4.5b shows the circuit layout. The circuit delay is five clock zones (1.25 clock cycle). Furthermore, this irreversible QCA JK flip-fop circuit requires an area of 0.11 μm², utilises 74 QCA cells, and employs 9 USE clocking tiles.




(a)




(b)

**Figure 4.5 (a) Logical synthesis design and (b) physical QCA layout of the proposed irreversible QCA JK flip-flop.**

Table 4.5 presents the truth table for the novel irreversible QCA JK flip-flop, offering a detailed analysis of the circuit's logical behaviour, across different combinations of clock *CLK* and data inputs *J* and *K*. This table is critical for understanding how the JK flip-flop operates in various scenarios, including setting, resetting, toggling, and holding the output *Q*. The truth table specifically outlines how the output responds when both *J* and *K* inputs are active, when they are individually high or low, and how the clock signal influences these transitions. By illustrating these input-output relationships, the truth table serves as an essential reference for verifying the functionality and reliability of the proposed QCA JK flip-flop circuit.

**Table 4.5 Truth table for irreversible JK flip-flop circuit shown in Figure 4.5.**

| Input | | | Output | | Description |
|---|---|---|---|---|---|
| ***CLK*** | ***J*** | ***K*** | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | |
| 0 | X | X | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | Hold |
| 1 | 0 | 0 | | | |
| 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 1 | 0 | 1 | 0 | Set |
| 1 | 1 | 1 | $\bar{Q}_{(t-1)}$ | $Q_{(t-1)}$ | Toggle |

#### 4.1.3.2. Reversible QCA JK flip-flop design

The innovative reversible JK flip-flop circuit utilises five reversible majority gates and two inverters to store data efficiently. Figure 4.6a presents the design synthesis, while Figure 4.6b illustrates the circuit layout, implemented using the USE clocking scheme. In the design diagrams of the reversible QCA JK flip-flop, the output labels marked "cp" represent copies of the input data, while "g" denotes the so-called garbage outputs. The circuit delay is seven clock zones (1.75 clock cycle). Additionally, the design occupies an area of 0.23 μm², requires 149 QCA cells, and employs 13 USE clocking tiles.

Table 4.6 presents the truth table for the reversible QCA JK flip-flop, providing a comprehensive analysis of the circuit's logical behaviour, under various combinations of clock *CLK* and data inputs *J* and *K*. This table elucidates how the reversible QCA JK flip-flop operates, highlighting its ability to handle different input scenarios, including setting, resetting, toggling, and maintaining the output *Q*.

**Table 4.6 Truth table for reversible JK flip-flop circuit shown in Figure 4.6.**

| Input | | | Output | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|
| ***CLK*** | ***J*** | ***K*** | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | $CLK_{cp}$ | $J_{cp}$ | $K_{cp}$ | $Q_{cp}$ | $\bar{Q}_{cp}$ | |
| 0 | X | X | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | 0 | X | X | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | Hold |
| 1 | 0 | 0 | | | 1 | 0 | 0 | | | |
| 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Set |
| 1 | 1 | 1 | $\bar{Q}_{(t-1)}$ | $Q_{(t-1)}$ | 1 | 1 | 1 | $\bar{Q}_{(t-1)}$ | $Q_{(t-1)}$ | Toggle |

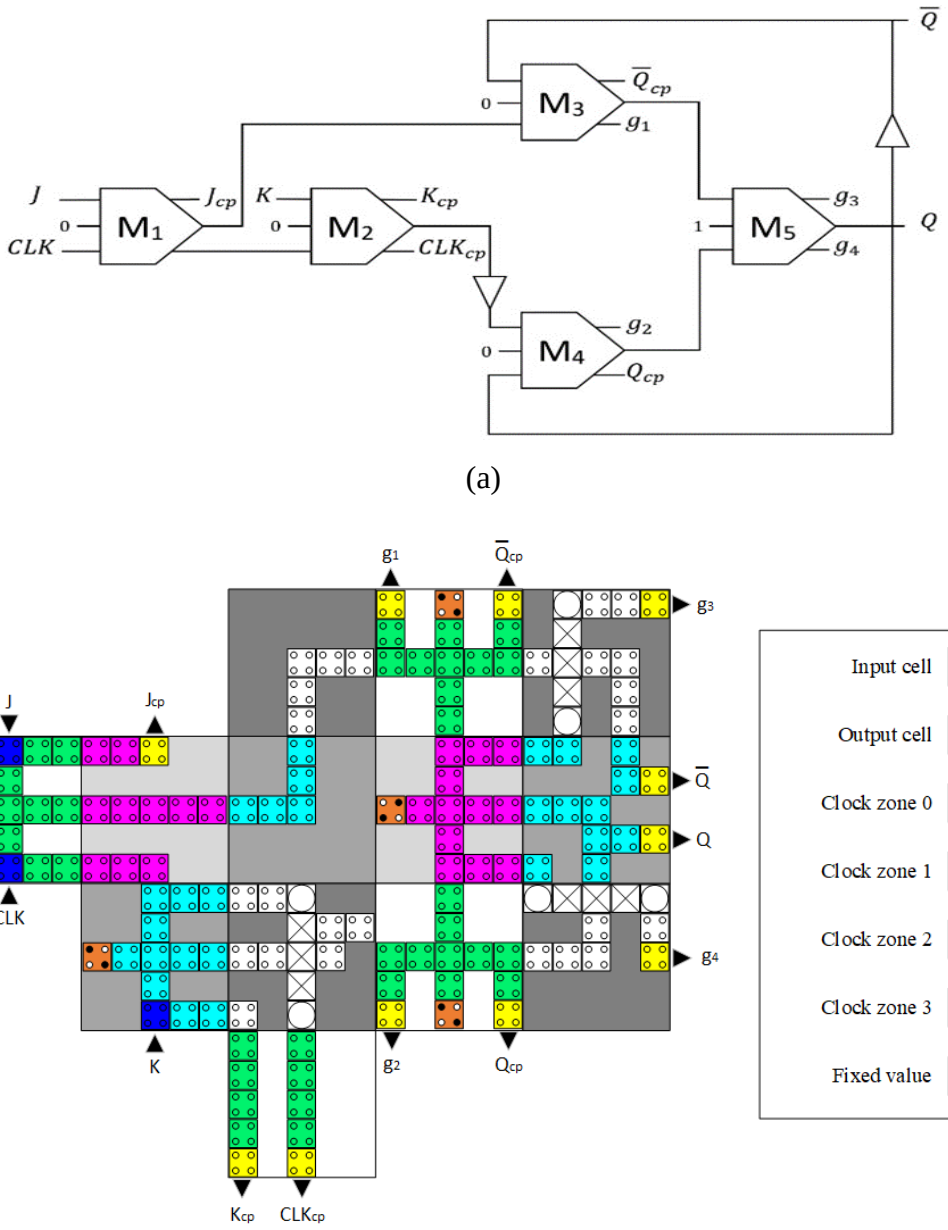



**Figure 4.6 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA JK flip-flop ($J_{cp}$, $K_{cp}$, $KLC_{cp}$, $Q_{cp}$, and $\overline{Q}_{cp}$ indicate copies of the inputs, while $g_1$, $g_2$, $g_3$, and $g_4$ are so-called garbage outputs).**

### 4.1.4. Designing QCA T flip-flop circuits

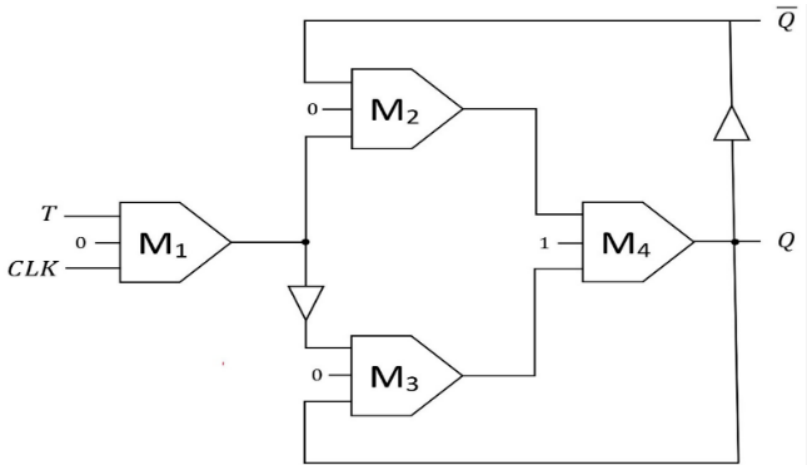
The QCA T flip-flop circuits are based on the JK flip-flop architecture, but with a simpler layout. The T flip-flop combines the JK flip-flop's two inputs by connecting a single input, labelled *T*, to both inputs. The input, *T*, acts as a toggle control, allowing the

flip-flop to function as a toggle switch. The T flip-flop switches between states when both the clock signal *CLK* and the toggle input *T* are in a high state, i.e., CLK = 1 and T = 1. Otherwise, the output remains the same. Equation 4.4 shows the Boolean expression for the QCA T flip-flop designs. In this equation, *T* represents the input, *CLK* represents the clock signal, and *Q* represents the stored output bit.

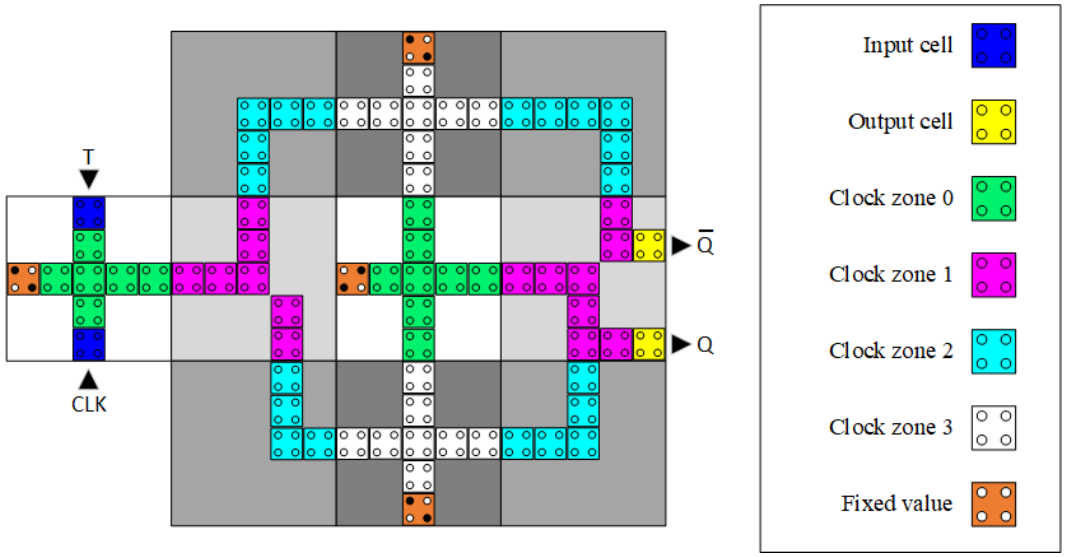
$$
\begin{aligned}
M_1 &= M\ (T, 0, CLK) \\
M_2 &= M\ (M_1, 0, \overline{Q}_{(t-1)}) \\
M_3 &= M\ (\overline{M}_1, 0, Q_{(t-1)}) \\
M_4 &= M\ (M_2, 1, M_3) \\
Q_{(t)} &= M\ (M\ (M\ (T, 0, CLK), 0, \overline{Q}_{(t-1)}), 1, M\ (\overline{M\ (T, 0, CLK)}, 0, Q_{(t-1)})) \\
&= T.CLK.\overline{Q}_{(t-1)} + \overline{T}.Q_{(t-1)} + \overline{CLK}.Q_{(t-1)}
\end{aligned}
\tag{4.4}
$$

#### 4.1.4.1. Irreversible QCA T flip-flop design

The proposed irreversible QCA T flip-flop circuit is designed using four irreversible majority gates and two inverters to store a single binary digit. This configuration ensures efficient and reliable operation within a compact design. The synthesis process of the irreversible QCA USE T flip-flop is illustrated in Figure 4.7a, providing a clear overview of the design logic. Figure 4.7b further details the circuit QCA layout, showing how the QCA design is implemented using the USE clocking scheme, which is essential for coordinating the signal flow and ensuring accurate timing within the circuit. The circuit operates with a delay of six clock zones, equivalent to 1.5 clock cycles, indicating a rapid response time suitable for high-speed digital applications. In terms of physical requirements, this irreversible QCA T flip-flop is designed to be highly area-efficient, occupying an area of just 0.13 μm². It makes use of 73 QCA cells, which are the fundamental building blocks of the circuit, and relies on 10 USE clocking tiles to manage the timing of operations effectively. Overall, this design represents a balance between performance and resource utilisation, making it an effective solution for applications where minimising delay and conserving area are critical considerations.




(a)




(b)

**Figure 4.7 (a) Logical synthesis design and (b) physical QCA layout of the proposed irreversible QCA T flip-flop.**

Table 4.7 presents the truth table for the conventional irreversible QCA T flip-flop, offering a comprehensive analysis of the circuit's logical behaviour under different combinations of clock *CLK* and data *T* inputs. This table provides a clear depiction of how the T flip-flop functions as a toggle switch, highlighting the conditions under which the output state *Q* changes. Specifically, the truth table details scenarios where the clock signal is high, demonstrating how the output toggles when the *T* input is also high, i.e., T = 1, and how it remains unchanged when the *T* input is low, i.e., T = 0. Conversely, when the clock signal is low, the table shows that the output remains stable, regardless of the *T* input. Understanding how to employ the QCA T flip-flop in digital circuits to efficiently

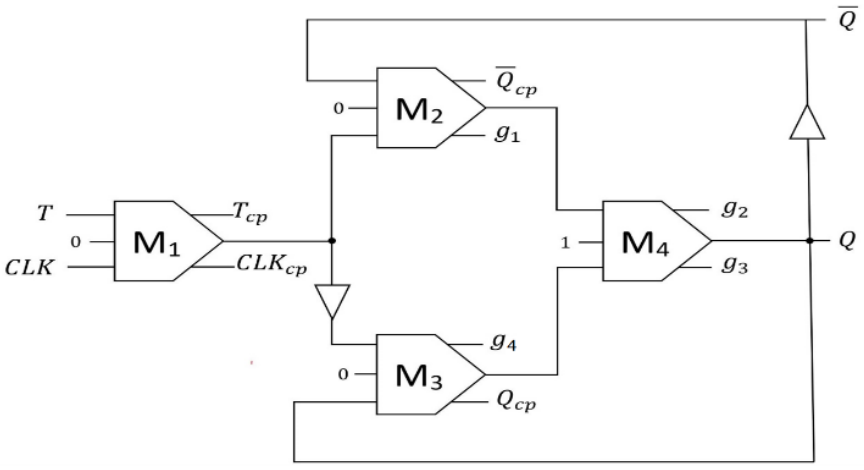
manage binary state changes, particularly in applications requiring a reliable toggling mechanism, requires a detailed breakdown.

**Table 4.7 Truth table for irreversible T flip-flop circuit shown in Figure 4.7.**

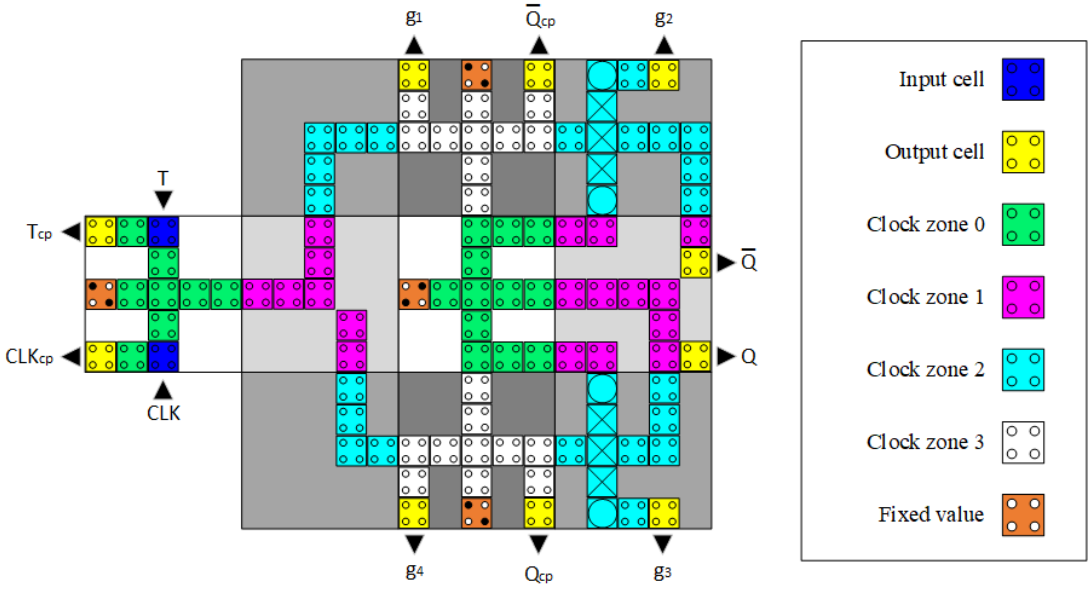
| Input | | Output | | Description |
|---|---|---|---|---|
| ***CLK*** | ***T*** | $Q_{(t)}$ | $\bar{Q}_{(t)}$ | |
| 0 | 0 | $Q_{(t-1)}$ | $\bar{Q}_{(t-1)}$ | Hold |
| 0 | 1 | | | |
| 1 | 0 | | | |
| 1 | 1 | 1 | 0 | Toggle |

#### 4.1.4.2. Reversible QCA T flip-flop design

The innovative reversible QCA T flip-flop circuit also uses four reversible majority gates and two inverters to store data. Figure 4.8a presents the design synthesis, while Figure 4.8b illustrates the circuit layout, implemented using the USE clocking scheme. In the design diagrams of the reversible QCA T flip-flop, the output labels marked "cp" represent copies of the input data, while "g" denotes the so-called garbage outputs. The reversible QCA T flip-flop operates with a delay of six clock zones (1.5 clock cycles), like the proposed irreversible ones. Additionally, the design occupies an area of 0.16 μm² area, requires 107 QCA cells, and employs 10 USE clocking tiles.




(a)




(b)

**Figure 4.8 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA T flip-flop ($T_{cp}$, $KLC_{cp}$, $Q_{cp}$, and $\overline{Q}_{cp}$ indicate copies of the inputs, while g1, g2, g3, and g4 are so-called garbage outputs).**

Table 4.8 presents the truth table for the innovative reversible QCA T flip-flop, offering a detailed overview of the circuit's logical behaviour under various input conditions. This table illustrates how the reversible QCA T flip-flop responds to different combinations of the clock *CLK* and toggle input *T*, highlighting its ability to toggle the output state or maintain the current state based on these inputs.

**Table 4.8 Truth table for reversible T flip-flop circuit shown in Figure 4.8.**

| **Input** | | **Output** | | | | | | **Description** |
|---|---|---|---|---|---|---|---|---|
| $\boldsymbol{CLK}$ | $\boldsymbol{T}$ | $\boldsymbol{Q_{(t)}}$ | $\boldsymbol{\overline{Q}_{(t)}}$ | $\boldsymbol{CLK_{cp}}$ | $\boldsymbol{T_{cp}}$ | $\boldsymbol{Q_{cp}}$ | $\boldsymbol{\overline{Q}_{(t)}}$ | |
| 0 | 0 | $Q_{(t-1)}$ | $\overline{Q}_{(t-1)}$ | 0 | 0 | $Q_{(t-1)}$ | $\overline{Q}_{(t-1)}$ | Hold |
| 0 | 1 | | | 0 | 1 | | | |
| 1 | 0 | | | 1 | 0 | | | |
| 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Toggle |

### 4.2. Reliability simulation

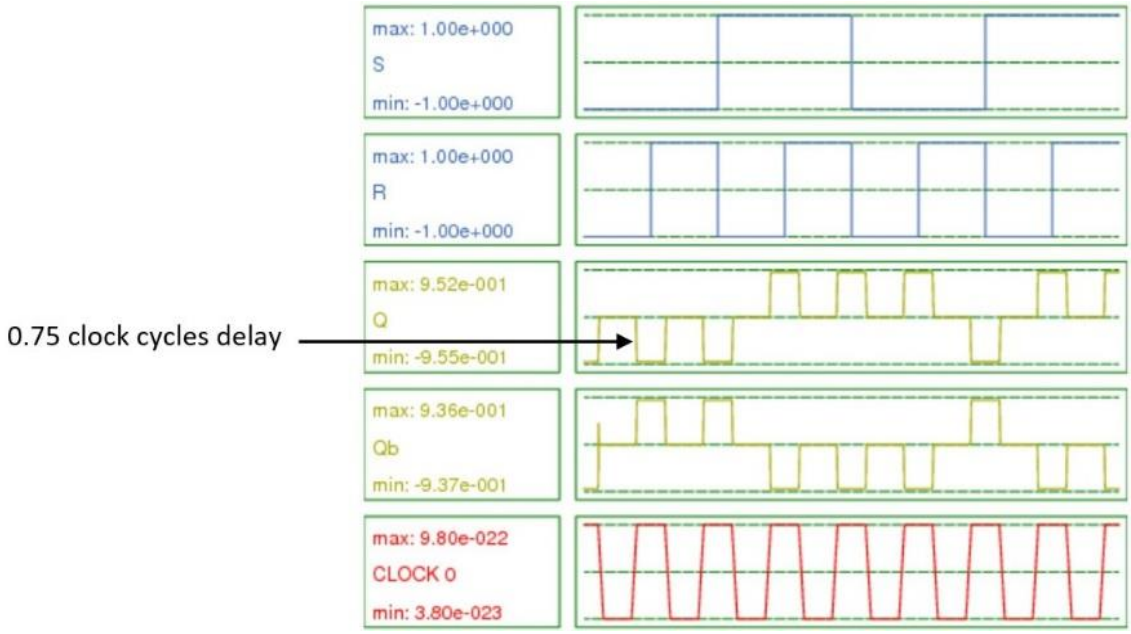
This section presents the simulated input/output response values for the eight proposed reversible and irreversible designs for the four flip-flop types under consideration, as detailed in Section 4.1. The performance of these circuits was validated using the

*QCADesigner 2.0.3* TCAD tool, utilising the technological and simulation parameters presented earlier in Table 2.1 and Table 2.2, respectively. For each flip-flop circuit, the simulation calculates the results and then displays waveforms representing the computational outputs and delay times.

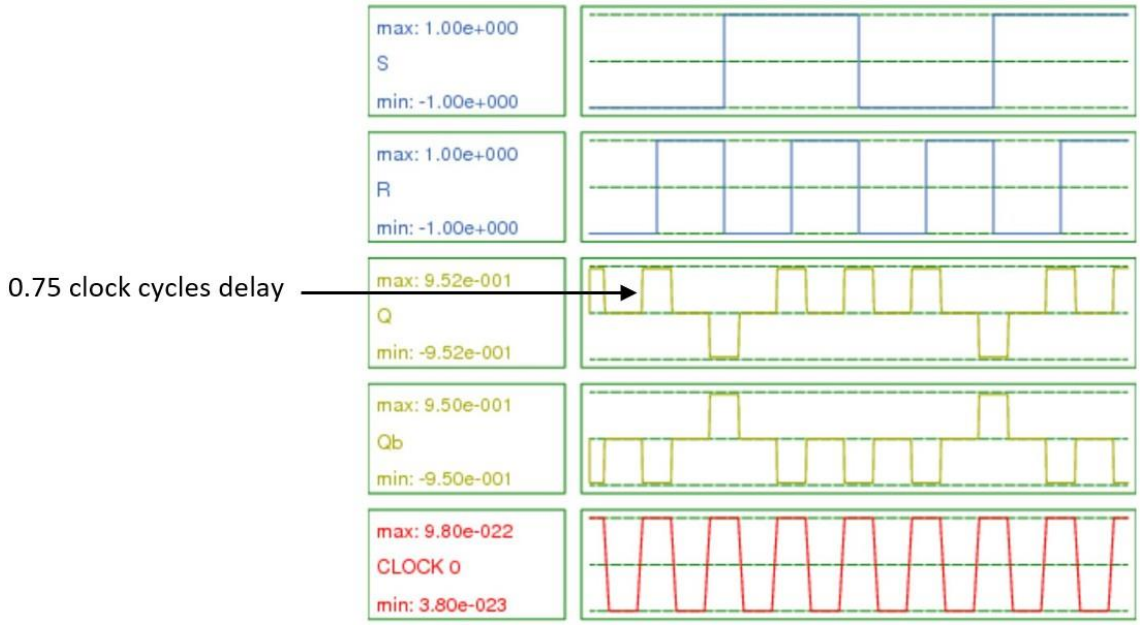
### 4.2.1. Simulating QCA SR flop-flop circuits

#### 4.2.1.1. Irreversible QCA SR flop-flop simulation

Figure 4.9 shows the simulation waveforms for the proposed irreversible QCA SR flip-flop, as shown in Figure 4.1. The simulation waveforms in the case of $Q_{(t-1)} = 0$ is represented in Figure 4.9a, while Figure 4.9b shows the waveforms of $Q_{(t-1)} = 1$. The results obtained from the simulations provide strong confirmation that the proposed irreversible QCA SR flip-flop computations align accurately with the expected outcomes given in Table 4.1. This agreement between the simulated data and the theoretical expectations demonstrates that the designed irreversible QCA SR flip-flop is functioning as intended, effectively implementing the desired computational gate action. The consistency of these results not only validates the underlying design principles but also attests to the robustness and reliability of the methodology employed.




(a)



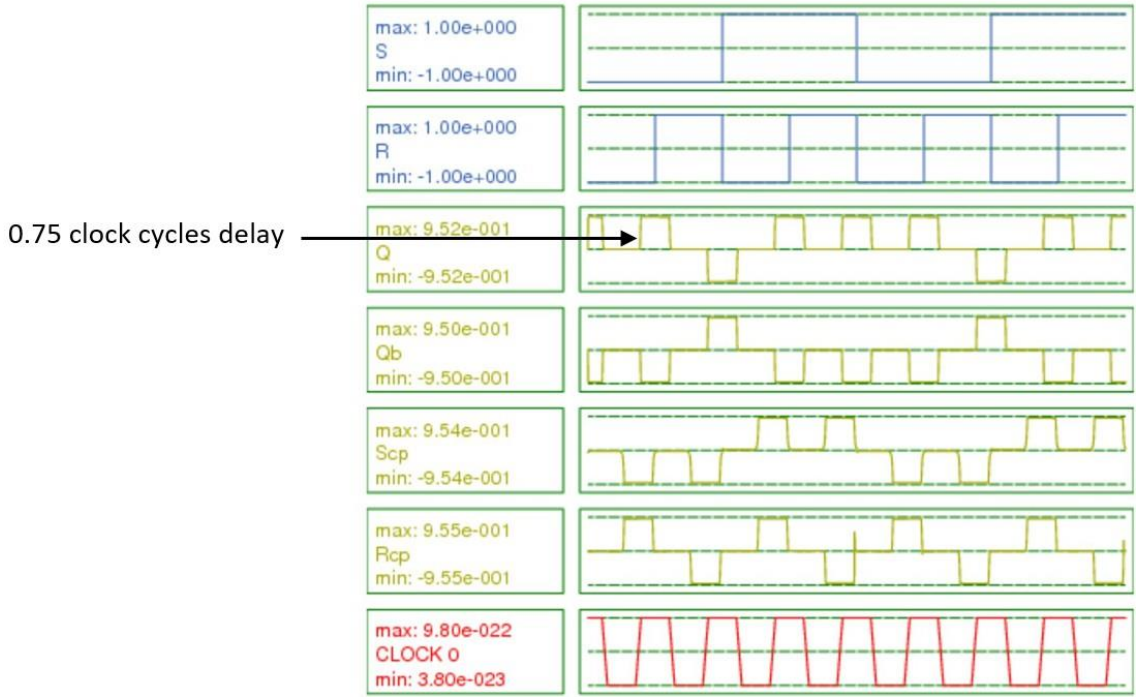

(b)

**Figure 4.9 Simulation waveforms of the proposed irreversible QCA SR flip-flop (a) for $Q_{(t-1)}$ = 0, (b) for $Q_{(t-1)}$ = 1**

#### 4.2.1.2. Reversible QCA SR flop-flop simulation

Figure 4.10a and Figure 4.10b show the input/output waveforms for the proposed reversible QCA SR flip-flop circuit for the cases $Q_{(t-1)}$ = 0 and $Q_{(t-1)}$ = 1, respectively. The design of the proposed reversible QCA SR flip-flop is illustrated in Figure 4.2. The simulation results confirm that the proposed reversible QCA SR flip-flop computations are fully consistent with the truth table values presented in Table 4.2. This alignment between the simulated outcomes and the expected truth table data highlights the design's accuracy and reliability, confirming that the circuits perform as intended according to the specified logic.


(b)



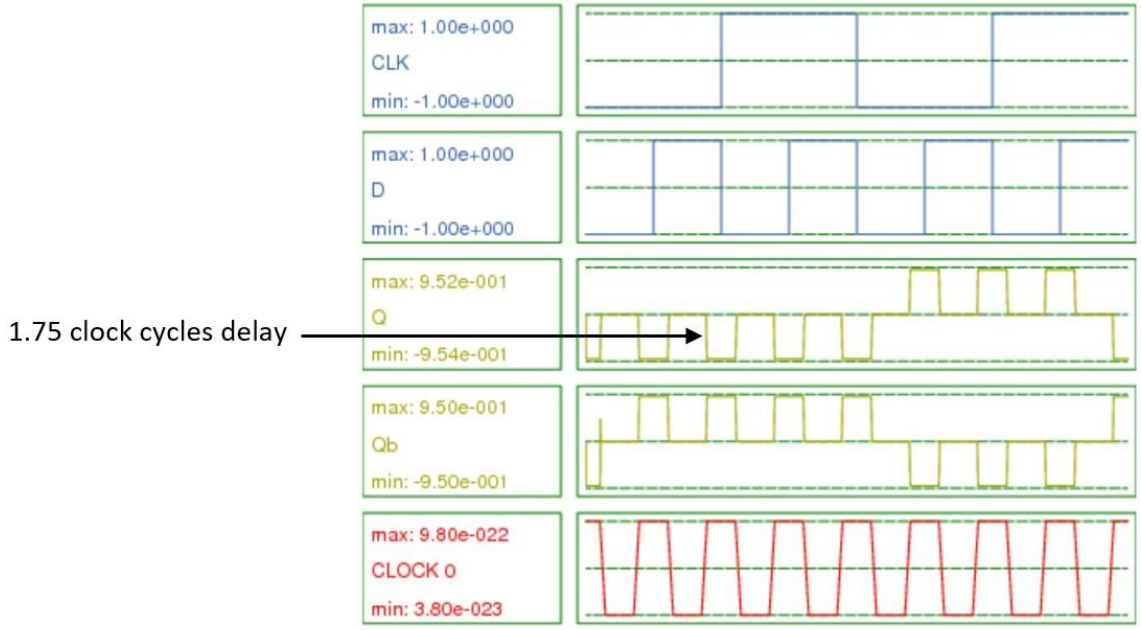

(b)

**Figure 4.10 Simulation waveforms of the proposed reversible QCA SR flip-flop (a) for $Q_{(t-1)} = 0$, (b) for $Q_{(t-1)} = 1$**

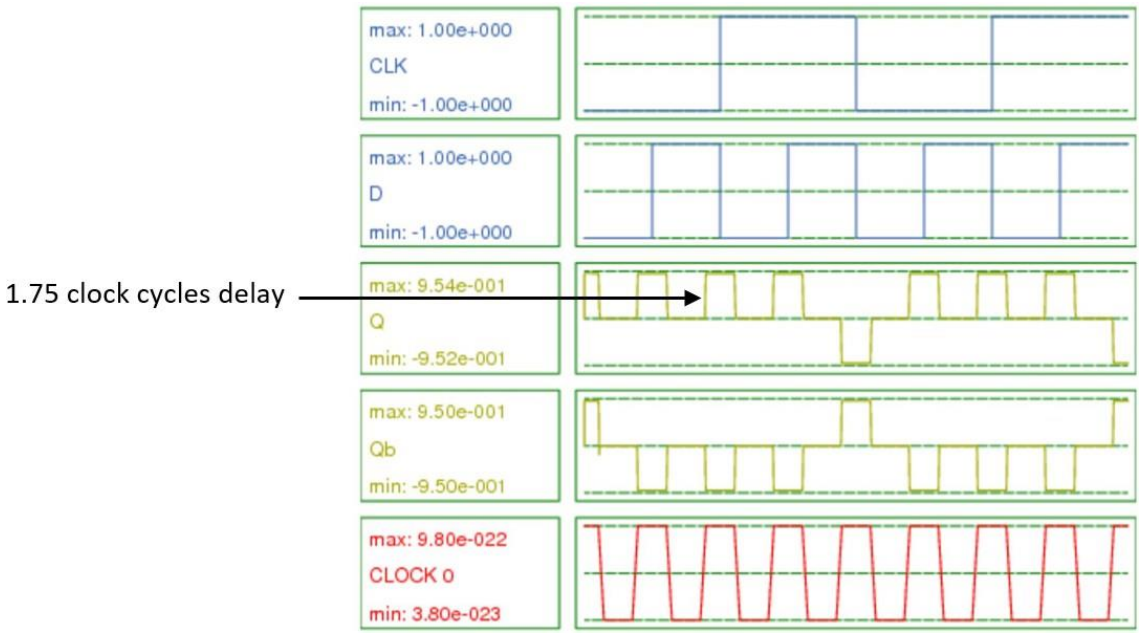
### 4.2.2. Simulating QCA D flop-flop circuits

#### 4.2.2.1. Irreversible QCA D flop-flop simulation

Figure 4.11 displays the simulation input/output waveforms for the proposed irreversible QCA D flip-flop. Specifically, Figure 4.11a and Figure 4.11b illustrate the waveforms for the circuit in the scenarios where $Q_{(t-1)} = 0$ and $Q_{(t-1)} = 1$, respectively. The design of the proposed irreversible QCA D flip-flop circuit is depicted in Figure 4.3. The simulation results are in full alignment with the expected behaviour detailed in Table 4.3, thereby confirming the accuracy and reliability of the proposed irreversible QCA D flip-flop's computational model. The alignment between the simulated and expected outcomes highlights the robustness of the design and confirms the effectiveness of the underlying computational framework.




(a)

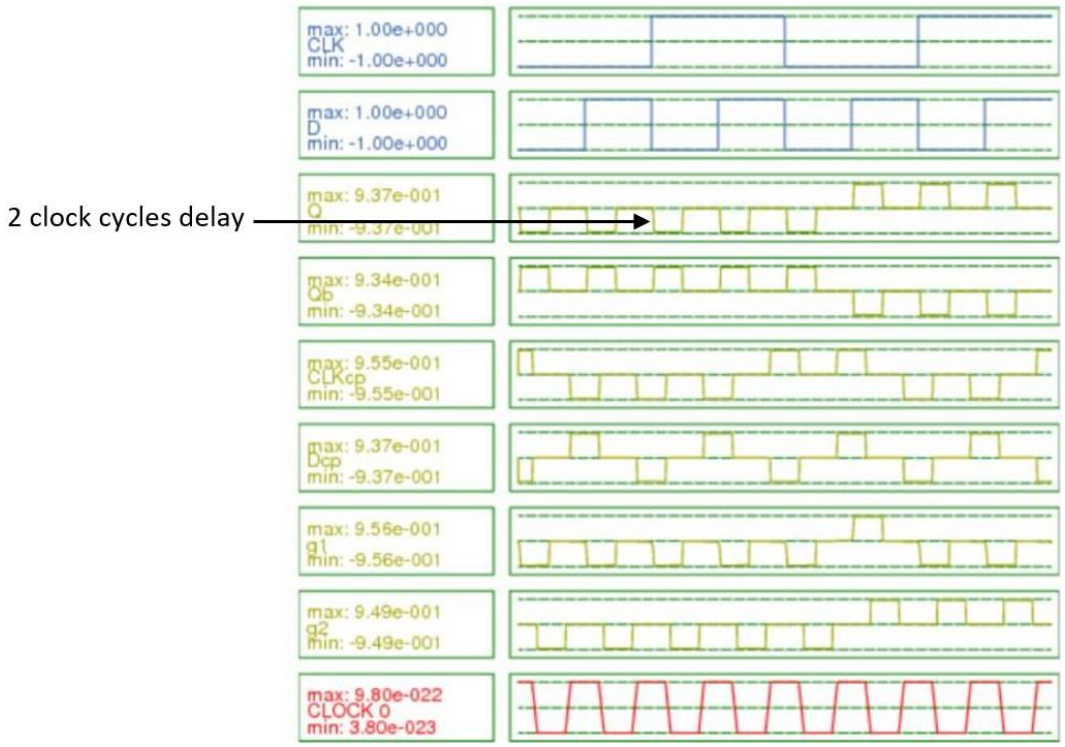



(b)

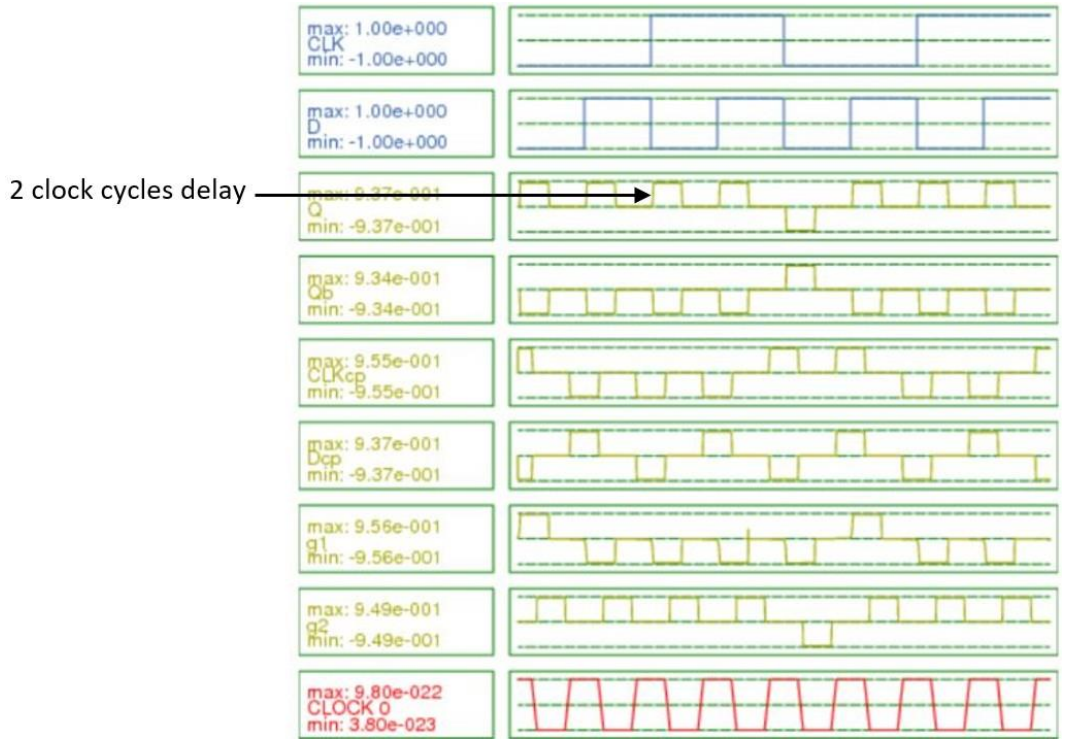
**Figure 4.11 Simulation waveforms of the proposed irreversible QCA D flip-flop (a) for $Q_{(t-1)}$ = 0, (b) for $Q_{(t-1)}$ = 1**

#### 4.2.2.2. Reversible QCA D flop-flop simulation

Figure 4.12 presents the simulation input/output waveforms for the proposed reversible QCA D flip-flop, as illustrated in Figure 4.4. Specifically, Figure 4.12a and Figure 4.12b show the input/output values for the circuit under conditions where $Q_{(t-1)}$ = 0 and $Q_{(t-1)}$ = 1, respectively. The simulation results fully correspond to the expected behaviour detailed in Table 4.4, thereby confirming the accuracy and reliability of the proposed reversible QCA D flip-flop's computational model. This precise alignment between the simulated outcomes and anticipated behavior validates the integrity of the design, affirming that the circuit functions as intended. The consistency of these results demonstrates the robustness of the innovative reversible design method, ensuring that the proposed reversible QCA D flip-flop reliably meets the required performance standards.




(b)



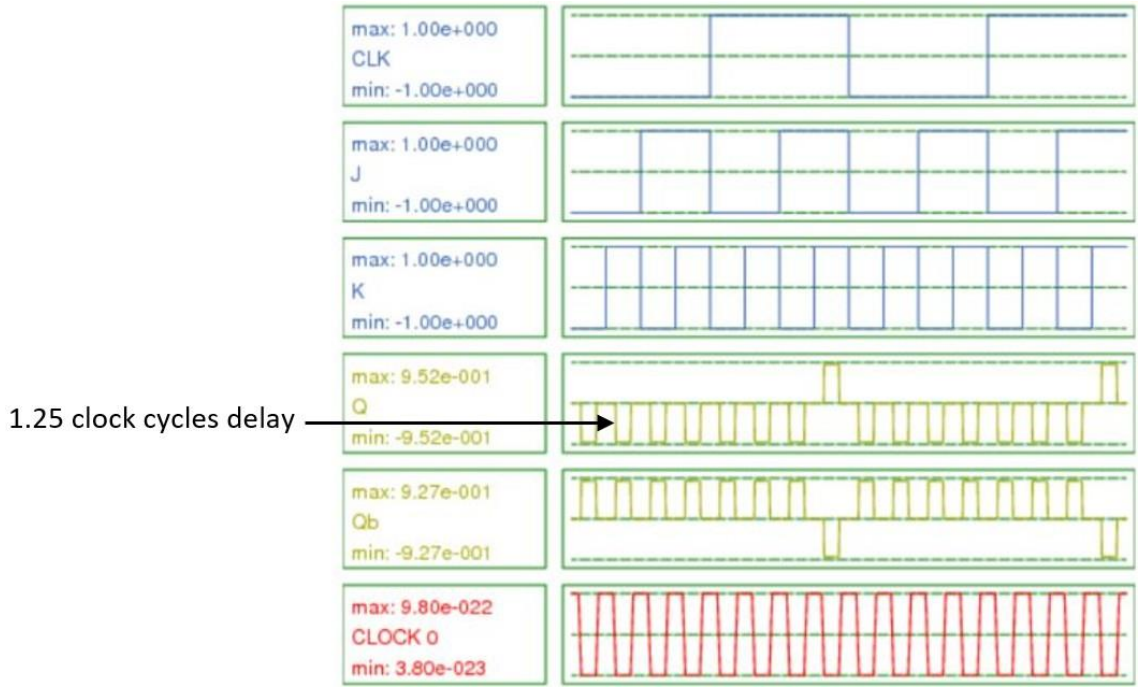

(b)

**Figure 4.12 Simulation waveforms of the proposed reversible QCA D flip-flop (a) for $Q_{(t-1)}$ = 0, (b) for $Q_{(t-1)}$ = 1**

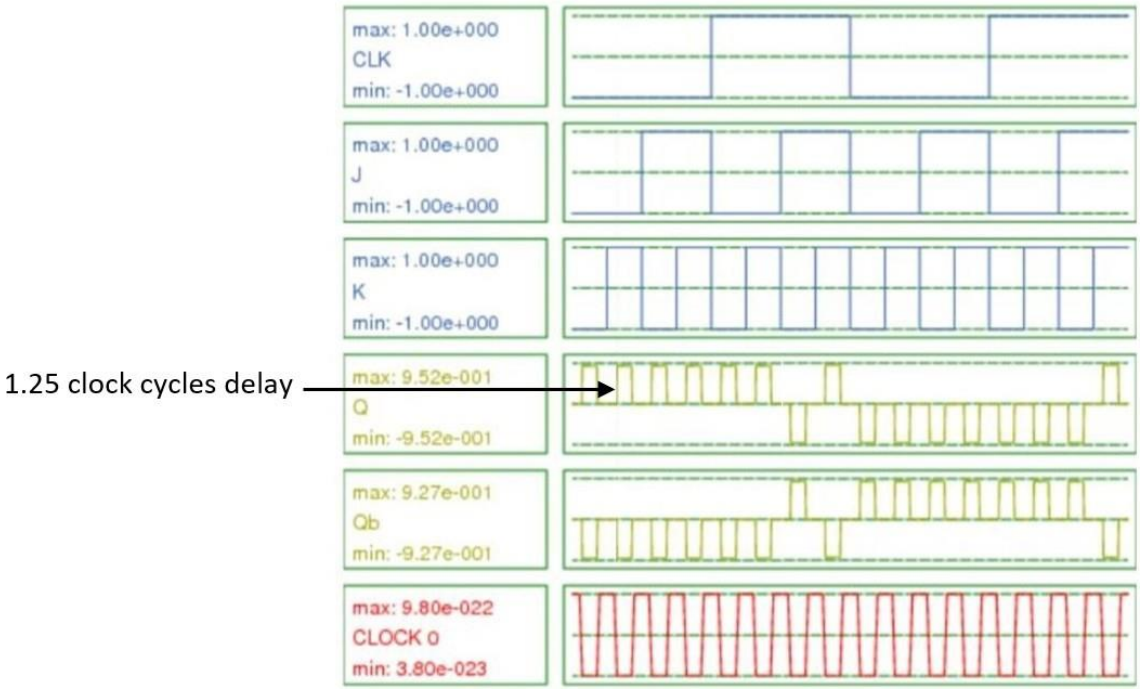
### 4.2.3. Simulating QCA JK flop-flop circuits

#### 4.2.3.1. Irreversible QCA JK flop-flop simulation

Figure 4.13 presents the simulation waveforms for the proposed irreversible QCA JK flip-flop. Figure 4.13a and Figure 4.13b specifically illustrate the input/output values for the circuit when $Q_{(t-1)}$ = 0 and $Q_{(t-1)}$ = 1, respectively. The design of the proposed irreversible QCA JK flip-flop is illustrated in Figure 4.5. The simulation results are in complete alignment with the expected behaviour detailed in Table 4.5, confirming the accuracy and reliability of the proposed irreversible QCA JK flip-flop's design. This strong correlation between the anticipated and observed outcomes not only validates the effectiveness of the design but also highlights the robustness of the underlying synthesis model. This consistency serves as a testament to the precision and soundness of the reversible design process, ensuring that the circuit performs as intended under the specified conditions and design rules.




(a)

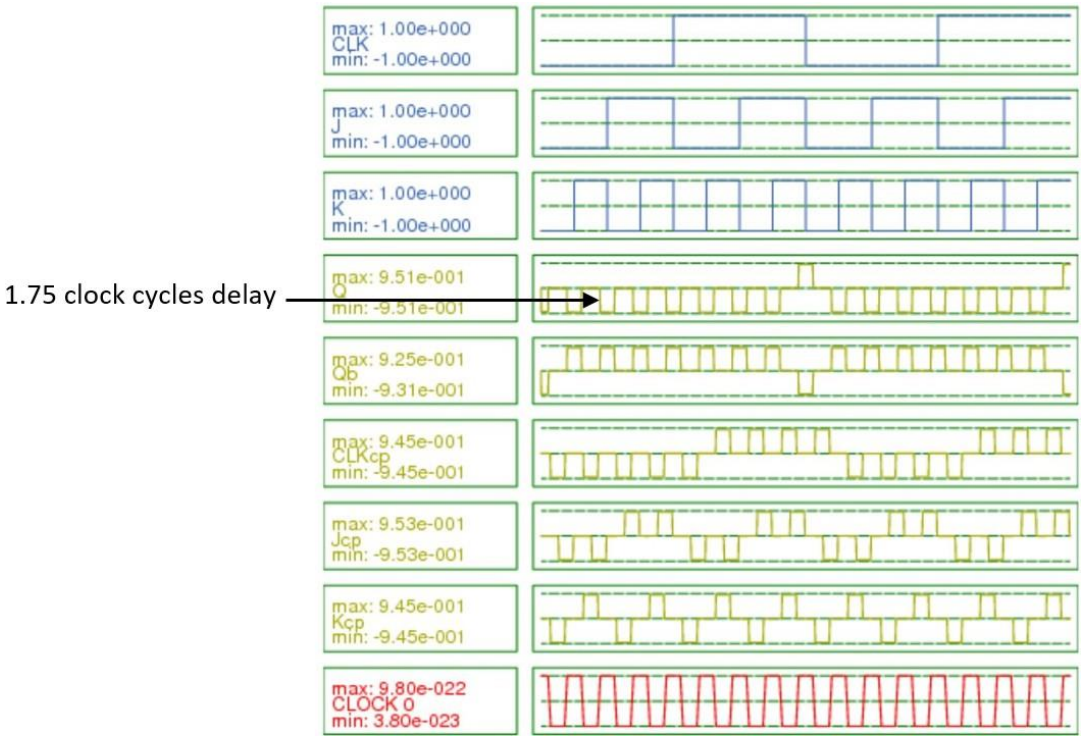



(b)

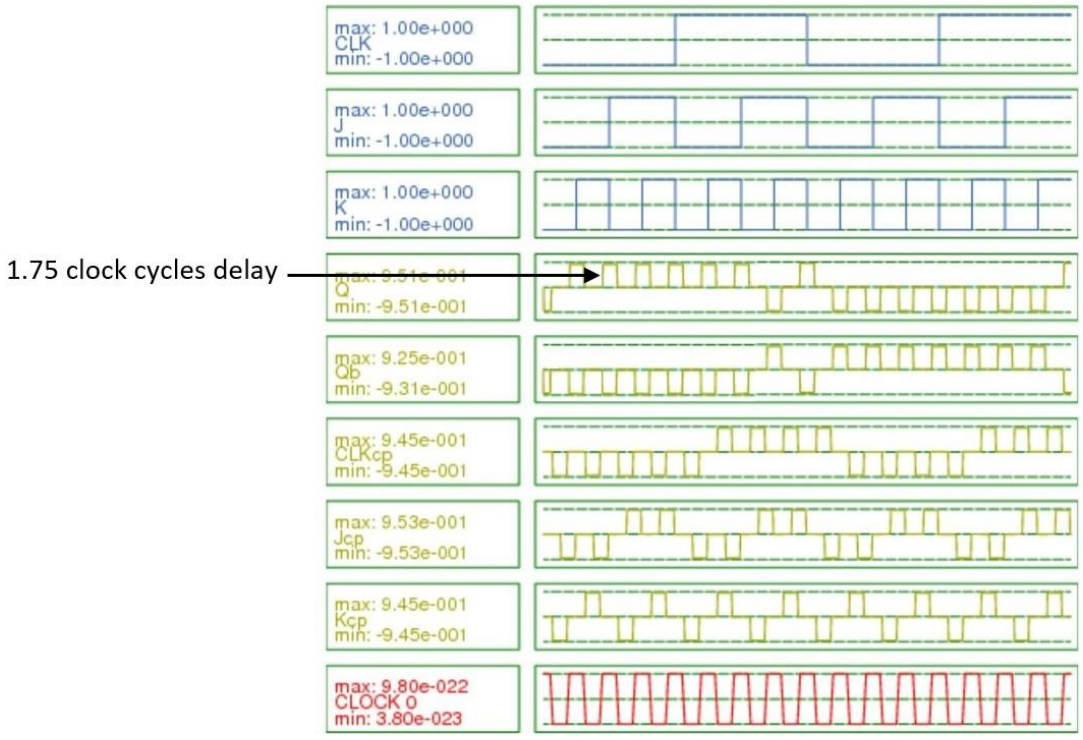
**Figure 4.13 Simulation waveforms of the proposed irreversible QCA JK flip-flop (a) for $Q_{(t-1)} = 0$, (b) for $Q_{(t-1)} = 1$**

#### 4.2.3.2. Reversible QCA JK flop-flop simulation

Figure 4.14 showcases the simulation waveforms for the proposed reversible QCA JK flip-flop, as illustrated in Figure 4.6. Figure 4.14a and Figure 4.14b detail the input/output values for the circuit under conditions where $Q_{(t-1)} = 0$ and $Q_{(t-1)} = 1$, respectively. The simulation results align with the expected behaviour presented in Table 4.6, providing strong evidence that the design of the proposed reversible QCA JK flip-flop is both accurate and reliable. This consistency not only validates the correctness of the design but also reinforces its credibility, confirming that the circuit operates as anticipated and adheres to the expected operational parameters.




(a)



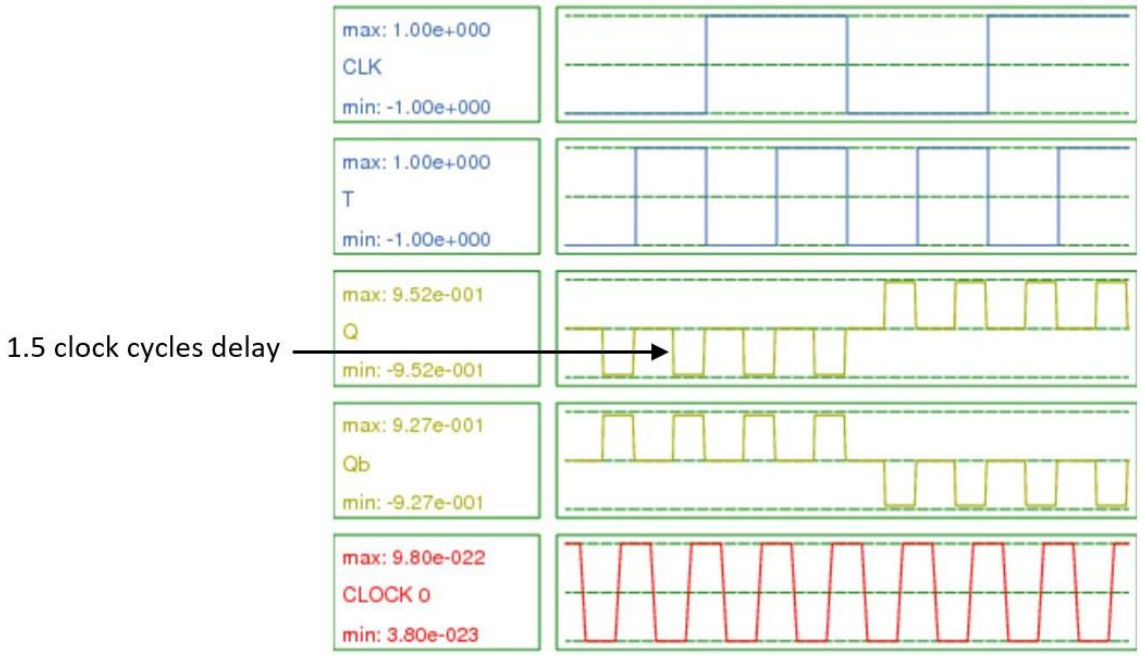

(b)

**Figure 4.14 Simulation waveforms of the proposed reversible QCA JK flip-flop (a) for $Q_{(t-1)} = 0$, (b) for $Q_{(t-1)} = 1$**

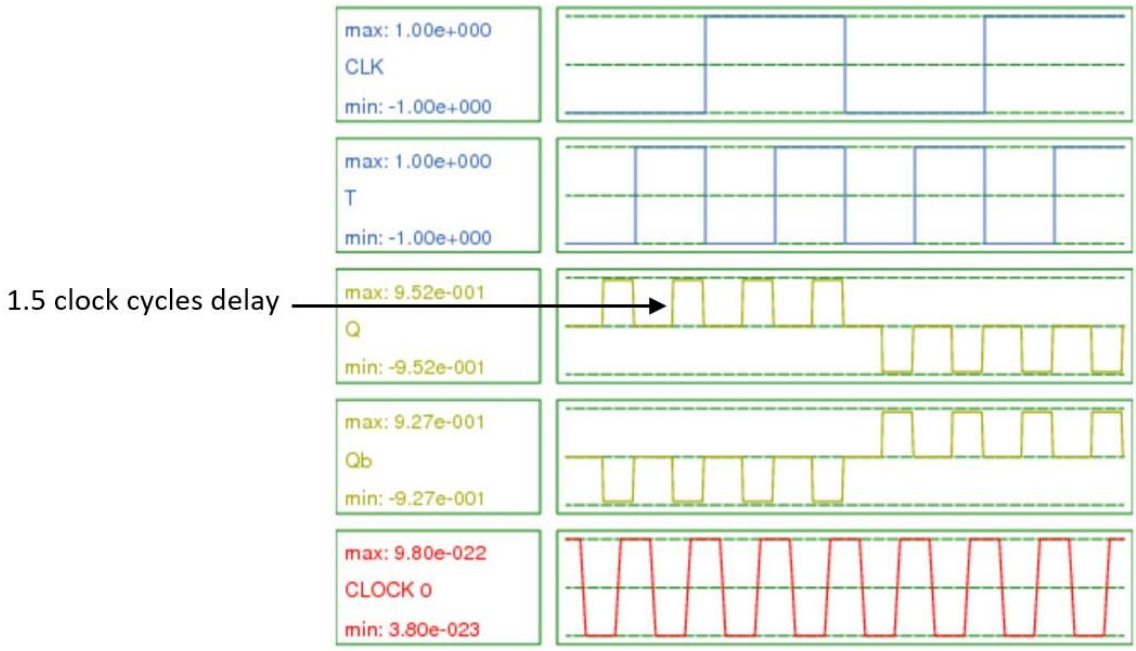
### 4.2.4. Simulating QCA T flop-flop circuits

#### 4.2.4.1. Irreversible QCA T flop-flop simulation

Figure 4.15 presents the simulation waveforms for the proposed irreversible QCA T flip-flop, as depicted in Figure 4.7. Figure 4.15a and Figure 4.15b illustrate the input/output values for the circuit when $Q_{(t-1)}$ = 0 and $Q_{(t-1)}$ = 1, respectively. The simulation results align with the expected behaviour outlined in Table 4.7, confirming the accuracy and reliability of the proposed irreversible QCA T flip-flop design.




(a)

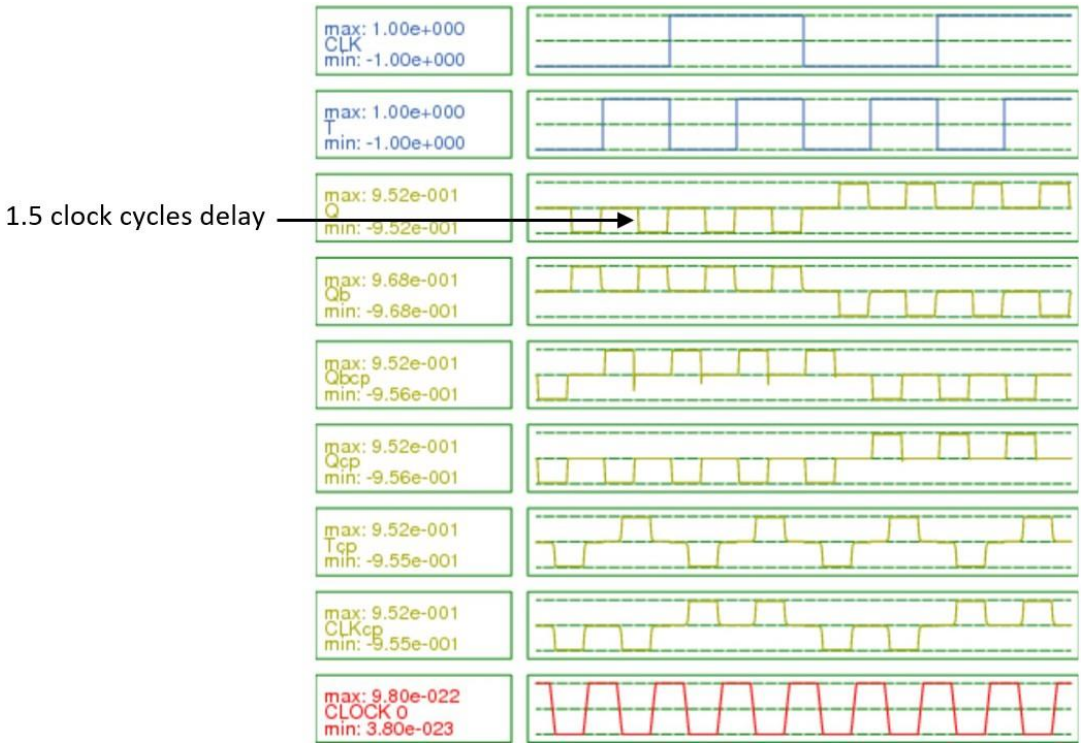



(b)

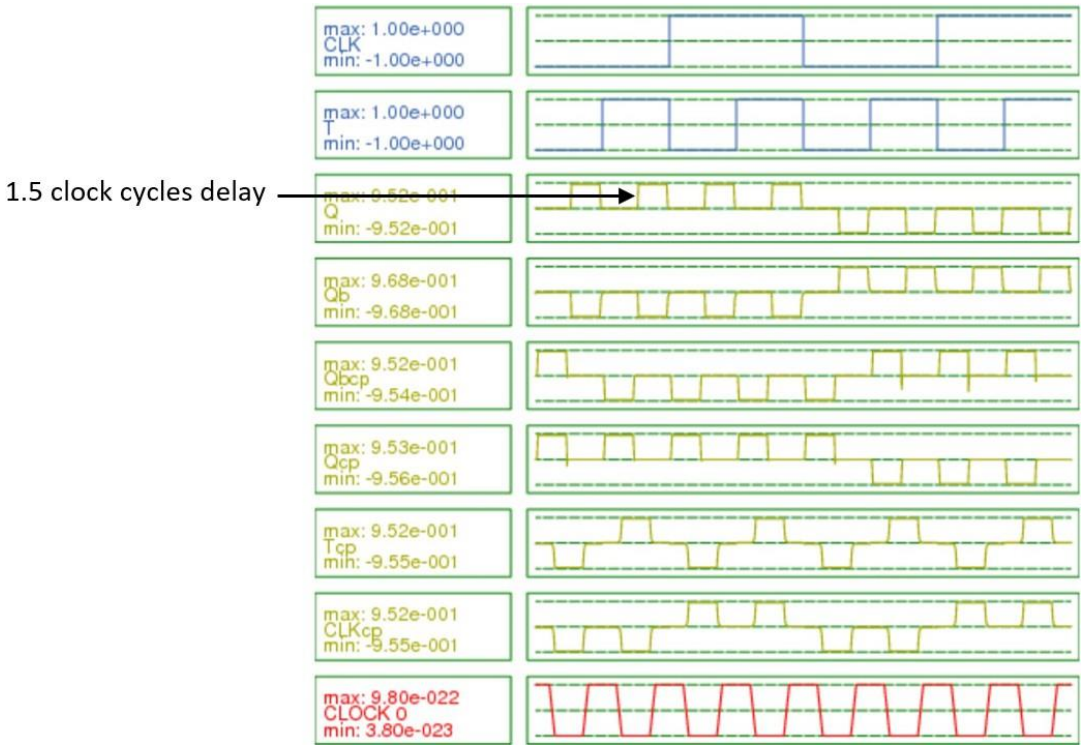
**Figure 4.15 Simulation waveforms of the proposed irreversible QCA T flip-flop (a) for $Q_{(t-1)}$ = 0, (b) for $Q_{(t-1)}$ = 1**

#### 4.2.4.2. Reversible QCA T flop-flop simulation

Figure 4.16 displays the simulation waveforms for the proposed reversible QCA T flip-flop, as shown in Figure 4.8. Figure 4.16a and Figure 4.16b depict the input/output values for the circuit under conditions where $Q_{(t-1)}$ = 0 and $Q_{(t-1)}$ = 1, respectively. The simulation results are consistent with the expected behaviour detailed in Table 4.8, thereby validating the accuracy and reliability of the proposed reversible QCA T flip-flop design.




(a)




(b)

**Figure 4.16 Simulation waveforms of the proposed reversible QCA T flip-flop (a) for $Q_{(t-1)} = 0$, (b) for $Q_{(t-1)} = 1$**

### 4.2.5. Summary of the reliability for the simulation of the flip-flops

The simulation waveforms provided compelling validation of the QCA flip-flop designs under investigation, for both the reversible and irreversible cases. Each waveform precisely reflects the expected behaviour as given in the corresponding truth tables and Boolean equations for the circuits, demonstrating a high degree of accuracy in the circuit functionality. This consistency between the simulated outputs and theoretical predictions not only stresses the robustness and reliability of the proposed QCA flip-flop designs, but also highlights their suitability for practical applications in nanoscale computing. Furthermore, the consistent simulation result of the proposed reversible QCA flip-flops reinforces the effectiveness of the underlying logically and physically reversible design methodology, proving its capability to develop reliable sequential QCA circuits.

## 4.3. Energy dissipation analysis

Energy efficiency is a critical consideration in the design of digital circuits [161]. This section investigates the energy dissipation of each proposed QCA flip-flop circuit, both reversible and irreversible, as presented in Section 4.1, through simulations conducted using the *QCADesigner-E 2.2* TCAD tool. The simulations utilise the technological and simulation parameters provided in Table 2.1 and Table 2.2, respectively. The reversible QCA flip-flops introduced in this chapter are designed to ensure that each internal majority gate functions reversibly and maintains an equal number of input and output signals, thereby achieving exceptional energy efficiency.

The proposed reversible QCA flip-flop circuits dissipate significantly less energy than their proposed irreversible counterparts, reaching values below the Landauer energy limit. Table 4.9 shows the energy dissipation values of all proposed reversible and irreversible QCA flip-flop circuits. For the proposed irreversible QCA SR flip-flop, the average dissipated energy across different input signal binary combinations is 0.365 meV. In the reversible implementation of the QCA SR flip-flop circuit, the value drops by an impressive 97.8% to 0.008 meV. Similarly, the irreversible QCA D flip-flop dissipates an average of 1.007 meV, which decreases by 95.5% to 0.045 meV in its reversible counterpart. The irreversible QCA JK flip-flop dissipates an average energy of 1.609 meV, with a reduction of 98.4% to 0.026 meV in the reversible version. Finally, the

irreversible QCA T flip-flop exhibits an average dissipated energy of 1.129 meV, which significantly drops by 96.9% to 0.035 meV in the reversible implementation.

To the best of our knowledge, no prior research has examined QCA flip-flop circuits that are both logically and physically reversible. Therefore, to assess the energy consumption efficiency of the proposed logically and physically reversible flip-flop circuits, a comparative analysis was conducted against the most recent logically reversible flip-flops documented in the literature. This evaluation aimed to assess how the new designs compared, in terms of energy efficiency, to the state-of-the-art reversible QCA flip-flops currently available. The logically reversible QCA flip-flops are typically composed of logically reversible gates like the 3 × 3 Fredkin gates and 2 × 2 Feynman gates. However, the internal majority gates, which form these flip-flop circuits, remain irreversible. Table 4.9 shows that the logically and physically reversible QCA flip-flops proposed in this chapter consume significantly less energy at the $1E_k$ tunnelling energy level compared to flip-flops previously documented in the literature [16, 162, 163], achieving nearly 98% energy reduction, with values near to zero.

**Table 4.9 Average and total energy dissipation comparison.**

| QCA Flip-Flop | Total Energy Dissipation [meV] | Average Energy Dissipation [meV] |
|---|---|---|
| SR flip-flop [163] | 40.850 | 13.940 |
| D flip-flop [16] | 97.100 | 18.500 |
| D flip-flop [164] | 10.770 | 4.920 |
| JK flip-flop [163] | 78.650 | 17.910 |
| T Flip-Flop Design 1 [162] | 16.600 | 1.510 |
| T Flip-Flop Design 2 [162] | 12.600 | 1.140 |
| T Flip-Flop Design 3 [162] | 16.000 | 1.450 |
| Irreversible majority gate | 1.460 | 0.182 |
| Proposed irreversible SR Flip-Flop | 3.011 | 0.365 |
| Proposed irreversible D Flip-Flop | 4.030 | 1.007 |
| Proposed irreversible JK Flip-Flop | 12.900 | 1.609 |
| Proposed irreversible T Flip-Flop | 4.521 | 1.129 |
| Reversible majority gate | 0.016 | 0.002 |
| Proposed reversible SR Flip-Flop | 0.032 | 0.008 |
| Proposed reversible D Flip-Flop | 0.180 | 0.045 |
| Proposed reversible JK Flip-Flop | 0.217 | 0.026 |
| Proposed reversible T Flip-Flop | 0.142 | 0.035 |

### 4.4. Occupied area and delay time calculation

The development of QCA sequential flip-flop digital circuits, that are both logically and physically reversible, represents a significant advance in reducing energy dissipation below the Landauer limit. This achievement is particularly necessary in the ongoing pursuit of more energy-efficient digital circuits. However, it is essential to recognise that this reduction in energy dissipation does not come without trade-offs. The design and implementation of such logically and physically reversible QCA flip-flop circuits often necessitate compromises, particularly in terms of increased area and/or latency. In the design of SR, D, JK, and T flip-flop circuits, a careful balance must be struck between the benefits of reduced energy dissipation and the potential drawbacks associated with increased area occupied and slower operational speeds. This delicate balancing act underscores the complexity and challenges inherent in the design of logically and physically reversible QCA digital circuits.

The evaluation of the proposed QCA flip-flop design metrics was meticulously conducted through an in-depth analysis of their physical layout structures. By closely examining these layouts, we were able to accurately derive the area and timing parameters, providing a detailed and precise characterisation of each circuit's performance. This approach ensures that the evaluation of each circuit is grounded in its actual physical implementation, thereby reflecting realistic performance metrics that are critical for assessing the overall efficiency and viability of the designs within practical applications. The rigorous extraction of these metrics from the physical layouts also enables a more reliable comparison between different circuit designs, facilitating the identification of the most optimal configurations in terms of resource utilisation and operational speed.

The assessment of circuit delay was conducted by carefully counting the clock zones along the critical path, which is defined as the longest path from an input pin to an output pin within the circuit. This critical path is essential for determining the overall speed of the circuit, as it dictates the maximum time required for a signal to propagate through the circuit. In this framework, each clock zone contributes a delay equivalent to one-quarter of a clock period, indicating that four clock zones collectively amount to one complete clock cycle. This method provides a precise measure of the circuit's timing characteristics, which is crucial for evaluating its performance.

Furthermore, the physical layout structure of the circuits offered a comprehensive view of various critical parameters, including the number of majority gates and inverters, the number of QCA cells, the quantity of USE clocking tiles, the overall occupied area, and the delay time for each circuit. Each USE clocking tile in the proposed flip-flop designs is composed of a 5 × 5 grid of QCA cells, a configuration that is instrumental in defining the spatial efficiency and operational dynamics of the circuit. These detailed insights into the physical characteristics of the circuits are systematically presented in Table 4.10, providing a clear and thorough overview of the design metrics. This information is essential for understanding the trade-offs and optimisations involved in the design process of reversible and irreversible flip-flop circuits. This information allows for a more informed evaluation of the circuit's overall effectiveness and potential applications in advanced digital systems.

**Table 4.10 Flip-flops area and delay time calculation.**

| QCA Flip-flop | Majority gates | Inverters | QCA cells | Area [$\mu m^2$] | USE tiles | Delay [clock cycles] |
|---|---|---|---|---|---|---|
| Irreversible SR Flip-Flop | 1 | 2 | 33 | 0.0606 | 5 | 0.75 |
| Reversible SR Flip-Flop | 1 | 2 | 37 | 0.0609 | 5 | 0.75 |
| Irreversible D Flip-Flop | 3 | 3 | 91 | 0.1686 | 13 | 1.75 |
| Reversible D Flip-Flop | 3 | 3 | 136 | 0.1888 | 13 | 2 |
| Irreversible JK Flip-Flop | 5 | 2 | 74 | 0.1089 | 9 | 1.25 |
| Reversible JK Flip-Flop | 5 | 2 | 149 | 0.2328 | 13 | 1.75 |
| Irreversible T Flip-Flop | 4 | 2 | 73 | 0.1288 | 10 | 1.5 |
| Reversible T Flip-Flop | 4 | 2 | 107 | 0.1589 | 10 | 1.5 |

The proposed reversible SR flip-flop design, which implements the logically and physically reversible design strategy, does not introduce any additional area or delay penalties compared to its irreversible counterpart. Both the irreversible and reversible SR flip-flops occupy an area of 0.060 $\mu m^2$ and exhibit a delay time of 3 clock zones, equivalent to 0.75 clock cycles. This indicates that the transition to reversible design in SR flip-flops can be achieved without compromising spatial efficiency or temporal performance.

However, this is not the case for other flip-flop designs. When implementing D, JK, and T flip-flops in a reversible manner, there are notable increases in both area and delay

time, compared to their irreversible designs. For instance, the irreversible D flip-flop occupies an area of 0.1686 μm² with a delay time of 7 clock zones (1.75 clock cycles). In the reversible design, the area increases by 10.7% to 0.1888 μm², and the delay time rises by 14.3% to 8 clock zones, corresponding to 2 clock cycles.

Similarly, the irreversible JK flip-flop requires an area of 0.1089 μm² and has a delay time of 5 clock zones (1.25 clock cycles). In contrast, the reversible JK flip-flop design incurs a 112.9% increase in area, occupying 0.2328 μm², and a 40% increase in delay time, reaching 7 clock zones (1.75 clock cycles).

In the case of T flip-flops, the irreversible design occupies 0.1288 μm², and the reversible design sees an 18.9% increase in area to 0.1589 μm². However, unlike the other flip-flop types, the delay time remains constant at 6 clock zones (1.5 clock cycles) for both irreversible and reversible T flip-flops.

These findings highlight the trade-offs involved in implementing sequential QCA flip-flop circuits using either reversible or irreversible methods. While reversible SR flip-flops can be achieved without penalties in area or delay, D, JK, and T flip-flops experience significant increases in both metrics, underscoring the complexity of balancing energy efficiency with spatial and temporal constraints in reversible computing.

Furthermore, it is important to highlight that the number of majority gates and inverters required for the implementation of each flip-flop type remains consistent, regardless of whether an irreversible or reversible design methodology is employed, as illustrated in Table 4.10. This consistency stresses the efficiency and robustness of the logically and physically reversible design approach in developing sequential digital circuits across different flip-flop types. Specifically, the QCA flip-flop circuits demonstrate the following requirements for majority gates and inverters: The SR flip-flops require a single majority gate and two inverters, reflecting the simplicity of their design. In contrast, the T flip-flops are slightly more complex, necessitating three majority gates and three inverters to achieve their functionality. The JK flip-flops demand a more substantial configuration, with five majority gates and two inverters required for their implementation. Lastly, the D flip-flops require four majority gates and two inverters, balancing complexity and performance. The uniformity in the number of majority gates and inverters required for both irreversible and reversible designs indicates that the

fundamental logical structure of the flip-flops remains consistent, regardless of the design approach. Such consistency is advantageous, as it simplifies the design process and allows for a more straightforward comparison of performance metrics, such as area efficiency and delay, between different flip-flop configurations. The detailed breakdown of these requirements further reinforces the practicality and scalability of the proposed designs in various digital applications.

### 4.5. Cost calculation

This section presents the total cost of each flip-flop design from Section 4.1. The cost function in Equation 1.16 has been used, as detailed earlier in Section 1.8, which serves as a standardised metric for evaluating the efficiency and effectiveness of QCA circuits. This cost function offers a quantitative measure that captures various design parameters, enabling a fair and objective comparison across different QCA circuit designs. Moreover, this section presents a comprehensive comparative analysis of the proposed reversible and irreversible QCA flip-flop designs against the most recent QCA flip-flop circuits documented in the literature [136, 162, 163, 165, 166].

Table 4.11 presents a comprehensive comparison of the proposed irreversible and reversible QCA flip-flop circuits, as well as the most recent flip-flop designs documented in the literature. This table provides a detailed breakdown of several key metrics, including the number of majority gates and inverters used, the number of crossovers, the cell count, the delay time, and the overall cost for each proposed QCA flip-flop. This thorough comparison not only highlights the advancements made by our designs but also positions them as highly competitive alternatives in the field of QCA-based digital circuits.

The analysis reveals that the proposed irreversible flip-flops deliver significant cost improvements over the best existing designs. Specifically, the proposed irreversible QCA flip-flop designs demonstrate remarkable cost reductions: 79.55% for the SR flip-flop, 9% for the D flip-flop, 16.67% for the JK flip-flop, and 20.59% for the T flip-flop, when compared to the comparable most cost-efficient designs currently available in the literature [44, 46–48]. These substantial reductions emphasise the efficiency of the proposed irreversible designs, highlighting their potential to achieve superior performance while minimising resource utilisation.

**Table 4.11 Flip-flops cost calculation.**

| QCA Flip-flop | Majority gates | Inverters | Delay [clock cycles] | Crossings | Cost function (FOM) |
|---|---|---|---|---|---|
| SR flip-flop [165] | 4 | 2 | 1.5 | 0 | 108 |
| SR flip-flop [163] | 3 | 2 | 1 | 0 | 44 |
| D flip-flop [165] | 4 | 4 | 1.25 | 0 | 100 |
| D Flip-Flop [136] | 5 | 4 | 1 | 1 | 120 |
| JK flip-flop [165] | 6 | 2 | 1.5 | 0 | 228 |
| JK flip-flop [166] | 4 | 2 | 1.5 | 3 | 162 |
| T flip-flop [165] | 6 | 2 | 1.5 | 0 | 228 |
| T Flip-Flop Design 1 [162] | 3 | 1 | 2.25 | 0 | 153 |
| T Flip-Flop Design 2 [162] | 3 | 2 | 2.25 | 0 | 162 |
| T Flip-Flop Design 3 [162] | 3 | 1 | 2 | 0 | 136 |
| Proposed irreversible SR Flip-Flop | 1 | 2 | 0.75 | 0 | 9 |
| Proposed irreversible D Flip-Flop | 3 | 3 | 1.75 | 1 | 91 |
| Proposed irreversible JK Flip-Flop | 5 | 2 | 1.25 | 0 | 135 |
| Proposed irreversible T Flip-Flop | 4 | 2 | 1.5 | 0 | 108 |
| Proposed reversible SR Flip-Flop | 1 | 2 | 0.75 | 0 | 9 |
| Proposed reversible D Flip-Flop | 3 | 3 | 2 | 3 | 168 |
| Proposed reversible JK Flip-Flop | 5 | 2 | 1.75 | 3 | 252 |
| Proposed reversible T Flip-Flop | 4 | 2 | 1.5 | 2 | 132 |

The advancements achieved by the proposed irreversible flip-flop designs reflect the advanced methodologies employed in their development, which prioritise not only functionality and reliability but also the optimisation of critical factors such as area, delay, and power consumption. This rigorous design approach has resulted in flip-flop circuits that are not only highly competitive but also establish new benchmarks in the field, offering a compelling alternative to existing irreversible solutions in QCA-based digital circuit design.

### 4.6. Conclusion

This chapter provides simulation-based confirmation that developing sequential QCA flip-flop circuits, in a logically and physically reversible manner, can result in circuits that dissipate less energy than the Landauer limit of $k_B T \ln 2$. Innovative designs for sequential QCA flip-flops, incorporating both logical and physical reversibility, have been successfully created for the most common flip-flop types, including SR, D, JK, and T flip-flops. To facilitate a comprehensive comparison, these circuits were also implemented in

an irreversible manner, allowing for an evaluation of energy dissipation, occupied area, delay time, and overall cost between reversible and irreversible designs.

All circuits were constructed utilising majority gates, a fundamental building block in QCA technology, ensuring design consistency and effectiveness. Reversible flip-flop circuits used a reversible majority gate as their main building block, whereas irreversible flip-flops were designed using irreversible majority gates. The USE clocking scheme, incorporating feedback paths, was employed to achieve precise timing control. To evaluate the performance of these designs, the *QCADesigner 2.0.3* and *QCADesigner-E 2.2* TCAD tools were used, providing accurate calculations of both polarisation input/output waveform responses and the energy dissipated by the sequential QCA flip-flop circuits. These calculations are based on a microscopic quantum mechanical model of the QCA cell, ensuring that the simulation results closely reflect the actual physical behaviour of the circuits.

The simulation results confirmed the feasibility of designing sequential QCA circuits that are both logically and physically reversible. Implementing logical and physical reversibility in QCA flip-flop circuits led to a reduction in energy dissipation by over 95% compared to their irreversible counterparts. The simulations demonstrated ultralow energy dissipation levels, with energies falling below the Landauer limit of 0.06 meV at a temperature of 1 K. However, designing sequential QCA flip-flops that are both logically and physically reversible may raise the area cost and/or delay time to levels higher than those of irreversible ones.

This chapter also systematically investigated the trade-off between energy dissipation, area cost, and delay time for both reversible and irreversible QCA circuits. The results showed that irreversible QCA flip-flop designs had area costs and delay times that were lower than or equal to those of the reversible designs. In the SR flip-flop design, there are no area costs or delay time penalties among the irreversible and reversible circuits. However, the area costs and delay times increase when developing the reversible D, JK, and T flip-flops. The area costs of reversible D, JK, and T flip-flop circuits are increased by 10.7%, 112,9%, and 18.9%, respectively, compared with irreversible circuits. Additionally, the delay times of the reversible D and JK flip-flops are raised by 14.3% and 40% more than irreversible circuits.

Additionally, the energy dissipation of the proposed logically and physically reversible flip-flops is much lower than that of the flip-flops introduced in the literature. Compared to earlier designs, the energy consumption of each type of flip-flop has decreased by approximately 98%. In addition, the cost of the proposed irreversible SR, D, JK, and T flip-flops is reduced by 91.67%, 9%, 40.79%, and 20.5%, respectively, as compared to the previously proposed flip-flops.

These results provide support for the serious consideration of QCA as an alternative to overcome the integration limitations of conventional irreversible CMOS sequential logic computation technologies. Future work is necessary to explore the logically and physically reversible design technique applied to more sophisticated QCA computing systems consisting of combined combinational and sequential logic circuits.

### 4.7. Contribution

The research findings presented in this chapter led to the publication of a research article titled “Novel Ultra-Energy-Efficient Reversible Designs of Sequential Logic Quantum-Dot Cellular Automata Flip-Flop Circuits” in the March 2023 edition of The *Journal of Supercomputing* [31] (refer to Figure 4.17). This article was later reissued as a chapter in The *Prime Archives in Electronics* in December 2023 [167] (refer to Figure 4.18). This publication makes a significant contribution to the ongoing research on energy-efficient QCA-based sequential digital circuits by presenting novel advancements in the design and simulation of reversible sequential flip-flop circuits with ultralow energy dissipation.

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# Novel ultra-energy-efficient reversible designs of sequential logic quantum-dot cellular automata flip-flop circuits

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**Abstract**
Quantum-dot cellular automata (QCA) is a technological approach to implement digital circuits with exceptionally high integration density, high switching frequency, and low energy dissipation. QCA circuits are a potential solution to the energy dissipation issues created by shrinking microprocessors with ultra-high integration densities. Current QCA circuit designs are irreversible, yet reversible circuits are known to increase energy efficiency. Thus, the development of reversible QCA circuits will further reduce energy dissipation. This paper presents novel reversible and irreversible sequential QCA set/reset (SR), data (D), Jack Kilby (JK), and toggle (T) flip-flop designs based on the majority gate that utilizes the universal, standard, and efficient (USE) clocking scheme, which allows the implementation of feedback paths and easy routing for sequential QCA-based circuits. The simulation results confirm that the proposed reversible QCA USE sequential flip-flop circuits exhibit energy dissipation less than the Landauer energy limit. Irreversible QCA USE flip-flop designs, although having higher energy dissipation, sometimes have floorplan areas and delay times less than those of reversible designs; therefore, they are also explored. The trade-offs between the energy dissipation versus the area cost and delay time for the reversible and irreversible QCA circuits are examined comprehensively.

**Keywords** Quantum-dot cellular automata (QCA) · Sequential flip-flop · Reversible · Energy dissipation · Universal, standard, and efficient clocking scheme (USE)

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Extended author information available on the last page of the article

Springer

**Figure 4.17 Article paper: Novel ultra-energy-efficient reversible designs of sequential logic quantum-dot cellular automata flip-flop circuits**

Prime Archives in Nanotechnology

**Book Chapter**

# Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit

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**Figure 4.18 Book chapter: Novel ultra-energy-efficient reversible designs of sequential logic quantum-dot cellular automata flip-flop circuits**

# Chapter 5

# 5. Advanced Reversible QCA Computing Circuits

This chapter provides new logically and physically reversible 8:1 multiplexer and ALU designs. The innovative reversible design methodology outlined in Chapter 2 is applied, utilising the geometric parameters of the underlying technology as detailed in Table 2.1. These designs serve as critical case studies, demonstrating the practical application and effectiveness of the reversible design methodology in advancing QCA-based computing circuits. The findings accentuate the substantial potential of logically and physically reversible design methodologies to drive innovation in digital integrated circuit engineering, offering a promising pathway toward the development of more sustainable, efficient, and high-performance computing systems.

## 5.1. Reversible QCA 8:1 multiplexer

In VLSI systems, multiplexers are important components used for building several digital circuits [30]. A multiplexer chooses which of several input data lines to send to a single output based on a set of control signals. Multiplexers are indispensable in digital electronics, extensively employing this functionality to optimise data selection and routing processes. Their ability to efficiently manage multiple data streams within complex circuits underscores their significance in the design and operation of modern digital systems, contributing to enhanced performance and resource utilisation in a wide range of computing applications.

The QCA 8:1 multiplexer circuit has garnered significant attention within the research community due to its crucial role in the construction of digital circuits for advanced computing systems [168, 169]. This circuit functions by selecting one of eight input signals and forwarding it to a single output line, based on the values of three control, or select, signals. Numerus studies have proposed various configurations for a reversible QCA 8:1 multiplexer circuit, primarily focusing on reducing energy dissipation [170]. However, these studies have typically focused only on reversibility at the logical synthesis

level, often overlooking the importance of achieving reversibility at the layout level, i.e., the physical realisation of the circuit.

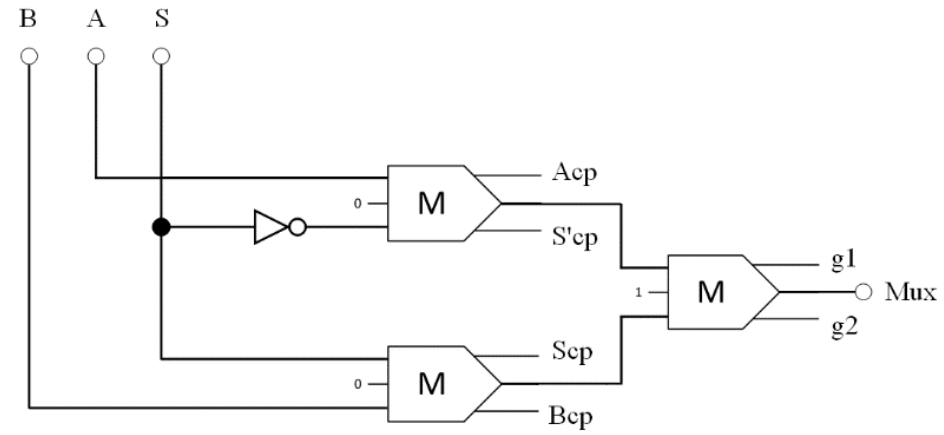
This section develops a new QCA 8:1 multiplexer circuit using the innovative logically and physically reversible design approach. This novel design effectively addresses and overcomes the limitations and challenges associated with previous QCA 8:1 multiplexer designs, offering enhanced performance and efficiency through logical and physical reversibility principles.

### 5.1.1. Designing reversible QCA 8:1 multiplexer

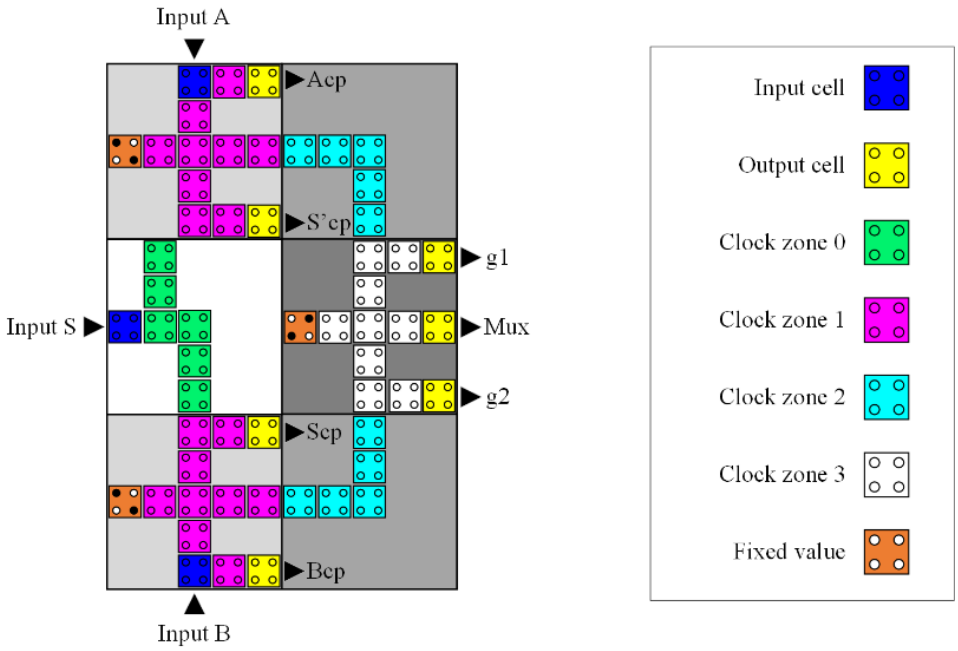
The hierarchical design process for developing a logically and physically reversible 8:1 multiplexer in QCA can be structured into distinct instance blocks. The process begins with the logically and physically reversible design of a QCA 2:1 multiplexer, which utilises three fully reversible majority gates and a single-branch inverter. The next stage involves the logically and physically reversible design of a QCA 4:1 multiplexer, which integrates three logically and physically reversible QCA 2:1 multiplexers. Finally, the process culminates in the logically and physically reversible design of a QCA 8:1 multiplexer, comprising two logically and physically reversible QCA 4:1 multiplexers and an additional single logically and physically reversible QCA 2:1 multiplexer.

#### 5.1.1.1. Reversible QCA 2:1 multiplexer design

The first step in the design process for a logically and physically reversible QCA 8:1 multiplexer circuit is to develop a logically and physically reversible QCA 2:1 multiplexer circuit, which serves as the design's central organ. The logically and physically reversible 2:1 multiplexer is composed of three fully reversible majority gates (two configured to operate as AND gates and one configured to operate as an OR gate), as well as a single-branch inverter. Figure 5.1a depicts the logic synthesis of this logically and physically reversible 2:1 multiplexer circuit, while Figure 5.1b displays the QCA cell layout design. The reversible QCA 2:1 multiplexer has a delay of four clock zones, which is equivalent to one complete clock cycle. This design requires the use of 56 QCA cells, occupying a total area of 0.09 $\mu m^2$.




(a)




(b)

**Figure 5.1 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA 2:1 multiplexer ($A_{cp}$, $B_{cp}$, $S_{cp}$, and $\bar{S}_{cp}$ indicate copies of the inputs, while g1, and g2 are so-called garbage outputs).**

Equation 5.1 provides a Boolean expression that represents the output of the proposed logically and physically reversible 2:1 multiplexer circuit, as a function of its inputs. Table 5.1 presents the corresponding truth table, detailing the circuit's logical behaviour for all possible input combinations. This table serves as a verification tool, confirming that the circuit operates as intended and adheres to the defined Boolean logic.

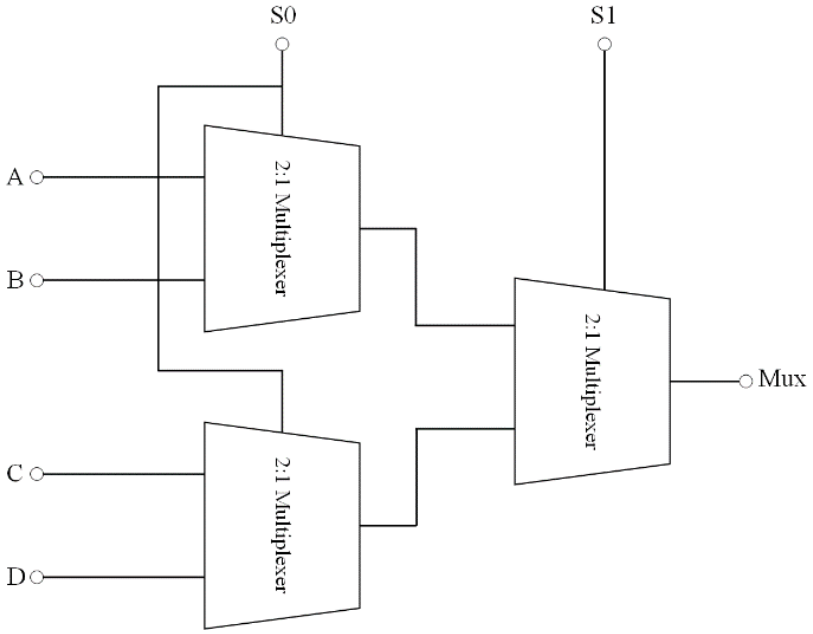
$$Mux = (A.\bar{S}) + (B.S) \quad (5.1)$$

**Table 5.1 Truth table for proposed 2:1 multiplexer circuit shown in Figure 5.1.**

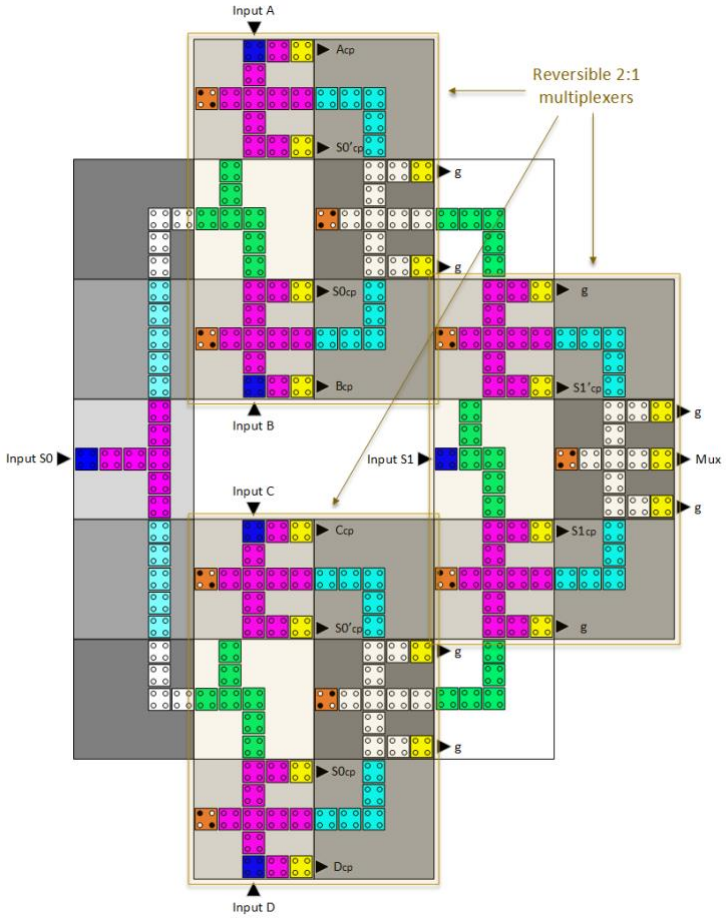
| S | Mux |
|---|---|
| 0 | A |
| 1 | B |

#### 5.1.1.2. Reversible QCA 4:1 multiplexer design

The logically and physically reversible QCA 4:1 multiplexer circuit is constructed by integrating three logically and physically reversible QCA 2:1 multiplexer circuits, as depicted in Figure 5.2. Consequently, the logically and physically reversible QCA 4:1 multiplexer comprises nine fully reversible majority gates (six fully reversible AND gates and three fully reversible OR gates) as well as three single-branch inverters. Figure 5.2a presents the schematic diagram of this QCA 4:1 multiplexer circuit, while Figure 5.2b illustrates the corresponding QCA cell layout design. The circuit utilises a total of 213 QCA cells and occupies an area of 0.46 μm², using the geometric technological parameters outlined in Table 2.1. The circuit exhibits a delay of 12 clock zones, equivalent to three clock cycles, demonstrating its efficient operation within the QCA framework.




(a)




(b)

**Figure 5.2 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA 4:1 multiplexer ($A_{cp}$, $B_{cp}$, $C_{cp}$, $D_{cp}$, $S0_{cp}$, $S1_{cp}$, $\overline{S0}_{cp}$, and $\overline{S1}_{cp}$ indicate copies of the inputs, while g is so-called garbage output).**

Equation 5.2 provides the output of the proposed 4:1 multiplexer circuit in terms of the Boolean inputs, while Table 5.2 presents the corresponding truth table for the circuit.

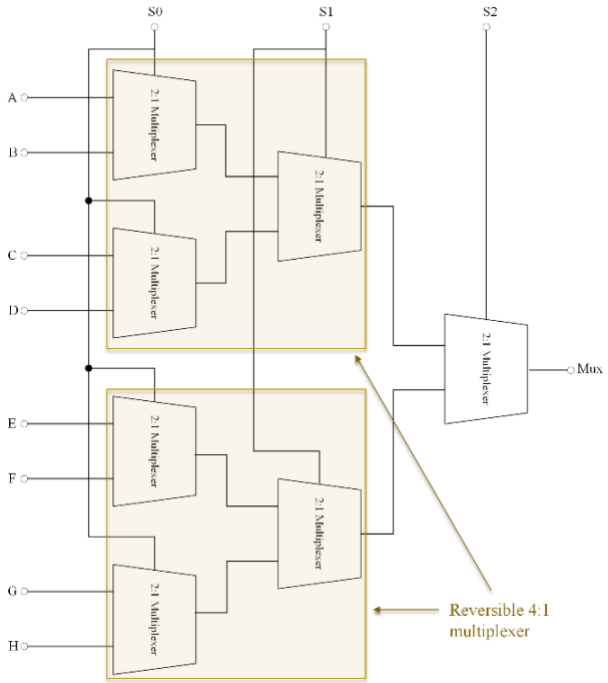
$$Mux = \left(\overline{S1}.\left(\left(\overline{S0}.A\right) + \left(S0.B\right)\right)\right) + \left(S1.\left(\left(\overline{S0}.C\right) + \left(S0.D\right)\right)\right) \tag{5.2}$$

**Table 5.2 Truth table for proposed 4:1 multiplexer circuit shown in Figure 5.2.**

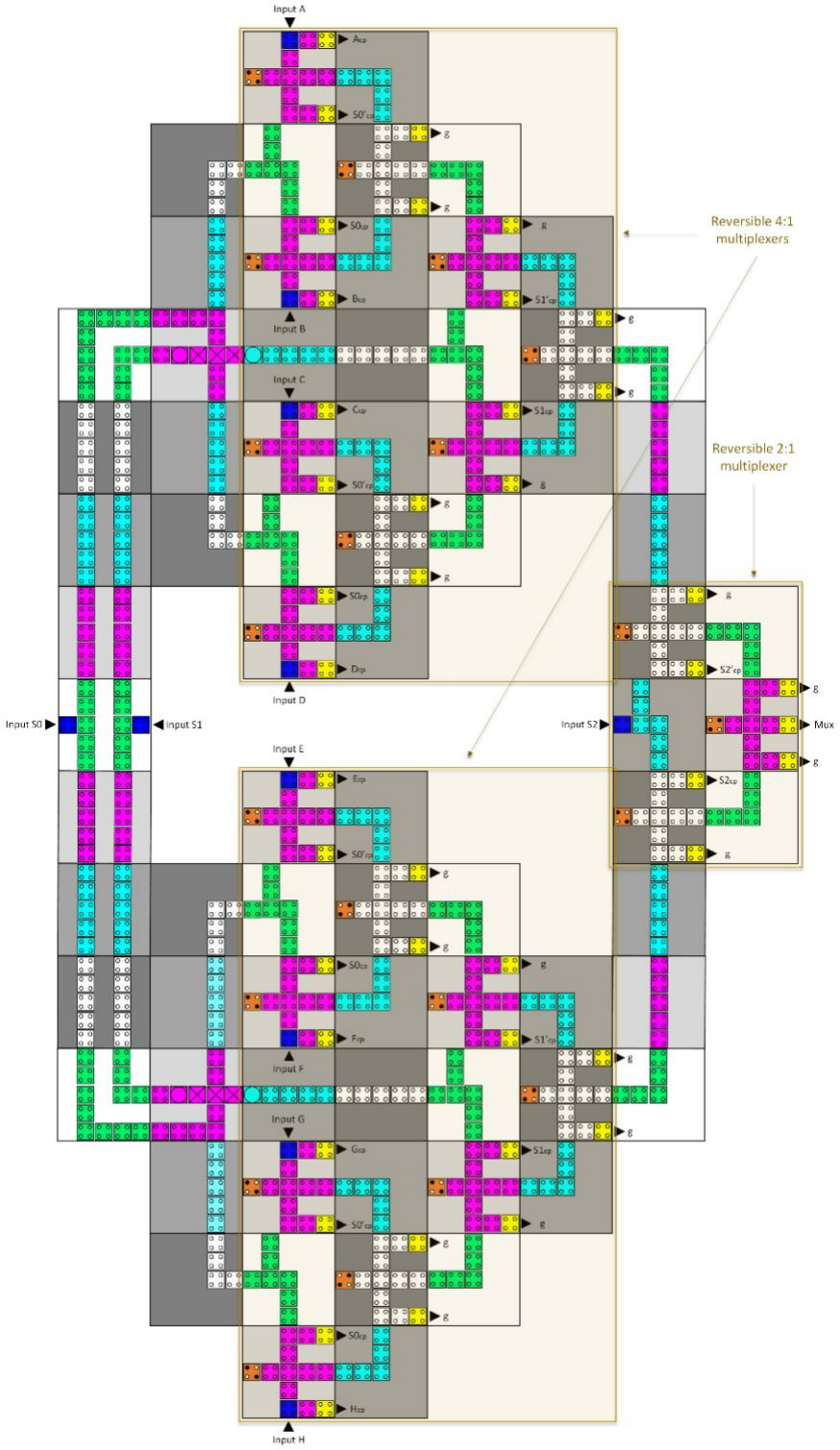
| S1 | S0 | Mux |
|---|---|---|
| 0 | 0 | A |
| 0 | 1 | B |
| 1 | 0 | C |
| 1 | 1 | D |

#### 5.1.1.3. Reversible QCA 8:1 multiplexer design

The construction of a logically and physically reversible QCA 8:1 multiplexer circuit can be achieved by employing two logically and physically reversible 4:1 multiplexers in conjunction with a single 2:1 logically and physically reversible multiplexer, resulting in a total of seven logically and physically reversible 2:1 multiplexers. Consequently, the logically and physically reversible QCA 8:1 multiplexer comprises 21 fully reversible majority gates (14 fully reversible AND gates and seven fully reversible OR gates) as well as seven single-branch inverters. This hierarchical design can be systematically divided into three distinct levels, as depicted in Figure 5.3. At the first level, a configuration of four 2:1 multiplexers generates four output signals, determined by the value of S0. Progressing to the second level, two 2:1 multiplexers produce two intermediate outputs, contingent upon the value of S1. Ultimately, at the third level, a single 2:1 multiplexer yields the final output, governed by the value of S2. Figure 5.3a displays the schematic diagram of the logically and physically reversible QCA 8:1 multiplexer, whereas Figure 5.3b displays the QCA cell layout architecture. This circuit incorporates a total of 646 QCA cells, encompassing a total area of 1.36 $\mu m^2$. The observed delay duration is 22 clock zones, which is equivalent to 5.5 clock cycles.




(a)




(b)

**Figure 5.3 (a) Logical synthesis design and (b) physical QCA layout of the proposed reversible QCA 8:1 multiplexer ($A_{cp}$, $B_{cp}$, $C_{cp}$, $D_{cp}$, $E_{cp}$, $F_{cp}$, $G_{cp}$, $H_{cp}$, $S0_{cp}$, $S1_{cp}$, $S2_{cp}$, $\overline{S0}_{cp}$, $\overline{S1}_{cp}$ and $\overline{S2}_{cp}$ indicate copies of the inputs, while g is so-called garbage output).**

Based on the Boolean input variables, Equation 5.3 shows how the proposed logically and physically reversible QCA 8:1 multiplexer circuit works at the output level. This equation encapsulates the logical relationships governing the circuit's operation. Correspondingly, Table 5.3 provides a comprehensive truth table that delineates the circuit's behaviour across all possible input combinations.

$$Mux = \left(\overline{S2}.\left(\overline{S1}.\left(\left(\overline{S0}.A\right) + (S0.B)\right)\right) + \left(S1.\left(\left(\overline{S0}.C\right) + (S0.D)\right)\right)\right) + \left(S2.\left(\overline{S1}.\left(\left(\overline{S0}.E\right) + (S0.F)\right)\right) + \left(S1.\left(\left(\overline{S0}.G\right) + (S0.H)\right)\right)\right) \quad (5.3)$$

**Table 5.3 Truth table for proposed 8:1 multiplexer circuit shown in Figure 5.3.**

| S1 | S0 | S1 | Mux |
|---|---|---|---|
| 0 | 0 | 0 | A |
| 0 | 0 | 1 | B |
| 0 | 1 | 0 | C |
| 0 | 1 | 1 | D |
| 1 | 0 | 0 | E |
| 1 | 0 | 1 | F |
| 1 | 1 | 0 | G |
| 1 | 1 | 1 | H |

### 5.1.2. Energy dissipation simulation results

The energy dissipation for each logically and physically reversible QCA multiplexer circuit, presented in Section 5.1.1, was calculated using the *QCADesigner-E 2.2* TCAD tool [96], applying the technology and simulation parameters presented in Table 2.1 and Table 2.2, respectively. Overall, the simulation results, shown in Table 5.4, demonstrate that using fully reversible 'AND' and 'OR' gates as a basic building block significantly improves the energy efficiency of the proposed logically and physically reversible QCA multiplexer circuits. Table 5.4 highlights the remarkably low energy dissipation values of the proposed logically and physically reversible multiplexer designs. Each elementary circuit used to build the 8:1 multiplexer circuit, including the ‘AND’ gate, the ‘OR’ gate,

the 2:1 multiplexer, and the 4:1 multiplexer, has an average energy dissipation that is lower than the Landauer energy threshold of 0.06 meV at a temperature of 1 K.

**Table 5.4 Energy dissipation analysis of the proposed multiplexer (The average energy dissipation refers to the mean energy value averaged over the various input signal combinations).**

| Proposed QCA Circuit | Total Energy Dissipation (meV) | Average Energy Dissipation (meV) |
|---|---|---|
| Reversible AND gate | 0.009 | 0.003 |
| Reversible OR gate | 0.009 | 0.002 |
| Reversible 2:1 multiplexer | 0.112 | 0.014 |
| Reversible 4:1 multiplexer | 0.525 | 0.057 |
| Reversible 8:1 multiplexer | 4.27 | 0.397 |

### 5.1.3. Cost calculation

This section presents the total cost associated with each logically and physically reversible QCA multiplexer design discussed in Section 5.1.1. The cost function in Equation 1.16, which is explained in Section 1.8, is used in the evaluation. It is a quantitative way to measure how efficient QCA circuits are.

Table 5.5 presents a comprehensive analysis of several critical metrics for each proposed logically and physically reversible QCA multiplexer design. This comprehensive breakdown includes the number of majority gates and inverters used, the number of crossovers implemented, the total QCA cell count, the occupied area, and the delay time associated with each design. Additionally, the table provides an evaluation of the overall cost, offering a holistic assessment of the efficiency and complexity of the proposed multiplexer circuits. These metrics collectively facilitate a thorough comparison and evaluation of the design trade-offs inherent in each multiplexer configuration.

**Table 5.5 QCA multiplexers cost.**

| QCA Multiplexer Circuit | Majority gates | Inverters | Crossing | QCA cells | Area ($\mu m^2$) | Delay [clock cycle] | Cost function (FOM) |
|---|---|---|---|---|---|---|---|
| Reversible 2:1 multiplexer | 3 | 1 | 0 | 56 | 0.09 | 1 | 10 |
| Reversible 4:1 multiplexer | 9 | 3 | 0 | 213 | 0.46 | 3 | 252 |
| Reversible 8:1 multiplexer | 21 | 7 | 2 | 646 | 1.36 | 5.5 | 2475 |

### 5.1.4. Discussion

For a comprehensive energy analysis, the energy dissipation of the proposed logically and physically reversible multiplexer circuits has been compared with that of existing designs in the literature, all evaluated under the same technological parameters as outlined in Table 2.1. First, the energy efficiency of the proposed logically and physically reversible QCA 2:1 multiplexer circuit has been compared against the energy dissipation values of the QCA 2:1 multiplexers reported in previous studies. Table 5.6 presents the comparative results, while Figure 5.4 illustrates them. The simulation results of the proposed logically and physically reversible QCA 2:1 multiplexer circuit demonstrate a significant 98% reduction in energy dissipation when compared to the most energy-efficient QCA 2:1 multiplexer circuit design previously reported in the literature [169].

**Table 5.6 Energy dissipation comparison of the 2:1 multiplexer circuit.**

| QCA 2:1 Multiplexer | Total Energy Dissipation (meV) | Average Energy Dissipation (meV) |
|---|---|---|
| [171] | 16.20 | 1.38 |
| [172] | 15.20 | 1.38 |
| [173] | 13.86 | 1.29 |
| [174] | 12.40 | 1.14 |
| [175] | 11.30 | 1.02 |
| [169] | 8.91 | 0.810 |
| **Proposed** | **0.112** | **0.014** |

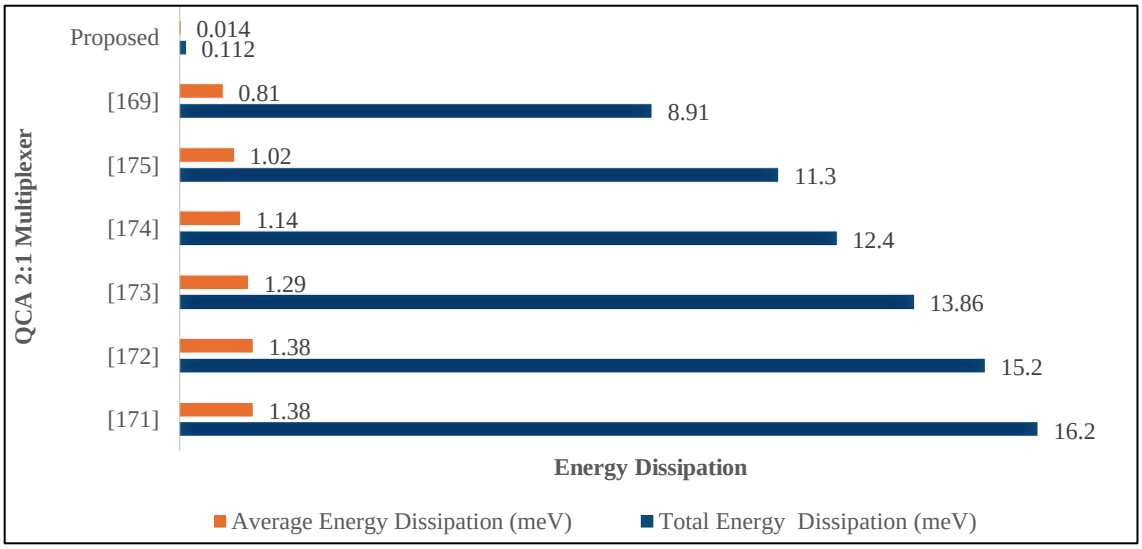



**Figure 5.4 Energy dissipation comparison of the 2:1 multiplexer circuit.**

Second, the energy dissipation values of the proposed logically and physically reversible QCA 4:1 multiplexer circuit were compared to the energy dissipation results of QCA 4:1 multiplexers from previous research. Table 5.7 and Figure 5.5 are presenting the simulation results. The proposed design demonstrates a remarkable 97% improvement in energy efficiency compared to the most energy-efficient 4:1 multiplexer circuit previously reported in the literature [169].

**Table 5.7 Energy dissipation comparison of the 4:1 multiplexer circuit.**

| QCA 4:1 Multiplexer | Total Energy Dissipation (meV) | Average Energy Dissipation (meV) |
|---|---|---|
| [176] | 97.1 | 15.65 |
| [177] | 27.73 | 4.76 |
| [178] | 19.42 | 2.54 |
| [169] | 17.9 | 1.63 |
| **Proposed** | **0.525** | **0.057** |

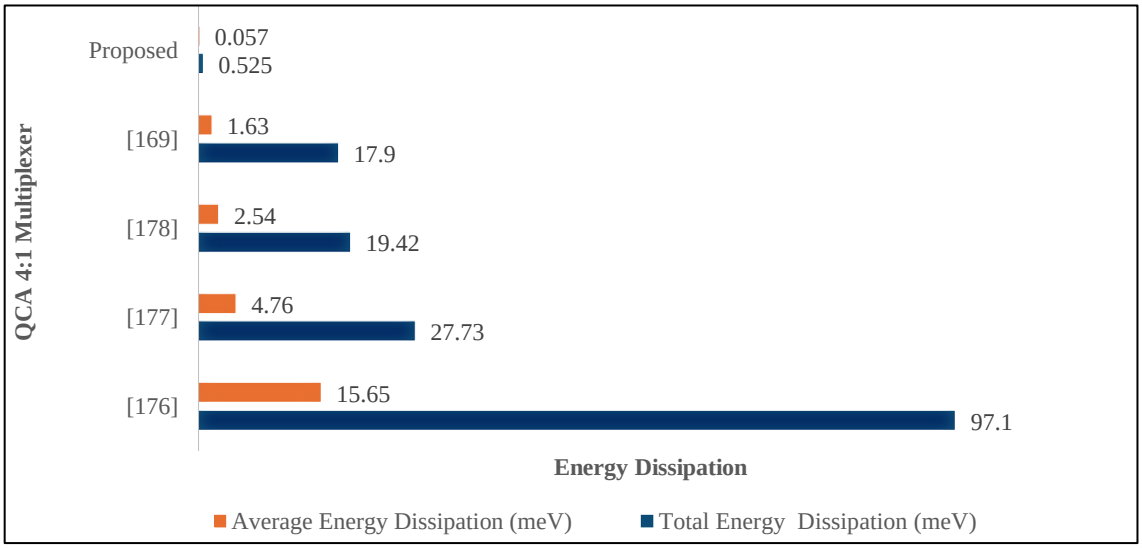



**Figure 5.5 Energy dissipation comparison of the 4:1 multiplexer circuit.**

Finally, the energy dissipation values of the innovative logically and physically reversible QCA 8:1 multiplexer circuit were compared with the energy dissipation results of previously researched QCA 8:1 multiplexers. Table 5.8 and Figure 5.6 provide a comparative analysis of energy dissipation results. This comparison highlights the significant advancements made in energy efficiency through the proposed design. Specifically, the results demonstrate an 89% reduction in power consumption when

compared to the most energy-efficient QCA 8:1 multiplexer circuit design previously reported in the literature [169]. This substantial decrease underscores the effectiveness of the proposed logically and physically reversible design approach in minimising energy dissipation, further establishing the proposed circuit as a highly efficient solution within the realm of QCA-based multiplexer designs.

**Table 5.8 Energy dissipation comparison of the 8:1 multiplexer circuit.**

| QCA 8:1 Multiplexer | Total Energy Dissipation (meV) | Average Energy Dissipation (meV) |
|---|---|---|
| [179] | 1110 | 370 |
| [180] | 700 | 250 |
| [173] | 205 | 53 |
| [181] | 108 | 46 |
| [169] | 39.3 | 3.58 |
| **Proposed** | **4.27** | **0.397** |

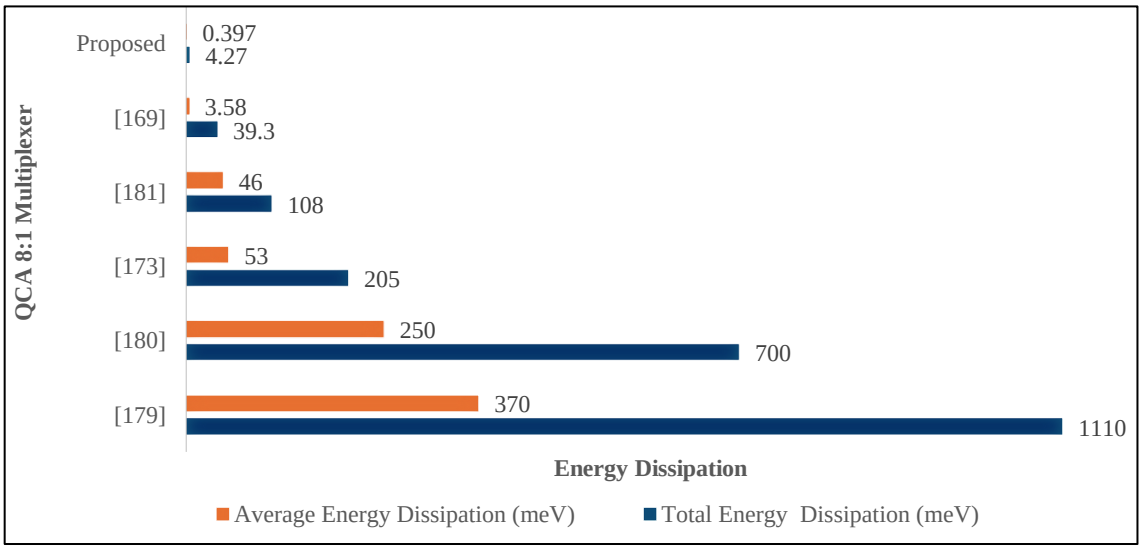



**Figure 5.6 Energy dissipation comparison of 8:1 multiplexer circuit.**

### 5.1.5. Summary for designing a reversible QCA 8:1 multiplexer

Multiplexers are fundamental components in many digital circuits, serving as essential elements for data routing and selection operations. The primary objective of this section was to design a logically and physically reversible 8:1 multiplexer circuitthat demonstrates exceptionally low power consumption, a critical factor in the advancement of energy-efficient digital systems. The process began with the development of a novel,

logically and physically reversible QCA 2:1 multiplexer circuit. This circuit was then employed as the foundational building block, for constructing logically and physically reversible QCA 4:1 and 8:1 multiplexer circuits, utilising hierarchical design techniques to be able to tackle the complexity, while maintaining reversibility and efficiency.

The power dissipation of these circuits was evaluated using the *QCADesigner-E 2.2* TCAD tool, which provides a detailed microscopic description of QCA physics. The simulation results, conducted with the parameters specified in Table 2.2, reveal that the logically and physically reversible QCA 2:1, 4:1, and 8:1 multiplexer circuits designed in this study achieve remarkable reductions in energy dissipation, specifically 98%, 97%, and 89% less energy, respectively, compared to the most energy-efficient QCA multiplexer circuits previously reported in the literature using the same standard technological parameters outlined in Table 2.1.

### 5.2. Reversible QCA ALU

The ALU is an integral component of the central processing unit (CPU), serving as the engine for executing a wide range of logical and arithmetic operations [182]. These operations are essential for the CPU's data processing and manipulation. The ALU operates by receiving input data from various sources, including registers, memory, or other peripheral devices. After processing this data, the ALU produces an output that it then transmits to a designated destination, which could be another register, a memory location, or an external device. This seamless flow of data through the ALU is fundamental to the CPU's overall functionality, enabling the execution of complex computational tasks necessary for the operation of modern nanocomputing systems.

Designing QCA ALUs using a logically and physically reversible design approach represents a significant advancement in the design of energy-efficient computational units. Their ability to reduce power consumption while maintaining high computational density and speed makes them an attractive solution for next-generation digital systems, especially in contexts where energy efficiency and minimisation of heat generation are paramount.

### 5.2.1. Designing reversible QCA ALU

This section presents a design for an innovative logically and physically reversible QCA ALU to achieve ultra-low energy efficiency. This design leverages a series of combinational logic circuits, each constructed with a focus on both logical and physical reversibility, ensuring minimal energy dissipation. The foundation of these circuits lies in the innovative application of the fully reversible design methodology, as outlined in Chapter 2. By applying the reversible design method, the ALU optimizes not only computational efficiency but also aligns with the growing demand for energy-conscious computing solutions, making it a significant advancement in the field of reversible computing.

The development process commenced with the creation of a high-level block diagram, which laid the foundation for the architecture of the proposed reversible ALU. As depicted in Figure 5.7, this architecture comprises three primary components: the Logic Unit (LU), the Arithmetic Unit (AU), and the Control Unit (CU). The Logic Unit (LU) is responsible for executing a set of logical operations on the input data, including AND, NAND, OR, NOR, XOR, XNOR, NOT, and transfer functions. Meanwhile, the Arithmetic Unit (AU) handles various arithmetic operations, such as addition, subtraction, multiplication, and division of binary numbers. The Control Unit (CU) plays the role of determining the nature of the operation, whether arithmetic or logical, based on its input signal, S0. This structured and modular approach to the ALU's design ensures both functionality and energy efficiency in processing data.

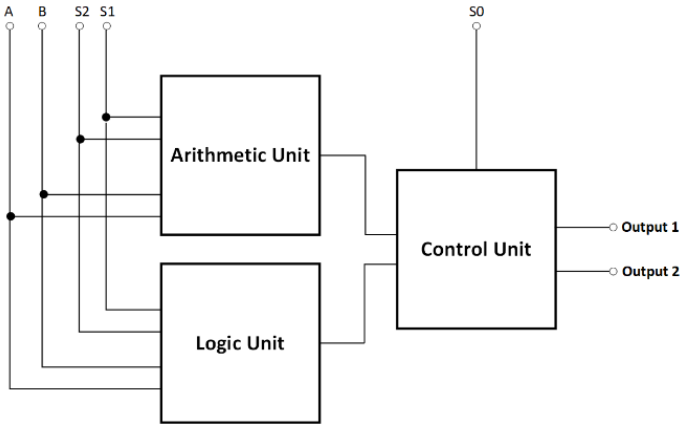



**Figure 5.7 The High-level block diagram of the proposed reversible QCA ALU**

The design of the reversible QCA ALU processes two input operands, A and B, and generates two corresponding output values, Output 1 and Output 2. The reversible nature of the circuit allows for the interchange or reverse of the outputs, thereby enabling the simultaneous execution of two distinct operations, either arithmetic or logical. This dual-functionality results in a comprehensive set of 16 operations, evenly divided between 8 logical and 8 arithmetic functions, as illustrated in Table 5.9. Three select input pins, designated as S0, S1, and S2, govern the selection of the specific operation to perform and the choice of operands. These select inputs are critical in configuring the ALU to carry out the desired operation, thereby offering significant flexibility and efficiency in computational tasks. The reversible QCA ALU's ability to perform multiple operations concurrently, not only enhances computational throughput, but also exemplifies the innovative potential of reversible computing paradigms in reducing power dissipation and improving the overall efficiency of digital computing circuits.

**Table 5.9 The operations of the proposed reversible QCA ALU.**

| Operation Type | Control Inputs | | | Output 1 | Output 2 (Inversion of Input 1) |
|---|---|---|---|---|---|
| | S0 | S1 | S2 | | |
| Logic operations (LU) | 0 | 0 | 0 | AND | NAND |
| | 0 | 0 | 1 | OR | NOR |
| | 0 | 1 | 0 | Buffer | NOT (Inverter) |
| | 0 | 1 | 1 | XOR | XNOR |
| Arithmetic operations (AU) | 1 | 0 | 0 | A+B | 1'Complement (A+B)' |
| | 1 | 0 | 1 | $C_{out}$ | A.B |
| | 1 | 1 | 0 | A'.B | (A'B)' |
| | 1 | 1 | 1 | A-B | (A-B)' |

#### 5.2.1.1. Logical synthesis design of the reversible QCA ALU

The synthesis process for each circuit block was initiated by designing and simulating the components to ensure accurate circuit behaviour. The logical synthesis designs for the Arithmetic Unit (AU), Logic Unit (LU), and Control Unit (CU) were carefully developed. These designs involved the careful definition and generation of netlists, as well as the establishment of precise input-output relationships for the circuits. To validate the performance and functionality of these synthesised circuits, simulations were conducted using *Logisim 2.7.1* logic simulation software, which provided a reliable environment for

testing and verification. During this phase, the circuit designs were assessed to ensure that they met the expected logical and operational criteria. The reversible logic circuit synthesis diagrams explicitly label certain outputs to clarify their roles: "cp" outputs are duplicates of the corresponding inputs, while "g" outputs are considered garbage outputs. The inclusion of garbage outputs is a characteristic of reversible computing, where they are necessary to maintain the reversibility of the logic functions. These outputs, although not useful for the primary computation, are essential for preserving the information required for the operations' reversibility.

Figure 5.8 illustrates the design of the proposed reversible LU. This LU is composed of a combination of key reversible components, including two reversible majority gates, an XOR gate, an inverter, a buffer, and a 4:1 multiplexer. These elements are connected up to facilitate the execution of eight distinct logic operations. The reversible majority gates play a paramount role in decision-making processes within the circuit, while the XOR gate, inverter, and buffer contribute to the necessary logic manipulations. The 4:1 multiplexer is employed to select the appropriate logic operation based on the input signals, ensuring the versatility and efficiency of the reversible LU in performing multiple logic functions.

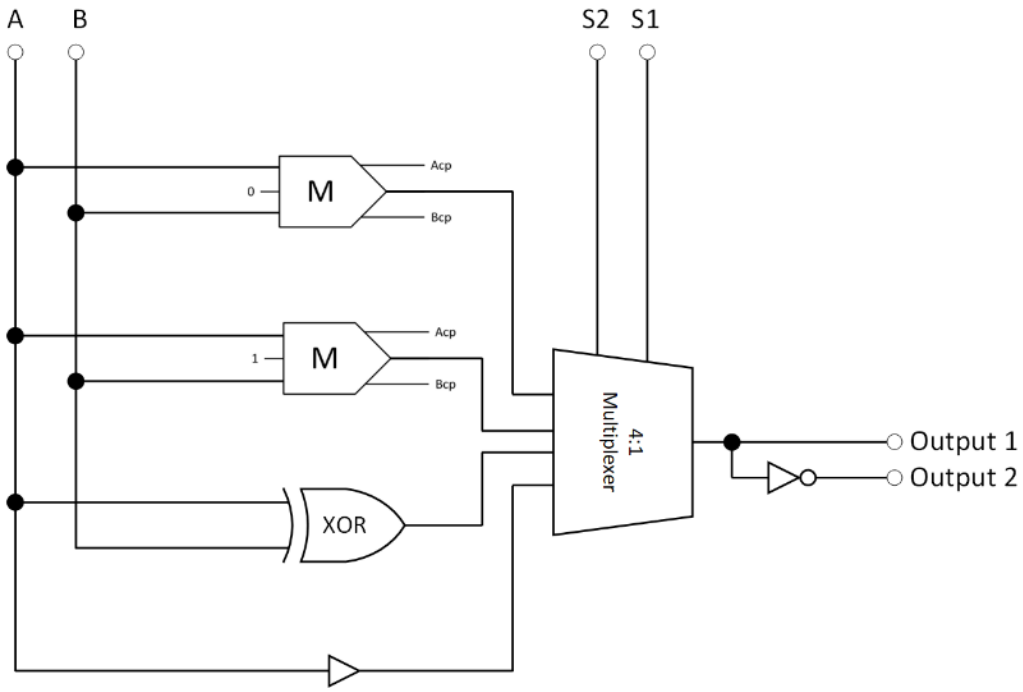



**Figure 5.8 The synthesis of the proposed reversible LU ($A_{cp}$ and $B_{cp}$ refer to copies of the inputs).**

Figure 5.9 depicts the architecture of the proposed reversible AU. This AU integrates several key components to achieve its functionality, including a half-adder, a half-subtractor, two reversible majority gates, an inverter, and a 4:1 multiplexer circuit. The strategic combination of these components enables the execution of eight distinct arithmetic operations. The half-adder and half-subtractor form the core of the arithmetic operations, facilitating the basic addition and subtraction processes. The reversible majority gates aid in decision-making and logic determination within the AU, while the inverter provides the required signal inversion. Based on the input control signals, the 4:1 multiplexer allows the choice of the right arithmetic operation. This makes sure that the reversible AU can do a wide range of arithmetic tasks quickly and correctly.

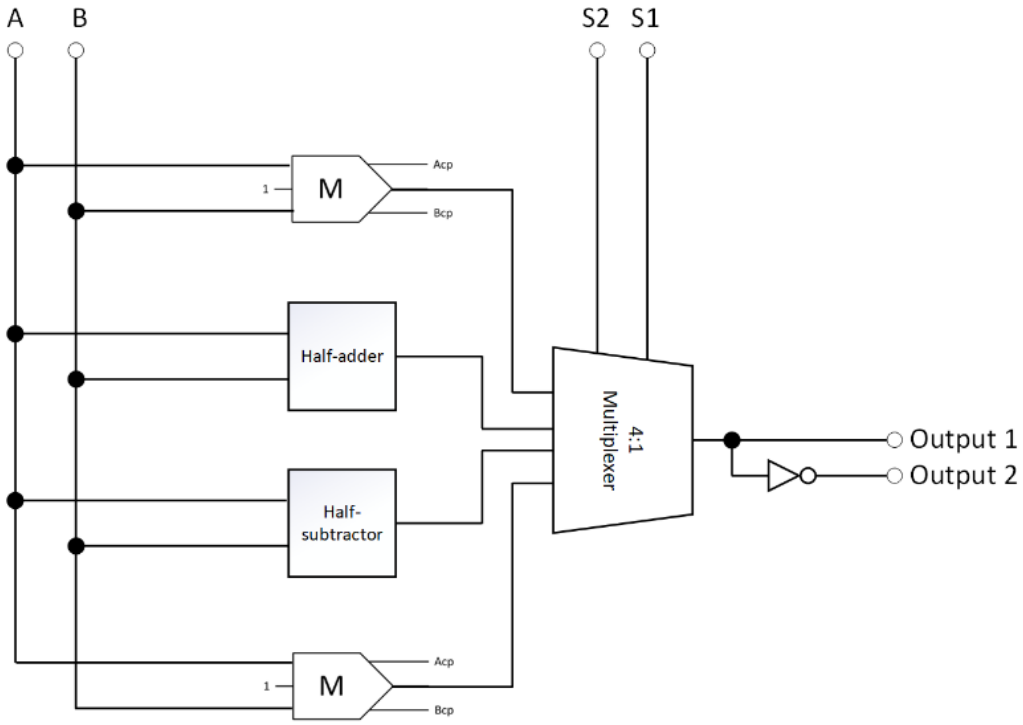



**Figure 5.9 The synthesis of the proposed reversible AU ($A_{cp}$ and $B_{cp}$ refer to copies of the inputs).**

Subsequently, the internal components essential for constructing the reversible LU and AU were developed. The circuits constituting the proposed reversible LU and AU include the reversible XOR gate, reversible half-adder, reversible half-subtractor, and reversible 4:1 multiplexer. Each of these circuits was carefully designed with a focus on maintaining the principles of reversibility, ensuring minimal power dissipation, and efficient

computation. The design process involved rigorous attention to detail, particularly in preserving the integrity of logical operations, while adhering to the constraints of reversible computing. To validate the reliability and functionality of these components, comprehensive simulations were conducted, confirming that each circuit performs as expected under various operational conditions. These simulations not only verified the correctness of the designs but also demonstrated their robustness in practical applications, thus laying a solid foundation for the overall architecture of the reversible LU and AU.

Figure 5.10 presents the synthesis design of the proposed reversible XOR gate. The design consists of two inverters and three reversible majority gates, forming the core structure of the XOR logic operation within a reversible computing framework. The design is optimised to adhere to the principles of reversibility, ensuring that no information is lost during the logical operations, thereby minimising energy dissipation. Equation 5.4 provides the standard Boolean expression representing the output of this reversible XOR logic circuit. This equation encapsulates the functional behaviour of the circuit, providing a mathematical foundation for its operation within more complex reversible systems. The combination of inverters and majority gates within this design is crucial for achieving the desired logical outcomes while maintaining the reversibility required in advanced energy efficient QCA circuits.

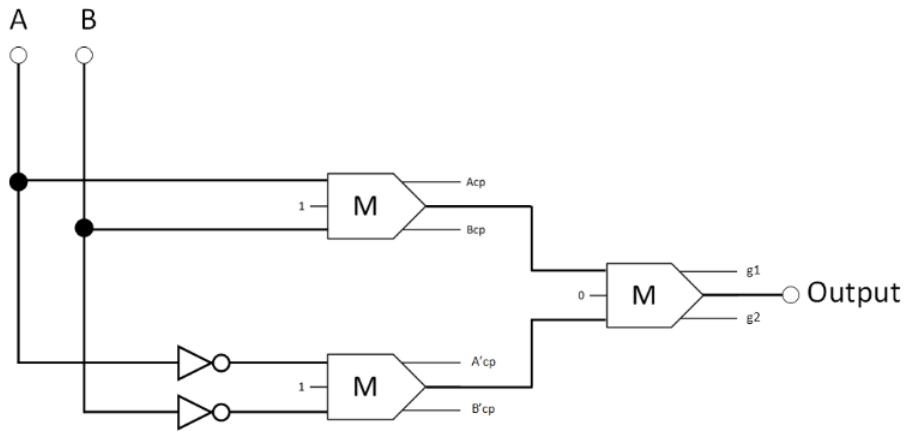



**Figure 5.10 The synthesis of the proposed reversible XOR ($A_{cp}$, $B_{cp}$, $A'_{cp}$, and $B'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

$$Output = (A + B).(\overline{A} + \overline{B}) \tag{5.4}$$

Figure 5.11 illustrates the proposed reversible half-adder circuit, which consists of four reversible majority gates and two inverters. The carefully engineered configuration enables the half-adder to perform addition operations while adhering to the principles of reversibility, ensuring no information loss and maintaining energy efficiency. The circuit leverages the reversible majority gates for decision-making and the inverters for signal processing, resulting in a fully reversible computation. Equation 5.5 gives the Boolean expressions that define the operation of this reversible half-adder circuit. These mathematical expressions represent the circuit's logical functions, capturing the relationship between the inputs and the resulting sum and carry outputs. The use of reversible components in this design exemplifies the potential for creating efficient, low-power arithmetic circuits suitable for integration into more complex reversible computing systems.

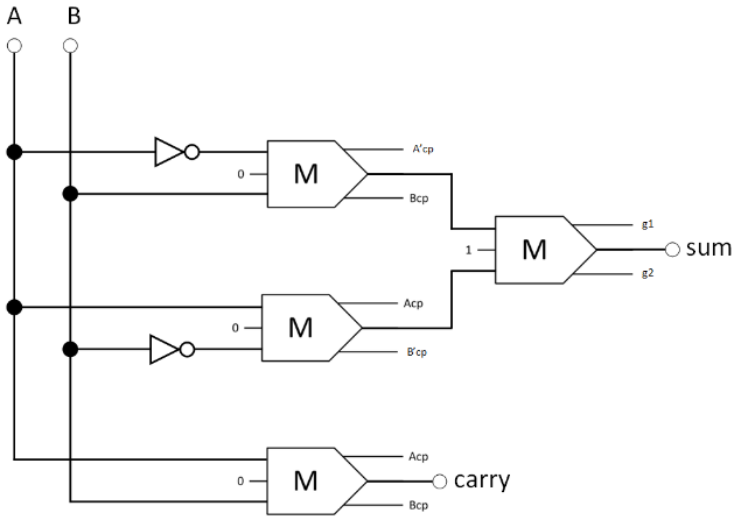



**Figure 5.11 The synthesis of the proposed reversible half-adder ($A_{cp}$, $B_{cp}$, $A'_{cp}$, and $B'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

$$\begin{aligned} \text{Sum} &= \left(\text{A}.\overline{\text{B}}\right) + \left(\overline{\text{A}}.\text{B}\right) \\ \text{Carry} &= (\text{A}.\text{B}) \end{aligned} \tag{5.5}$$

Two inverters and three reversible majority gates construct the proposed circuit for the reversible half-subtractor, as shown in Figure 5.12. This design is optimised to perform subtraction operations in a reversible manner, ensuring that all input information is

preserved, and no energy is dissipated unnecessarily. The reversible majority gates play a central role in determining the logical output based on the inputs, while the inverters provide the necessary signal inversion to complete the subtraction process. Equation 5.6 gives the Boolean expression that characterises the output of this reversible half-subtractor circuit. This expression encapsulates the circuit's functional behaviour, detailing the logical relationship between the inputs and the difference and borrow outputs, and ensuring that the circuit operates correctly within reversible logic constraints. The efficient design of this circuit makes it a vital component for advanced reversible computing architectures.

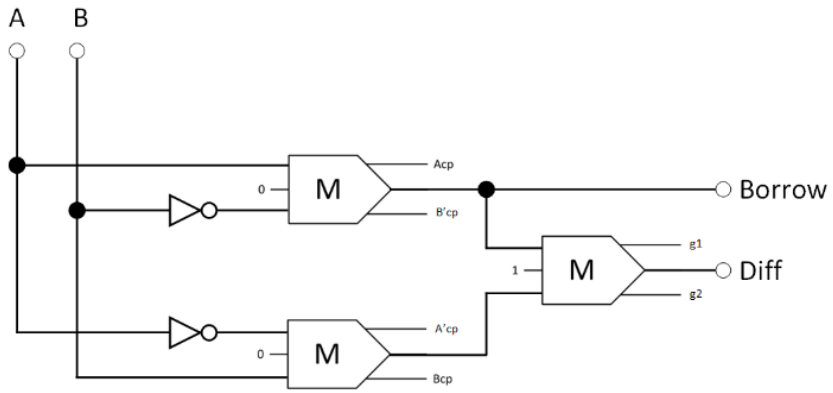



**Figure 5.12 The synthesis of the proposed reversible half-subtractor ($A_{cp}$, $B_{cp}$, $A'_{cp}$, and $B'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

$$\begin{aligned} \text{Diff} &= \left(\overline{\text{A}}.\,\text{B}\right) + \left(\text{A}.\,\overline{\text{B}}\right) \\ \text{Borrow} &= \left(\overline{\text{A}}.\,\text{B}\right) \end{aligned} \tag{5.6}$$

The proposed circuit for the reversible 4:1 multiplexer, as illustrated in Figure 5.13, consists of three inverters and nine reversible majority gates. This sophisticated design is tailored to perform multiplexing operations while adhering to the principles of reversible logic, ensuring minimal energy loss and preserving input information. The selection process relies on the reversible majority gates, which route the input to the output based on the control signals, and the inverters, which provide the necessary signal inversions to achieve the correct logical output. Equation 5.7 details the Boolean equation that defines the output of this reversible 4:1 multiplexer circuit. This equation captures the precise

logical relationship between the inputs, control signals, and the resulting output, ensuring that the circuit functions correctly and efficiently within a reversible computing framework. The design serves as an essential component for advanced digital systems, demonstrating the reversible implementation of complex logical operations.

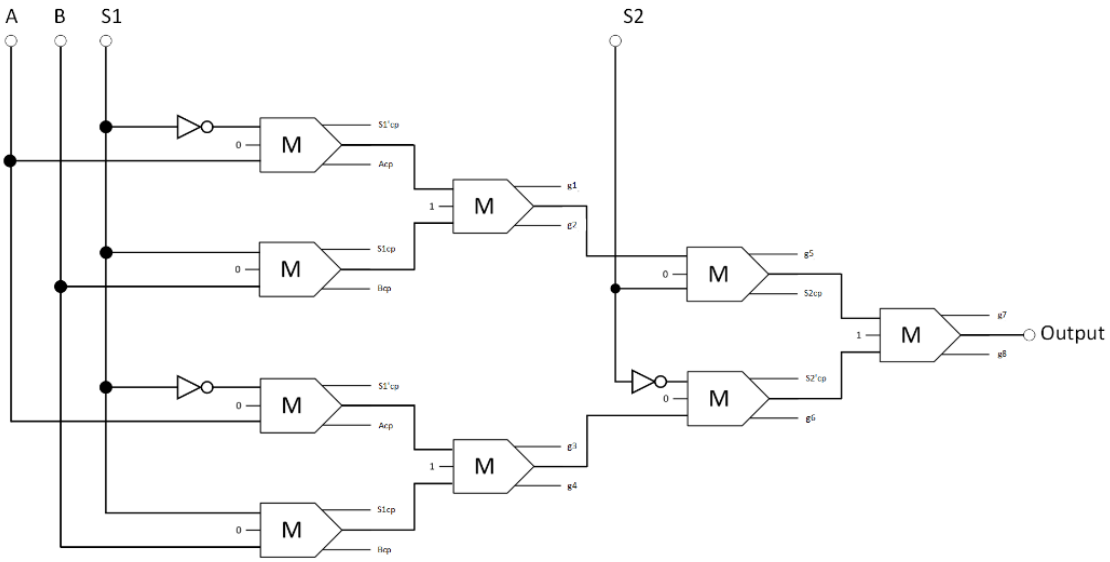



**Figure 5.13 The synthesis of the proposed reversible 4:1 multiplexer ($A_{cp}$, $B_{cp}$, $S1_{cp}$, $S2_{cp}$, $S1'_{cp}$, and $S2'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

$$\text{Output} = \left(\left(\left(\overline{\text{S1}}.\text{A}\right) + \left(\text{S1}.\text{B}\right)\right).\text{S2}\right) + \left(\left(\left(\overline{\text{S1}}.\text{A}\right) + \left(\text{S1}.\text{B}\right)\right).\overline{\text{S2}}\right) \qquad (5.7)$$

Figure 5.14 depicts the logical synthesis of the control unit CU. This design employs a reversible 2:1 multiplexer as the CU, which activates either the AU or the LU to carry out the corresponding arithmetic or logic operation. This reversible 2:1 multiplexer is constructed using three reversible majority gates and an inverter, ensuring that the selection process adheres to the principles of reversible logic, thereby preserving input information and minimising energy dissipation. Equation 5.8 provides the Boolean expression governing the output of the proposed 2:1 multiplexer circuit. The multiplexer performs a logical operation, where the control signal determines which unit, AU or LU, to activate based on the input conditions. This reversible multiplexer's design is critical for the overall functionality of the CU because it ensures efficient and accurate selection between arithmetic and logic operations within the reversible computing framework.

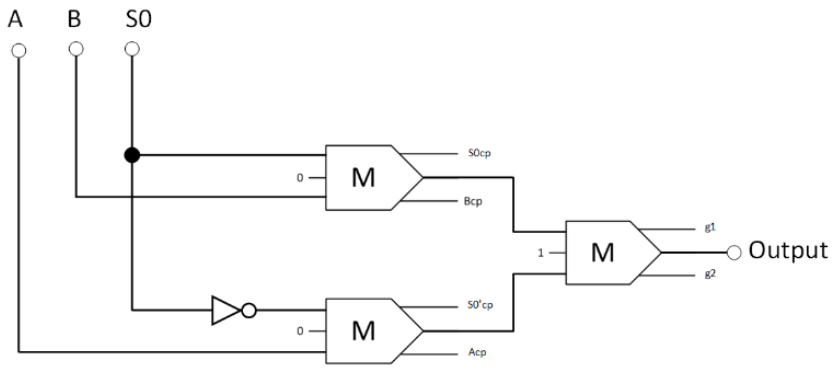



**Figure 5.14 The synthesis of the proposed reversible 2:1 multiplexer ($A_{cp}$, $B_{cp}$, $S0_{cp}$, and $S0'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

$$Output = (A.\overline{S0}) + (B.S0) \tag{5.8}$$

#### 5.2.1.2. Physical layout of the reversible QCA ALU

The logical synthesis for each component, building up the ALU, was subsequently translated into a physical QCA layout suitable for fabrication on a semiconductor chip. QCA technology creates the physical layout by interconnecting a group of QCA cells to form a functional circuit, with QCA cells forming both wiring and logic devices. The physical layout of the introduced reversible QCA ALU was constructed using the *QCADesigner 2.0.3* TCAD tool. This layout development process is intricate, involving several key steps, such as partitioning, placement, and routing. Each of these steps plays a crucial role in effectively realising the logical design in a physical form, all while maintaining the circuit's functionality and performance.

Initially, the layout configurations for the reversible QCA XOR, half adder, half subtractor, 2:1 multiplexer, and 4:1 multiplexer were developed. Subsequently, the layout configuration of the reversible QCA LU, AU, and CU that constitute the reversible QCA ALU were constructed using these foundational reversible QCA circuits. The layout of each of these circuits was constructed according to the reversible design methodology outlined in Chapter 2. This methodology is crucial for ensuring that the circuits adhere to the principles of reversibility, which are essential for minimising power dissipation and maintaining the integrity of input information, throughout the computation process. The

block diagram in Figure 5.7 guided the interconnection of these QCA digital circuit blocks, leading to the proposed reversible QCA ALU layout.

Figure 5.15 illustrates the layout of the proposed reversible QCA XOR logic gate. The proposed reversible QCA XOR gate demonstrates a delay time of eight clock zones, equivalent to two clock cycles. The gate occupies an area of 0.15 μm², reflecting a compact design that is well-suited for integration into larger circuits. Furthermore, the design employs a total of 101 QCA cells, demonstrating the layout's efficiency in terms of cell usage. This combination of low delay time, minimal area, and efficient cell utilization highlights the effectiveness of the proposed reversible QCA XOR gate within the context of the advanced reversible QCA computing circuit design.

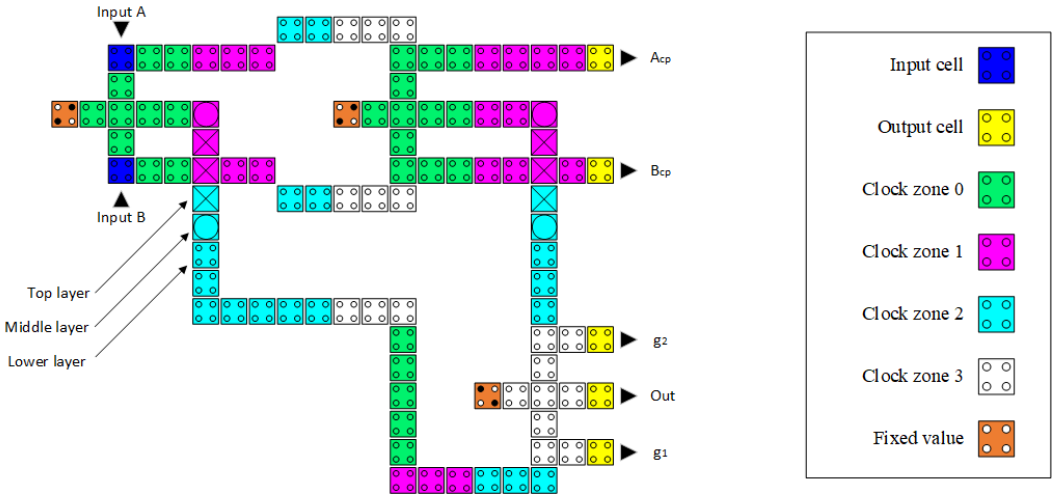



**Figure 5.15 The layout of the proposed reversible QCA XOR ($A_{cp}$ and $B_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

Figure 5.16 illustrates the layout of the proposed reversible QCA half-adder circuit. The proposed reversible QCA half-adder exhibits a delay of 12 clock zones, corresponding to three clock cycles. The circuit occupies an area of 0.27μm$^2$ and requires 156 QCA cells, making it relatively compact considering its functionality. These specifications for delay, area, and QCA cell counts reflect the careful balance between performance and resource utilisation in the design of this reversible QCA half-adder, ensuring it meets the necessary criteria for efficient operation within more advanced reversible computing systems.

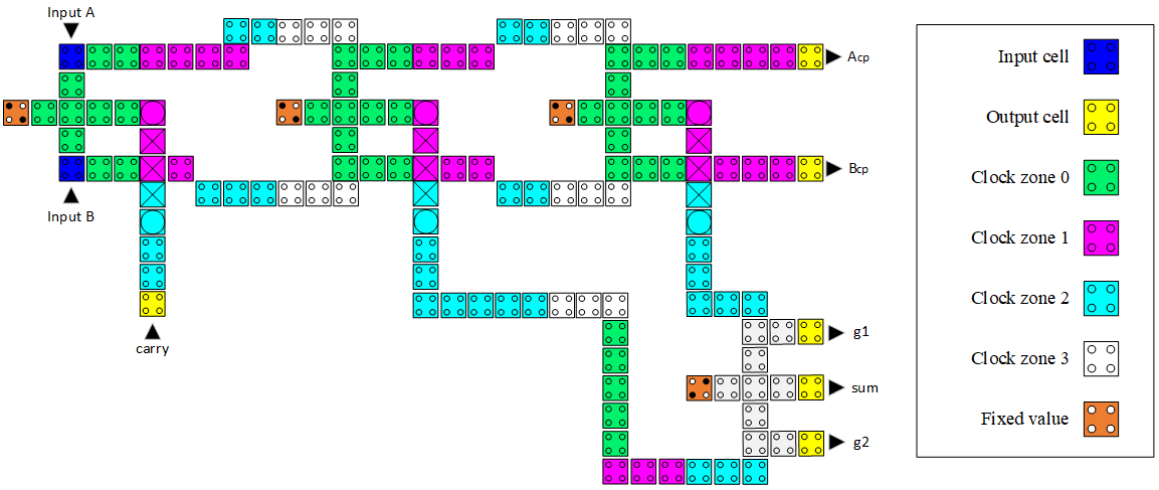



**Figure 5.16 The layout of the proposed reversible QCA half-adder ($A_{cp}$ and $B_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

Figure 5.17 illustrates the layout of the proposed reversible QCA half-subtractor circuit. The reversible QCA half-subtractor has a latency of eight clock zones, which is equivalent to two clock cycles. The circuit occupies an area of 0.15 $\mu m^2$, reflecting its efficient use of space. The implementation of this half-subtractor requires 116 QCA cells, highlighting the balance between achieving reversibility and maintaining a compact design. Finally, the proposed design works well in providing a low-latency, space-efficient solution for reversible QCA circuit architectures based on these factors: latency, area, and cell count.

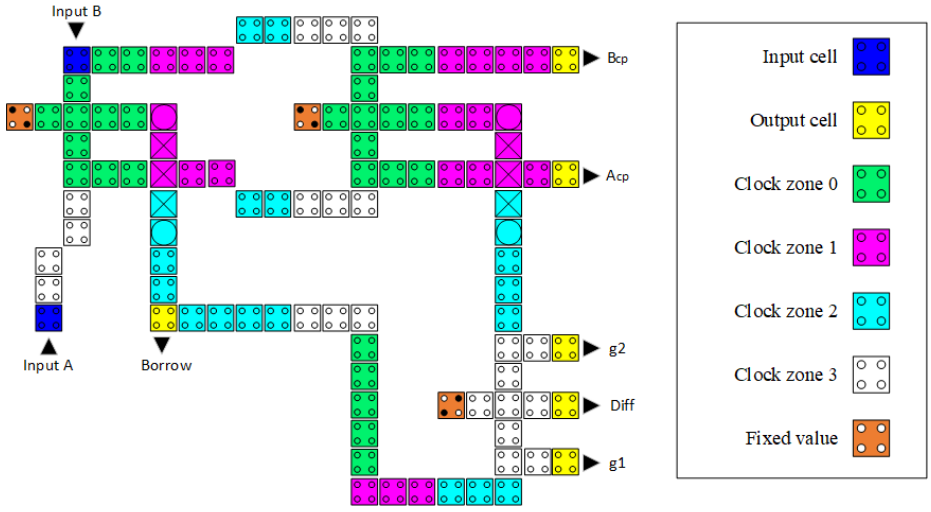



**Figure 5.17 The layout of the proposed reversible QCA half-subtractor ($A_{cp}$ and $B_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

Figure 5.18 illustrates the layout of the proposed reversible QCA 2:1 multiplexer. The reversible QCA 2:1 multiplexer is delaying four clock zones, corresponding to one clock cycle. The implementation of this multiplexer is resource-efficient, requiring only 56 QCA cells and occupying an area of 0.09 $\mu m^2$. These specifications highlight the multiplexer's low-latency performance and compact design, making it an ideal component for integration into more complex reversible QCA circuits. The efficient use of QCA cells and minimal area requirements further underscore the multiplexer's suitability for applications where space and speed are critical considerations.

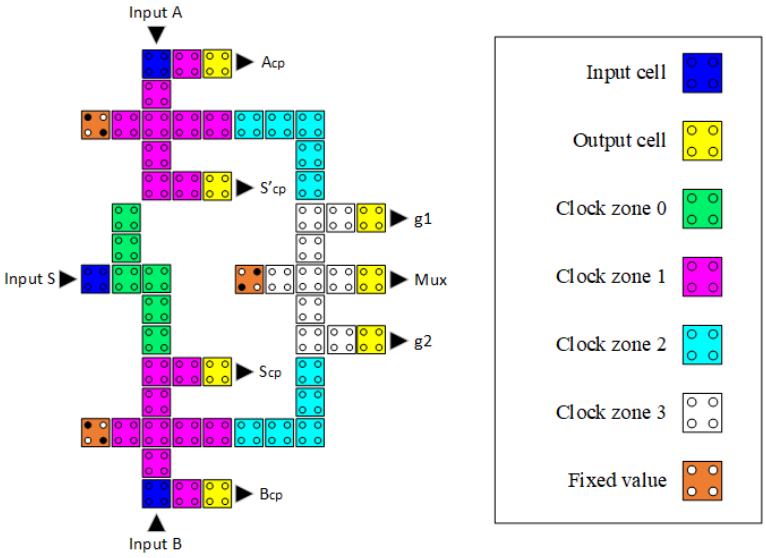



**Figure 5.18 The layout of the proposed reversible QCA 2:1 multiplexer ($A_{cp}$, $B_{cp}$, $S_{cp}$, and $S'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).**

Figure 5.19 illustrates the layout of the proposed reversible QCA 4:1 multiplexer. The circuit for the reversible QCA 4:1 multiplier was constructed by integrating three 2:1 multiplexers. This design requires 213 QCA cells, occupies an area of 0.46 µm2, and exhibits a delay time of 12 clock zones, which is equivalent to three clock cycles. The integration of multiple 2:1 multiplexers to create the 4:1 configuration results in a more complex design, reflected in the higher cell count and area usage. Despite this complexity, the circuit maintains an efficient delay time, making it a robust choice for applications that demand both versatility and performance in reversible QCA circuit designs.

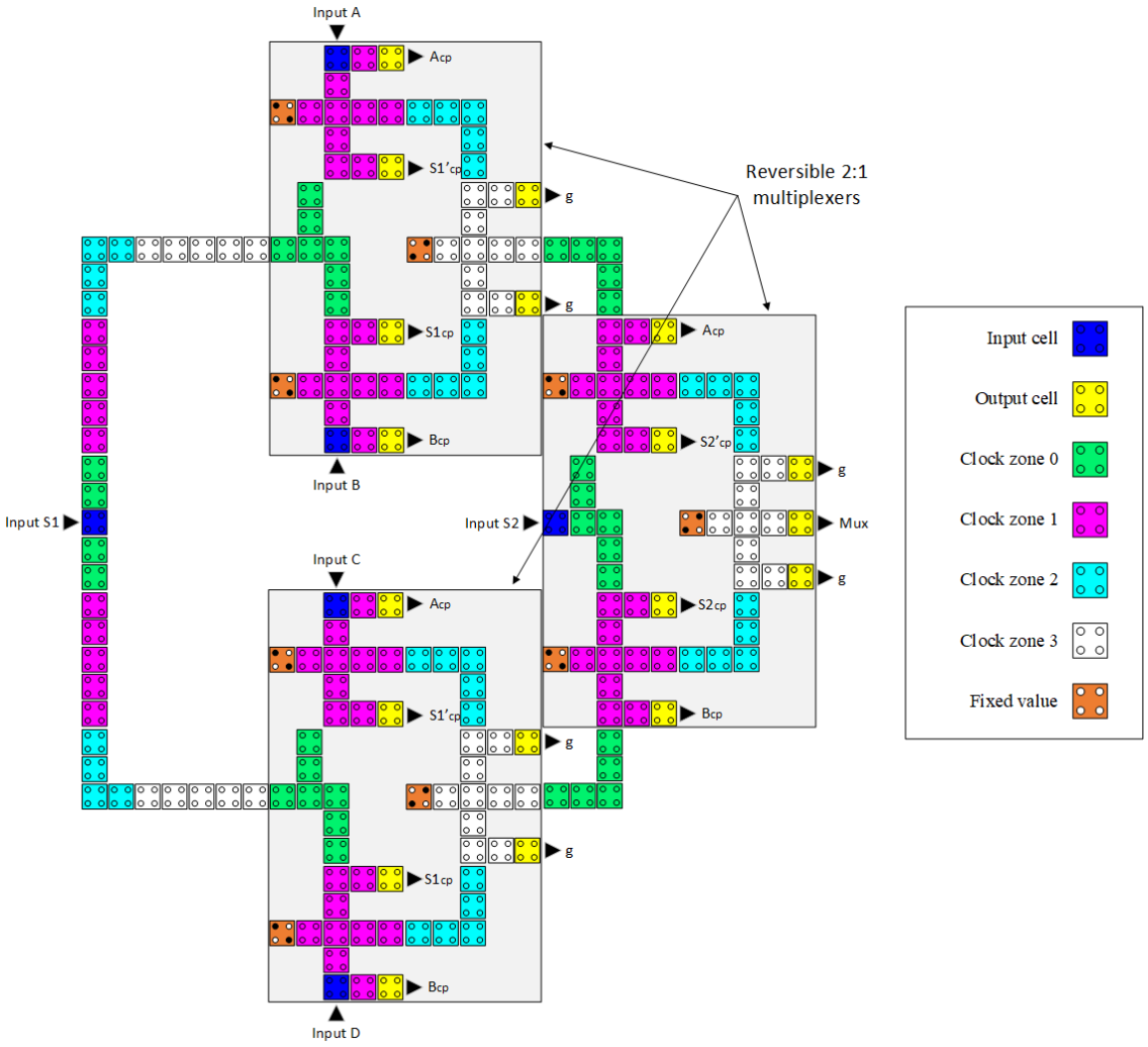



**Figure 5.19 The layout of the proposed reversible QCA 4:1 multiplexer ($A_{cp}$, $B_{cp}$, $C_{cp}$, $D_{cp}$, $S1_{cp}$, $S1'_{cp}$, $S2_{cp}$, and S2'cp refer to copies of the input data, whereas g variables indicate the garbage outputs).**

Figure 5.20 illustrates the layout of the proposed reversible QCA LU. The proposed reversible QCA LU was constructed by integrating three reversible QCA majority gates, a reversible QCA XOR gate, and a reversible QCA 4:1 multiplexer. This reversible QCA LU exhibits a latency of 14 clock zones (equivalent to 3.5 clock cycles), an area cost of 0.63 µm2, and requires 380 QCA cells for implementation.

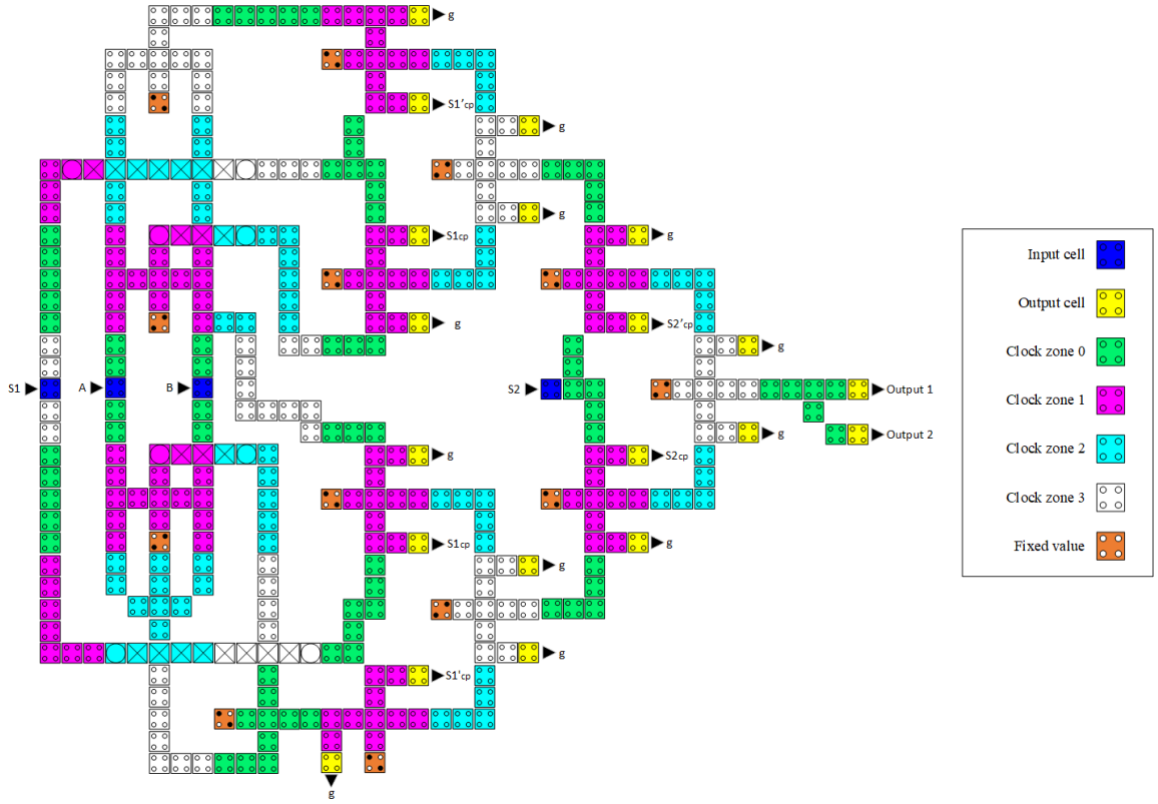



**Figure 5.20 The layout of the proposed reversible QCA LU ($S1_{cp}$, $S1'_{cp}$, $S2_{cp}$, and $S2'_{cp}$ refer to copies of the input data, whereas g variables indicate the garbage outputs).**

Figure 5.21 illustrates the layout of the proposed reversible QCA AU. The construction of this reversible QCA AU is achieved through the integration of two reversible QCA majority gates, a reversible QCA half-adder, a reversible QCA half-subtractor, and a reversible QCA 4:1 multiplexer. The circuit implementation necessitates 463 QCA cells and occupies an area of 0.83 $\mu m^2$. The delay time for this circuit is 14 clock zones, equivalent to 3.5 clock cycles.

The layout of the reversible QCA CU was developed using the layout of the proposed reversible QCA 2:1 multiplexer design, as shown in Figure 5.18. The CU plays a vital role in the operation of the reversible QCA ALU, as it is responsible for selecting a specific function to be executed, whether it be an arithmetic or logical operation. This functionality is essential for ensuring the versatility and effectiveness of the ALU in performing a wide range of computational tasks.

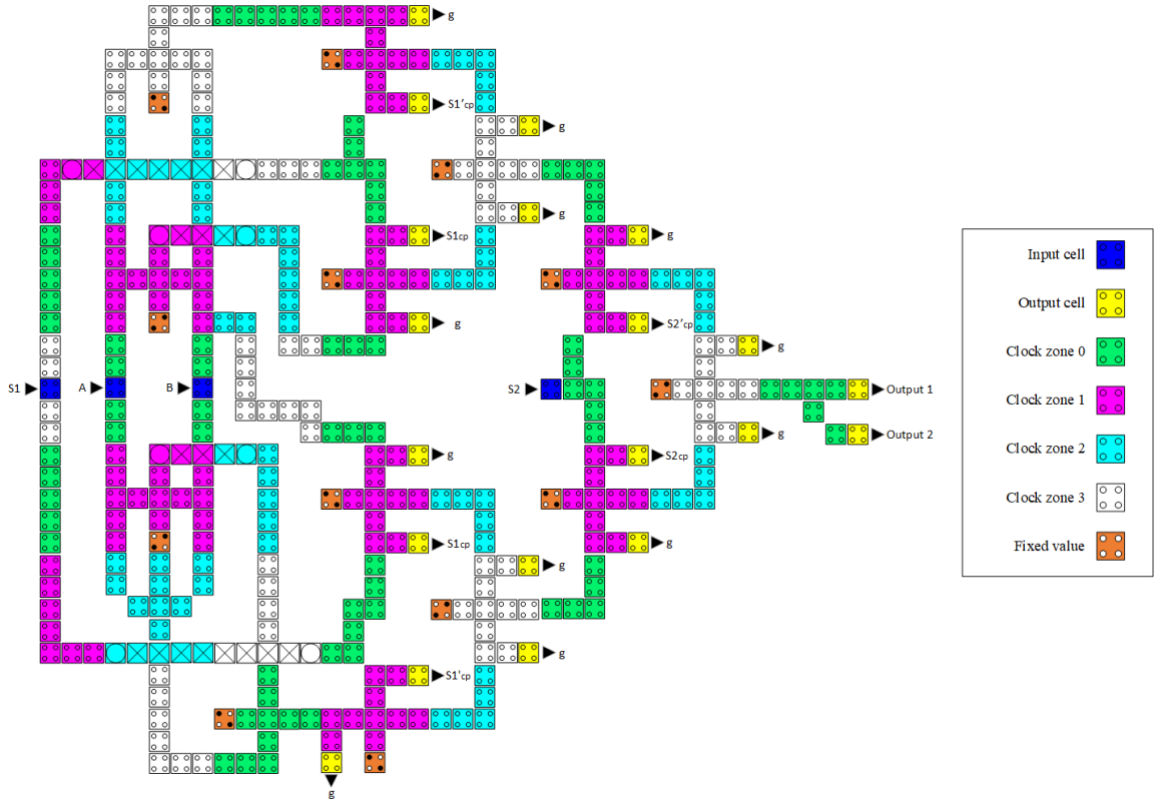



**Figure 5.21 The layout of the proposed reversible QCA AU ($A_{cp}$, $B_{cp}$, $S1_{cp}$, $S1'_{cp}$, $S2_{cp}$, and $S2'_{cp}$ refer to copies of the input data, whereas g variables indicate the garbage outputs).**

Finally, the complete physical layout of the novel reversible QCA ALU was successfully completed by integrating the layout configurations of the three key components: the LU, AU, and CU. This integration process also involved the precise placement of the necessary QCA wiring lines, ensuring seamless connectivity and functionality across the entire ALU structure. Figure 5.22 depicts the final layout of the proposed reversible QCA ALU. The implementation of this innovative reversible QCA ALU demonstrates significant achievements in both design efficiency and performance. The entire circuit requires 1,153 QCA cells, reflecting the complexity and intricacy of the design. Despite this complexity, the design maintains a compact footprint, occupying an area of just 2.14 μm². This compactness is critical in nanoscale computing, where space optimisation is paramount. In terms of operational performance, the reversible QCA ALU exhibits a delay time of 24 clock zones, corresponding to 6 clock cycles. This delay metric is a critical indicator of the ALU's speed and efficiency in executing computational tasks. The balance between the number of QCA cells, area consumption, and delay time

underscores the effectiveness of the proposed design in achieving a high-performance, energy-efficient ALU within the QCA framework.

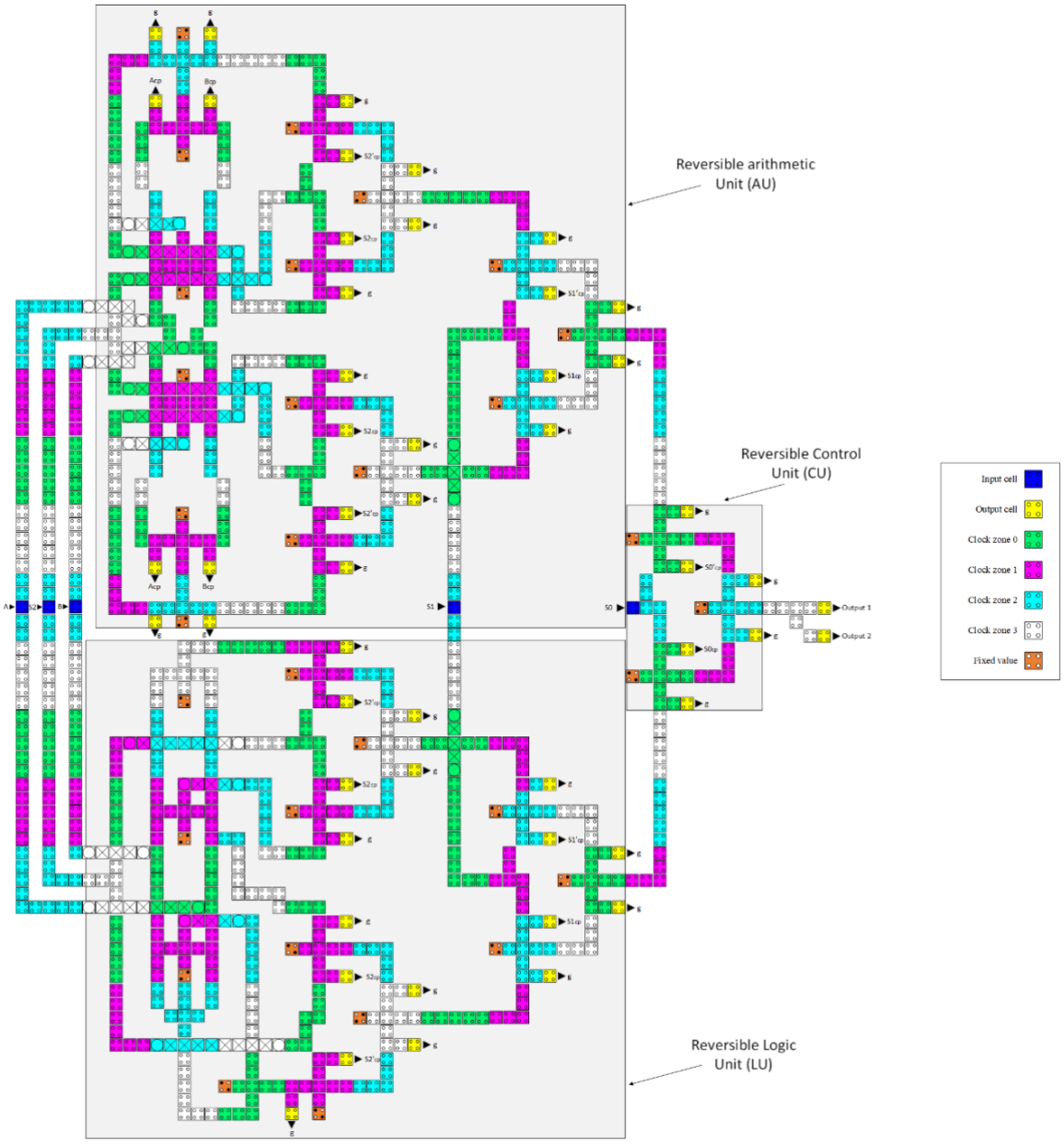



**Figure 5.22 The layout of the proposed reversible QCA ALU ($A_{cp}$, $B_{cp}$, $C_{cp}$, $D_{cp}$, $S1_{cp}$, $S1'_{cp}$, $S1_{cp}$, $S1'_{cp}$, $S2_{cp}$, and $S2'_{cp}$ refer to copies of the input data, whereas g variables indicate the garbage outputs).**

Overall, the successful completion and integration of the reversible QCA ALU is a big step forward in the field of reversible computing. It also demonstrates the potential of QCA technology in enabling the development of next-generation digital systems.

### 5.2.2. Energy dissipation simulation results

The most significant advantage of designing digital circuits to be both logically and physically reversible lies in the substantial improvement in energy efficiency. This section conducted a comprehensive investigation of the energy dissipation for the proposed logically and physically reversible QCA ALU to quantify this benefit. The energy dissipation was meticulously calculated for each component of the proposed reversible QCA ALU, including the reversible AND, OR, and XOR gates, as well as the reversible half-adder, half-subtractor, 2:1 multiplexer, and 4:1 multiplexer. Additionally, the energy dissipation of the logically and physically reversible QCA LU, AU, and the overall ALU was thoroughly evaluated. These energy dissipation values were obtained using the *QCADesigner-E 2.2* TCAD tool, and the findings are comprehensively summarised in Table 5.10. The simulation results underscore the exceptional energy efficiency achieved through the application of physically and logically reversible design techniques in the construction of the QCA ALU. This efficiency highlights the potential of reversible computing methodology, presented in this thesis, to create highly efficient digital systems, paving the way for significant advancements in the field.

**Table 5.10 The energy dissipation analysis of the proposed reversible QCA ALU.**

| Logically and physically reversible QCA ALU build-up circuits | Total energy dissipation (meV) | Average energy dissipation (meV) |
|---|---|---|
| Reversible AND | 0.009 | 0.002 |
| Reversible OR | 0.009 | 0.002 |
| Reversible XOR | 0.054 | 0.014 |
| Reversible half-adder | 0.099 | 0.025 |
| Reversible half-subtractor | 0.063 | 0.016 |
| Reversible 4:1 multiplexer | 0.525 | 0.057 |
| Reversible CU - Reversible 2:1 multiplexer | 0.112 | 0.014 |
| Reversible LU | 2.28 | 0.397 |
| Reversible AU | 2.84 | 0.405 |
| Reversible ALU | 6.54 | 0.908 |

At a temperature of 1 K, every component, including the reversible AND, OR, and XOR gates, as well as the reversible half-adder, half-subtractor, 2:1 multiplexer, and 4:1 multiplexer, exhibited exceptional energy dissipation values below the Landauer energy limit of $k_B T \ln 2$. Moreover, the proposed designs for a logically and physically reversible

QCA LU, AU, and ALU possess ultralow energy dissipation with averages of 0.397 meV, 0.405 meV, and 0.908 meV per operation, respectively.

### 5.2.3. Cost Calculation

The cost was calculated for each component of the proposed logically and physically reversible QCA ALU discussed in Section 5.2.1, including the logically and physically reversible XOR gate, half-adder, half-subtractor, 2:1 multiplexer, and 4:1 multiplexer. Additionally, the cost of the logically and physically reversible QCA LU, AU, and the overall ALU was thoroughly evaluated. The cost function in Equation 1.16, which is explained in Section 1.8, is used in the evaluation. It is a quantitative way to measure how efficient and effective QCA circuits are.

Table 5.11 presents a comprehensive analysis of several critical metrics for each component of the proposed logically and physically reversible QCA ALU design. This comprehensive breakdown includes the number of majority gates and inverters used, the number of crossovers implemented, the total QCA cell count, the occupied area, and the delay time associated with each design. Additionally, the table provides an evaluation of the overall cost, offering a holistic assessment of the efficiency and complexity of the proposed reversible QCA ALU. These metrics collectively facilitate a thorough comparison and evaluation of the design trade-offs inherent in each design configuration.

**Table 5.11 QCA ALU components cost.**

| QCA ALU build-up circuits | Majority gates | Inverters | Crossing | QCA cells | Area ($\mu m^2$) | Delay [clock cycle] | Cost function (FOM) |
|---|---|---|---|---|---|---|---|
| Reversible XOR | 3 | 2 | 1 | 101 | 0.15 | 2 | 24 |
| Reversible half-adder | 4 | 2 | 3 | 156 | 0.27 | 3 | 30 |
| Reversible half-subtractor | 3 | 2 | 2 | 116 | 0.15 | 2 | 17 |
| Reversible 4:1 multiplexer | 9 | 3 | 0 | 213 | 0.46 | 3 | 252 |
| Reversible 2:1 multiplexer (CU) | 3 | 1 | 0 | 56 | 0.09 | 1 | 10 |
| Reversible LU | 14 | 6 | 4 | 380 | 0.63 | 3.5 | 763 |
| Reversible AU | 15 | 10 | 15 | 463 | 0.83 | 3.5 | 1610 |
| Reversible ALU | 32 | 17 | 19 | 1153 | 2.14 | 6 | 8412 |

### 5.2.4. Discussion

While QCA-based systems offer significant potential for energy-efficient, high-density computing in the nanoscale domain, their technological immaturity, practical implementation challenges, and reliance on simulation-based assumptions make direct comparisons with traditional CMOS systems both challenging and, in some cases, infeasible. Consequently, the proposed logically and physically reversible QCA ALU design has been evaluated against the most recent QCA ALU designs available in the literature. Table 5.12 compares the energy efficiency, number of operations, occupied area, number of required QCA cells, and latency of the proposed logically and physically reversible QCA ALU design to the most recent QCA ALU designs in the literature. Additionally, this table presents the method used to deal with wire junctions as well as the reversibility status of each design. The logically and physically reversible QCA ALU design proposed in this study requires 1153 QCA cells, 2.14 $\mu m^2$ of area, and 6 clock cycles of delay to execute 16 operations. Using three distinct layers, the multilayer crossover method was utilised for wire crossing.

**Table 5.12 Comparison of performance and energy dissipation (Note that there are only three references [181,188,189] that calculate the energy dissipation for the QCA ALU).**

| Reference | Operations | QCA cells | Area ($nm^2$) | Delay (Clock cycles) | Wire crossing | Total energy dissipation (meV) | Average energy dissipation (meV) | Reversibility |
|---|---|---|---|---|---|---|---|---|
| [183] | 16 | 2,857 | 4,440 | 6 | Coplanar | **NG** | **NG** | Logically |
| [184] | 8 | 1097 | 3,740 | 3.75 | Multilayer | **NG** | **NG** | Logically |
| [185] | 4 | 332 | 380 | 3 | Multilayer | **NG** | **NG** | Logically |
| [186] | 4 | 452 | 740 | 2.5 | Coplanar | 819.22 | 79.95 | Irreversible |
| [187] | 16 | 35,596 | 11,370 | 9 | Coplanar | **NG** | **NG** | Irreversible |
| [188] | 16 | 2,370 | 4,010 | 6 | Coplanar | **NG** | **NG** | Logically |
| [189] | 4 | 420 | 850 | 3 | Multilayer | **NG** | **NG** | Irreversible |
| [190] | 12 | 485 | 790 | 5 | Multilayer | **NG** | **NG** | Irreversible |
| [191] | 4 | 464 | 780 | 4 | Multilayer | **NG** | **NG** | Irreversible |
| [192] | 4 | 1,010 | 1,860 | 4.25 | Coplanar | **NG** | **NG** | Irreversible |
| [193] | 8 | 231 | 280 | 3 | Multilayer | 89.40 | 8.12 | Irreversible |
| [194] | 10 | 1,069 | 2,340 | 3 | Coplanar | 907.01 | 93.00 | Logically |
| **Proposed** | **16** | **1,153** | **2,140** | **6** | **Multilayer** | **6.54** | **0.908** | **Logically & physically** |

According to the simulation results, the proposed logically and physically reversible QCA ALU shows a significant reduction in energy dissipation compared with previous QCA ALU designs. As illustrated in Figure 5.23, the proposed reversible QCA ALU consumes 88.8% less energy than the most energy-efficient QCA ALU designs previously reported in the literature [193]. This remarkable improvement highlights the effectiveness of integrating logically and physically reversible design principles to achieve superior energy efficiency in QCA-based computing systems.

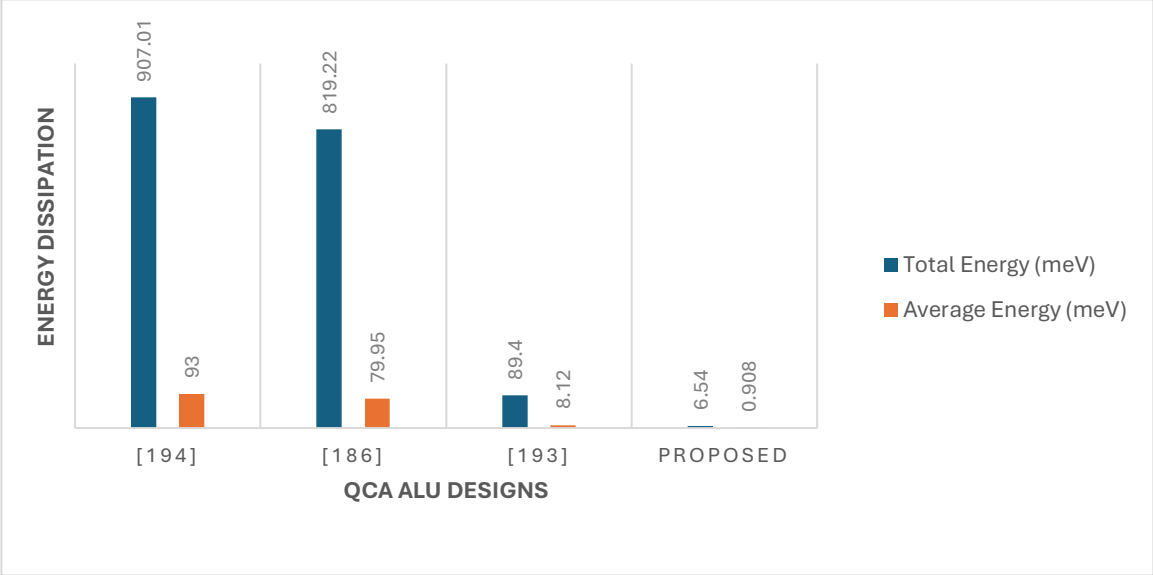



**Figure 5.23 Energy dissipation comparison of QCA ALU designs.**

Figure 5.24 and Figure 5.25 demonstrate the number of operations, delay time, occupied area, and required QCA cells for the novel logically and physically reversible QCA ALU design and the existing designs. Although many previous designs utilized fewer QCA cells and shorter delay times, and some others occupied less area than the proposed ALU, these ALUs performed fewer operations. These previous ALUs can perform either 12 operations, 10 operations, eight operations, or just four operations .

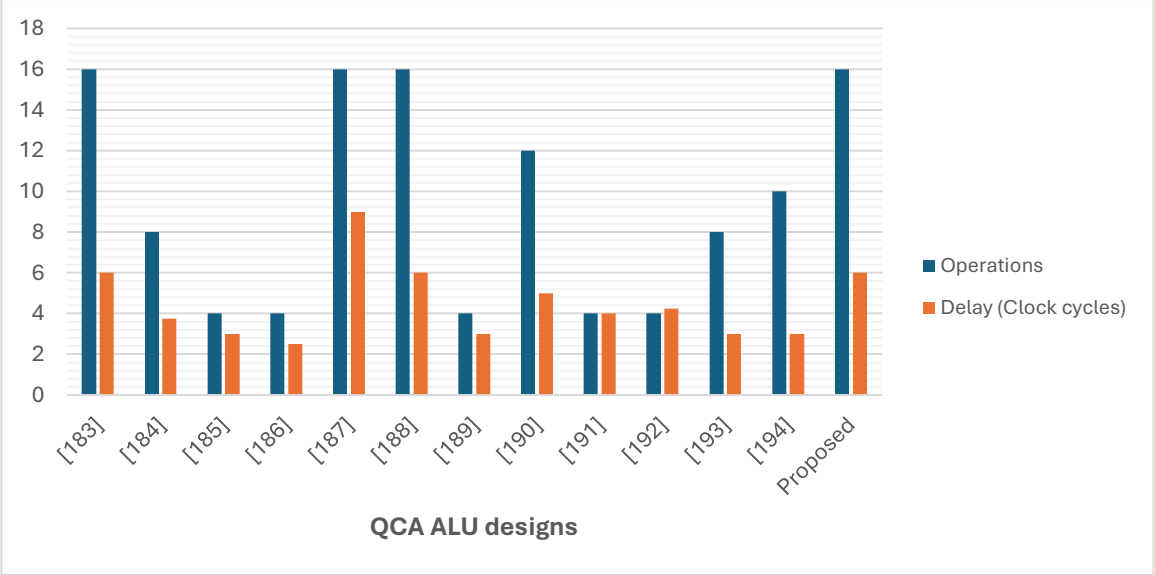



**Figure 5.24 Number of operations and delay time of the QCA ALU designs.**

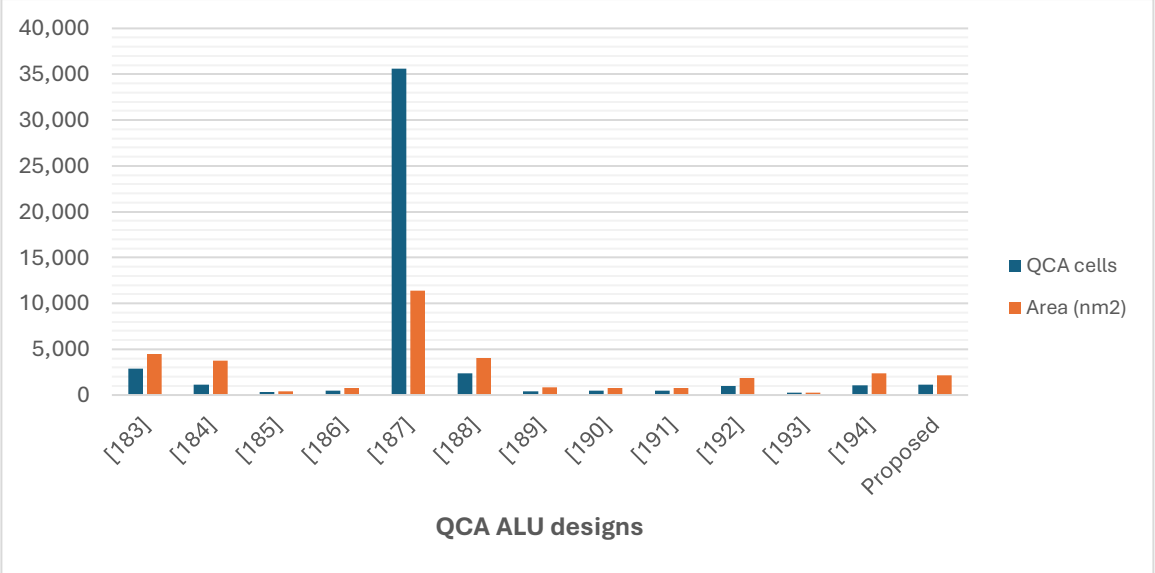



**Figure 5.25 QCA cells and occupied areas utilized to design the QCA ALUs.**

Thus, for a more precise comparison, we compared our proposed ALU with QCA ALU designs that can perform a similar number of operations, as presented in Figure 5.26 and Figure 5.27. This comparison demonstrates that the logically and physically reversible design proposed in this study requires 51% fewer QCA cells, 47% less area, and a comparable latency compared to the best QCA ALU design previously presented that can perform 16 operations [188].

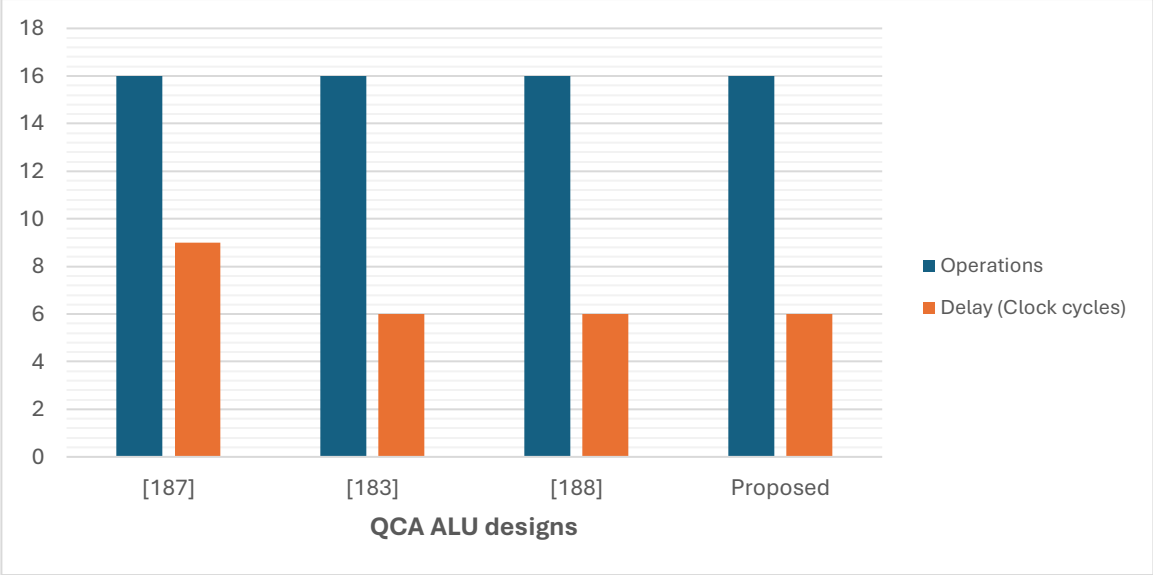



**Figure 5.26 Number of operations and delay time of the QCA ALU designs that perform 16 operations.**

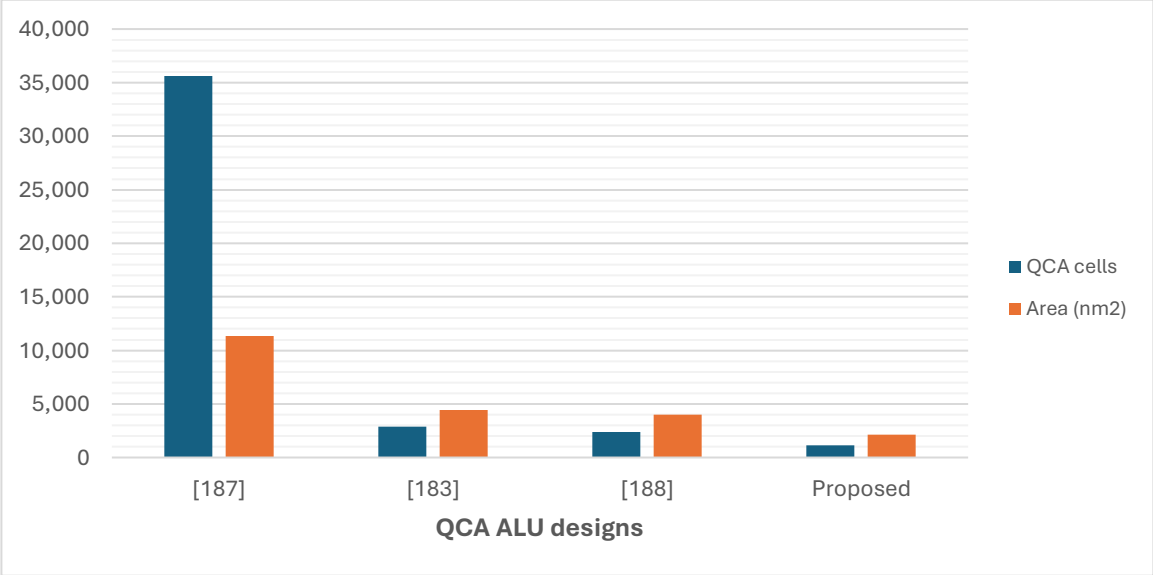



**Figure 5.27 QCA cells and occupied areas utilized to design the QCA ALUs that can perform 16 operations.**

### 5.2.5. Summary for designing a reversible QCA ALU

In this section, the logically and physically reversible design approach was employed to develop all the components necessary for constructing a logically and physically reversible QCA ALU, with the primary goal of achieving extremely low power consumption. These components were then integrated into an innovative multilayer design

for a QCA ALU, which demonstrates exceptionally low energy dissipation, two orders of magnitude lower than the values reported in existing scientific literature. A key advantage of this design is that it maintains reversibility down to the physical level of individual QCA gates. Theoretically, this characteristic ensures no information loss during operation, thereby significantly reducing or even eliminating energy dissipation into the environment.

The reversible QCA ALU developed in this study can perform sixteen distinct operations, evenly split between logical and arithmetic functions. The performance simulation and energy dissipation evaluation were conducted using the *QCADesigner-E 2.2* TCAD tool, which provides a microscopic treatment, incorporating both quantum mechanical effects within QCA cells and electrostatic interactions between cells. To implement the 16 operations, the proposed logically and physically reversible QCA ALU design utilises 1153 QCA cells, occupies an area of 2.14 $\mu m^2$, and exhibits a delay of 6 clock cycles.

The simulation results validate the concept that logically and physically reversible design can lead to ALU circuits with minimal energy loss during operation. Each logically and physically reversible component used to construct the ALU, such as reversible AND, OR, and XOR gates, along with reversible half-adders, half-subtractors, and 2:1 and 4:1 multiplexer circuits, demonstrated energy dissipation values below the Landauer limit of $K_B T \ln 2$. This confirms the effectiveness of the reversible approach in maintaining energy efficiency at the fundamental level.

Furthermore, the simulation findings indicate that the proposed logically and physically reversible QCA ALU achieves an 88.8% improvement in energy efficiency compared to the most energy-efficient ALU designs reported in the literature [193]. In addition, when compared to the most efficient 16-operation QCA ALU designs previously introduced, the proposed ALU design utilises 51% fewer QCA cells and requires 47% less area, highlighting its superior efficiency and compactness.

### 5.3. Conclusion

To validate the efficiency of the logically and physically reversible design method outlined in Chapter 2 for developing advanced QCA computer systems, this chapter

presents two sophisticated computing circuits designed using this innovative approach. The first circuit addressed is the 8:1 multiplexer, another critical component widely utilised in computing systems. Multiplexers play a key role in data selection and routing, enabling the efficient management of multiple input signals by directing them through a single output line based on control signals. The second circuit tackled is the ALU, a fundamental component of the CPU responsible for executing a broad spectrum of logical and arithmetic operations on data within the CPU. The ALU is integral to the CPU's functionality, directly influencing the processing speed and efficiency of computational processes. The findings underscore the significant advancements in energy efficiency achieved through the use of the logically and physically reversible design approach for designing sophisticated QCA digital circuits, highlighting its potential for applications in low-power digital computing environments. The hierarchical approach to constructing advanced QCA computing systems taken here for multiplexer and ALU circuits from basic logically and physically reversible QCA circuits preserves the low power characteristics and also ensures scalability. The logically and physically reversible hierarchical design methodology is thus highly suitable for the development of complex, energy-efficient digital systems.

### 5.4. Contribution

The research findings given in this chapter have culminated in the publication of two peer-reviewed articles. First, the results of Section 5.1 were published in a paper entitled “An Ultra-Energy-Efficient Reversible Quantum-Dot Cellular Automata 8:1 Multiplexer Circuit.” This paper was published in January 2024 in the journal *Quantum Reports* [33] (refer to Figure 5.28). Second, the findings of Section 5.2 were published in a paper titled “Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit” in the August 2023 edition of the journal *Nanomaterials* [34] (refer to Figure 5.29). This article was later reissued as a chapter in The *Prime Archives in Nanotechnology* in November 2023, as depicted in Figure 5.29 [195]. These publications contribute to the ongoing research in sophisticated multiplexer and ALU QCA-based computer digital circuits, key ingredients for constructing a CPU and embedded systems.

Furthermore, the research findings were presented at the *Single-Molecule Sensors and Nano Systems International Conference 2023*, which was held at the University Pompeu Fabra in Barcelona, Spain, on November 22–24, 2023, as a poster titled “Fully Reversible Quantum-Dot Cellular Automata Multiplexer Circuits with Ultralow Energy Dissipation,” as illustrated in Figure 5.31 [196].

quantum reports

MDPI

*Communication*

# An Ultra-Energy-Efficient Reversible Quantum-Dot Cellular Automata 8:1 Multiplexer Circuit

**Mohammed Alharbi [1,*], Gerard Edwards [1] and Richard Stocker [2]**

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**Abstract:** Energy efficiency considerations in terms of reduced power dissipation are a significant issue in the design of digital circuits for very large-scale integration (VLSI) systems. Quantum-dot cellular automata (QCA) is an emerging ultralow power dissipation approach, distinct from traditional, complementary metal-oxide semiconductor (CMOS) technology, for building digital computing circuits. Developing fully reversible QCA circuits has the potential to significantly reduce energy dissipation. Multiplexers are fundamental elements in the construction of useful digital circuits. In this paper, a novel, multilayer, fully reversible QCA 8:1 multiplexer circuit with ultralow energy dissipation is introduced. The power dissipation of the proposed multiplexer is simulated using the QCADesigner-E version 2.2 tool, describing the microscopic physical mechanisms underlying the QCA operation. The results show that the proposed reversible QCA 8:1 multiplexer consumes 89% less energy than the most energy-efficient 8:1 multiplexer circuit previously presented in the literature.

**Keywords:** quantum-dot cellular automata (QCA); multiplexer; reversible; energy dissipation; QCADesigner-E



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## 1. Introduction

Advancements in complementary metal-oxide semiconductor (CMOS) technology have led to growing concern about its associated shortcomings, including subthreshold voltage and gate leakage current [1]. Additionally, the escalating demand for increasing the number of devices in CMOS systems on a chip (SoC), already at a count of billions, exacerbates the issue of excessive power dissipation [2]. Quantum-dot cellular automata (QCA) is a promising computing concept in which cells containing four quantum dots are used to perform computations at the nanoscale level. The QCA concept is based on a transistor-less paradigm in which binary information is encoded via the electron charge location in the four quantum dots of a QCA cell in antipodal configurations [3]. QCA offers several advantages over conventional semiconductor-based technologies such as CMOS, including highly reduced power consumption, the potential for high-speed operation, and the ability to create 'nanochip' integrated circuits with a high QCA cell density. Designing QCA digital circuits using a reversible design technique can yield enhanced circuits with ultralow-energy dissipation [4]. Theoretically, reversible computation operations, which maintain reversibility from the synthesis of a circuit to its physical layout, can mitigate information loss and require zero accompanying energy dissipation [5].

The implementation of the QCA paradigm has been proposed utilising many technologies, such as solid-state metallic island dots, magnetic implementations, and molecular electronic methods [6–9], with particularly promising atomic silicon quantum dot work employing a silicon dangling bond on a hydrogen-terminated silicon surface [10]. Molecular field-coupled nanocomputing (FCN) is anticipated to offer QCA circuits with extremely



**Figure 5.28 Article paper: An ultra-energy-efficient reversible QCA 8:1 multiplexer**

*nanomaterials*

MDPI

*Article*

# Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit

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**Abstract:** Quantum-dot cellular automata (QCA) are a promising nanoscale computing technology that exploits the quantum mechanical tunneling of electrons between quantum dots in a cell and electrostatic interaction between dots in neighboring cells. QCA can achieve higher speed, lower power, and smaller areas than conventional, complementary metal-oxide semiconductor (CMOS) technology. Developing QCA circuits in a logically and physically reversible manner can provide exceptional reductions in energy dissipation. The main challenge is to maintain reversibility down to the physical level. A crucial component of a computer's central processing unit (CPU) is the arithmetic logic unit (ALU), which executes multiple logical and arithmetic functions on the data processed by the CPU. Current QCA ALU designs are either irreversible or logically reversible; however, they lack physical reversibility, a crucial requirement to increase energy efficiency. This paper shows a new multilayer design for a QCA ALU that can carry out 16 different operations and is both logically and physically reversible. The design is based on reversible majority gates, which are the key building blocks. We use *QCADesigner-E* software to simulate and evaluate energy dissipation. The proposed logically and physically reversible QCA ALU offers an improvement of 88.8% in energy efficiency. Compared to the next most efficient 16-operation QCA ALU, this ALU uses 51% fewer QCA cells and 47% less area.

**Keywords:** quantum-dot cellular automata (QCA); arithmetic logic unit (ALU); reversible; energy dissipation



**Citation:** Alharbi, M.; Edwards, G.; Stocker, R. Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit. *Nanomaterials* **2023**, *13*, 2445. https://doi.org/10.3390/nano13172445

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## 1. Introduction

Heat dissipation in conventional, complementary metal-oxide-semiconductor (CMOS) technology is a major challenge for the design and operation of integrated circuits (ICs). As CMOS technology scales down, the power density and the operating temperature increase, which can degrade the performance, reliability, and lifetime of devices [1,2].

Conventional methods of computing typically include irreversible operations, which result in some input bits of information being erased during the process. In 1961, Landauer [3] proved that irreversible computations cause information loss and involve an amount of heat dissipation of $k_B T \ln 2$ per bit erased, where $k_B$ is the Boltzmann constant, and $T$ is the temperature. In 1996, Gershenfeld [4] argued that the actual amount of energy dissipated due to information loss is much higher than Landauer's lower bound. As nanoelectronics circuits and systems decrease in size and become more efficient, their energy dissipation levels approach Landauer's limit. Therefore, to continue the trend of reducing power consumption and to reach Landauer's lower bound, unconventional computation methods that allow for reversible logic operations without information loss are needed [5].

Reversible logic operations, which have a one-to-one correspondence between the number of input and output signals, are a promising alternative to conventional irreversible



**Figure 5.29 Article paper: Reversible QCA-based ALU**

Prime Archives in Nanotechnology

**Book Chapter**

# Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit

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**Figure 5.30 Book chapter: Reversible QCA-based ALU**

# Fully Reversible Quantum-Dot Cellular Automata Multiplexer Circuits with Ultralow Energy Dissipation

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## Abstract

Quantum-dot cellular automata (QCA) is a promising nanocomputing technology that exploits the electrostatic interaction and quantum mechanical tunnel coupling between electrons in quantum dots. Developing QCA circuits in a fully reversible manner has the potential to significantly reduce energy dissipation. This study introduces a novel fully reversible hierarchical design technique for developing a QCA 4:1 multiplexer circuit, with ultralow energy dissipation.

## Background

Using reversible logic operations, instead of the standard irreversible computations, maintains a one-to-one correspondence between the number of input and output signals. Thus, unlike irreversible computations, reversible operations have no information loss with the accompanying dissipation of energy into the environment, due to the second law of thermodynamics. However, substantially reducing energy usage in reversible computing requires preserving reversibility down to the circuit physical level [1]. As a result, the synthesis and layout architecture of the circuit should be designed in a completely reversible manner to avoid energy dissipation.

## Methods

The primary cause of energy dissipation in quantum-dot cellular automata (QCA) circuits is attributed to the use of conventional irreversible majority gates [2]. Therefore, our methodology focuses on developing a reversible majority gate with three inputs and three outputs (see Figure 1) as the main building 'block' in the development of the fully reversible QCA circuits.


**Figure 1.** (**a**) Logical synthesis and (**b**) Physical layout of the reversible QCA majority gate.

- ***The data flow synchronization*** is achieved by utilizing the unified, standard, and efficient (USE) clocking scheme [3].
- ***The wire crossing*** problem is solved by using the multilayer technique [4], with three distinct layers.
- ***The energy dissipation*** is calculated using the *QCADesigner-E* software version 2.2 [5], applying the technology and simulation parameters presented in Table 1. *QCADesigner-E* implements a quantum mechanical microscopic treatment within the QCA cell, including the electrostatic interaction and tunnel coupling, between the dots. In addition, the electrostatic forces between cells are incorporated.

**Table 1.** The technology used and simulation parameters.

| Parameter | Description | Value |
|---|---|---|
| QD size | Quantum-dot size | 5 nm |
| Cell area | Dimensions of each cell | 18 x 18 nm |
| Cell distance | Distance between two cells | 2 nm |
| Layer separation | Distance between QCA layers in multilayer crossing | 11.5 nm |
| Clock high | Max. saturation energy of clock signal | 9.8E-22 J |
| Clock low | Min. saturation energy of clock signal | 3.8E-23 J |
| permittivity | Relative permittivity of material for QCA system (GaAs & AlGaAs) | 12.9 |
| Radius of effect | Maximum distance between cells whose interaction is considered | 80 nm |
| Temp | Operating temperature | 1 K |
| $\tau$ | Relaxation time | 1E-15 s |
| $T_y$ | Period of the clock signal | 1E-9 s |
| $T_{in}$ | Period of the input signals | 1E-9 s |
| $T_{step}$ | Time interval of each iteration step | 1E-16 s |
| $T_{sim}$ | Total simulation time | 8E-9 s |
| $\gamma_{shape}$ | Shape of clock signal slopes | GAUSSIAN |
| $\gamma_{slope}$ | Rise and fall time of the clock signal slopes | 1E-10 s |

## Proposed fully reversible 4:1 multiplexer

***First***, a QCA 2:1 multiplexer containing three reversible majority gates and an inverter, as shown in Figure 2, is designed reversibly.

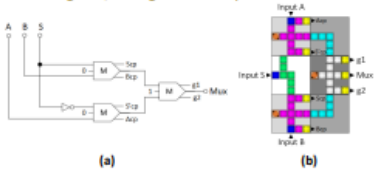


**Figure 2.** (**a**) The synthesis and (**b**) Layout of the proposed reversible 2:1 multiplexer ($A_{cp}$, $B_{cp}$, $S_{cp}$, and $S'_{cp}$ refer to copies of the input data, whereas g1 and g2 indicate the garbage outputs).

## Proposed fully reversible 4:1 multiplexer (cont.)

***Second***, a QCA 4:1 multiplexer circuit by combining three reversible QCA 2:1 multiplexer circuit, 'connected up' as illustrated in Figure 3, is designed reversibly.

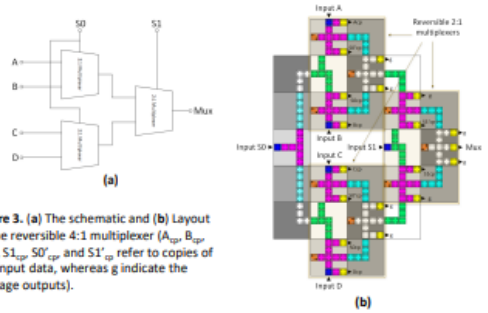


**Figure 3.** (**a**) The schematic and (**b**) Layout of the reversible 4:1 multiplexer ($A_{cp}$, $B_{cp}$, $S0_{cp}$, $S1_{cp}$, $S0'_{cp}$, and $S1'_{cp}$ refer to copies of the input data, whereas g indicate the garbage outputs).

The area cost and delay time of the presented multiplexers are illustrated in Table 2.

**Table 2.** The multiplexer circuits cost.

| Parameter | 2:1 multiplexer circuit | 4:1 multiplexer circuit |
|---|---|---|
| Delay (Clock cycle) | 1 | 2.75 |
| Area ($\mu m^2$) | 0.09 | 0.46 |
| QCA cells | 56 | 213 |

## Results and discussion for ultralow power dissipation

The numerical simulation results from *QCADesigner-E*, presented in Table 3, demonstrate that the proposed fully reversible design approach is capable of developing QCA circuits, with ultralow energy dissipation values, below the Landauer energy threshold of 0.06 meV, at a temperature of 1 K.

**Table 3.** Energy dissipation analysis of the proposed multiplexer. The average energy dissipation denotes the mean energy value averaged over the various input signal combinations.

| Proposed QCA Circuits | Total Energy Dissipation (meV) | Average Energy Dissipation (meV) |
|---|---|---|
| Reversible majority gate | 0.009 | 0.002 |
| Reversible 2:1 multiplexer | 0.112 | 0.014 |
| Reversible 4:1 multiplexer | 0.525 | 0.057 |

Figure 4 shows the energy dissipation of our novel 4:1 multiplexer circuit in comparison to previous research. The energy efficiency of our 4:1 multiplexer circuit design is improved by 97% compared to the previous studies.

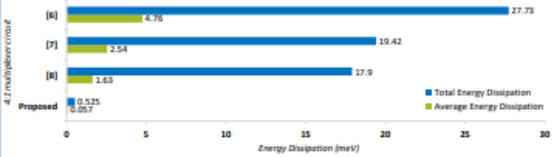


**Figure 4.** Energy dissipation comparison of the 4:1 multiplexer circuit.

## Conclusion

This work presents a novel hierarchical design technique for developing QCA multiplexer circuits that are fully reversible, utilising reversible majority gates. To verify the energy efficiency of this method, a fully reversible QCA 4:1 multiplexer was designed and simulated employing *QCADesigner-E software*. The results show an energy dissipation reduction improvement by 97%.

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**Figure 5.31 Poster: Fully reversible QCA multiplexer circuits with ultralow energy dissipation**

# Chapter 6

## 6. Partially Reversible Design Method

Developing QCA digital circuits logically and physically reversible leads to substantial reductions in energy dissipation [32, 149]. However, this typically results in time delays and increased circuit cost metrics [31, 33, 34]. This chapter introduces an innovative, partially reversible method that addresses the limitations of the logically and physically reversible design method in terms of latency and circuit cost.

The proposed partially reversible design method serves as a middle ground between the logically and physically reversible design methodology and conventional irreversible design methodologies. Compared with irreversible design methods, the partially reversible design method still optimises energy efficiency. Moreover, the partially reversible design method improves the speed and decreases the circuit cost in comparison with the logically and physically reversible design technique. The key ingredient of the proposed partially reversible design methodology is the introduction of a partially reversible majority gate element building block. To validate the effectiveness of the proposed partially reversible design approach, a novel partially reversible half-adder circuit is designed and simulated.

The implementation of QCA circuits via logically and physically reversible approaches results in significantly less energy dissipation than that in irreversible circuits [27]. Although the development of QCA circuits, via logical and physically reversible design techniques, significantly reduces the energy dissipation of the circuit compared to that of equivalent irreversible circuits, these methods typically lead to time delays as well as increases in the number of QCA cells used. Thus, the QCA circuit's occupied area increases, leading to a corresponding increase in the circuit cost metric [99].

Ottavi *et al.* (2011) introduced a partially reversible design method to balance energy dissipation, delay time, and the area used by including memory stages and a control mechanism resembling a pipeline [197]. However, this strategy is less efficient when more pipeline clock zones are utilised [198]. Chaves *et al.* (2019) presented an alternative

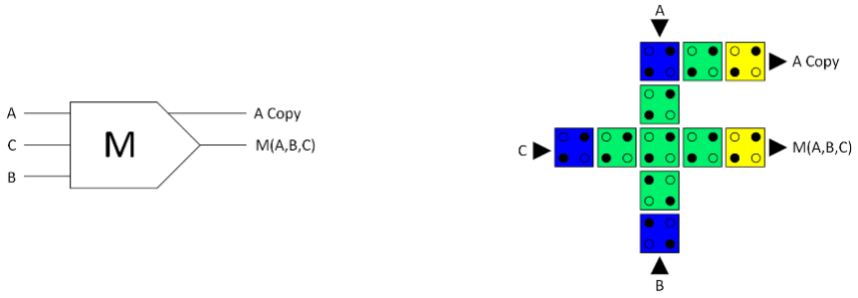
approach to designing partially reversible circuits in FCN technologies by considering layout alterations rather than timing modifications [199]. This approach relies on recycling one input signal for each logic gate used to construct the circuit. To our knowledge, this method has not yet been fully explored for the design of digital circuits using QCA nanocomputing technology.

This section presents, for the first time, an implementation of the partially reversible design method, which relies on recycling one input signal for each logic gate in the design of QCA digital circuits. The main objective of developing partially reversible QCA circuits is to achieve an optimal trade-off among power consumption, delay time, occupied area, and circuit cost. Initially, a partially reversible QCA majority gate that recycles one input signal was developed. Subsequently, a partially reversible QCQ half-adder circuit was designed, employing the partially reversible QCA majority gate as its fundamental component.

### 6.1. Designing partially reversible QCA half-adder

The majority gate is an essential element in the construction of QCA circuits because it is used to produce the fundamental logic gates AND and OR. In previous studies, either conventional irreversible [200] or fully reversible [34] majority gates were typically used to design QCA digital circuits. The conventional irreversible majority gate is characterised by three inputs and a single output. In contrast, the fully reversible variant of this majority gate features three inputs and three outputs.

The design process for a partially reversible half-adder circuit begins with the formulation of a three-input-two-output partially reversible majority gate. This gate, which recycles one input signal, results in a configuration consisting of three inputs and two outputs, as shown in Figure 6.1. The logical symbolic diagram of this partially reversible majority gate is shown in Figure 6.1a, and the QCA layout is shown in Figure 6.1b. The functionality of this partially reversible majority gate is determined by setting one of its inputs to a binary value of 0 or 1, which determines whether the gate operates as an AND gate or an OR gate. For example, when the input C is set to a value of 0, the gate is an AND gate, whereas when the input C is set to a value of 1, the gate is an OR gate.

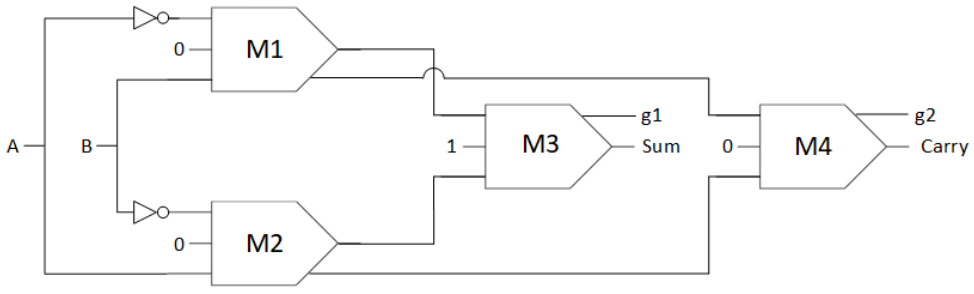



(a) (b)

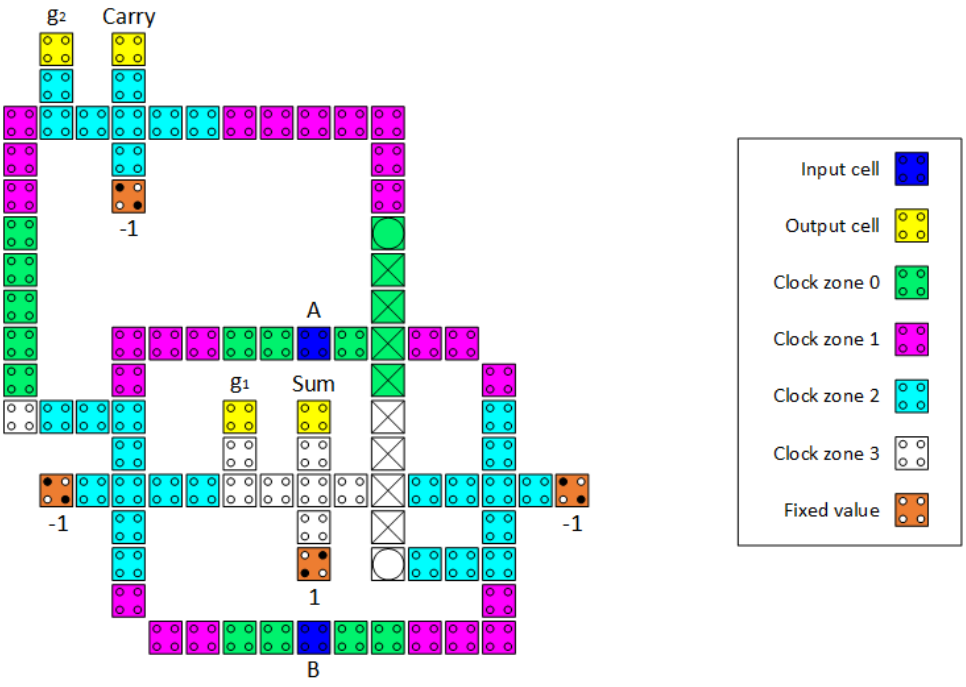
**Figure 6.1 (a) Logical symbolic diagram of the proposed partially reversible majority gate and (b) QCA layout of the proposed partially reversible majority gate.**

Subsequently, a novel partially reversible QCA half-adder circuit is designed using three partially reversible AND gates and one partially reversible OR gate, as illustrated in Figure 6.2. The logic synthesis of the partially reversible half-adder circuit is shown in Figure 6.2a, and the QCA layout is shown in Figure 6.2b. The technological parameters utilised for the development of the proposed QCA half-adder circuits are listed in Table 2.1. The circuit consists of 94 QCA cells, occupying an area of 0.12 μm2. The measured latency is 4 clock phases, which is equal to 1 clock cycle.

To manage the timing of QCA circuits, external clocks are employed to precisely adjust the tunnelling barriers between QCA cells [78]. The USE clocking scheme [78], detailed in Section 1.5, is integrated with proposed partially reversible QCA half-adder design to synchronise the data transmission of the circuit. In addition, wire crossing is a crucial issue in digital circuits. The multilayer approach proposed by Bajec and Pecar [72], detailed in Section 1.6.2, is used to address this issue. The proposed partially reversible half-adder circuit was designed with three different layers to prevent wire junctions.




(a)




(b)

**Figure 6.2 Logical synthesis of the proposed partially reversible QCA half-adder. (b) QCA layout of the proposed partially reversible QCA half-adder (g1 and g2 indicate garbage outputs).**

## 6.2. Simulation results and discussion

The input/output behaviour, energy dissipation, and cost of the proposed partially reversible half-adder circuit are discussed comprehensively. In addition, the performance of the partially reversible half-adder circuit designed in this study is compared with that of existing fully reversible and irreversible half-adder circuits. In the comparison, the amount of energy dissipated to the environment and the cost of the circuit are evaluated.

### 6.2.1. Performance evaluation

The simulation input and output waveforms for the polarisation of the proposed partially reversible QCA half-adder circuit are depicted in Figure 6.3. The waveforms confirm the reliability of the proposed partially reversible design approach for developing QCA digital circuits. The numerical output accurately represents the truth table values of the half-adder circuit shown in Table 3.3, demonstrating the reliable physical input/output behaviour of the proposed partially reversible QCA half-adder circuit.

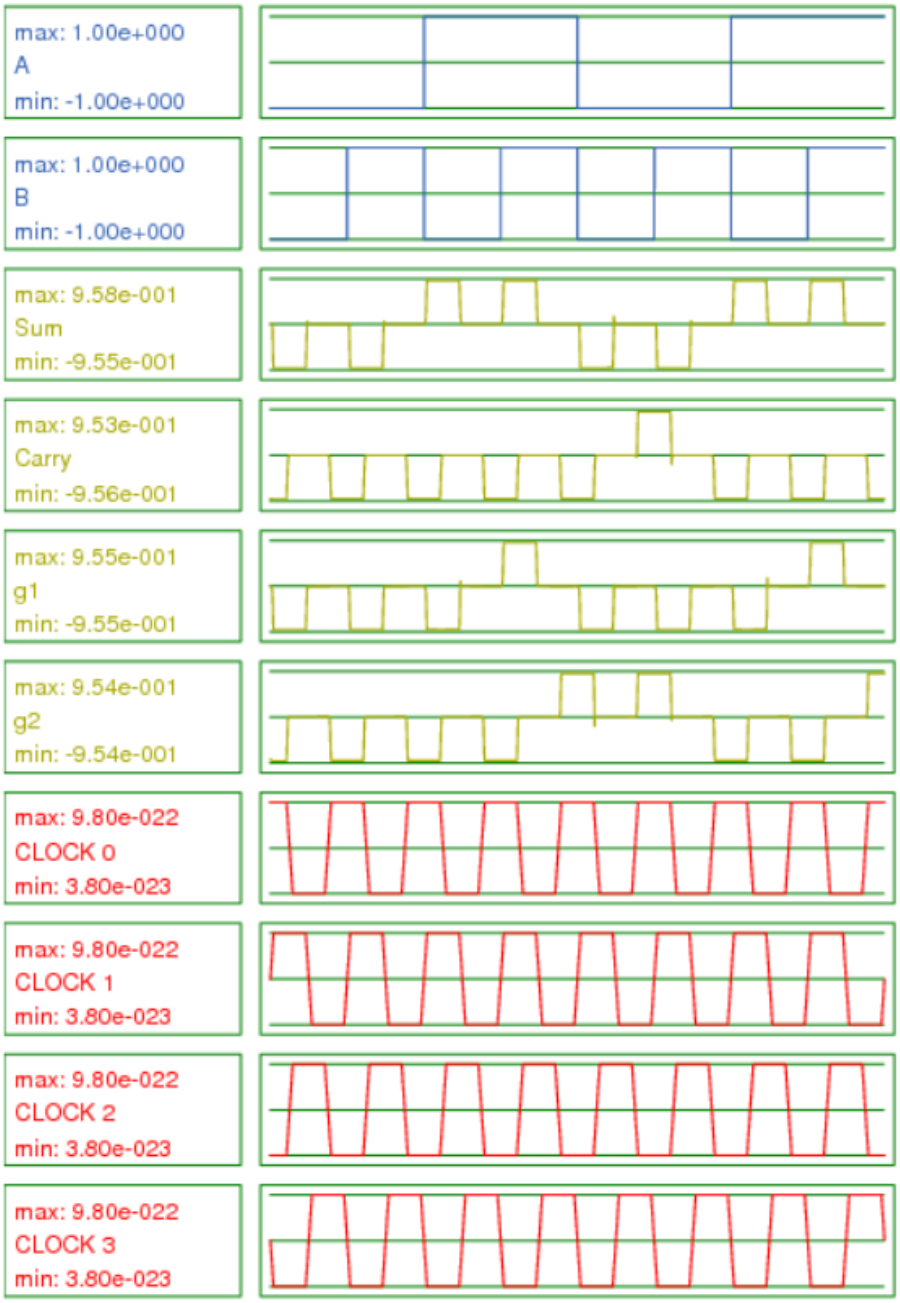



**Figure 6.3 Waveforms of the proposed partially reversible half-adder.**

### 6.2.2. Energy dissipation simulation

The *QCADesigner-E 2.2* TCAD tool was utilised to evaluate the energy dissipation of the proposed partially reversible QCA half-adder circuit. The time interval for each iteration $T_{step}$ was set at 0.1 $\tau$=0.1 fs, where $\tau$ represents the relaxation period. Using an appropriately small time step is essential for reducing simulation errors, obtaining more

precise results, and, simultaneously, ensuring a reasonable simulation time. The simulation errors related to numerical energy conservation with this time step are tolerable, with a value of approximately $\epsilon_{env} \leq 5\%$. A comprehensive description of the simulation parameters used to simulate the energy dissipation of the proposed partially reversible half-adder circuit is presented in Table 2.2.

Table 6.1 presents a comparison of energy dissipation between the innovative, partially reversible QCA majority gate and both irreversible and fully reversible majority gates, commonly used in QCA digital circuit construction. The simulation results show that the previously reported fully reversible QCA majority gate [149] uses 93% less energy than the proposed partially reversible QCA majority gate presented in this study. However, the proposed partially reversible QCA majority gate exhibits 92% lower energy dissipation than the standard irreversible majority gate.

**Table 6.1 Energy Dissipation Values for Majority Gates with Different Reversibility Levels.**

| **Majority Gate** | **Energy dissipation for an input combination signal [meV]** | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **000** | **001** | **010** | **011** | **100** | **101** | **110** | **111** |
| Standard irreversible [149] | 0.001 | 0.709 | 0.714 | 0.711 | 0.709 | 0.714 | 0.711 | 0.001 |
| Fully reversible [149] | 0.003 | 0.003 | 0.003 | 0.003 | 0.003 | 0.003 | 0.003 | 0.003 |
| Partially reversible (Figure 6.1) | 0.002 | 0.052 | 0.052 | 0.053 | 0.053 | 0.053 | 0.052 | 0.002 |

Table 6.2 displays the energy dissipation simulation results of the innovative partially reversible QCA half-adder circuit, designed using the proposed partially reversible majority gate. The table also shows the energy dissipation values of both irreversible and fully reversible half-adder circuits presented in the literature. The energy dissipation values were simulated using the *QCADesigner-E 2.2* TCAD tool, employing the simulation and technology parameters presented in Table I. The fully reversible QCA half-adder circuits described in the literature dissipate up to 78% less energy than the partially reversible QCA half-adder circuit proposed in this study. However, the proposed partially reversible QCA half-adder circuit exhibits up to an 86% improvement in energy efficiency compared to the existing irreversible QCA half-adder circuit.

**Table 6.2 Energy Dissipation Values for Half-Adder Circuits with Different Reversibility Levels.**

| QCA Half-Adder Circuit | Energy dissipation [meV] for an input combination signal | | | |
|---|---|---|---|---|
| | **00** | **01** | **10** | **11** |
| ***Irreversible*** | | | | |
| [201] | 1.305 | 1.314 | 1.490 | 1.306 |
| [202] | 1.941 | 1.440 | 1.951 | 1.945 |
| [203] | 1.163 | 1.090 | 1.171 | 1.479 |
| ***Fully reversible*** | | | | |
| [149] | 0.022 | 0.025 | 0.029 | 0.022 |
| [32] | 0.014 | 0.021 | 0.014 | 0.014 |
| ***Partially reversible*** | | | | |
| Proposed | 0.563 | 0.611 | 0.621 | 0.565 |

### 6.2.3. Cost Calculation

Equation 1.16, detailed in Section 1.8, was employed to compute the cost of the proposed partially reversible half-adder, as well as for evaluating comparable irreversible and fully reversible half-adders documented in the literature. Table 6.3 presents the cost comparison between the developed partially reversible half-adder and the existing irreversible and fully reversible half-adder circuits.

**Table 6.3 Cost Values for Half-Adder Circuits with Different Reversibility Levels.**

| QCA Half-Adder | Inverters | Majority Gates | QCA Cells | Area [$\mu m^2$] | Delay [clock cycles] | Number of Crossings | Circuit Cost [FOM] |
|---|---|---|---|---|---|---|---|
| ***Irreversible*** | | | | | | | |
| [201] | 1 | 3 | 24 | 0.04 | 0.5 | 0 | 20 |
| [202] | 2 | 3 | 21 | 0.04 | 0.5 | 0 | 22 |
| [203] | 3 | 4 | 38 | 0.05 | 1 | 0 | 76 |
| ***Fully reversible*** | | | | | | | |
| [149] | 3 | 4 | 129 | 0.29 | 3.25 | 3 | 364 |
| [32] | 3 | 4 | 139 | 0.21 | 3 | 3 | 336 |
| ***Partially reversible*** | | | | | | | |
| Proposed | 2 | 4 | 94 | 0.12 | 1 | 2 | 88 |

Although the proposed partially reversible QCA half-adder has a higher cost than the previously developed irreversible QCA half-adder circuits, with the cost increasing by up to 78%, the cost of the proposed partially reversible QCA half-adder is 77% less than that of existing fully reversible QCA half-adder circuits. In addition, the existing irreversible

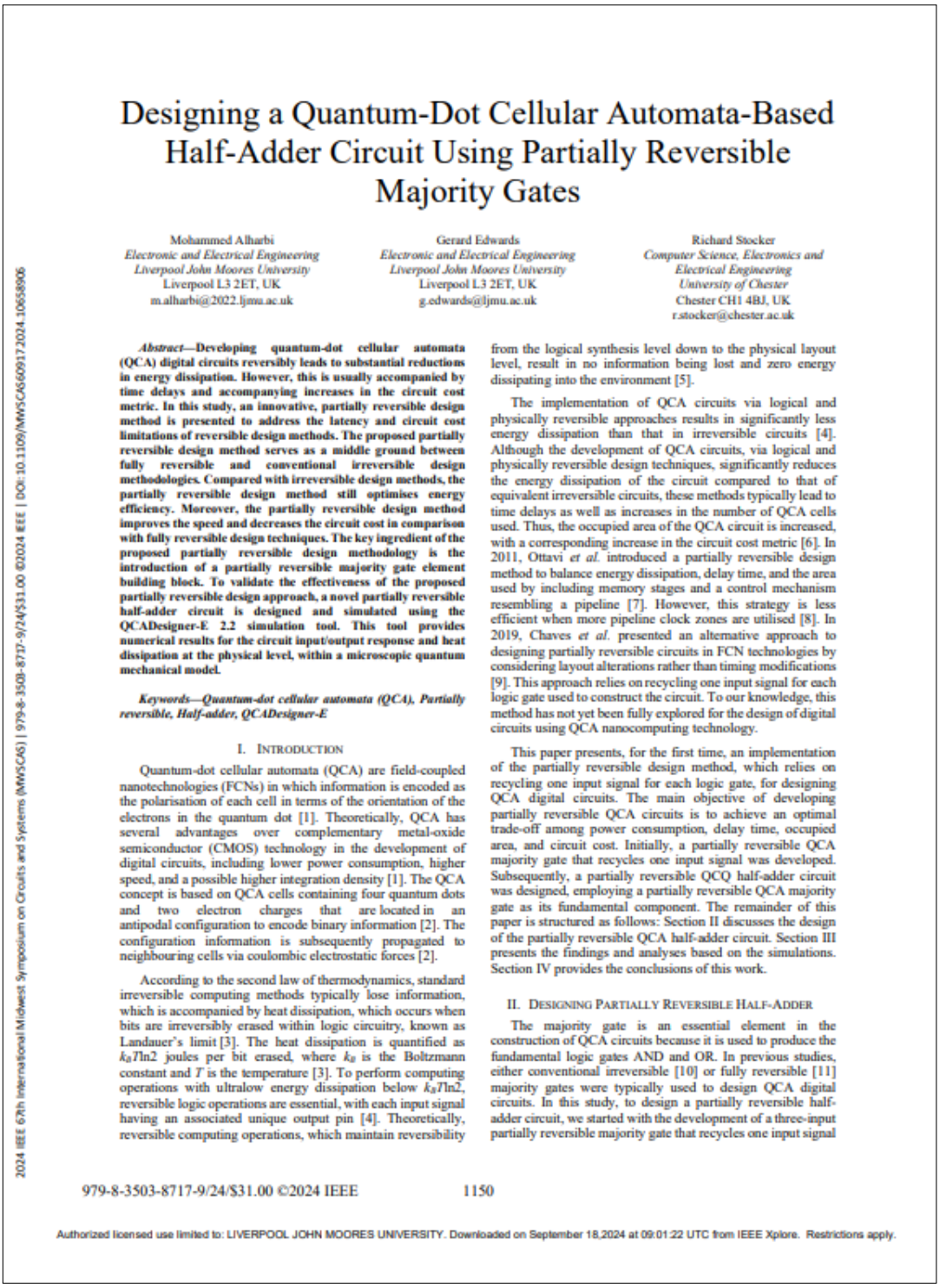
QCA half-adder requires up to 78% fewer QCA cells and 67% less area than the proposed partially reversible QCA half-adder. However, compared with existing fully reversible QCA half-adder circuits, the proposed partially reversible QCA half-adder uses up to 27% fewer QCA cells, and the occupied area is decreased by up to 43%. Finally, although the speed of the proposed partially reversible QCA half-adder is up to 50% less than that of existing irreversible QCA half-adders, the proposed design is up to 67% faster than that of existing fully reversible QCA half-adders.

### 6.3. Conclusion

The innovative partially reversible design approach strikes a balance between the advantages of fully reversible and irreversible design methods by employing a partially reversible majority gate as its fundamental building block. This partially reversible majority gate was used to design a novel, partially reversible QCA half-adder circuit. The simulation results show that the proposed partially reversible QCA half-adder reduces energy dissipation by up to 86% compared with irreversible QCA half-adder circuits reported in the literature. Furthermore, although existing fully reversible QCA half-adder circuits dissipate up to 78% less energy than the proposed partially reversible half-adder circuit, the proposed partially reversible QCA half-adder circuit has time delays up to 67% less, costs up to 77% less, uses up to 27% fewer QCA cells, and occupies up to 43% less area than existing fully reversible QCA half-adder circuits.

### 6.4. Contribution

The research findings from this chapter were presented as a lecture at the *IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS)*, Springfield, MA, USA, 2024, and subsequently published as a conference paper entitled “Designing a Quantum-Dot Cellular Automata-Based Half-Adder Circuit Using Partially Reversible Majority Gates” (refer to Figure 6.4) [35], contributing to the QCA literature on building QCA circuits employing partially reversible logic gates.



# Designing a Quantum-Dot Cellular Automata-Based Half-Adder Circuit Using Partially Reversible Majority Gates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***Abstract*—Developing quantum-dot cellular automata (QCA) digital circuits reversibly leads to substantial reductions in energy dissipation. However, this is usually accompanied by time delays and accompanying increases in the circuit cost metric. In this study, an innovative, partially reversible design method is presented to address the latency and circuit cost limitations of reversible design methods. The proposed partially reversible design method serves as a middle ground between fully reversible and conventional irreversible design methodologies. Compared with irreversible design methods, the partially reversible design method still optimises energy efficiency. Moreover, the partially reversible design method improves the speed and decreases the circuit cost in comparison with fully reversible design techniques. The key ingredient of the proposed partially reversible design methodology is the introduction of a partially reversible majority gate element building block. To validate the effectiveness of the proposed partially reversible design approach, a novel partially reversible half-adder circuit is designed and simulated using the QCADesigner-E 2.2 simulation tool. This tool provides numerical results for the circuit input/output response and heat dissipation at the physical level, within a microscopic quantum mechanical model.**



***Keywords*—Quantum-dot cellular automata (QCA), Partially reversible, Half-adder, QCADesigner-E**


## I. Introduction

Quantum-dot cellular automata (QCA) are field-coupled nanotechnologies (FCNs) in which information is encoded as the polarisation of each cell in terms of the orientation of the electrons in the quantum dot [1]. Theoretically, QCA has several advantages over complementary metal-oxide semiconductor (CMOS) technology in the development of digital circuits, including lower power consumption, higher speed, and a possible higher integration density [1]. The QCA concept is based on QCA cells containing four quantum dots and two electron charges that are located in an antipodal configuration to encode binary information [2]. The configuration information is subsequently propagated to neighbouring cells via coulombic electrostatic forces [2].

According to the second law of thermodynamics, standard irreversible computing methods typically lose information, which is accompanied by heat dissipation, which occurs when bits are irreversibly erased within logic circuitry, known as Landauer's limit [3]. The heat dissipation is quantified as $k_B 7\ln 2$ joules per bit erased, where $k_B$ is the Boltzmann constant and $T$ is the temperature [3]. To perform computing operations with ultralow energy dissipation below $k_B 7\ln 2$, reversible logic operations are essential, with each input signal having an associated unique output pin [4]. Theoretically, reversible computing operations, which maintain reversibility from the logical synthesis level down to the physical layout level, result in no information being lost and zero energy dissipating into the environment [5].

The implementation of QCA circuits via logical and physically reversible approaches results in significantly less energy dissipation than that in irreversible circuits [4]. Although the development of QCA circuits, via logical and physically reversible design techniques, significantly reduces the energy dissipation of the circuit compared to that of equivalent irreversible circuits, these methods typically lead to time delays as well as increases in the number of QCA cells used. Thus, the occupied area of the QCA circuit is increased, with a corresponding increase in the circuit cost metric [6]. In 2011, Ottavi *et al.* introduced a partially reversible design method to balance energy dissipation, delay time, and the area used by including memory stages and a control mechanism resembling a pipeline [7]. However, this strategy is less efficient when more pipeline clock zones are utilised [8]. In 2019, Chaves *et al.* presented an alternative approach to designing partially reversible circuits in FCN technologies by considering layout alterations rather than timing modifications [9]. This approach relies on recycling one input signal for each logic gate used to construct the circuit. To our knowledge, this method has not yet been fully explored for the design of digital circuits using QCA nanocomputing technology.

This paper presents, for the first time, an implementation of the partially reversible design method, which relies on recycling one input signal for each logic gate, for designing QCA digital circuits. The main objective of developing partially reversible QCA circuits is to achieve an optimal trade-off among power consumption, delay time, occupied area, and circuit cost. Initially, a partially reversible QCA majority gate that recycles one input signal was developed. Subsequently, a partially reversible QCQ half-adder circuit was designed, employing a partially reversible QCA majority gate as its fundamental component. The remainder of this paper is structured as follows: Section II discusses the design of the partially reversible QCA half-adder circuit. Section III presents the findings and analyses based on the simulations. Section IV provides the conclusions of this work.

## II. Designing Partially Reversible Half-Adder

The majority gate is an essential element in the construction of QCA circuits because it is used to produce the fundamental logic gates AND and OR. In previous studies, either conventional irreversible [10] or fully reversible [11] majority gates were typically used to design QCA digital circuits. In this study, to design a partially reversible half-adder circuit, we started with the development of a three-input partially reversible majority gate that recycles one input signal





**Figure 6.4 Conference paper: Novel ultra-energy-efficient reversible designs of sequential logic quantum-dot cellular automata flip-flop circuits**

# Chapter 7

# 7. Hybrid Design Method

Power consumption, operating frequency, and occupied area are critical specifications in the design of digital ICs [30]. In conventional CMOS technology, these parameters are often interdependent, resulting in trade-offs where optimising one aspect can negatively affect the others [204]. For example, enhancing the operating frequency may lead to increased power consumption, whereas minimising the occupied area could degrade speed or elevate power consumption. Therefore, achieving an optimal balance among these competing factors is essential to ensure the circuit fulfils the desired performance, efficiency, and application's specific requirements [204].

In QCA, previous studies have demonstrated a significant trade-off between area, speed, and power consumption. Designing QCA circuits in a logically and physically reversible manner can significantly reduce energy dissipation [31-34, 141]. However, this approach is often associated with penalties in terms of increased area and reduced speed [205, 206]. On the other hand, designing QCA circuits in an irreversible manner typically requires less area and achieves higher speed compared to their reversible counterparts [207, 208]. However, this comes at the cost of increased power consumption compared to reversible QCA circuits [93].

Current QCA design methodologies utilise a single form of majority gates, either reversible or irreversible, to construct QCA digital circuits. When cost efficiency, in terms of operating frequency and occupied area, is the primary consideration, QCA circuits employ irreversible majority gates. On the other hand, reversible majority gates are used when power efficiency is prioritised. Most applications require circuits that balance optimal efficiency across all key metrics: power consumption, speed, and area.

This chapter introduces an innovative hybrid design method that represents a compromise solution between energy efficiency-orientated reversible design methods and cost efficiency-orientated irreversible design methods. This hybrid design method simultaneously uses three types of majority gates to develop QCA digital circuits. It

employs the conventional irreversible majority gate, the reversible majority gate introduced in Chapter 2, and the partially reversible majority gate introduced in Chapter 6, as the primary building blocks for creating hybrid QCA circuits. The key advantage of the proposed hybrid design method is its ability to provide a high level of control over the circuit characteristics during the design process. The ultimate function of the circuit determines the number of each type of majority gate that is used.

For example, if energy efficiency is prioritised for the circuit, while maintaining an appropriate level of cost efficiency, then the number of reversible majority gates must surpass the number of irreversible and partially reversible majority gates, in the circuit. In contrast, if minimising area costs, while maintaining a suitable level of energy efficiency is the focus, then the circuit must include more irreversible majority gates, than reversible and partially reversible majority gates. To establish the optimal trade-off between energy dissipation and circuit cost, the use of a greater proportion of partially reversible majority gates than of reversible and irreversible majority gates, is advisable. Thus, the hybrid design method allows the designer to determine the number of different types of majority gate in the circuit, i.e., reversible, partially reversible, or irreversible, thereby providing significant control over the circuit characteristics throughout the design process.

### 7.1. Designing hybrid QCA half-adders

To evaluate the efficiency of the innovative hybrid design method, four hybrid QCA half-adder circuits were designed and simulated. Each circuit incorporates various types of majority gates. A comprehensive case study is a valuable exploration, demonstrating the practical applicability and effectiveness of the proposed hybrid design methodology in designing QCA digital circuits.

The type and number of majority gates used to design a QCA circuit are critical aspects that can influence circuit specifications. In previous studies, only one type of majority gate, either the reversible majority gate [32, 149] or the irreversible majority gate [12, 202, 209-212], was used in the design of QCA half-adder circuits. In terms of the number of majority gates used for designing the half-adder circuit, a few prior studies used five majority gates [210, 212], whereas others used four majority gates [32, 149, 202]. In this case study, we have developed hybrid QCA half-adder circuits by simultaneously using

three types of majority gates: reversible, irreversible, and partially reversible. Furthermore, the total number of majority gates used to build these half-adders was four. By using the three different types of majority gates to represent the four majority gates that constitute the half-adder, we can obtain a total of 81 different possible combinations that can represent the same QCA half-adder circuit. Despite all these designs having the same functionality, each has unique gate composition and interconnections. The number of majority gates for each of the three types of majority gates used in the circuit determines the energy consumption, delay time, and area occupied. Thus, by changing the types of majority gates included in the circuit, the designer can achieve a higher level of control over the final specifications of the circuit.

Describing the complete 81 possible combinations, that represent the hybrid QCA half-adder circuit, is a large design configuration space. This section takes four distinct combinations of majority gates, to design four different hybrid QCA half-adder circuits, as a sample of the full design configuration space. These four versions are sufficient to effectively illustrate the concept of the hybrid design methodology; the other 77 designs are permutations of each of these four combinations. The main difference between these four hybrid QCA half-adder circuits lies in the number of reversible, partially reversible, and irreversible majority gates employed in designing the half-adder circuit, as illustrated in Table 7.1.

**Table 7.1 The number and types of majority gates utilised in the design of the four proposed hybrid QCA half-adders.**

| Proposed Half-Adder Design | Number of Majority Gates Used | | |
|---|---|---|---|
| | Fully Reversible | Partially Reversible | Irreversible |
| HA-1 | 3 | 0 | 1 |
| HA-2 | 2 | 1 | 1 |
| HA-3 | 2 | 0 | 2 |
| HA-4 | 0 | 2 | 2 |

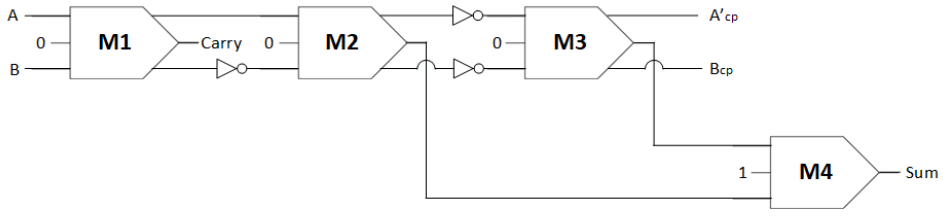
The first proposed design of a hybrid QCA half-adder (HA-1) uses three fully reversible majority gates and one irreversible majority gate. The second proposed hybrid QCA half-adder design (HA-2) uses two fully reversible majority gates, one partially reversible majority gate, and one irreversible majority gate. The third proposed hybrid QCA half-adder design (HA-3) consists of two fully reversible and two irreversible

majority gates. The fourth proposed hybrid half-adder design (HA-4) consists of two partially reversible and two irreversible majority gates.

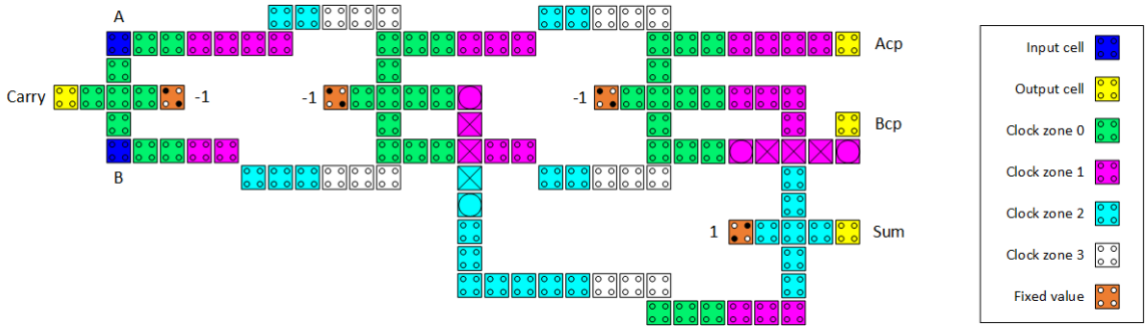
The novel hybrid QCA half-adder designs used the standard technological parameters previously listed in Table 2.1. To prevent wire junction issues, a multilayer approach with three distinct layers was used [72]. Furthermore, the USE clocking technuiqe was employed to synchronise the data transmission [78].

### 7.1.1. The HA-1 design

Figure 7.1 presents the design of HA-1, which uses three fully reversible majority gates (M1, M2, and M3) and one irreversible majority gate (M4). Figure 7.1a depicts the logic synthesis of this hybrid half-adder circuit, whereas Figure 7.1b displays the QCA layout. The circuit consists of 117 QCA cells, which occupy an area of 0.16 µm2. The measured latency is 11 clock phases, which is equal to 2.75 clock cycles.




(a)




(b)

**Figure 7.1 The HA-1 design (a) logic synthesis and (b) QCA layout.**

### 7.1.2. The HA-2 design

Two fully reversible majority gates (M1 and M2), one partially reversible majority gate (M3), and one irreversible majority gate (M4) make up HA-2. Figure 7.2a shows the

logic synthesis of this hybrid half-adder, whereas Figure 7.2b shows the QCA layout. In the HA-2 design, the only modification compared with the HA-1 design is the change in the reversibility of one majority gate, M3, from fully to partially reversible. Consequently, there is a 6% decrease in the number of QCA cells compared to the HA-1 design, resulting in a total of 110 QCA cells in the HA-2 design. However, the occupied area and delay time are consistent with those of the HA-1 design, with an area of 0.16 m2 and a delay of 11 clock phases, equivalent to 2.75 clock cycles.

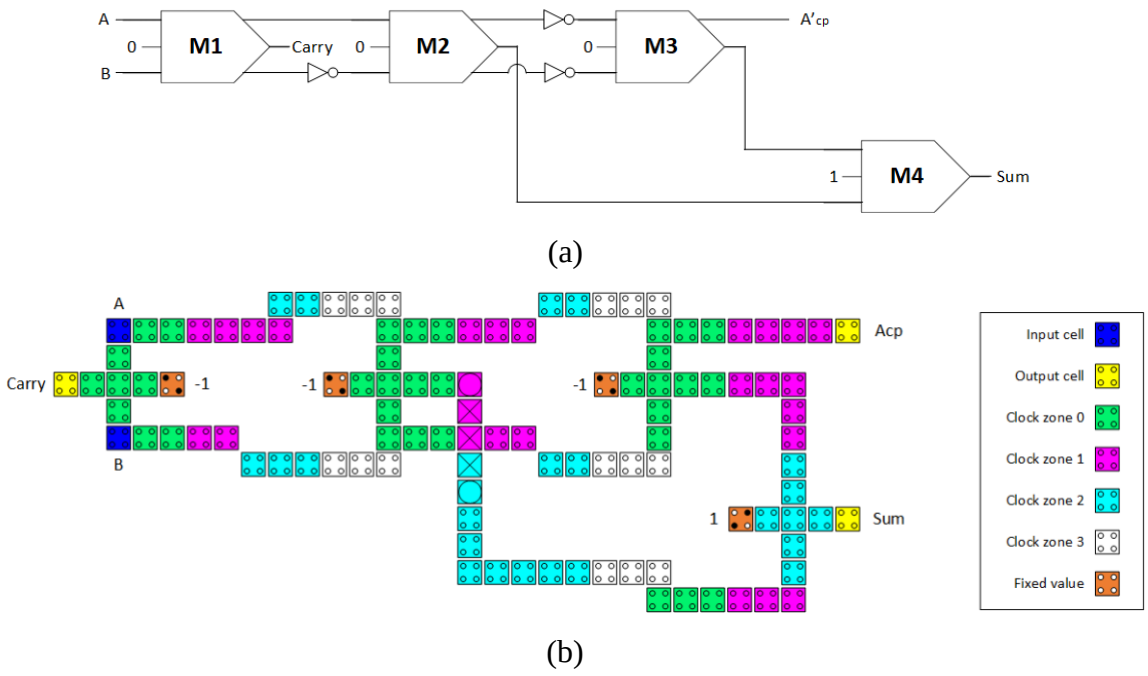



**Figure 7.2 The HA-2 design (a) logic synthesis and (b) QCA layout.**

### 7.1.3. The HA-3 design

Two fully reversible majority gates (M1 and M2) and two irreversible majority gates (M3 and M4) make up the HA-3 design, as shown in Figure 7.3. Figure 7.3a depicts the logic synthesis of the HA-3 circuit, whereas Figure 7.3b displays the QCA layout. In the HA-3 design, the only modification compared with the HA-2 design is the change in the reversibility of one majority gate, M3, from partially reversible to irreversible. As a result, the number of QCA cells decreased by 8.2%, the occupied area decreased by 18.8%, and the speed improved by 9% compared to the HA-2 design. The HA-3 design utilises 101

QCA cells to construct the circuit, occupying an area of 0.13 m2. The measured latency is 10 clock phases, which is equal to 2.5 clock cycles.

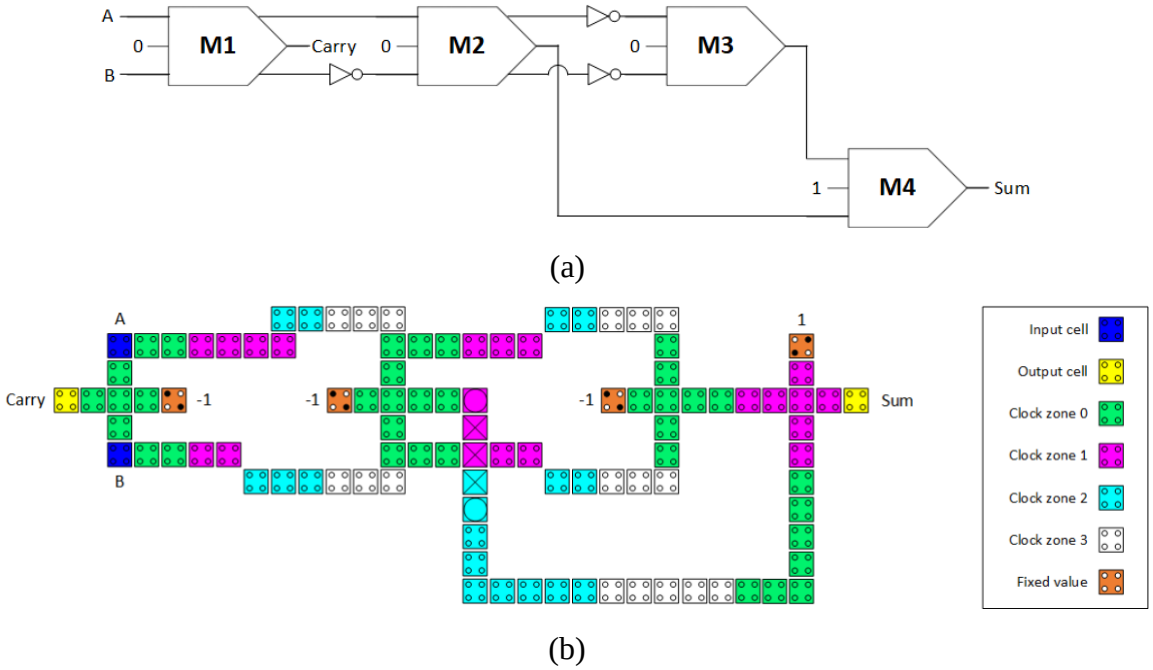
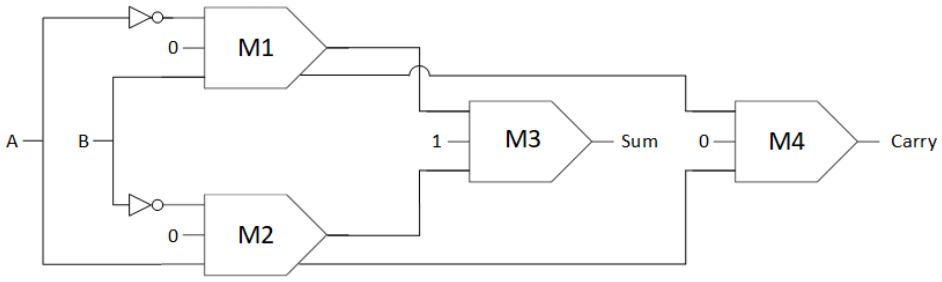


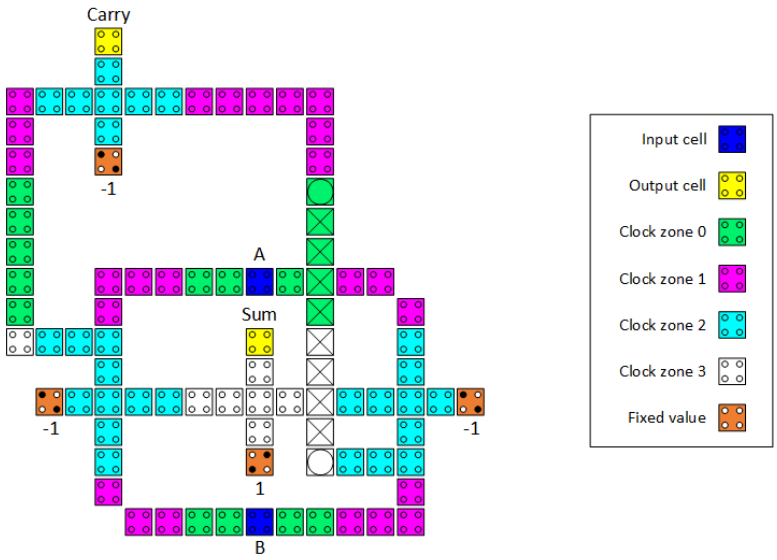

**Figure 7.3 The HA-3 design (a) logic synthesis and (b) QCA layout.**

### 7.1.4. The HA-4 design

Figure 7.4 presents the HA-4 design, which consists of two partially reversible majority gates (M1 and M2) and two irreversible majority gates (M3 and M4). Figure 7.4a shows the logic synthesis of this hybrid half-adder circuit, whereas Figure 7.4b shows the QCA layout. The HA-4 design differs from the HA-3 design in that the reversibility of two majority gates, M1 and M2, changes from partially reversible to irreversible. As a result, compared to the HA-3 design, the number of QCA cells decreases by 11.9%, the occupied area decreases by 7.7%, and the speed improves significantly by 60%. The HA-4 circuit consists of 90 QCA cells, which occupy an area of 0.12 µm2. The measured latency is 4 clock phases, which is equal to 1 clock cycle.




(a)




(b)

**Figure 7.4 The HA-4 design (a) logic synthesis and (b) QCA layout.**

## 7.2. Simulation results

This section gives an in-depth examination of the hybrid QCA half-adder circuits discussed in Section 7.1, focusing on their performance reliability, information loss, energy dissipation, and circuit cost.

### 7.2.1. Performance evaluation

The *QCADesigner 2.0.3* simulation tool has been used to simulate the input/output behaviour of the four devised hybrid QCA half-adder designs. To validate the reliability of the innovative hybrid design method in developing QCA digital circuits, the simulated waveforms have been compared with the values in the truth table of the half-adder circuit given earlier in Table 3.3.

#### 7.2.1.1. Simulated waveforms of HA-1 design

Figure 7.5 shows the simulated waveforms for the HA-1 design. The correct polarisation output corresponds to the half-adder truth table values, confirming the HA-1 design's performance reliability.

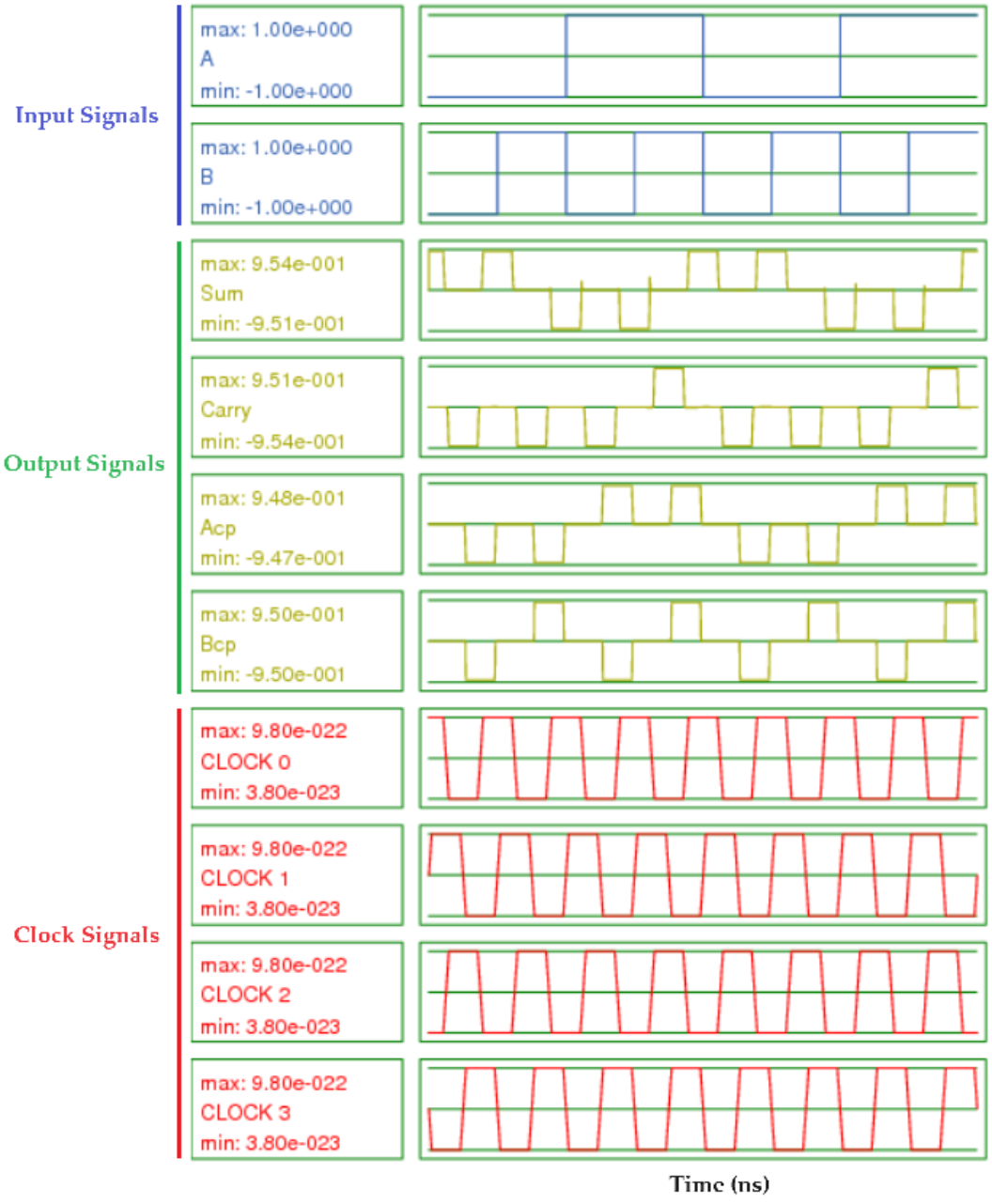



**Figure 7.5 Simulated waveforms of HA-1.**

#### 7.2.1.2. Simulated waveforms of HA-2 design

Figure 7.6 illustrates the simulated waveforms for the HA-2 design. The polarisation output accurately matches the half-adder truth table values, confirming the performance reliability of HA-2.


**Figure 7.6 Simulated waveforms of HA-2.**

### 7.2.1.3. Simulated waveforms of HA-3 design

Figure 7.7 depicts the simulated waveforms for the HA-3 design. The polarisation output exactly matches the truth table values of the half-adder circuit, proving that the HA-3 design is reliable.

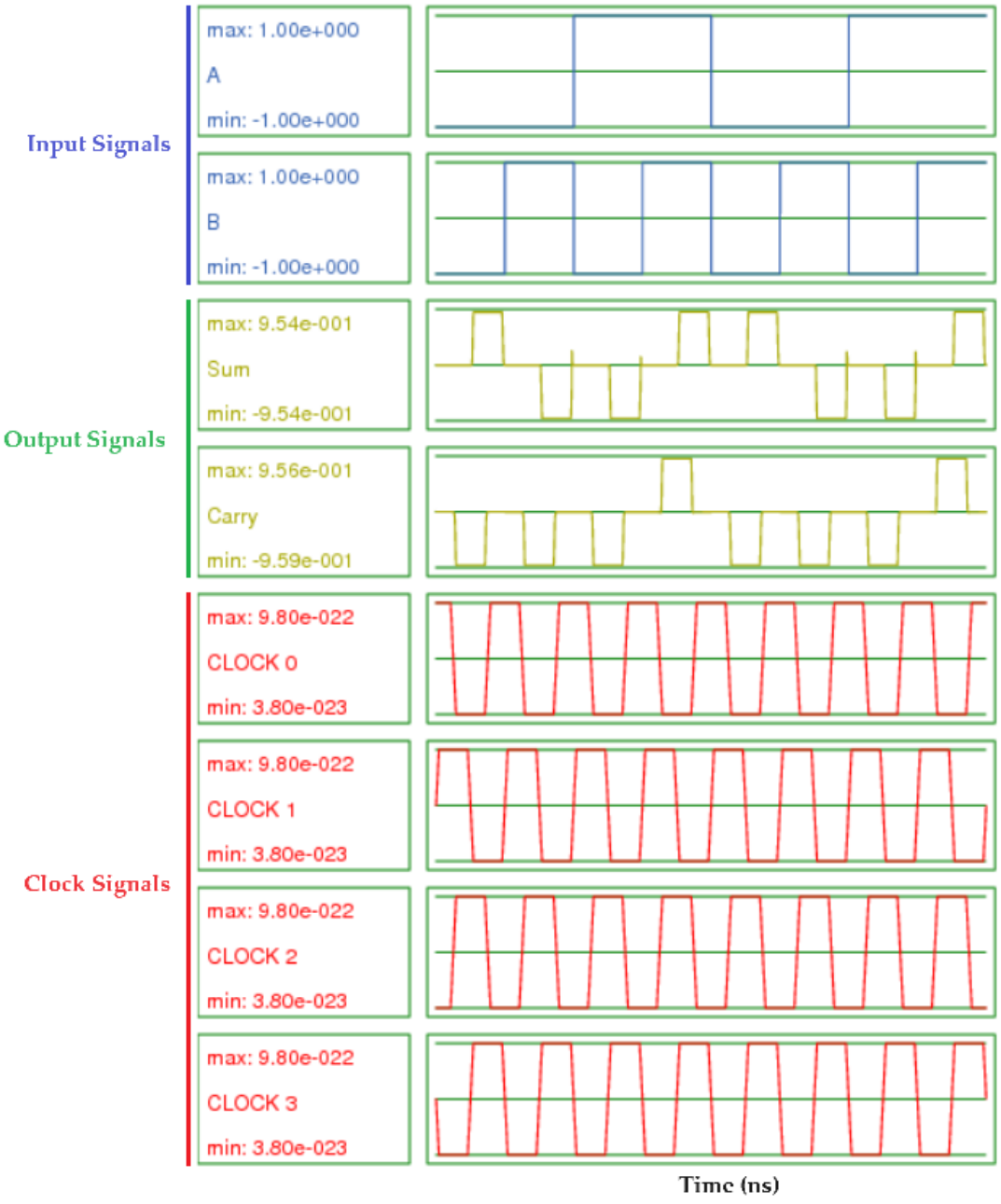



**Figure 7.7 Simulated waveforms of HA-3.**

#### 7.2.1.4. Simulated waveforms of HA-4 design

Figure 7.8 displays the simulated waveforms for the HA-4 design. The polarisation output precisely matches the half-adder truth table values, proving the performance reliability of the HA-4.

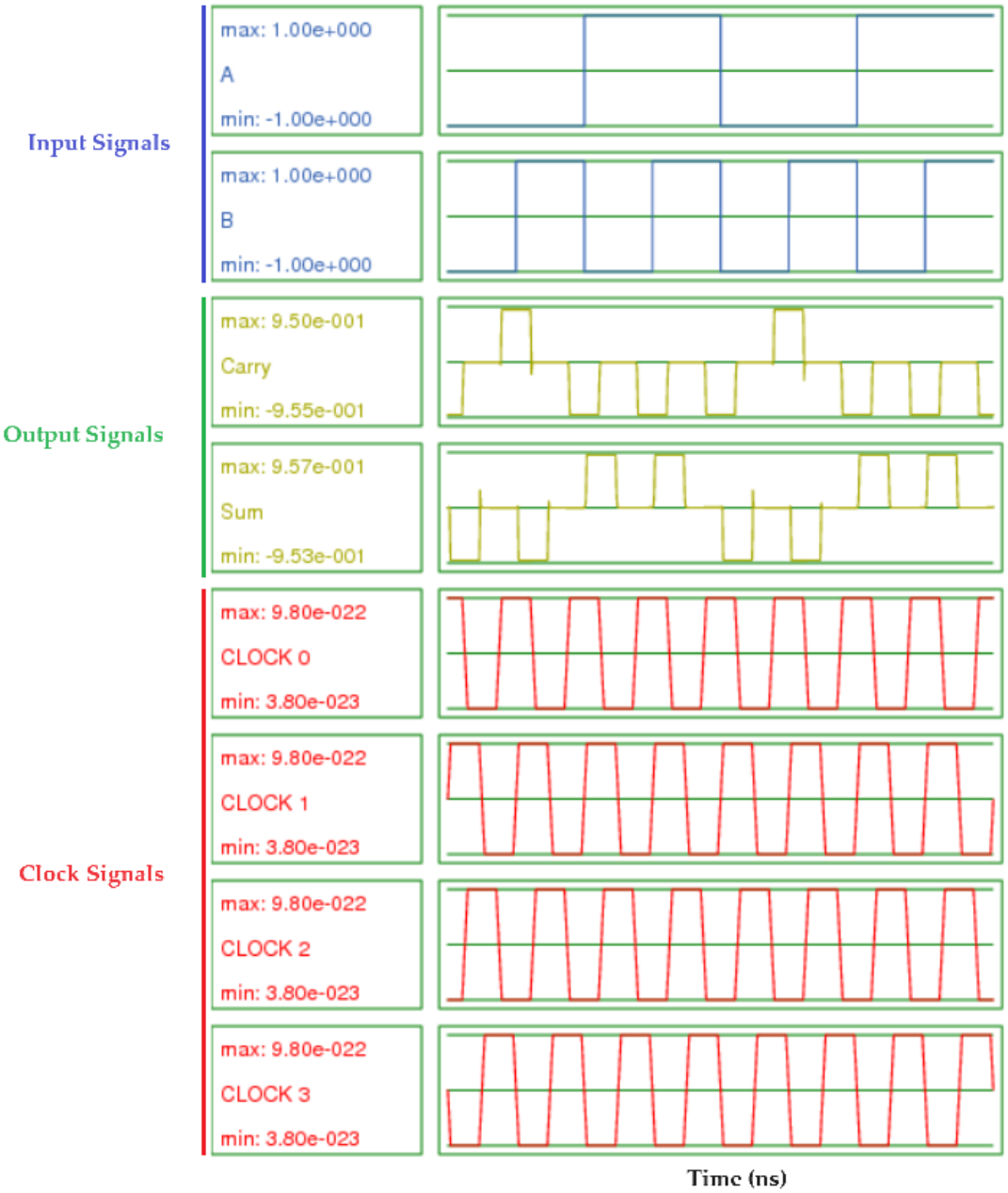



**Figure 7.8 Simulated waveforms of HA-4.**

### 7.2.2. Information dissipation calculation

This section presents calculations of the information dissipation for the hybrid QCA half-adder circuits under consideration. Shannon's entropy [213] is a key concept in information theory that quantifies the level of information contained within a set of possible outcomes. Various disciplines, including telecommunications [214, 215], encryption [216, 217], and data compression [218], commonly employ Shannon's entropy. Thus, Shannon's entropy was used to calculate the total amount of information dissipated in each of the four hybrid QCA half-adder circuits presented in this study. The formula for Shannon's entropy $H(X)$ for a discrete random variable $X$ with possible values of $x_1, x_2, x_3, \dots, x_n$ is given by Equation 7.1:

$$H(X) = -\sum_{i=1}^{n} P(x_i) \times \log_2 P(x_i), \tag{7.1}$$

where $P(x_i)$ is the probability of outcome $x_i$ and $\log_2$ is the logarithm of the two-bit entropy.

To determine the amount of information lost in each gate, we measured the difference between Shannon's entropy for the probability distributions of the initial and final states of the gates, i.e., $H(X) - H(Y)$, where the entropy $H(X)$ of $X$ is the summation of the contributions of all initial states and the entropy $H(Y)$ of $Y$ is the summation of the contributions of all final states. Finally, the total information dissipated in a circuit is computed by summing the information lost for the gates comprising the circuit using Equation 7.2.

$$T = \sum_{i=1}^{n} H(X_i), \tag{7.2}$$

where $n$ is the number of gates used to construct the circuit.

To determine the information dissipation of the four proposed hybrid QCA half-adders, we first calculate Shannon's entropy using equation 7.1 and then calculate the total information loss using equation 7.2.

#### 7.2.2.1. Information dissipation of HA-1

The information dissipation of HA-1, represented in Figure 7.1, is shown in Table 7.2. The fully reversible majority gates M1, M2, and M3 recycle all the information without any information loss, as listed in Table 7.2a, Table 7.2b, and Table 7.2c. In contrast, Table 7.2d shows that the irreversible majority gate M4 loses 0.5 bits of information. Thus, the information loss in HA-1 is solely due to the irreversible majority gate M4, resulting in an information loss of 0.5 bits.

**Table 7.2 Information dissipation calculation of HA-1.**

(a) **Gate M1**

| | **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $A$ | $B$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $carry$ | $A_{cp}$ | $B_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ¼ | 0.5 | $y_0$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_1$ | 0 | 1 | ¼ | 0.5 | $y_1$ | 0 | 0 | 1 | ¼ | 0.5 |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 0 | 1 | 0 | ¼ | 0.5 |
| $x_3$ | 1 | 1 | ¼ | 0.5 | $y_3$ | 1 | 1 | 1 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | | $H(Y)$ | 2 |
| | | | | $H(X) - H(Y) = 0$ | | | | | | |

(b) **Gate M2**

| | **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $A_{cp}$ | $\overline{B}_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M2_{outp}$ | $A_{cp}$ | $\overline{B}_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 1 | ¼ | 0.5 | $y_0$ | 0 | 0 | 1 | ¼ | 0.5 |
| $x_1$ | 0 | 0 | ¼ | 0.5 | $y_1$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_2$ | 1 | 1 | ¼ | 0.5 | $y_2$ | 1 | 1 | 1 | ¼ | 0.5 |
| $x_3$ | 1 | 0 | ¼ | 0.5 | $y_3$ | 0 | 1 | 0 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | | $H(Y)$ | 2 |
| | | | | $H(X) - H(Y) = 0$ | | | | | | |

(c) **Gate M3**

| | **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $\overline{A}_{cp}$ | $B_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M3_{outp}$ | $\overline{A}_{cp}$ | $B_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 1 | 0 | ¼ | 0.5 | $y_0$ | 0 | 1 | 0 | ¼ | 0.5 |
| $x_1$ | 1 | 1 | ¼ | 0.5 | $y_1$ | 1 | 1 | 1 | ¼ | 0.5 |
| $x_2$ | 0 | 0 | ¼ | 0.5 | $y_2$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_3$ | 0 | 1 | ¼ | 0.5 | $y_3$ | 0 | 0 | 1 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | | $H(Y)$ | 2 |
| | | | | $H(X) - H(Y) = 0$ | | | | | | |

(d) **Gate M4**

| | **Input** | | | | | **Output** | | |
|---|---|---|---|---|---|---|---|---|
| $x_i$ | $M2_{outpu}$ | $M3_{output}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $sum$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ½ | 0.5 | $y_0$ | 0 | ½ | 0.5 |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $x_1$ | 0 | 1 | | | $y_1$ | 1 | | | |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 1 | ½ | 0.5 | |
| $x_3$ | 0 | 0 | ¼ | 0.5 | $y_3$ | 0 | | | |
| | | | $H(X)$ | 1.5 | | | $H(Y)$ | 1 | |
| $H(X) - H(Y) = 0.5$ | | | | | | | | | |

#### 7.2.2.2. Information dissipation of HA-2

The information dissipation of HA-2, represented in Figure 7.2, is shown in Table 7.3. Table 7.3a and Table 7.3b show that the fully reversible majority gates M1 and M2 recycle all the information without any information loss. In contrast, Table 7.3c and Table 7.3d show that the partially reversible majority gate M3 and the irreversible majority gate M4 lose 0.5 bits of information each. The information loss of the HA-2 design is attributable to the partially reversible majority gate M3 and irreversible majority gate M4. Thus, the total amount of information lost is equivalent to the summation of the M3 and M4 information losses, which is 1 bit.

**Table 7.3 Information dissipation calculation of HA-2.**

(a) **Gate M1**

| **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $A$ | $B$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $carry$ | $A_{cp}$ | $B_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ¼ | 0.5 | $y_0$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_1$ | 0 | 1 | ¼ | 0.5 | $y_1$ | 0 | 0 | 1 | ¼ | 0.5 |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 0 | 1 | 0 | ¼ | 0.5 |
| $x_3$ | 1 | 1 | ¼ | 0.5 | $y_3$ | 1 | 1 | 1 | ¼ | 0.5 |
| $H(X)$ | | | | 2 | | | $H(Y)$ | | | 2 |
| $H(X) - H(Y) = 0$ | | | | | | | | | | |

(b) **Gate M2**

| **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $A_{cp}$ | $\bar{B}_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M2_{outp}$ | $A_{cp}$ | $\bar{B}_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 1 | ¼ | 0.5 | $y_0$ | 0 | 0 | 1 | ¼ | 0.5 |
| $x_1$ | 0 | 0 | ¼ | 0.5 | $y_1$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_2$ | 1 | 1 | ¼ | 0.5 | $y_2$ | 1 | 1 | 1 | ¼ | 0.5 |
| $x_3$ | 1 | 0 | ¼ | 0.5 | $y_3$ | 0 | 1 | 0 | ¼ | 0.5 |
| $H(X)$ | | | | 2 | | | $H(Y)$ | | | 2 |
| $H(X) - H(Y) = 0$ | | | | | | | | | | |

(c) **Gate M3**

| **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $\bar{A}_{cp}$ | $B_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M3_{output}$ | $\bar{A}_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 1 | 0 | ¼ | 0.5 | $y_0$ | 0 | 1 | ¼ | 0.5 |

| $x_1$ | 1 | 1 | ¼ | 0.5 | $y_1$ | 1 | 1 | ¼ | 0.5 |
|---|---|---|---|---|---|---|---|---|---|
| $x_2$ | 0 | 0 | ¼ | 0.5 | $y_2$ | 0 | 0 | ½ | 0.5 |
| $x_3$ | 0 | 1 | ¼ | 0.5 | $y_3$ | 0 | 0 | | |
| | | $H(X)$ | | 2 | | | $H(Y)$ | | 1.5 |
| | | | | $H(X) - H(Y) = 0.5$ | | | | | |

(d) **Gate M4**

| **Input** | | | | | **Output** | | | |
|---|---|---|---|---|---|---|---|---|
| $x_i$ | $M2_{output}$ | $M3_{outp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $sum$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ½ | 0.5 | $y_0$ | 0 | ½ | 0.5 |
| $x_1$ | 0 | 1 | | | $y_1$ | 1 | | |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 1 | ½ | 0.5 |
| $x_3$ | 0 | 0 | ¼ | 0.5 | $y_3$ | 0 | | |
| | $H(X)$ | | | 1.5 | | $H(Y)$ | | 1 |
| | | | | $H(X) - H(Y) = 0.5$ | | | | |

### 7.2.2.3. Information dissipation of HA-3

The information dissipation of HA-3, represented in Figure 7.3, is shown in Table 7.4. Table 7.4a and Table 7.4b demonstrate that the fully reversible majority gates M1 and M2 recycle all the information without any information loss. In contrast, Table 7.4c and Table 7.4d show that the irreversible majority gates M3 and M4 lose 1.19 bits and 0.5 bits of information, respectively. The information loss of HA-3 is attributable to the irreversible majority gates M3 and M4. Thus, the total amount of information lost is equivalent to the summation of the M3 and M4 information losses, which is 1.69 bits.

**Table 7.4 Information dissipation calculation of HA-3.**

(a) **Gate M1**

| **Input** | | | | | **Output** | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $A$ | $B$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $carry$ | $A_{cp}$ | $B_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ¼ | 0.5 | $y_0$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_1$ | 0 | 1 | ¼ | 0.5 | $y_1$ | 0 | 0 | 1 | ¼ | 0.5 |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 0 | 1 | 0 | ¼ | 0.5 |
| $x_3$ | 1 | 1 | ¼ | 0.5 | $y_3$ | 1 | 1 | 1 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | | $H(Y)$ | 2 |
| | | | | | $H(X) - H(Y) = 0$ | | | | | |

(b) **Gate M2**

| **Input** | | | | | **Output** | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $A_{cp}$ | $\bar{B}_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M2_{outp}$ | $A_{cp}$ | $\bar{B}_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 1 | ¼ | 0.5 | $y_0$ | 0 | 0 | 1 | ¼ | 0.5 |
| $x_1$ | 0 | 0 | ¼ | 0.5 | $y_1$ | 0 | 0 | 0 | ¼ | 0.5 |
| $x_2$ | 1 | 1 | ¼ | 0.5 | $y_2$ | 1 | 1 | 1 | ¼ | 0.5 |

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $x_3$ | 1 | 0 | ¼ | 0.5 | $y_3$ | 0 | 1 | 0 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | | $H(Y)$ | 2 |
| $H(X) - H(Y) = 0$ | | | | | | | | | | |

(c) **Gate M3**

| **Input** | | | | | **Output** | | | |
|---|---|---|---|---|---|---|---|---|
| $x_i$ | $\overline{A}_{cp}$ | $B_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M3_{output}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 1 | 0 | ¼ | 0.5 | $y_0$ | 0 | ¼ | 0.5 |
| $x_1$ | 1 | 1 | ¼ | 0.5 | $y_1$ | 1 | | |
| $x_2$ | 0 | 0 | ¼ | 0.5 | $y_2$ | 0 | ¾ | 0.31 |
| $x_3$ | 0 | 1 | ¼ | 0.5 | $y_3$ | 0 | | |
| | | | $H(X)$ | 2 | | | $H(Y)$ | 0.81 |
| $H(X) - H(Y) = 1.19$ | | | | | | | | |

(d) **Gate M4**

| **Input** | | | | | **Output** | | | |
|---|---|---|---|---|---|---|---|---|
| $x_i$ | $M2_{output}$ | $M3_{outp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $sum$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ½ | 0.5 | $y_0$ | 0 | ½ | 0.5 |
| $x_1$ | 0 | 1 | | | $y_1$ | 1 | | |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 1 | ½ | 0.5 |
| $x_3$ | 0 | 0 | ¼ | 0.5 | $y_3$ | 0 | | |
| | | | $H(X)$ | 1.5 | | | $H(Y)$ | 1 |
| $H(X) - H(Y) = 0.5$ | | | | | | | | |

#### 7.2.2.4. Information dissipation of HA-4

Table 7.5 displays the information dissipation of HA-4, as shown in Figure 7.4. Table 7.5a, Table 7.5b, Table 7.5c, and Table 7.5d show that the partially reversible majority gates M1 and M2 and the irreversible majority gates M3 and M4 lose 0.5, 0.5, 0.5, and 1.19 bits of information, respectively. The information loss of HA-4 is attributable to the partially reversible majority gates M1 and M2, as well as the irreversible majority gates M3 and M4. Thus, the total amount of information lost in the HA-4 design is equivalent to the summation of the M1, M2, M3, and M4 information losses, which is 2.69 bits.

**Table 7.5 Information dissipation calculation of HA-4.**

(a) **Gate M1**

| **Input** | | | | | **Output** | | | | |
|---|---|---|---|---|---|---|---|---|---|
| $x_i$ | $\overline{A}$ | $B$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M1_{output}$ | $B_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 1 | 0 | ¼ | 0.5 | $y_0$ | 0 | 0 | ½ | 0.5 |
| $x_1$ | 1 | 1 | ¼ | 0.5 | $y_1$ | 1 | 1 | | |
| $x_2$ | 0 | 0 | ¼ | 0.5 | $y_2$ | 0 | 0 | ¼ | 0.5 |
| $x_3$ | 0 | 1 | ¼ | 0.5 | $y_3$ | 0 | 1 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | $H(Y)$ | 1.5 |

| $H(X) - H(Y) = 0.5$ | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| (b) **Gate M2** | | | | | | | | | |
| **Input** | | | | | **Output** | | | | |
| $x_i$ | $A$ | $\bar{B}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $M2_{output}$ | $A_{cp}$ | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 1 | ¼ | 0.5 | $y_0$ | 0 | 1 | ½ | 0.5 |
| $x_1$ | 0 | 0 | ¼ | 0.5 | $y_1$ | 0 | 0 | | |
| $x_2$ | 1 | 1 | ¼ | 0.5 | $y_2$ | 1 | 1 | ¼ | 0.5 |
| $x_3$ | 1 | 0 | ¼ | 0.5 | $y_3$ | 0 | 0 | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | $H(Y)$ | 1.5 |
| $H(X) - H(Y) = 0.5$ | | | | | | | | | |
| (c) **Gate M3** | | | | | | | | | |
| **Input** | | | | | **Output** | | | | |
| $x_i$ | $M1_{output}$ | $M2_{outp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $sum$ | | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ½ | 0.5 | $y_0$ | 0 | | ½ | **0**.5 |
| $x_1$ | 1 | 0 | | | $y_1$ | 1 | | | |
| $x_2$ | 0 | 1 | ¼ | 0.5 | $y_2$ | 1 | | ½ | 0.5 |
| $x_3$ | 0 | 0 | ¼ | 0.5 | $y_3$ | 0 | | | |
| | | | $H(X)$ | 1.5 | | | | $H(Y)$ | 1 |
| $H(X) - H(Y) = 0.5$ | | | | | | | | | |
| (d) **Gate M4** | | | | | | | | | |
| **Input** | | | | | **Output** | | | | |
| $x_i$ | $A_{cp}$ | $B_{cp}$ | $P(x_i)$ | $H(x_i)$ | $y_i$ | $carry$ | | $P(y_i)$ | $H(y_i)$ |
| $x_0$ | 0 | 0 | ¼ | 0.5 | $y_0$ | 0 | | | |
| $x_1$ | 0 | 1 | ¼ | 0.5 | $y_1$ | 0 | | ¾ | 0.31 |
| $x_2$ | 1 | 0 | ¼ | 0.5 | $y_2$ | 0 | | | |
| $x_3$ | 1 | 1 | ¼ | 0.5 | $y_3$ | 1 | | ¼ | 0.5 |
| | | | $H(X)$ | 2 | | | | $H(Y)$ | 0.81 |
| $H(X) - H(Y) = 1.19$ | | | | | | | | | |

#### 7.2.2.5. Summary of information dissipation in the four designs

Table 7.6 summarises the calculated information dissipation of the four hybrid half-adder designs discussed earlier in this section. The calculated information loss clearly demonstrate that reduced circuit reversibility correlates with increased information loss. Specifically, replacing a reversible majority gate with an irreversible or partially reversible gate, or substituting a partially reversible majority gate with an irreversible gate, leads to a greater loss of information within the circuit.

The HA-1 design exhibits an information loss of 0.5 bits. Changing the M3 majority gate from fully reversible in HA-1 to partially reversible in HA-2 results in a twofold increase in information dissipation, from 0.5 bits to 1 bit. M3 becomes irreversible in the

HA-3 design. This leads to a 69% increase in information loss compared to HA-2, from 1 bit to 1.69 bits. Furthermore, HA-3 exhibits a 238% increase in information loss compared to HA-1, from 0.5 bits to 1.69 bits. For the HA-4 design, it excludes the use of fully reversible majority gates, with M1 and M2 modified to be partially reversible, while M3 and M4 remain irreversible, consistent with the HA-3 design. The HA-4 exhibits a 1-bit increase in information dissipation compared to the HA-3, rising from 1.69 bits to 2.69 bits, which corresponds to a 59% increase. In comparison to the HA-2, the HA-4 design has demonstrated a 1.69-bit increase in information dissipation, representing a 169% increase from 1 bit to 2.69 bits. Compared to the HA-1 design, the HA-4 design has seen a substantial rise in information dissipation with a 2.19-bit increase, equivalent to a 438% increase from 0.5 bits to 2.69 bits.

**Table 7.6 Information dissipation for the hybrid QCA half-adder designs.**

| Proposed hybrid QCA Half-Adder Design | Information Loss |
|---|---|
| HA-1 | 0.5 |
| HA-2 | 1 |
| HA-3 | 1.69 |
| HA-4 | 2.69 |

### 7.2.3. Energy dissipation simulation

Precise calculations of energy dissipation are essential for evaluating the efficiency of QCA circuits. In QCA, energy efficiency is crucial because it enables a promising solution for realising low-power computing, which is a major challenge in contemporary integrated circuit architecture. An in-depth assessment of circuit energy management is essential for improving circuit design and performance since the circuit involves the dissipation of energy between the clock, cells, and environment.

The *QCADesigner-E 2.2* [96] simulation tool was used to evaluate the energy dissipation in hybrid QCA half-adder circuits. The technological and simulation parameters, presented earlier in Table 2.1 and Table 2.2, respectively, have been employed. Table 7.7 shows the total and average energy dissipation calculations for the proposed hybrid QCA half-adder circuits. The average energy dissipation represents the average energy dissipation value across all input signal combinations in a circuit.

**Table 7.7 Energy dissipation values for the proposed hybrid QCA half-adder circuits.**

| Proposed Hybrid QCA Half-Adder Design | Energy Dissipation for an Input Combination Signal [meV] | | | | Total Energy Dissipation [meV] | Average Energy Dissipation [meV] |
|---|---|---|---|---|---|---|
| | 00 | 01 | 10 | 11 | | |
| HA-1 | 0.367 | 0.283 | 0.378 | 0.228 | 1.256 | 0.314 |
| HA-2 | 0.550 | 0.641 | 0.635 | 0.641 | 2.467 | 0.617 |
| HA-3 | 0.646 | 0.641 | 0.726 | 0.642 | 2.655 | 0.664 |
| HA-4 | 1.470 | 1.310 | 1.250 | 1.466 | 5.496 | 1.374 |

The simulation findings on the energy dissipation in the proposed hybrid QCA half-adder circuits indicate that the use of majority gates with a higher level of reversibility, which can recycle more input data, can lead to a decrease in the energy dissipation of the QCA circuit. Each half-adder has been designed to be slightly less reversible than the previous, i.e., HA-1 is more reversible than HA-2, HA-2 is more reversible than HA-3, and so on. HA-2 reduces reversibility of HA-1 by switching the third majority gate (M3) from a fully reversible gate to a partially reversible gate. This causes an average 97% increase in energy loss to 0.617 mV. HA-3 replaces this same majority gate (M3) with an irreversible gate, further increasing the energy dissipation by 6.7% over HA-2 to 6.7 mV. HA-4 retains the two irreversible majority gates (M3 and M4) from HA-3 while replacing the two reversible majority gates (M1 and M2) with two partially reversible majority gates, resulting in a 107% increase in energy dissipation over HA-3 to 1.374 mV.

### 7.2.4. Cost calculation

Equation 1.16, previously discussed in Section 1.8, calculates the cost of the proposed hybrid QCA half-adder circuits, and Table 7.8 presents the results. The cost calculations for the hybrid QCA half-adder circuits demonstrate that using majority gates with lower reversibility can effectively decrease the circuit's overall cost. HA-1 has a total cost of 253. The HA-2, which has lower reversibility than the HA-1, has decreased in cost by 13%, from 253 to 220. HA-3, which has lower reversibility than the HA-2, reduces circuit cost by an additional 9%, from 220 to 200, compared to the HA-2 design. HA-4 has the lowest reversibility among the proposed hybrid half-adders, as it does not incorporate any fully reversible majority gates. Compared to the HA-3, the HA-4 has a 56% reduction in circuit cost, from 200 to 88.

**Table 7.8 Cost values for the proposed hybrid QCA half-adder circuits.**

| QCA Half-Adder Circuit | Majority Gates | Inverters | QCA Cells | Area [μm2] | Delay [clock cycles] | Crossovers | Circuit Cost (FOM) |
|---|---|---|---|---|---|---|---|
| HA-1 | 4 | 3 | 117 | 0.16 | 2.75 | 2 | 253 |
| HA-2 | 4 | 3 | 110 | 0.16 | 2.75 | 1 | 220 |
| HA-3 | 4 | 3 | 101 | 0.13 | 2.5 | 1 | 200 |
| HA-4 | 4 | 2 | 90 | 0.12 | 1 | 2 | 88 |

### 7.3. Discussion

This section provides a comprehensive analysis of the simulation results for the four hybrid QCA half-adder circuits under consideration. The four hybrid QCA half-adder designs demonstrate various degrees of reversibility. This is attributed to the utilisation of diverse combinations of distinct types of majority gates, including irreversible, partially reversible, and fully reversible majority gates. The analysis of the simulation findings elucidates the direct relationship between the level of reversibility, amount of information lost, quantity of energy dissipated into the environment, and circuit cost.

The principles of thermodynamics and information theory confirm the intrinsic correlation between reversibility, information loss, and energy dissipation in computer circuits [219]. The ability of the circuit to recycle input information directly correlates with the level of reversibility, where recycling more input information increases the level of reversibility and thus reduces data erasure [27]. Put succinctly, QCA circuits with a greater capacity to reuse input information are intrinsically more reversible because they preserve a greater amount of information throughout their processes. Therefore, if a circuit's level of reversibility decreases, in terms of a reducing number of reversible gates, information loss increases. Figure 7.9 shows that the information loss and energy dissipation steadily increase as the reversibility level decreases, moving from HA-1 to HA-2, HA-3, and HA-4.

The reduction in the circuit reversibility, on the other hand, can result in a decrease in the circuit cost. However, reducing the circuit reversibility to achieve a lower cost can result in an increase in information loss and energy dissipation. Figure 7.10 shows that the HA-1, which has the highest level of reversibility among the four considered designs, also

has the highest cost compared to the other three designs. As the degree of reversibility decreases, the circuit cost gradually decreases for the HA-2, HA-3, and HA-4 circuits.

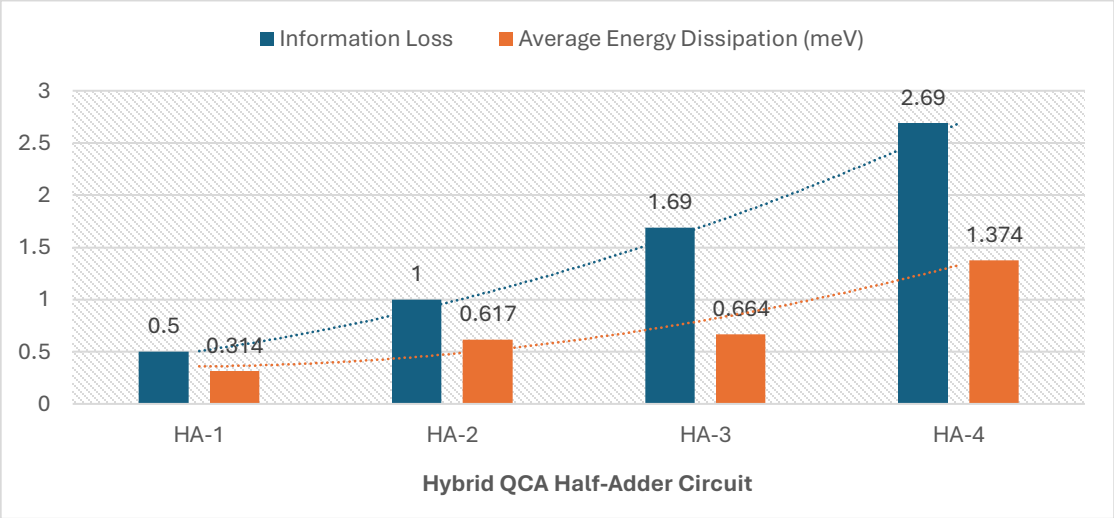



**Figure 7.9 Information loss (see Table 7.6) and average energy dissipation (see Table 7.7) of the four hybrid QCA half-adder circuits (see Table 7.1 for the gate composition of the 4 designs).**

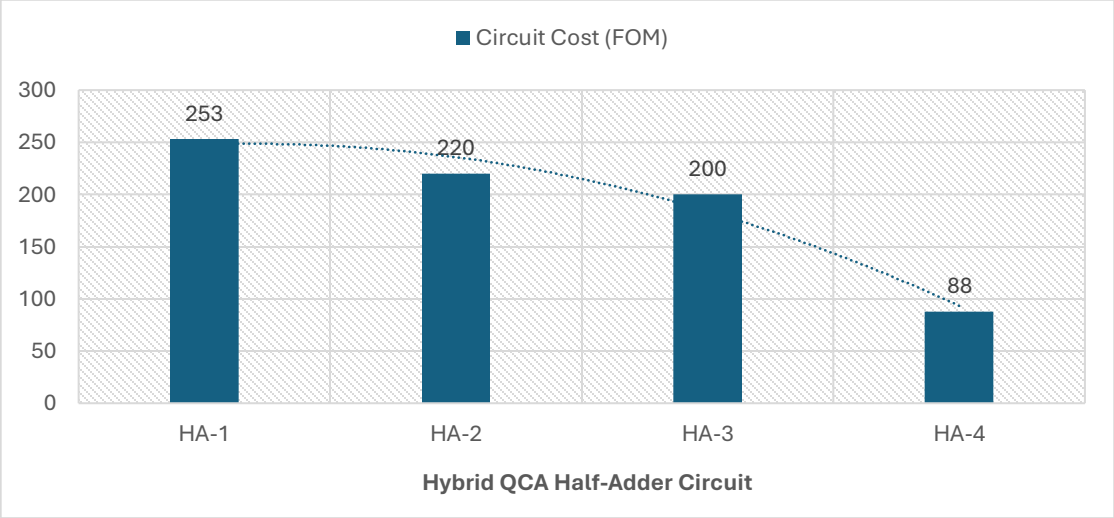



**Figure 7.10 The circuit cost FoM (see Table 7.8) of the four hybrid QCA half-adders.**

## 7.4. Conclusion

This chapter presents an innovative hybrid design method for developing QCA digital circuits. The hybrid design method uses a combination of irreversible, partially reversible, and fully reversible majority gates, as the basic building blocks. The hybrid design method offers a significant degree of flexibility in controlling the QCA circuit metrics of chip

power, speed, and area, during the design development process. Thus, the designer can establish an optimal balance between the QCA circuit power, speed, and area tailoring the circuit to meet various system requirements.

The use of the hybrid design method was validated using the half-adder circuit as a case study. Four hybrid QCA half-adder circuits were designed, each of which used a specific combination of the three types of reversible, partially reversible, and irreversible majority gates. The major difference between these four hybrid QCA half-adder circuits lie in the actual numbers of reversible, partially reversible, and irreversible majority gates employed in designing the half-adder circuit. These four half adder circuits designs are effectively illustrate the concept of the hybrid design methodology. The *QCADesigner-E 2.2* simulation tool was used to simulate the performance and energy efficiency of the hybrid QCA half-adders, at the physical level. Shannon's entropy was used to calculate the information lost for each half-adder circuit and the associated energy dissipation.

The simulation findings confirm that the hybrid design method can be used to control QCA circuit metrics, including information loss, energy dissipation, delay time, data transmission, and circuit cost, by manipulating the degree of reversibility. An increase in the circuit reversibility can negatively affect its cost. At the same time, the circuit energy efficiency can be improved by reducing the information loss and energy dissipation. Conversely, a decrease in the reversibility level of the circuit can positively affect its cost, while negatively affecting the power consumption, by increasing information loss and energy dissipation.

### 7.5. Contribution

A research article titled "Hybrid Quantum-Dot Cellular Automata Nanocomputing Circuits," based on the results from this chapter, was published in the July 2024 edition of the journal *Electronics* (refer to Figure 7.11) [36]. The article makes a significant contribution by introducing the hybrid QCA design technique, bringing enhanced design flexibility to the field.

*electronics*

MDPI

*Article*

# Hybrid Quantum-Dot Cellular Automata Nanocomputing Circuits

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**Abstract:** Quantum-dot cellular automata (QCA) is an emerging transistor-less field-coupled nanocomputing (FCN) approach to ultra-scale 'nanochip' integration. In QCA, to represent digital circuitry, electrostatic repulsion between electrons and the mechanism of electron tunnelling in quantum dots are used. QCA technology can surpass conventional complementary metal oxide semiconductor (CMOS) technology in terms of clock speed, reduced occupied chip area, and energy efficiency. To develop QCA circuits, irreversible majority gates are typically used as the primary components. Recently, some studies have introduced reversible design techniques, using reversible majority gates as the main building block, to develop ultra-energy-efficient QCA circuits. However, this approach resulted in time delays, an increase in the number of QCA cells used, and an increase in the chip area occupied. This work introduces a novel hybrid design strategy employing irreversible, reversible, and partially reversible QCA gates to establish an optimal balance between power consumption, delay time, and occupied area. This hybrid technique allows the designer to have more control over the circuit characteristics to meet different system needs. A combination of reversible, irreversible, and innovative partially reversible majority gates is used in the proposed hybrid design method. We evaluated the hybrid design method by examining the half-adder circuit as a case study. We developed four hybrid QCA half-adder circuits, each of which simultaneously incorporates various types of majority gates. The QCADesigner-E 2.2 simulation tool was used to simulate the performance and energy efficiency of the half-adders. This tool provides numerical results for the circuit input/output response and heat dissipation at the physical level within a microscopic quantum mechanical model.

**Keywords:** quantum-dot cellular automata (QCA); hybrid; half-adder; QCADesigner-E



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## 1. Introduction

Quantum-dot cellular automata (QCA) is a field-coupled nanocomputing (FCN) approach in which information is encoded as the polarisation of each cell in terms of the orientation of the electrons in a quantum dot [1]. The QCA concept for encoding binary information relies on QCA cells, which consist of four quantum dots and two electron charges, arranged in an antipodal orientation [2]. The information is subsequently propagated to neighbouring cells via Coulombic electrostatic forces [3], which results in energy-efficient digital circuits with no current flow and no associated ohmic dissipation.

Theoretically, QCA offers several advantages over complementary metal oxide semiconductor (CMOS) technology in the development of digital circuits, including a lower power consumption, higher speed, and higher integration density. QCA circuits are significantly smaller than CMOS circuits due to the use of quantum dots, which measure just a few nanometres across, with a view to being implemented at the molecular level. The R. Wolkow University of Alberta research group has made fantastic progress on experimentally implementing QCA cells and forming useful digital circuits with the quantum dots that form dangling hydrogen bonds on the surface of silicon [4]. In comparison, even the smallest transistors in advanced CMOS technology are relatively larger. This size reduction



**Figure 7.11 Article paper: Hybrid QCA nanocomputing circuits**

# Chapter 8

# 8. Conclusion and Future Work

## 8.1. Conclusion

QCA is an emerging transistor-less FCN technology candidate poised to replace conventional CMOS technology in the development of next-generation computing systems. This research study aims to develop novel, adaptable, and efficient techniques for designing QCA-based ICs that can be customised to meet a wide range of application-specific requirements. To achieve this goal, this thesis introduces three innovative design methodologies for developing QCA digital circuits, including:

- Logically and physically reversible design method (see Chapter 2).
- Partially reversible design method (see Chapter 6).
- Hybrid design approach (see Chapter 7).

By exploring these innovative design strategies, this work seeks to enhance the scalability, performance, and versatility of QCA circuits, making them suitable for diverse use cases in future computing systems. The proposed design methods consider critical design parameters such as area, speed, and circuit complexity, with a strong emphasis on optimising energy efficiency.

The logically and physically reversible design method focuses on conserving information at the gate level and enhancing energy efficiency by employing fully reversible gates, which ensure minimal energy dissipation. The key component of the reversible designs is an innovative reversible majority gate. Simulation results demonstrate that the logically and physically reversible design method produces functional QCA circuits, both combinational and sequential, with an exceptional reduction in energy dissipation. This approach, however, typically results in time delays and an increase in circuit cost.

When optimising time delay and overall circuit cost is crucial, alongside achieving high energy efficiency, the partially reversible design technique offers an effective

alternative solution. This design method relies on a partially reversible majority gate element, which serves as the fundamental component of the design framework. The partially reversible design approach serves as an intermediary between logically and physically reversible design methodologies and conventional irreversible approaches. It not only improves energy efficiency compared to traditional irreversible methods but also provides significant improvements in speed and cost reduction over logically and physically reversible designs.

The hybrid design method incorporates a combination of irreversible, partially reversible, and fully reversible majority gates as its fundamental building blocks. This approach provides substantial flexibility in managing key QCA circuit metrics such as power, speed, and area during the design process. Designers can thus achieve an optimal balance among these metrics, tailoring the circuit to align with specific system requirements. Simulation results demonstrate that the hybrid design method effectively allows control of QCA circuit metrics, including information loss, energy dissipation, delay time, data transmission, and circuit cost, by adjusting the level of reversibility. Increasing circuit reversibility can improve energy efficiency by reducing information loss and energy dissipation but may also lead to higher circuit costs. Conversely, decreasing the level of reversibility can lower costs but may compromise energy efficiency due to increased information loss and energy dissipation.

In addition, a novel library of QCA designs has been developed in this research study using the innovative logically and physically reversible, partially reversible, and hybrid design methods presented in this thesis. This library consists of sequential and combinational reversible QCA circuits described in Chapters 3, 4, and 5, along with partially reversible and hybrid QCA circuits discussed in Chapters 6 and 7, respectively. In summary, the novel QCA-based design library consists of the following designs:

***Reversible QCA-Based Circuits:***

- *Combinational QCA Circuits:*
  - *Reversible QCA Majority Gate*
  - *Reversible QCA XOR Gate*
  - *Reversible QCA XNOR Gate*
  - *Reversible QCA Half-Adder*

- *Reversible QCA Half-Subtractor*
- *Reversible QCA 1:2 Demultiplexer*
- *Reversible QCA 1-bit Comparator*
- *Reversible QCA 2:4 Decoder*
- *Reversible QCA 2:1 Multiplexer*
- *Reversible QCA 4:1 Multiplexer*
- *Reversible QCA 8:1 Multiplexer*
- *Reversible QCA ALU*

➢ *Sequential QCA Circuits:*

- *Reversible QCA SR Flip-Flop*
- *Reversible QCA D Flip-Flop*
- *Reversible QCA JK Flip-Flop*
- *Reversible QCA T Flip-Flop*

***Partially Reversible QCA-Based Circuits***

➢ *Combinational QCA Circuits:*

- *Partially Reversible QCA Majority Gate*
- *Partially Reversible QCA Half-Adder*

***Hybrid QCA-Based Circuits***

➢ *Combinational QCA Circuits:*

- *Hybrid QCA Majority Gate*
- *Hybrid QCA Half-Adder 1 (consist of three reversible and one irreversible majority gates)*
- *Hybrid QCA Half-Adder 2 (consist of two reversible, one partially reversible and one irreversible majority gates)*
- *Hybrid QCA Half-Adder 3 (consist of two reversible and two irreversible majority gates)*
- *Hybrid QCA Half-Adder 4 (consist of two partially reversible and two irreversible majority gates)*

The proposed QCA-based circuits could play a signifficant role in applications demanding ultra-low power consumption, high computational density, and scalability,

particularly in fields where CMOS technology is limited by its inherent energy and scaling constraints. This innovation could revolutionise diverse fields such as medical devices, IoT, AI, cryptography, and beyond, particularly in scenarios where energy efficiency, compactness, and scalability are essential for performance and practicality.

### 8.2. Future work

Future studies can extend the findings from this thesis in two specific research directions, paving the way for targeted advancements and innovative developments in the QCA field.

First, the innovative logically and physically reversible design technique (detailed in Chapter 2), partially reversible design method (explained in Chapter 6), and hybrid design approach (discussed in Chapter 7) can all be used to develop other QCA-based reversible, partially reversible, and hybrid digital circuits in the future. These circuits include, but are not limited to:

- QCA full-adders [220].
- QCA full-subtractors [221].
- QCA ripple carry adders [222]
- QCA encoders [223].
- QCA multipliers [224].
- QCA shift registers [225].
- QCA counters [226].
- QCA Latches [227].

Second, researchers can construct more complex QCA-based circuits and systems using the cutting-edge QCA-based design library that this thesis developed (see Section 8.1). The promising simulation results obtained for the proposed reversible, partially reversible, and hybrid QCA digital circuits underscore the potential for further exploration. These results should encourage additional research efforts to develop advanced QCA-based computing circuits and systems with enhanced characteristics in speed, size, and power consumption, tailored to meet the needs of diverse applications. The integration, among QCA-based circuits with deferent levels of reversibility, holds

potential for creating sophisticated computing systems that leverage the strengths of each circuit type.

Integrating the proposed QCA designs with other QCA-based circuits and systems requires harmonising the inherent properties of QCA technology, including clocking mechanisms, wire crossing techniques, polarisation-based signal propagation, and layout design rules. This unified approach facilitates seamless integration with other QCA circuits, enabling the development of complex, energy-efficient, and highly scalable computing systems tailored to diverse applications. By adopting this strategy, the computing system fully harnesses the advantages of QCA technology while ensuring compatibility, synchronisation, and reliability across all components. These computing systems include, but are not limited to:

- QCA-based nanoprocessors [228].
- QCA-based communication systems, including QCA Network-on-Chip (NoC) architectures [229], alongside QCA serial and parallel communication links [230].
- QCA-based memory systems, including QCA random access memory (RAM) [181], read-only memory (ROM) [231], and static random access memory (SRAM) [232].
- QCA-based digital signal processing (DSP) systems [233].
- QCA-based cryptographic systems [234].
- QCA-based fault-tolerant systems, such as error correction codes (ECC) units [235] and redundant QCA circuits [236].
- QCA-based discrete cosine transform (DCT) systems [237].

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# Appendices

# Appendix I: Published Article Papers

[1] **M. Alharbi**, G. Edwards, and R. Stocker, "Design and Simulation of Reversible Time-Synchronized Quantum-Dot Cellular Automata Combinational Logic Circuits with Ultralow Energy Dissipation," *International Transaction Journal of Engineering, Management, & Applied Sciences & Technologies*, vol. 13, no. 12, pp. 1-22, 2022, Art no. 13A12I, doi: 10.14456/ITJEMAST.2022.240.

*The article published online:* **14 September 2022**



International Transaction Journal of Engineering, Management, & Applied Sciences & Technologies
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Manuscript Acceptance Letter

Manuscript entitled:
**Design and Simulation of Reversible Time-Synchronized Quantum-Dot Cellular Automata Combinational Logic Circuits with Ultralow Energy Dissipation**

Authors:
**Mohammed Alharbi[1] , Gerard Edwards[1] , Richard Stocker[2]**

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Dear Authors,
After the peer-reviewed process and revision of the manuscript following the reviewers' and editorial comments as well as improvement on the title of this paper, we would like to inform you that your manuscript is accepted for publication in the International Transaction Journal of Engineering, Management, & Applied Sciences & Technologies, V13(2022).

Congratulations and thank you for being part of the International Transaction Journal of Engineering, Management, & Applied Sciences & Technologies.

Thank you.

Best regards,

Hillary Rosy
Editorial Manager

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**Figure 0.1 The acceptance letter of publication for the article titled: Design and simulation of reversible time-synchronized quantum-dot cellular automata combinational logic circuits with ultralow energy dissipation**

[2] **M. Alharbi**, G. Edwards, and R. Stocker, "Novel ultra-energy-efficient reversible designs of sequential logic quantum-dot cellular automata flip-flop circuits," *The Journal of Supercomputing*, pp. 1-28, 2023.

*The article published online:* **1 March 2023**

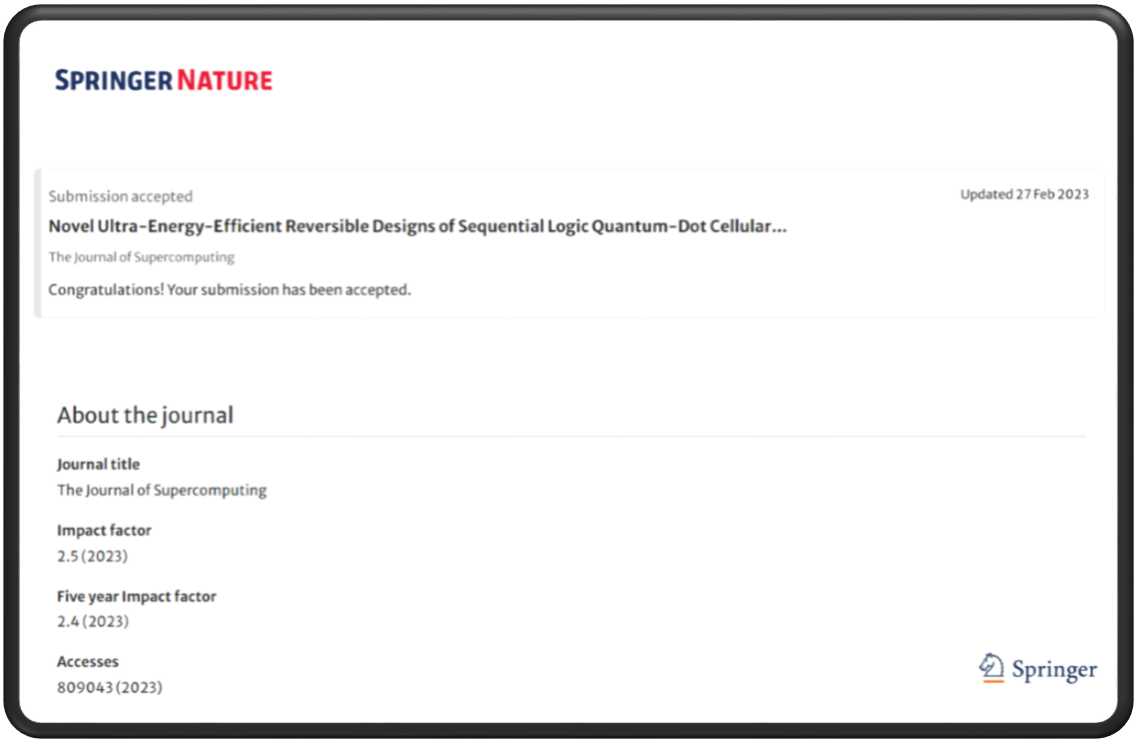


**Figure 0.2 The conformation of acceptance for the article titled: Novel ultra-energy-efficient reversible designs of sequential logic quantum-dot cellular automata flip-flop circuits**

[3] **M. Alharbi**, G. Edwards, and R. Stocker, "Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit," *Nanomaterials*, vol. 13, no. 17, p. 2445, 2023.

*The article published online:* **29 August 2023**


**Figure 0.3 The certificate of acceptance for the article titled: Reversible quantum-dot cellular automata-based arithmetic logic unit**

[4] **M. Alharbi**, G. Edwards, and R. Stocker, "An Ultra-Energy-Efficient Reversible Quantum-Dot Cellular Automata 8: 1 Multiplexer Circuit," *Quantum Reports*, vol. 6, no. 1, pp. 41-57, 2024.

*The article published online:* **16 January 2024**


**Figure 0.4 The certificate of acceptance for the article titled: Ultra-energy-efficient reversible quantum-dot cellular automata 8:1 multiplexer circuit**

[5] **M. Alharbi**, G. Edwards, and R. Stocker, "Hybrid Quantum-Dot Cellular Automata Nanocomputing Circuits," *Electronics*, vol. 13, no. 14, p. 2760, 2024.

*The article published online:* **13 July 2024**


**Figure 0.5 The certificate of acceptance for the article titled: Hybrid Quantum-dot cellular automata nanocomputing circuits**

# Appendix II: Published Book Chapters

[1] **M. Alharbi**, G. Edwards, and R. Stocker, "Reversible Quantum-Dot Cellular Automata-Based Arithmetic Logic Unit," in *Prime Archives in Nanotechnology*, T. C. Jackson Ed., 1 ed. Hyderabad, India: Vide Leaf, 2023, p. 42.

*The chapter published online:* **24 November 2023**

[2] **M. Alharbi**, G. Edwards, and R. Stocker, "Novel Ultra-Energy-Efficient Reversible Designs of Sequential Logic Quantum-Dot Cellular Automata Flip-Flop Circuits," in *Prime Archives in Electronics*, L. N. N. Thanh Ed., 1 ed. Hyderabad, India: Vide Leaf, 2023, p. 38.

*The chapter published online:* **19 December 2023**

# Appendix III: Published Conference Paper

[1] **M. Alharbi**, G. Edwards, and R. Stocker, "Designing a Quantum-Dot Cellular Automata-Based Half-Adder Circuit Using Partially Reversible Majority Gates," in *2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 2024: IEEE, pp. 1150-1153.

*The paper proceeding published online:* **16 September 2024**

# Appendix IV: Presented Conference Poster

*Poster titled*:

Reversible quantum-dot cellular automata digital circuits with ultralow energy dissipation.

*Conference*:

Single-Molecule Sensors and Nano Systems International Conference.

*Date*:

22-24 November 2023.

*Place*:

Barcelona, Spain.

*Authors*:

Mohammed Alharbi, Gerard Edwards, Richard Stocker

*Presenter*:

**Mohammed Alharbi**


**Figure 0.6 The certificate of participation and presenting a poster titled: Reversible quantum-dot cellular automata digital circuits with ultralow energy dissipation**