AC Current Controller with Error-Free Feedback Acquisition System

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***Abstract*—In this paper, we introduce an improved ac current controller with robustness against the noise in the feedback path. This three-phase current controller is suited for inverter supplied ac machines and grid-connected power converters. Conventional solutions make use of symmetric pulse-width modulation (PWM) techniques with feedback sampling in the middle of the voltage pulses. Single-sample-based feedback acquisition gets affected by the noise and parasitic phenomena. We perform a thorough analytical and experimental study on feedback errors with conventional sampling, and we consider the impact of the lockout time, motor cables, winding capacitance, and anti-aliasing filters. In order to suppress a significant spectral content in the area of low-order harmonics, we apply an improved acquisition technique, which uses a period-average and removes any PWM noise from the feedback signals. Both anti-aliasing filter and proposed period-average filter introduce delays, which impair the control-loop performance. The conventional current controller is then extended to suppress the effects of the delays. Parameter setting procedure is devised to achieve both the bandwidth and the robustness against the parameter changes. Analytical and experimental studies prove that the proposed feedback acquisition technique improves the robustness in the presence of variable delays and switching transients. Experimental tests show that the extended current controller with period-average feedback acquisition reaches the same bandwidth and robustness as the state-of-the-art controller.**

***Index Terms*—AC motor drives, current control, high performance control, signal acquisition.**

I. Introduction

ELECTRICAL drives employ position or speed control as the outer control loop. Most drives comprise a digital current controller as an inner loop [1], [2]. A fast and accurate current loop is crucial for the drive performance [3], [4]. In high-speed drives, it is essential to provide the proper decoupling of transients in *d*-axis (flux) and *q*-axis (torque) [5]–[7] and to achieve a robust operation with relatively large fundamental frequency f_e for the given sampling frequency f_S [8]–[11]. In grid-connected inverters, current loop accuracy determines the quality of the current waveforms injected into the grid.

Performance limits of current controllers are mostly related to time delays in computation, modulation, and feedback acquisition [12]. The switching ripple of the current is caused by pulse-width modulated (PWM)-based voltage actuation, and it coincides with the Nyquist frequency. Consequential anti-aliasing filtering and feedback-sampling techniques introduce delays which add to computational delays and delays related to the PWM implementation. Closed-loop performance requires the proper modeling and accounting for such delays [8], [9], [11]. Dead-beat and predictive controllers [13] are fast, but their sensitivity to parameter changes reduces their practical use.

Most widely used are the proportional-integral (PI) current controllers in synchronous frame [8], [9], [14]. Well-established parameter-setting procedures [7], [8], [12], [14] allow a straightforward implementation with the possibility to achieve a fast step response and the required disturbance rejection. The use of internal model control (IMC) concept [7] results in current controllers that cancel undesired dynamics and achieve the closed-loop bandwidth up to $f_{\mathrm{BW}} = 0.11 \cdot f_S$. Similar bandwidth is achieved with stationary-frame current controllers in [12], where $f_{\mathrm{BW}} = 0.07 \cdot f_S$. Gain tuning proposed in [14] considers both the reference tracking and the disturbance rejection and proposes the optimum closed-loop gain and active resistance parameter. The closed-loop bandwidth ranges from $0.08{\cdot}f_{\mathrm{S}}$ with no overshoot, up to $0.14{\cdot}f_{\mathrm{S}}$ with an overshoot of 40%. The PI controller design in [8] considers exact model and all the relevant delays, using neither Tustin nor other approximations. A comprehensive controller design is based on applying the IMC concept in discrete time domain. The closed-loop gain suggested in [8] is similar to the gain of [14]. The available bandwidth is $f_{\mathrm{BW}} = 0.1 \cdot f_S$, with a very large value of the fundamental frequency f_e for the given sampling frequency f_S. In most recent current control solutions, suggested gain is close to $k = 0.25 \cdot f_S$, while the closed-loop bandwidth stays next to $f_{\mathrm{BW}} = 0.1 \cdot f_S$.

All the controllers acquire the feedback signals by means of synchronous sampling, wherein the current samples are taken at the center of the voltage pulses [1], [8], [9], [12]. In this way, the feedback path has unity gain and a negligible delay. In an ideal case, the feedback is not affected by the switching ripple. In cases where the feedback waveform gets affected by delays of the anti-aliasing filter [15], delays introduced by the lockout time, by the driver circuit and switching delays, the switching ripple affects the samples and introduces an error in the feedback path. Single-sample-based acquisition is also prone to switching transients caused by the cable capacitance, the winding parasitic capacitance and other parasitic *LC* elements.

The motivation of this paper is to measure and study the sampling errors in a practical PWM converter and to reduce these errors by an improved sampling technique. In order to cope with the associated delays, we propose an enhanced current

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controller which ensures excellent overall performance. Thus, the main contributions of the paper can be summarized as follows: 1) a detailed study, illustrated with experimental results, of the impact of various parasitic phenomena on accuracy of digital current control; 2) a proposal for an improved method of sampled current averaging that is capable of significant accuracy enhancement of the current feedback signal; and 3) a novel structure of the current controller that utilizes the developed current averaging method and achieves excellent dynamic and steady-state performance.

The paper is organized as follows. Section II at first discusses current sampling errors and then suggests a method for achieving error-free sampling. Section III describes the development of the enhanced current controller. Experimental verification of the developed current controller is provided in Section IV, where a comparison with a state-of-the-art current controller is also included. Section V concludes the paper.

II. Sampling Errors and Novel Acquisition Technique

Practical current controllers acquire the feedback signals from an A/D converter. The converter receives the output currents as continuous, analog signals; it takes the samples at regular $T_S = 1/f_S$ spaced instants and converts them into digital forms. According to the sampling theorem [16], the sampled analog signal should be free from any spectral content above the frequency of $f_S/2$, also called the Nyquist frequency. Otherwise, the train of samples comprises the sampling errors, also called the aliased frequencies.

In PWM converters, the feedback currents comprise the switching ripple current, which brings in the frequency components around switching frequency f_{PWM} and its multiples. Most current controllers [8], [9], [12], [14] use synchronous sampling, where the samples are taken twice in each T_{PWM} period, in the middle of both positive and negative voltage pulses, as shown in Fig. 1. The sampling instants are spaced by $T_{\mathrm{PWM}}/2$, thus resulting in $f_S = 2 \cdot f_{\mathrm{PWM}}$. In cases where the zero-crossing of the switching ripple coincides with the sampling instants, the conventional synchronous sampling provides error-free feedback signals, unaffected by the ripple.

Whenever the switching ripple is shifted with respect to the sampling instants, the feedback signal contains an error. In Fig. 1, the zero-crossing of the switching ripple is delayed by $t_{DT}/2$ due to the lockout time, and the sample of the current contains an error. At the same time, the zero-crossing of the ripple can be shifted by the intrinsic time-delay of the anti-aliasing low-pass filter (LPF) [15].

Sampling errors are also introduced by disturbances other than the ripple. Conventional sampling is prone to the noise, as it takes a single sample per period T_{S}. The noise attenuation of the anti-aliasing LPF is increased by lowering its cutoff frequency [15], [17]. Yet, an LPF with low cutoff frequency delays the feedback and interferes with the control loop [17], [18]. Therefore, the available attenuation is restrained. At the same time, large d*v*/d*t* values of the PWM voltage waveforms in conjunction with parasitic capacitance of the cables and windings give rise to poorly damped oscillations [19] of the output voltages and currents. Passing through the LPF, these oscillations affect the samples and compromise the feedback signal. Other noise signals may produce similar effects.

In this section, we consider the errors in the feedback path, provide experimental evidence, evaluate the impact of the sampling errors on the closed-loop performance, and propose

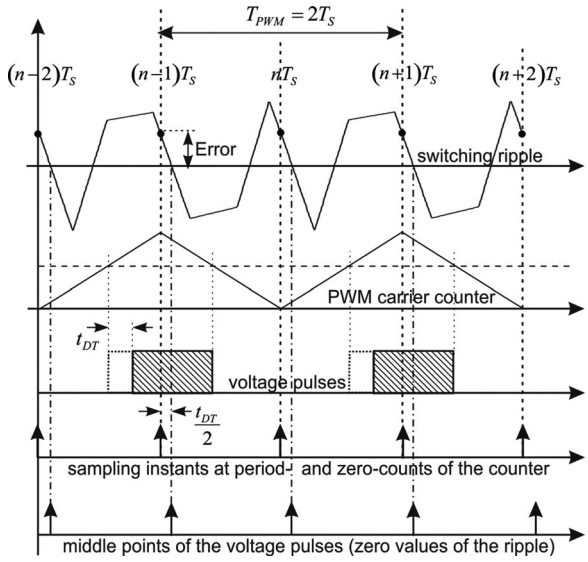

Fig. 1. Conventional synchronous sampling of the output currents. The switching ripple is obtained for $\tau_e = L_S/R_S \gg T_{\mathrm{PWM}}$. The sampling period T_S is equal to $T_{\mathrm{PWM}}/2$. The current is sampled twice at instants when the PWM carrier reaches either zero or the period count. The same events trigger the control interrupt.

TABLE I
Impact of the Lockout Time on I_q Measurement Errors

$\Delta I_{\mathrm{rms}}/I_{\mathrm{nom}}$ (%) obtained with $I_q = 4$ A, $f_{\mathrm{out}} = 275$ Hz, no cable, and $\tau_{\mathrm{LPF}} = 5\ \mu$s

Lockout time t_{DT}	**2 μs**	**3 μs**	**4 μs**	**5 μs**	**7 μs**
Synchronous sampling	1.68	1.96	2.27	2.64	3.33
Averaging in each T_{PWM}	0.68	0.73	0.82	0.89	0.95

TABLE II
Impact of the LPF Delays on I_q Measurement Errors

$\Delta I_{\mathrm{rms}}/I_{\mathrm{nom}}$ (%) obtained with $I_q = 4$ A, $f_{\mathrm{out}} = 275$ Hz, no cable, and $t_{DT} = 3\ \mu$s

LPF time constant τ_{LPF}	**5 μs**	**10 μs**	**15 μs**	**20 μs**	**80 μs**
Synchronous sampling	2.05	3.40	4.07	4.22	2.02
Averaging in each T_{PWM}	0.74	0.73	0.71	0.65	0.73

TABLE III
Impact of the Cable Length on I_q Measurement Errors

$\Delta I_{\mathrm{rms}}/I_{\mathrm{nom}}$ (%) obtained with $I_q = 4$ A, $f_{\mathrm{out}} = 275$ Hz, $\tau_{\mathrm{LPF}} = 5\ \mu$s, and $t_{DT} = 3\ \mu$s

***l* (m) of the shielded cable**	**0**	**5**	**10**	**15**	**20**
Synchronous sampling	2.02	2.55	4.24	5.69	7.03
Averaging in each T_{PWM}	0.72	0.78	0.82	0.83	0.91

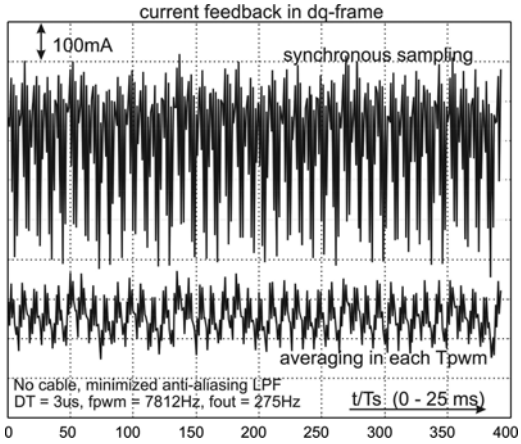

Fig. 2. Waveforms of steady-state q-axis current obtained from the experimental setup of the Appendix. The motor is connected with short wires (no cable), with $T_{\rm PWM} = 128$ μs, $t_{DT} = 3$ μs, $f_{\rm OUT} = 275$ Hz and with the minimum indispensable anti-aliasing LPF.

the method for error-free feedback acquisition. The experimental setup used in this section, as well as in Section IV, comprises a six-pole synchronous motor with surface-mounted permanent magnets, supplied from an insulated gate bipolar transistor (IGBT)-based inverter running with $E_{\rm DC} = 520$ V at $f_{\rm PWM} = 7.812$ kHz. The setup is controlled from a digital signal processor (DSP)-based platform, which uses TMS320F28335 device. All the measurements are obtained from internal DSP variables, logged in real time on a dedicated secure digital (SD) card. The relevant parameters are given in the Appendix.

In order to get the proper insight into sampling errors, the experimental results in Tables I–III and Figs. 2–4, discussed shortly, are obtained in steady state, with reduced gains of the current controller. Low gains are used to avoid sustained oscillations, caused by interaction of high gains and erroneous sampling.

A. Impact of the Lockout Time

In common PWM converters, the lockout time t_{DT} ranges from 2 to 4 μs [20], [21], and it delays turn-on of the power transistors. Depending on the sign of the output current, delay affects either the on-going or the off-going edge of the successive voltage pulse. As a consequence, the center of the successive voltage pulse is delayed by $t_{DT}/2$ (see Fig. 1), and the sampling instant misses the zero-crossing of the switching ripple. The feedback signal gets affected by the switching ripple, thus introducing the error in the actual output current. In most cases, erroneous sampling compromises the system performance. Sampling error depicted in Fig. 1 depends on the slope of the current $\mathrm{d}i/\mathrm{d}t \approx E_{\rm DC} \cdot t_{DT}/L_S$, and it increases for lower values of the load inductance $L_{\rm S}$. The error gets very large with low-inductance synchronous motors, which have surface-mounted magnets and particularly low $L_{\rm S}$.

Experimental waveforms with the q-axis current errors caused by the sampling process are given in Fig. 2. In the absence of the cable capacitance and with minimized LPF, the errors are related mainly to the lockout time. The upper waveform of Fig. 2 is obtained with conventional synchronous sampling. The lower waveform is obtained by oversampling the signals each $T_{\rm ADC} = 4$ μs and then deriving the average value each $T_{\rm S}$ for the past $T_{\rm PWM} = 2T_S$.

It is of interest to provide experimental evidence on the error in feedback signals produced by variable t_{DT}. For this purpose, the experimental setup of the Appendix is tested in steady state, with minimized output capacitance and with the lowest permissible attenuation of the LPF. In Table I, the rms values of the q-axis current measurement errors are given for conventional synchronous sampling. For t_{DT} ranging from 2 up to 7 μs, the errors change between 1.68% and 3.33% of the rated current. In parallel, the feedback samples of I_q are also obtained by oversampling, wherein the samples are taken each 4 μs, and an average of 32 samples is derived in $T_{\rm PWM}$ period. The latter computation acts as a finite impulse response (FIR) filter with an infinite attenuation at $f_{\rm PWM} = 1/T_{\rm PWM}$, thus eliminating the ripple. For this reason, the errors reported in Table I and obtained with the prescribed averaging are introduced by the disturbances other than the ripple, where the most emphasized are the slot-related harmonics within the motor back-electromotive force.

B. Impact of the Anti-aliasing Filters

Sampling errors arise from the spectral components of the input analog signal at frequencies above $f_S/2$ [18]. In digital current controllers with $f_S = 2 \cdot f_{\rm PWM}$ [8], [14], the analog signals that are brought to the analog-to-digital converter (ADC) inputs should be free from any spectral components above the Nyquist limit of $f_{\rm PWM}$. Suppression of harmful frequencies is performed by anti-aliasing LPF. This filter can be a simple *RC* network or an active filter [15], [18]. Due to a limited attenuation of analog filters, suppression of harmful frequencies is only partial. In most cases, it is sufficient to reduce the harmful signals down to the level of 1 LSB of the ADC. Attenuation of *RC* filter at high frequencies is close to $1/(\omega \cdot \tau_{\rm LPF})$, where $1/\tau_{\rm LPF} = 1/RC$ is the cutoff frequency. An increased $\tau_{\rm LPF}$ helps the filtering, but it also introduces phase delay and impairs the control loop. With synchronous sampling of Fig. 1, *RC* filter delays the zero-crossing of the ripple and contributes to the sampling errors. Experimental evidence showing the impact of the time constant $\tau_{\rm LPF} = RC$ on the rms value of the q-current is given in Table II. The error increases with $\tau_{\rm LPF}$ and exceeds 4%. With $\tau_{\rm LPF}$ as large as 80 μs, the cutoff frequency drops below 2 kHz, attenuation at high frequencies is increased and the errors are lower. With the cutoff frequency $1/\tau_{\rm LPF}$ reaching the desired closed-loop bandwidth, the phase delay of the filter brings in an unacceptable performance deterioration.

C. Impact of Parasitic LC Oscillations

In both motor-connected and grid-connected inverters, there are parasitic *LC* elements, such as the series inductance and parallel capacitance of the cables, winding-to-winding and winding-to-ground capacitance, as well as series and parallel elements of electromagnetic interference (EMI) filters. These elements create *LC* circuits with resonant frequencies f_{LC},

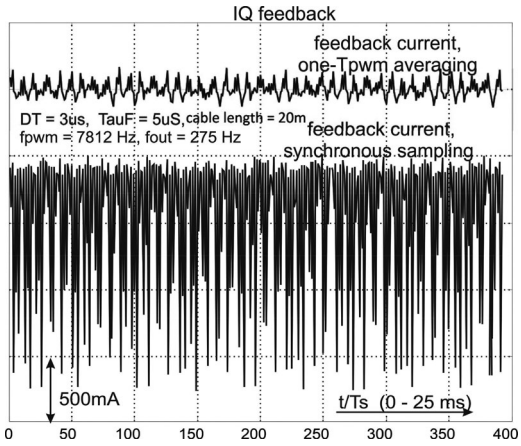

Fig. 3. Waveforms of steady-state q-axis current obtained with a 20-m-long shielded motor cable. The cable characteristic impedance is 62 Ω. The experimental setup of the Appendix runs with $f_{\rm OUT} = 275$ Hz, $T_{\rm PWM} = 128$ μs, $t_{DT} = 3$ μs, and with the anti-aliasing LPF of $\tau_{\rm LPF} = 5$ μs.

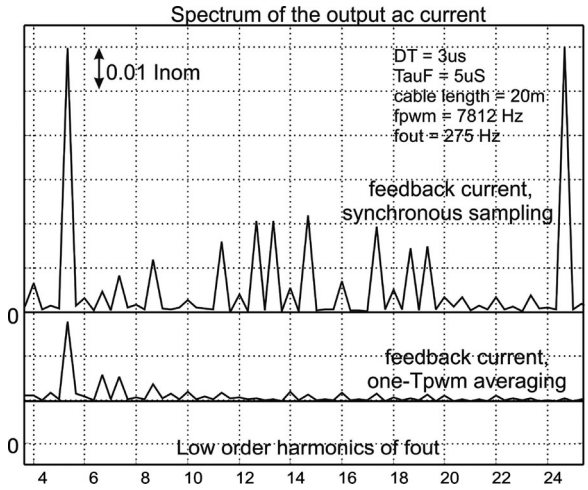

Fig. 4. Waveforms of steady-state q-axis current obtained with a 20-m-long shielded motor cable. The cable characteristic impedance is 62 Ω. The experimental setup of the Appendix runs with $f_{\rm OUT} = 275$ Hz, $T_{\rm PWM} = 128$ μs, $t_{DT} = 3$ μs, and with the anti-aliasing LPF of $\tau_{\rm LPF} = 5$ μs.

which exceed 1 MHz [19]. At the same time, the output voltages of IGBT inverters have the rate of change larger than 2500 V/μs [20]. The switching events give rise to *LC* oscillations whose amplitude decays away in less than 12 μs [19]. Whenever the sampling instant in Fig. 1 approaches the preceding switching, the sample gets affected by the parasitic oscillations. For decay of 12 μs and $T_{\rm PWM} = 128$ μs, erroneous sampling arises for the pulse width from 0% to 20%, as well as the pulse width from 80% to 100%.

Experimental waveforms of q-axis current errors obtained with a 20-m-long shielded motor cable are given in Fig. 3. The lower trace represents the error obtained with synchronous sampling. The upper trace is obtained with the same oversampling procedure used in Fig. 2.

Harmonic content of the output ac current is given in Fig. 4, obtained in the same operating conditions as those of Fig. 3. The fifth harmonic reaches 6%, while a number of harmonics between 11th and 19th reach 2% of the rated current. In Table III, the change in the rms value error of the q-axis current is given as a function of the cable length. With a 10-m-long motor cable, the rms value of the error exceeds 4%.

Sampling errors comprise high-frequency components (see Fig. 4), which reduce permissible gain of current controller and impair the closed-loop bandwidth. In a similar manner, the sampling errors reduce the applicable values of the active resistance, which is often used to improve disturbance rejection of the controller [14]. At the same time, the presence of low-order harmonics contributes to distortions and an increase in THD of the output current, which is of particular importance in grid-connected power converters.

D. Means for Achieving Error-Free Sampling

The errors caused by delayed zero-crossing of the switching ripple can be reduced but not eliminated by delaying the sampling instants [15]. Delay of the voltage pulses is affected by the lockout time, but it also depends on delays in gate drivers and on the switching waveforms of semiconductor power switches, where the latter change with current and operating temperature. Therefore, delay of the sample instants by $t_{DT}/2$ can reduce, but it cannot eliminate the errors introduced by voltage-pulse delays. Delays introduced by the anti-aliasing LPF are predictable, and they do not change. Harmonic content of the switching ripple comprises several components, with the most emphasized residing next to $f_{\rm PWM}$ and $2f_{\rm PWM}$. Individual harmonic components have different time delays. Therefore, the zero-crossing of the filtered switching ripple changes with the harmonic content of the ripple. The latter changes with the modulation index, thus making the LPF delay compensation only partial.

Sampling errors in Tables I and II are caused by t_{DT} and LPF delays. For lower values of t_{DT} and $\tau_{\rm LPF}$, the errors remain close to 2%, the value which can be tolerated in some cases. The errors in Table III are obtained with shielded cable. Parasitic load capacitance brings in high-frequency oscillations and increases the errors up to 7%. Therefore, it is necessary to devise the feedback acquisition technique capable of an error-free operation in the presence of variable delays, LPF, and spurious oscillations. This need is more emphasized in cases with elevated winding capacitance, long cables, but also in high-performance drives where the bandwidth is high, closed-loop gains are large, and where the sampling errors cannot be tolerated.

Contemporary DSP controllers such as TMS320F28335 comprise a fast 12-bit, 16-channel ADC peripheral, which can be synchronized with the PWM pulse generator. It is possible to take one sample on each of 16 channels in a sequence much shorter than 4 μs. The results can be collected and stored automatically by means of a dedicated on-chip direct memory access (DMA) unit. These tools can be used to acquire $T_{\rm ADC}$-spaced samples of the output current and to calculate the feedback signal as an average value of the past $N_{\rm OV} = T_{\rm PWM}/T_{\rm ADC}$, covering the time span of $T_{\rm PWM}$. The process is illustrated in Fig. 5. The experimental setup of the Appendix runs with $T_{\rm PWM} = 128$ μs, $T_{\rm ADC} = 4\mu s$, and it takes $N_{\rm OV} = 32$ samples in each PWM period.

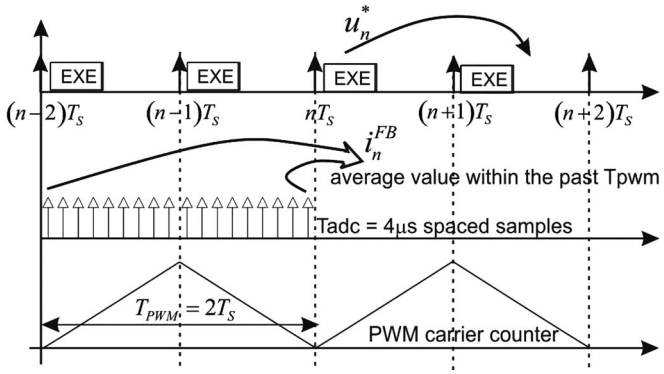

Fig. 5. Oversampling of the output current and derivation of the feedback signal i^{FB}. Execution of the control interrupts is denoted by EXE. In interrupt that executes after nT_{S}, the feedback signal i_n^{FB} is calculated as the average value within the interval $[(n-2)T_S \ldots nT_S]$.

In control interrupt triggered at nT_{S}, the feedback signal i_n^{FB} is calculated by summing the 32 equidistant samples acquired between $(n-2)T_{\mathrm{S}}$ and nT_{S} and dividing the sum by 32

$$i_n^{\mathrm{FB}} = \frac{1}{32}\sum_{k=0}^{31} i\left(nT_S - kT_{\mathrm{ADC}}\right) \tag{1}$$

where $i(nT_S - kT_{\mathrm{ADC}})$ is the sample of the analog input that represents the output current, taken by DMA-ADC machine at instant $t = nT_S - kT_{\mathrm{ADC}}$. To probe the effects of such a technique, it is of interest to represent the averaging formula by FIR filter, which runs with the sampling time of $T_{\mathrm{ADC}} = 4\ \mu$s. The transfer function of such a filter is

$$\frac{i^{\mathrm{FB}}(z)}{i(z)} = W_{\mathrm{FIR}}(z) = \frac{1}{32}\sum_{k=0}^{31} z^{-k}. \tag{2}$$

Calculated attenuation of the above filter at the switching frequency $f_{\mathrm{PWM}} = 1/(32 \cdot T_{\mathrm{ADC}})$ is infinite. The same attenuation is achieved for the integer multiples $n \cdot f_{\mathrm{PWM}}$. Hence, the feedback i^{FB} of (1) is unaffected by the switching ripple. It has to be noticed that spurious oscillations [19], caused by the switching transients, may affect one or two adjacent samples. In (1), these samples get divided by 32. Therefore, their impact is considerably smaller than in the case of conventional synchronous sampling, as shown by experimental evidence in Table III.

With oversampling technique, design of the anti-aliasing LPF is greatly simplified. The actual sampling process takes place at $N_{\mathrm{OV}} = 32$ times larger frequency. Hence, the practical Nyquist frequency is N_{OV} times larger. For the same alias-suppression results, the anti-aliasing LPF can be designed with a 32 times larger cutoff frequency. Namely, a passive *RC* filter has a 32 times lower $\tau_{\mathrm{LPF}} = RC$. Design choice of $\tau_{\mathrm{LPF}} \geq 5\ \mu$s is driven by other disturbances, related neither to the motor nor to the inverter.

Experimental verification of the feedback acquisition with one T_{PWM} averaging is summarized in Tables I–III and also in Figs. 2–4, where the resulting I_q errors are compared to errors obtained with conventional synchronous sampling.

Proposed feedback acquisition introduces delay into the control loop. It adds to the delay in applying the voltage reference. The value u_n^*, calculated in the interrupt triggered at nT_{S}, reloads into the PWM registers at instant $(n+1)T_S$ and affects the average value of the output voltage within the interval $[(n+1)T_S \ldots (n+2)T_S]$. In order to compensate delays and maintain the current loop performance, it is necessary to enhance the controller structure.

III. Enhanced Current Controller

This section addresses the structure, parameter setting, and closed-loop performance of state-of-the-art current controllers, considers the impact of the proposed feedback acquisition on the closed-loop bandwidth and the robustness of the controller, and eventually introduces enhancement of the controller structure and parameter setting, designed to help using the benefits of error-free sampling while maintaining the current control performances.

A. State-of-the-Art Current Controllers

Most widely used are the PI current controllers in synchronous frame [5]–[11], [14]. The feedback acquisition is mostly based on synchronous sampling (see Fig. 1) with $f_S = 2f_{\mathrm{PWM}}$, as explained in [3], [8], and [12].

Analysis and design of current controllers are simplified by introducing complex vectors [5], [6], [10], where the stator current in stationary frame is represented by $i^s = i_{\alpha s} + j i_{\beta s}$, while the current in the synchronous *d–q* frame is $i^e = i_d + j i_q$. Modeling should include the computation delays, as well as modulation delays and feedback acquisition delays [1], [12]. An accurate model of the current controller is given in [8]. It includes unambiguous model of all the delays and coordinate transforms, and it does not rely on Tustin approximation. Developments described further on rely on [8] and make use of the same nomenclature.

In Fig. 5, the voltage reference calculated in an interrupt gets applied in the successive sampling period. Hence, the reference u_{n-1}^*, calculated in interrupt $(n-1)T_{\mathrm{S}}$ gets applied in interval $[nT_S \ldots (n+1)T_S]$. Assuming that the e_n^s stands for the average value of the electromotive force over the same interval, the difference equation expressing the change of the stator current is

$$i_{n+1}^s = i_n^s e^{-\beta} + \frac{1-e^{-\beta}}{R}\left(u_{n-1}^s - e_n^s\right) \tag{3}$$

where $\beta = RT_S/L$, while R and L are the resistance and inductance of the windings. Complex vectors in stationary and synchronous frames are related by

$$\begin{aligned} i_{n+1}^s &= i_{n+1}^e \cdot e^{\mathrm{j}\theta_{n+1}}, \quad i_n^s = i_n^e \cdot e^{\mathrm{j}\theta_n}, \\ u_{n-1}^s &= u_{n-1}^e \cdot e^{\mathrm{j}\theta_{n-1}} \end{aligned} \tag{4}$$

where θ_n represents the position of the *d–q* frame at instant nT_{S}. Assuming that the speed $\omega_e = \mathrm{d}\theta/\mathrm{d}t$ does not exhibit a meaningful change in T_{S}, the advance of the *d–q* frame is $\theta_{n+1} = \theta_n + \omega_e T_S, \theta_n = \theta_{n-1} + \omega_e T_S$, while the average

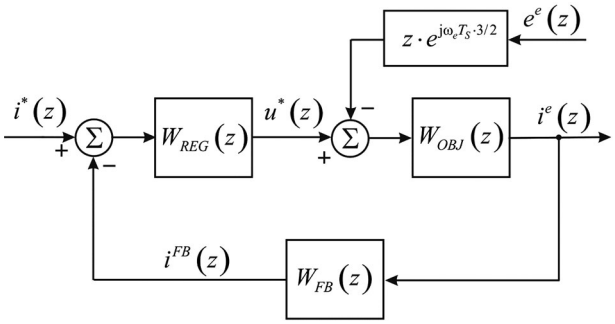

Fig. 6. Block diagram of generic current controller in synchronous *d–q* frame. With conventional synchronous sampling, $W_{\mathrm{FB}}(z) = 1$.

value of the electromotive force becomes

$$e_n^e = \frac{1}{T}\int_{nT_S}^{(n+1)T_S} e^e(t)\cdot dt \approx e_n^s \cdot e^{-j(\theta_{n+1}+\theta_n)/2}. \quad (5)$$

The difference equation is obtained by introducing the results of (4) and (5) into (3), dividing the resulting expression by $e^{j\theta n}$ and introducing $(1-e^{-\beta})/R \approx T_S/L$

$$\begin{aligned} i_{n+1}^e e^{j\omega_e T_S} &= i_n^e e^{-\beta} \\ &+\frac{T_S}{L}\left(u_{n-1}^e \cdot e^{-j\omega_e T_S} - e_n^e \cdot e^{j\omega_e T_S/2}\right). \end{aligned} \quad (6)$$

The transfer function of the plant is obtained by dividing the complex images $i^e(z)$ and $u^e(z)$, obtained in conditions where the disturbance $e^e(z)$ is equal to zero. From (6)

$$W_{\mathrm{OBJ}}(z) = \left.\frac{i^e(z)}{u^e(z)}\right|_{e^e=0} = \frac{T_S}{L}\frac{1}{z\cdot e^{j\omega_e T_S}\left(z\cdot e^{j\omega_e T_S} - e^{-\beta}\right)}. \quad (7)$$

In the presence of both $u^e(z)$ and $e^e(z)$, the output current is obtained from (3), (6), and (7)

$$i^e(z) = W_{\mathrm{OBJ}}(z)\cdot u^e(z) - z\cdot e^{j\omega_e T_S\cdot 3/2} W_{\mathrm{OBJ}}(z)\cdot e^e(z). \quad (8)$$

The closed-loop current controller is given in Fig. 6. State-of-the-art current controllers use conventional synchronous sampling with unity gain and no delays in the feedback path ($W_{\mathrm{FB}} = 1$). In IMC-based design, $W_{\mathrm{REG}}(z)$ comprises inverted dynamics of $W_{\mathrm{OBJ}}(z)$, and it is obtained by applying the method of [7] and [8] on $W_{\mathrm{OBJ}}(z)$ of (7)

$$\begin{aligned} W_{\mathrm{REGX}}(z) &= \frac{\alpha z}{z-1}\cdot W_{\mathrm{OBJ}}^{-1} \\ &= \frac{\alpha L}{T_S}\frac{z^2\cdot e^{j\omega_e T_S}\left(z\cdot e^{j\omega_e T_S} - e^{-\beta}\right)}{z-1} \end{aligned}$$

where α is the gain. Compared with *s*-domain implementation in [7], where $k_p = kL$ and $k_i = kR$, the gain α corresponds to kT_{S}.

The function $W_{\mathrm{REGX}}(z)$ implies prediction, which cannot be implemented. Therefore, the practical controller becomes

$$W_{\mathrm{REG}}(z) = \frac{\alpha L}{T_S}\frac{e^{j\omega_e T_S}\left(z\cdot e^{j\omega_e T_S} - e^{-\beta}\right)}{z-1} \quad (9)$$

TABLE IV
CLOSED-LOOP PERFORMANCE OF STATE-OF-THE-ART CONTROLLERS

Gain α	Settling time (1%)	$f_{\mathrm{BW}}(-45°)$	$f_{\mathrm{BW}}(-3\,\mathrm{dB})$	VM	Overshoot
0.300	9 T_{S}	0.0374 f_{S}	0.1034 f_{S}	0.679	0.0120
0.287	9 T_{S}	0.0362 f_{S}	0.0954 f_{S}	0.667	0.0053
0.277	9 T_{S}	0.0350 f_{S}	0.0894 f_{S}	0.655	0.0020

which leads to the open loop gain of

$$W_{\mathrm{PP}}(z) = W_{\mathrm{REG}}(z)\,W_{\mathrm{OBJ}}(z) = \frac{\alpha}{z(z-1)} \quad (10)$$

and to the closed-loop transfer function

$$W_{\mathrm{SS}}(z) = \left.\frac{i^e(z)}{i^*(z)}\right|_{e^e=0} = \frac{W_{\mathrm{PP}}(z)}{1+W_{\mathrm{PP}}(z)} = \frac{\alpha}{z^2-z+\alpha}. \quad (11)$$

The closed-loop performances obtained with $W_{\mathrm{SS}}(z)$ of (11) are obtained analytically and given in Table IV. Considered are the step-response overshoot, the frequency $f_{\mathrm{BW}}(-45°)$ where the phase of W_{SS} drops to −45°, the frequency $f_{\mathrm{BW}}(-3\,\mathrm{dB})$ where the amplitude of W_{SS} drops to –3 dB and the settling time. The vector margin (VM) as calculated as an indicator of robustness against the changes in a system parameter. According to results in Table IV, the closed-loop bandwidth of $f_{\mathrm{BW}}(-3\,\mathrm{dB}) = 0.1\cdot f_S$ can be achieved with a very small overshoot and with the vector margin of VM = 0.67.

B. Delays Introduced by the Feedback Averaging

Error-free feedback acquisition of (1) is based on feedback oversampling with a period of $T_{\mathrm{ADC}} = T_{\mathrm{PWM}}/N_{\mathrm{OV}}$ and then taking the average of N_{OV} samples, acquired within the past period T_{PWM}. The value i^{FB} at instant nT_{S} (see Fig. 5) represents the average of the current over the interval $[(n-2)T_S \ldots nT_S]$. It can be expressed in terms of the current samples i_{n-2}, i_{n-1} and i_{n} as $i_n^{\mathrm{FB}} = (i_n + 2i_{n-1} + i_{n-2})/4$. The transfer function in the feedback path becomes

$$W_{\mathrm{FB}}(z) = \frac{i^{\mathrm{FB}}(z)}{i(z)} = \frac{z^2+2\cdot z+1}{z^2}. \quad (12)$$

Delays introduced by W_{FB} into the feedback path affect the closed-loop transfer function W_{SS}. Assuming that the system is controlled using the same controller W_{REG} (9), the closed-loop transfer function W_{SS} is obtained from the diagram in Fig. 6

$$\begin{aligned} W_{\mathrm{SS}}(z) &= \frac{W_{\mathrm{REG}}(z)\cdot W_{\mathrm{OBJ}}(z)}{1+W_{\mathrm{REG}}(z)\cdot W_{\mathrm{OBJ}}(z)\cdot W_{\mathrm{FB}}(z)} \\ &= \frac{4\alpha z^2}{4z^4-4z^3+\alpha z^2+2\alpha z+\alpha}. \end{aligned} \quad (13)$$

Due to delays introduced by W_{FB}, the gain $\alpha = 0.3$ introduces an overshoot of 25% and reduces the vector margin down to 0.5 (see Table V). In order to maintain the overshoot and the vector margin at the previous levels, it is necessary to reduce the feedback gain. Table V presents the summary of analytical considerations. For the same VM and the same overshoot, it proves

TABLE V
CLOSED-LOOP PERFORMANCE WITH PROPOSED AVERAGING AND NO D-ACTION

Gain α	Settling time (1%)	$f_{\mathrm{BW}}(-45^\circ)$	$f_{\mathrm{BW}}(-3\,\mathrm{dB})$	VM	Overshoot
0.300	9 T_S	0.042 f_S	0.1110 f_S	0.507	0.251
0.182	9 T_S	0.0274 f_S	0.0608 f_S	0.695	0.0198
0.170	9 T_S	0.0258 f_S	0.0545 f_S	0.714	0.0077
0.164	9 T_S	0.0246 f_S	0.0509 f_S	0.724	0.0038

necessary to reduce the gain down to 60%, with roughly proportional reduction of the closed-loop bandwidth $f_{\mathrm{BW}}(-3\,\mathrm{dB})$. Hence, the feedback delay introduced by the proposed feedback averaging produces a considerable reduction of the closed-loop performances.

C. Enhanced Controller

Delays in feedback acquisition can be compensated by changing the transfer function of the current controller. Current control law W_{REG} in (9) is designed to cancel the undesired dynamics of the plant (W_{OBJ}). Therefore, it comprises inverted dynamics of $W_{\mathrm{OBJ}}(z)$. In order to maintain the proper cancelation of the plant dynamics, the control law should be changed by introducing a multiplicative factor

$$W_{\mathrm{REG}}^{\mathrm{NEW}}(z) = W_{\mathrm{REG}}^{\mathrm{OLD}}(z) \cdot W_{\mathrm{MUL}}(z). \tag{14}$$

In order to improve the phase and compensate time delays, the factor W_{MUL} has to be of differential nature, with

$$W_{\mathrm{MUL}}(z) = 1 + d\frac{z-1}{z} \tag{15}$$

where d is adjustable parameter, the current controller is enhanced with differential action, and it has the transfer function W_{REGD}

$$\begin{aligned} W_{\mathrm{REGD}}(z) &= \frac{\alpha L}{T_S}\frac{z+d(z-1)}{z}\left(\frac{e^{j\omega_e T_S}\left(z\cdot e^{j\omega_e T_S}-e^{-\beta}\right)}{z-1}\right) \\ &= \frac{\alpha L}{T_S}e^{j\omega_e T_S}\frac{[(d+1)z-d]\left(z\cdot e^{j\omega_e T_S}-e^{-\beta}\right)}{z(z-1)}. \end{aligned} \tag{16}$$

Considering the block diagram of the current controller in Fig. 6, the closed-loop transfer function obtained with the proposed feedback averaging and the enhanced current controller of (16) is eqn. (17), at the bottom of the page.

The closed-loop performance of W_{SS} in (17) depends on two parameters, α and d. It is necessary to obtain the pair of parameters (α, d), which improves the performance features of Table V, and brings them to those of Table IV, obtained without the proposed feedback averaging. Two-dimensional (α, d) plane is searched, using the following criteria.

TABLE VI
PERFORMANCE WITH FEEDBACK AVERAGING AND W_{REGD} CONTROLLER

Gain α	Gain d	Settling time (1%)	$f_{\mathrm{BW}}(-45^\circ)$	$f_{\mathrm{BW}}(-3\,\mathrm{dB})$	VM	Overshoot
0.2238	0.555	8 T_S	0.0366 f_S	0.0895 f_S	0.643	0.0047
0.2283	0.641	9 T_S	0.0378 f_S	0.0963 f_S	0.637	0.0000
0.2373	0.638	9 T_S	0.0394 f_S	0.1042 f_S	0.624	0.0100

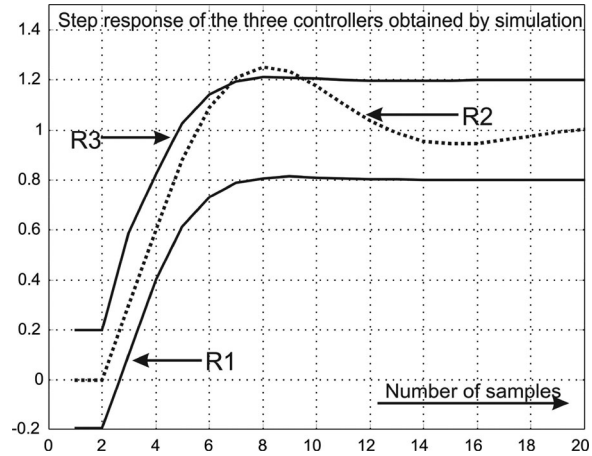

Fig. 7. Step response obtained with the current controller of [8], with conventional synchronous sampling and with $f_{\mathrm{BW}} = 0.1 \cdot f_S$ is denoted by R1. Response obtained from (13), with feedback averaging but with no controller enhancement is denoted by R2. Response obtained with feedback averaging and with enhanced controller is denoted by R3. Response R1 is shifted vertically by 0.4 downward, to enable a better comparison.

1) Limit values: VM > 0.6, Overshoot $< 1\%$.
2) Fixed targets: VM $= 0.65$, Overshoot $= 0\%$.
3) Variable target: $f_{\mathrm{BW}}(-3\,dB) = [0.08 \cdot f_S \ldots 0.12 \cdot f_S]$.

In Table VI, performance parameters are given for the three characteristic parameter sets. The values demonstrate that VM, f_{BW}, settling time, and overshoot features obtained with the proposed feedback averaging and an enhanced controller correspond to performances of the state-of-the-art controllers, listed in Table IV. The values of α and d in Table VI are relative, and they do not depend on the motor or the grid parameters.

Simulated step responses of the three current controllers are given in Fig. 7. The controller proposed in [8] is tuned for $f_{\mathrm{BW}}(-3\,\mathrm{dB}) = 0.1 \cdot f_S$. Corresponding step response is denoted by R1. Using the same gain setting, the proposed averaging technique is introduced into the feedback path, while keeping the same controller of [8]. The relevant trace in Fig. 7 is R2. Eventually, the step response R3 is obtained with the feedback averaging and the enhanced controller, using the gain setting which results in $f_{\mathrm{BW}}(-3\,\mathrm{dB}) = 0.1 \cdot f_S$. The traces in Fig. 7 show that the feedback averaging introduces delays and deteriorates the step response. They also prove that the extended controller W_{REGD} of (16) restores the closed-loop performance,

$$W_{\mathrm{SS}}(z) = \frac{W_{\mathrm{REGD}}(z)\cdot W_{\mathrm{OBJ}}(z)}{1 + W_{\mathrm{REGD}}(z)\cdot W_{\mathrm{OBJ}}(z)\cdot W_{\mathrm{FB}}(z)} = \frac{4\alpha(1+d)z^3 - 4\alpha d z^2}{4z^5 - 4z^4 + \alpha(1+d)z^3 + \alpha(2+d)z^2 + \alpha(1-d)z - \alpha d}. \tag{17}$$

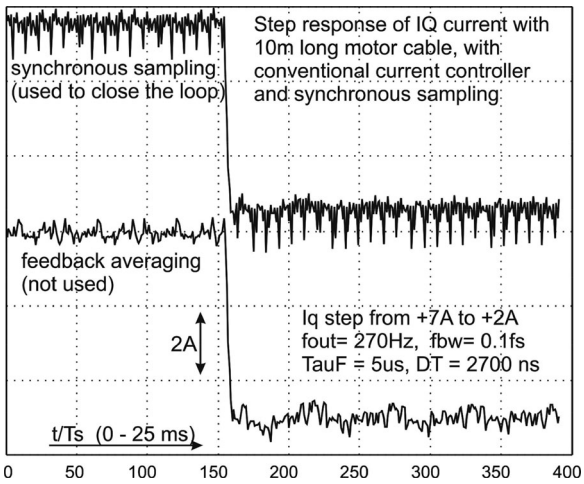

Fig. 8. Step response obtained with state-of-the-art controller, synchronous sampling, $\alpha = 0.3$, and with $l =$ 10-m-long motor cable. The upper trace is obtained by synchronous sampling and used to close the loop. Elevated noise is due to the sampling errors being amplified by the loop gains. The lower trace is obtained by averaging (1)–(2), and it is not used to close the feedback.

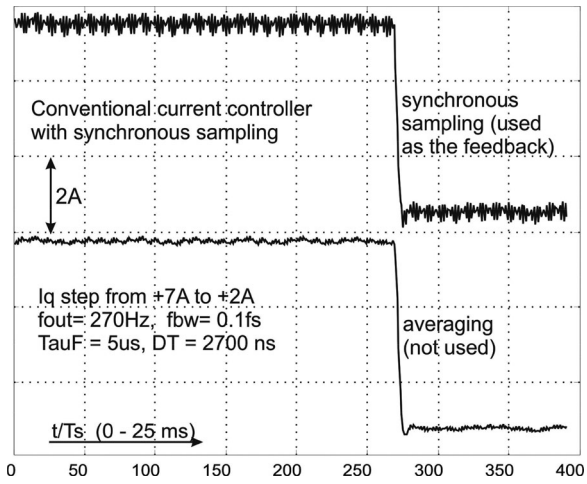

Fig. 9. Step response obtained with state-of-the-art controller, synchronous sampling and $\alpha = 0.3$. Lower sampling errors are obtained by reducing $t_{\rm DT}$ and $\tau_{\rm LPF}$ and using short leads instead of shielded motor cable. The upper trace is obtained by synchronous sampling and is used to close the loop. The lower trace is obtained by averaging [(1)–(2), $W_{\rm FB}$]. It is not used as the feedback.

providing the step response which is very close to the one obtained with state-of-the-art controller [8] and with conventional sampling.

IV. Experimental Tests With Enhanced Controller

Experimental study of the sampling errors is given in Section II, Tables I–III, and Figs. 2–4. The proposed feedback acquisition technique (1)–(2) removes the errors and introduces the transfer function $W_{\rm FB}$ (12) into the feedback path. In order to maintain the closed-loop performance, the current controller has to be extended as shown in (16). The subsequent experimental tests are performed in order to explore the capability of the enhanced controller to maintain the closed-loop performance in the presence of feedback averaging (1)–(2).

With conventional current controller and synchronous sampling, the step response obtained with a 10-m-long motor cable is shown in Fig. 8. In Figs. 8–11, the two traces are logged simultaneously, during the same run. The upper traces are obtained with conventional synchronous sampling, while the lower traces are obtained from (1) to (2), by the proposed feedback averaging. In Fig. 8, the upper trace is used as the feedback signal. Increased errors are due to interaction of the sampling errors and relatively high loop gains.

For the proper comparison of dynamic performance of the conventional and the proposed current controller, it is convenient to perform the tests in low-noise conditions. Therefore, the step response test of the conventional controller [8] is repeated with no motor cable and with reduced t_{DT} and $\tau_{\rm LPF}$. The results are given in Fig. 9, demonstrating the closed-loop bandwidth of $f_{\rm BW} = 0.1 f_S$ with a very low overshoot.

The sampling errors are reduced by introducing the described feedback averaging (1)–(2), modeled by $W_{\rm FB}$ in (12). It provides a considerable reduction of the noise content in the feedback signals (see Figs. 2–4, Tables I–III). It also introduces delay into the loop (see Fig. 6). The step response obtained with a conven-

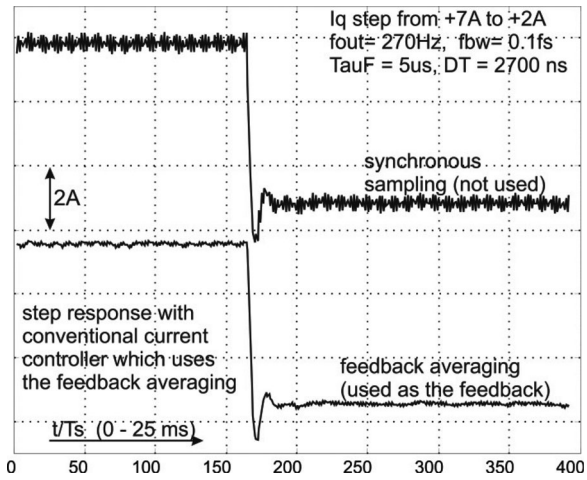

Fig. 10. Step response obtained with conventional current controller and with the feedback averaging of (1)–(2). The upper trace is obtained by synchronous sampling and it is not used as the feedback. The lower trace is obtained by averaging [(1)–(2), $W_{\rm FB}$], and it is used as the feedback signal.

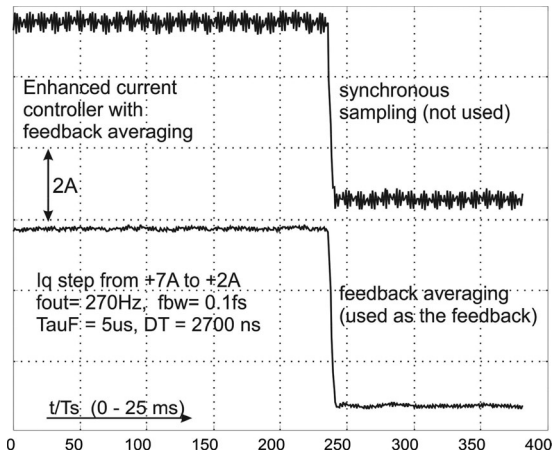

Fig. 11. Step response obtained with the feedback averaging and with enhanced current controller. The lower, averaged trace is used as the feedback signal, while the upper, synchronous-sampled trace is given for the reference.

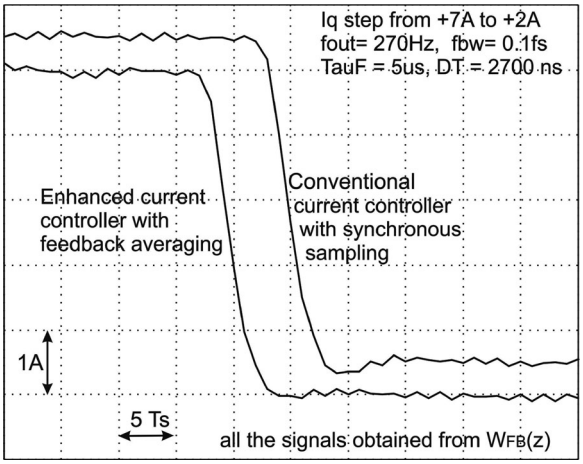

Fig. 12. Comparison of the step response features of the conventional current controller which uses the synchronous sampling (upper trace) and the enhanced current controller with the feedback averaging (lower trace). Both traces are obtained in the same way, by the averaging proposed in (1)–(2). The waveforms are intentionally shifted to facilitate comparison.

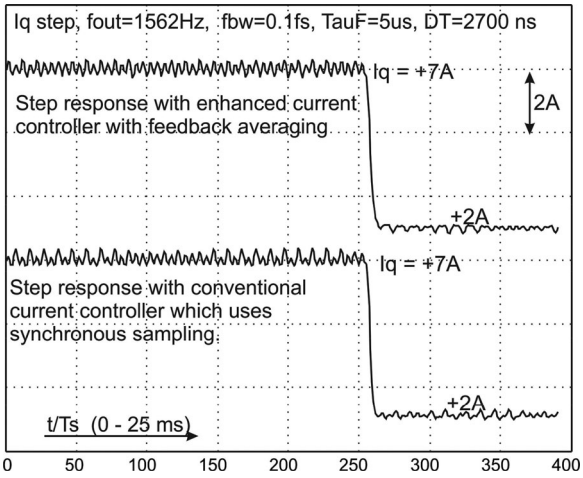

Fig. 13. Comparison of the step responses obtained with a high output frequency of 1562 Hz (that is, 0.1 f_S). For the purposes of comparison, both traces are obtained in the same way, by the averaging proposed in (1)–(2).

tional controller [8], which uses the feedback averaging (1)–(2), is given in Fig. 10. The role of the two shown signals, with regard to the use in the control, is now reversed when compared to the results in Figs. 8–9. Feedback acquisition delays produce a relatively large overshoot, which corresponds to simulation results given in Fig. 7.

Enhanced controller W_{REGD} of (16) has a multiplicative factor of differential nature. The values of design parameter *d*, which can restore dynamic performances are listed in Table VI. The step response obtained with an enhanced current controller that uses the feedback averaging are given in Fig. 11. Corresponding gains α and *d* are set to achieve $f_{\mathrm{BW}} = 0.1 f_S$. The waveforms of Fig. 11 are very similar to those in Fig. 9, proving the capability of the enhanced controller to use the error-free feedback acquisition of (1)–(2) and yet to obtain the same level of the closed-loop performances as the state-of-the-art controllers, based on synchronous sampling. In Fig. 12, the

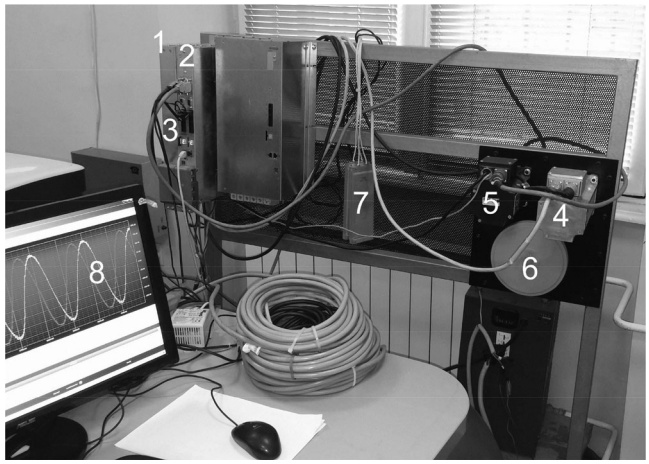

Fig. 14. Experimental setup with six-pole synchronous permanent-magnet motor. (1) Main power supply unit providing $E_{\mathrm{DC}} = 520$ V. (2) Two-axis module comprising two 3-phase inverters and control circuits. (3) SD-card slot used for data logging. (4) The motor under the test. (5) Speed-controlled motor. (6) Inertia coupled by a toothed belt with the two motors. (7) Dynamic braking resistors. (8) PC-based GUI connected over the EtherCat link.

step responses obtained with the two controllers are zoomed in and aligned for the ease of comparison.

An important feature of the current controller is the capability to maintain the response quality even with very large output frequencies. The current controller of [8] shows an excellent performance even with $f_{\mathrm{OUT}} = 0.083 f_S$. In order to verify the proposed controller, it is compared to the former in Fig. 13, where the two step responses are compared at the output frequency of $f_{\mathrm{OUT}} = 0.1 f_S$. The experiment is carried out by using three inductances as the load. The basic features of the two responses are similar, proving the possibility to obtain an error-free feedback acquisition, while maintaining at the same time a superior dynamic performance.

V. Conclusion

In this paper, we consider the errors encountered in the feedback path of state-of-the-art digital ac current controllers. Most recent solutions use synchronous sampling, wherein a single sample of the current is taken at the center of the voltage pulses. Experimental investigation reported in the paper includes the impact of the lockout time and the effects of delays introduced by anti-aliasing filters. We also considered the sampling errors introduced by parasitic oscillations. These oscillations are created in an interaction of fast switching transients and parasitic *LC* elements of the motor cables and/or the winding capacitance. The sampling errors from 2% up to 7% introduce considerable disturbance and they limit the feedback gains and performances of the current controller.

In order to suppress the errors in the feedback path, we developed a feedback acquisition technique. In each half of the PWM cycle, an average value of the feedback is calculated within the past PWM cycle. The process is aided by automated DMA-driven ADC sequences of contemporary DSP controllers. The method removes all the sampling errors caused by the lock-out time, and anti-aliasing filter delays, and it features an infinite

attenuation of the switching ripple. It also reduces the errors introduced by parasitic *LC* oscillations. In cases where the motor cables increase the errors by 5% with conventional synchronous sampling, the errors are increased by only 0.2% with the proposed feedback averaging.

The feedback averaging introduces delays, overshoots and deteriorates the closed-loop response. In order to maintain dynamic performances, the current controller is enhanced by proposing a series compensator and the parameter setting that are focused on maintaining the same dynamic performances and robustness as the state-of-the-art solutions. Proposed control solutions are verified by simulations and experimental runs performed on DSP-controlled setup with synchronous permanent magnet motor and IGBT inverter.

APPENDIX

The experimental setup is shown in Fig. 14. Rotor-flux-oriented control is used at all times.

Synchronous Motor with Surface-Mounted Magnets	
Stack length	$L = 128$ mm
Number of poles	$2p = 6$
Rated torque	$T_{\mathrm{nom}} = 6$ Nm
Rated current	$I_{\mathrm{nom}} = 7.3$ Arms
Torque constant	$k_t = 0.821$ N·m/$\mathrm{A_{rms}}$
Back-EMF constant	$k_e = 0.687$ $\mathrm{V_{peak}}$/(rad/s)
Stator resistance	$R_S = 0.47\ \Omega$
Stator inductance	$L_S = (L_d + L_q)/2 = 3.4$ mH
PWM inverter	
DC-bus voltage	$E_{\mathrm{DC}} = 520$ V dc
PWM frequency	$f_{\mathrm{PWM}} = 1/T_{\mathrm{PWM}} = 7.812$ kHz
Rated lockout time	$t_{DT} = 3\ \mu$s
Peak current	$I_{\mathrm{max}} = 45$ A
Digital control platform	
DSP controller	TMS320F28335
ADC resolution	$N_{\mathrm{ADC}} = 12 - \mathrm{bit}$
Anti-aliasing LPF	$\tau_{\mathrm{LPF}} \geq 5\ \mu$s
Oversampling period	$T_{\mathrm{ADC}} = 4\ \mu$s
Oversampling handle	embedded DMA machine
No. of samples per period	$N_{\mathrm{OV}} = T_{\mathrm{PWM}}/T_{\mathrm{ADC}} = 32$
PWM method	Symmetrical PWM

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