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NBTI-Generated Defects in Nanoscaled Devices: Fast Characterization Methodology and Modeling

NBTI-generated defects in nano-scaled devices: fast characterizaton methodology and modelling

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***Abstract*— NBTI-generated Defects (GD) have been widely observed and known to play an important role in device's lifetime. However, its characterization and modelling in nano-scaled devices is a challenge due to their stochastic nature. The objective of this work is to develop a fast and accurate technique for characterizing the statistical properties of NBTI aging, which can be completed in one day and thus reduce test time significantly. The fast speed comes from replacing the conventional Constant Voltage Stress (CVS) by the Voltage Step Stress (VSS), while the accuracy comes from capturing the Generated Defects (GD) without recovery. The key advances are two-fold: First, we demonstrate that this VSS-GD technique is applicable for nano-scaled devices; Second, we verify the accuracy of the statistical model based on the parameters extracted from this technique against independently measured data. The proposed method provides an effective solution for GD evaluation, as required when qualifying a CMOS process.**

Keywords: Negative bias tempeture instabilty; Variabilty; defect generation; hole trapping;

I. INTRODUCTION

As the CMOS nodes scale down to nano-meter regime, time-dependent variations induced by negative bias temperature instability (NBTI) has become a big concern for circuit design [1-5]. These nano-scaled devices are dominated by only a handful of defects, which are usually categorized into the recoverable and permanent components [6]. However, such classification is very sensitive to the measurement conditions and cannot reflect the nature of the defects [7]. Recent work revealed that there exist two different types of defects, the as-grown hole traps (AHTs) and generated defects (GDs), which exhibit different energy distributions and temporal kinetics [8]. AHTs and a small portion of GDs can be ascribed to the recoverable components, while most of GDs belong to the permanent component [7]. AHT has received many attentions recently: RTN [9] and TDDS [10] techniques are widely used to understand their properties, based on which the defect-centric distribution [2] was proposed for modelling.

Manuscript received MMM DDD, 2017. The review of this paper was arranged by Editor ???. This work was supported by the Newton Research Collaboration program of The Royal Academy of Engineering under the grant no. NRCP1516/4/77 and Engineering and Physical Science Research Council of UK under the grant no. EP/L010607/1.

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However, there is less research on the GD component [6,11,12]. The GD follows an empirical power law against both stress time and gate [13],

$$GD = g_0 \cdot V_{gov}^{m} \cdot t^{n} \qquad (1)$$

Wherein, the overdrive voltage, Vgov is defined as Vg-Vth. To accelerate NBTI stresses, Vgov is raised above its normal operation level. Accelerated test under constant voltage stress (CVS) scheme is normally applied with typical total testing time of a few days [14]. This is tolerable for big devices, where device-to-device variation (DDV) is negligible. However, scaled device requires repetitive tests to retrieve statistical properties of DDV and the task becomes laborious. The voltage ramp stress (VRS) methodology was introduced to yield meaningful reliability data in short time [15,16]. VRS is an efficient screening tool for comparing different processes, but its accuracy is less satisfactory: **Fig. 1** shows there can be large differences between ΔVth measured by CVS tests and that predicted by the model extracted from VRS tests.

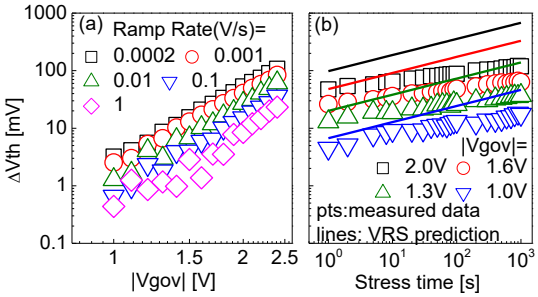

Fig. 1 (a) Typical result from the VRS test, the voltage step (ΔV) was set to 100 mV, and the stress duration (Δt) varied from 500 s to 0.1s, providing ramp rates from 0.0002 to 1 V/s, all with a sense delay of 1ms. **(b)** A comparison between the VRS prediction and the measurements from CVS test. Both VRS and CVS measurements are performed on multiple devices on the process described in section II.

The objective of this work is to develop a technique that is not only fast, but also accurate, for characterizing the stochastic GDs and to verify the accuracy of the model based on it. This technique combines the two methods proposed by us recently for large devices: One of them captures GDs in their entirety, so that the extracted n becomes independent of measurement conditions [17]; The other uses a voltage-step-stress (VSS) for extracting the voltage exponent, m, rapidly [18]. Unlike the VRS that changes device for each voltage ramp, VSS uses the same device for all voltage steps. In section III, we will develop the technique and verify its prediction capability against test data for large devices. In

section IV, for the first time, this technique is applied to characterize the statistical properties of GDs, use them for statistical modelling, and verify its accuracy against experimental data. Section IV concludes this paper.

II. Devices and Experiments

The pFETs with TiN gate are used in this work. The gate dielectric stack is HfO_2 with Al_2O_3 capping layer and the equivalent oxide thickness is 1.45nm. Devices with channel length/width of 1µm/1µm and 0.07µm/0.09µm are used in this work. The pulse measurement is used to monitor the full Id~Vg within 3µs [19]. For variability tests, the proposed method is repeated on multiple samples and Id~Vg measurements are repeated for 100 times to capture its Within-Device-Fluctuation that will be elaborated in section IV. Vth was measured as the Vg shift at a constant Id= 0.5µA. The testing temperature is 125°C unless otherwise specified.

III. Voltage Stepping Stress (VSS) technique For GD characterization

A. GD determination

The time exponent, n in eq. (1), extracted by the conventional CVS depends on the delay between stress and measurement. Our recent work reveals that this is due to the discharging of some GD within the Si bandgap [17]. By adding a recharge stage after discharging as shown in **Fig.2a**, the discharged GD can be refilled, so that all the GD can be captured without recovery. This makes the extracted n independent of the stress and measurement conditions. The details and results can be found in ref. 15.

B. Voltage Step Stress (VSS) technique and validation

GD under any overdrive voltage, Vgov, can be predicted if the parameters, g0, m and n in Eqn (1), are accurately determined. n can be obtained by performing a single short CVS test under constant Vgov [17]. To determine g0 and m, the conventional methods apply several Vgov [13], while VRS applies several different ramp rates [15]. Both require device-change for each Vgov or ramp rate. The voltage step stress (VSS) technique, on the other hand, uses a sequence of Vgov steps, does not need device-change [18], and will be adopted here.

The Vgov waveform used by VSS is given in **Fig. 2b**: Vg_ov starts from a value close to operating condition (i.e. -0.3V) and then gradually increases with a small step (20mV in our test). Each step is applied for a pre-defined time, Δt (10s here). At the end of each step, GDs are monitored by the procedure in **Fig. 2a**. In this way, we combine the GD measurement method described in section III.A [17] with the VSS method [18] and the combined technique will be referred to as VSS-GD technique.

Under a given Vgov, GD are generated and the AHTs below the *fermi-level* corresponding to this Vgov will be charged. By applying positive Vgdisch, all the AHT and some GD within the bandgap will be discharged. What is worth noting is that although AHTs are difficult to be fully discharged under 0V, this can be achieved when applying a positive Vgdisch. The intended normal operation voltage for a process, Vgch (-1.2V here) is then applied to re-charge the discharged GD, so that they can be captured in their entirely.

A typical result is shown in **Fig.3**. Under low Vgov, there is a flat plateau. This is because the generation is negligible in 10sec when Vgov is low. The ΔVth in this plateau actually comes from the AHTs corresponding to the charging Vgch. Since AHTs are 'as-grown', they will not increase with stress and remain the same, so long the same Vgch is applied. This explains the plateau for low Vgov in **Fig. 3**.

As Vg_ov increases, GD becomes higher, resulting in the rise in **Fig.3**. By subtracting AHT in the plateau from the total ('◊'), GD under different Vg_ov can be obtained ('□'). According to the VSS method based on Eqn (2) [18], to generate the same amount of GD, a stress under a Vgov for a time Δt is equivalent to a stress under another overdrive voltage Vgeff for the effective stress time of Δteff:

$$\Delta t_{eff} = \left(\frac{V_{gov}}{V_{geff}}\right)^{m/n} \cdot \Delta t \qquad (2)$$

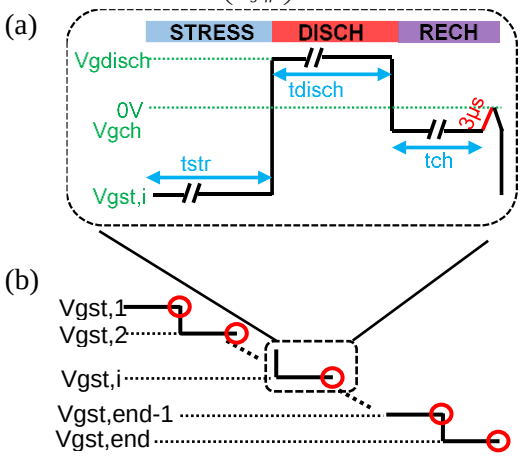

Fig. 2 (a) The test procedure under each voltage step. A stress-discharge-recharge sequence is used. At the end of recharge step, ΔVth was monitored from a corresponding Id~Vg, which was taken from the 3µs pulse edge with Vd = -0.1V applied. tdisch and tch has negligible impact on GD extraction [17]. In this work, tdisch=tch=10s is used. **(b)** The Vg waveform for the fast VSS technique.

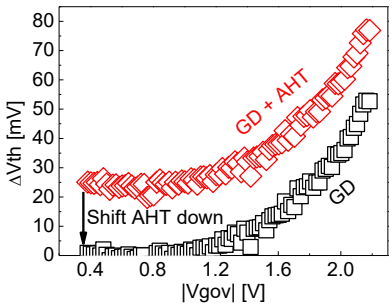

Fig. 3 Fast-VSS measurement with overdrive Vgov gradually increasing under 125 °C. Each volage lasts 10s and the voltage step of 20mV is used. The total degradation includes both AHT and GD. AHT can be determined under low stress condition where GD is neglible. By subtracting AHT from the total, GD can be extracted.

With the time exponent, n, predetermined from CVS method (0.2 for this process) [17], Δt for each step in the VSS test can be converted to Δteff under any given m value using

Eqn (2). To minimize the measurement inaccuracy, GD over 5mV is used for the analysis. **Fig.4a** shows that GD~Δt ('□') is transformed to GD~Δteff kinetics under three different m. With the larger m value, the device takes longer to reach the same degradation, leading to smaller apparent time exponent, n'. Only when m is correctly determined, the n' from the transformed kinetics equals to the predetermined n. The corresponding parameter g_0 can then be determined simultaneously, as shown in **Fig.4b**.

C. *Validation of the VSS-GD method*

To validate the VSS-GD method, the extracted parameters are used to predict the GD under various constant Vgov. In **Fig. 5**, GDs were measured under constant Vgov and these data were not used to fit the n, m and g0. Good agreement has been achieved even when Vgov is as low as -0.9 V, validating the proposed VSS-GD method.

When extracting the parameters in the power law, VRS uses the total degradation, i.e. the sum of AHTs and GDs. AHTs saturate quickly and do not follow the power law. This is the reason for the inaccuracy of VRS. The VSS-GD method can reliably remove AHTs and only fit the GDs with the power law. This delivers the accuracy.

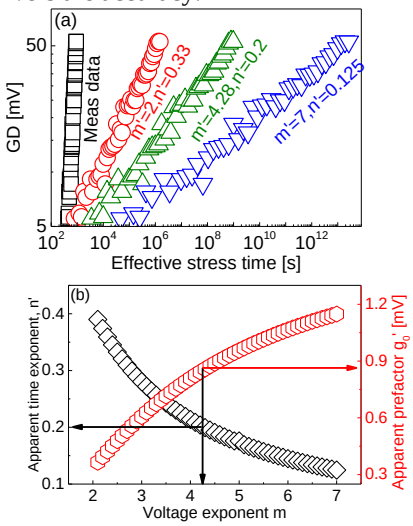

Fig. 4 (a) The measured degradation is plotted against time ('□'). By assuming different m', the real stress time under each stepping voltage can be transformed to effective stress time under a certain constant Vgeff (1V used). **(b)** The extracted n' and g0' under given m'. The correct m and g0 corresponds to n=0.2.

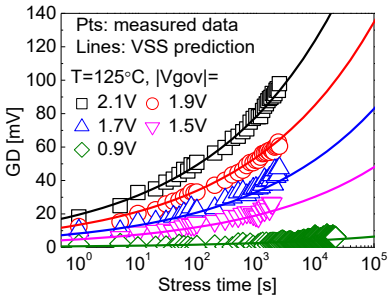

Fig. 5 Validation of the extacted model parameters using fast-VSS technique under different overdrive voltages ranging from low to high under 125 ºC. A good agreement is achieved.

IV. GENERATED DEFECTS IN NANO-SCALED DEVICES

Defects in nano-scaled devices can induce two types of stochastic variations: Device-to-Device Variation (DDV) [20-22] and Within-Device-Fluctuation (WDF) [6,23,24].

A. *Within-Device-Fluctuation (WDF) of GDs*

The same procedure in **Fig.2** is applied on a nano-scaled pFET with the channel length and width of 70nm and 90nm. WDF is caused by random charging and discharging within the same device. In order to capture it, after the discharge and recharge is applied at each voltage step, Id~Vg curves were measured 100 times with the interval of 30ms. The distribution of ΔVth measured from these Id~Vg is shown in **Fig. 6a**. The average value increases after higher Vgov stress, but the shift is broadly in parallel. **Fig. 6b** shows the standard deviation of WDF, σ_WDF, being insensitive to the stress Vgov. This strongly supports that WDF is dominated by AHTs and GD contributes little to it. This can be explained by their different energy location: compared with AHTs, GDs have higher energy levels and are above the *fermi level* at the interface when devices are switched on, so that their charges fluctuate little.

Fig. 6c shows the ΔVth measured for each Id~Vg and the average value of the 100 ΔVth after each Vgov, μ_WDF ('◊'). Some step-like rise can be observed, most likely due to the generation of an individual defect. Importantly, μ_WDF also has a plateau when Vgov is low, similarly to the large device in **Fig. 3**. As a result, GD can again be separated from the total ΔVth by subtracting this plateau in **Fig. 6c**.

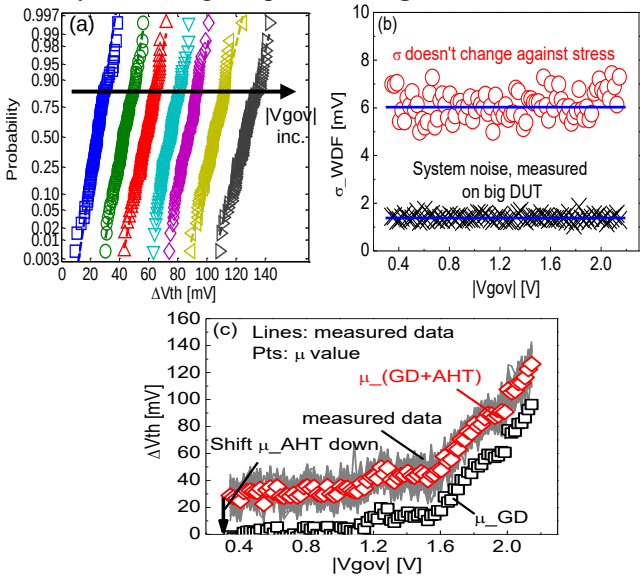

Fig. 6 (a) Statistical Within-Device-Fluctuation distrbiution of ΔVth from 100 Id~Vg measured after each Vgov step. The impact of measurement sequence on the data is found to be negligible (not shown). The distribution is caused by Within-Device-Fluctuation (WDF). **(b)** The standard deviation for the data in (a) ('o') and the data from large device ('x'). σ_WDF from nano-scaled device is much larger than the one from large device which is dominated by system noise. In addition, σ_WDF changes little with stress Vgov, confirming that it is dominated by as-grown hole traps (AHT). **(c)** For each Vgov, the 100 ΔVth were ploted as lines and their mean value as '◊'. The μ_GD_WDF ('□') was obtained by subtracting the μ_AHT in the flat plateau.

B. Device-to-Device variation (DDV) of GDs

After extracting the GD in one single device, the same test like **Fig.6c** was repeated on different pFETs to study the DDV of GDs, as shown in **Fig.7**. *In favor of the proposed VSS measurement, each test only takes less than one hour*. This dramatically improves the test efficiency.

Interestingly, although GD does not introduce time-dependent WDF, it exhibits clear DDV. This is because the defect generation is a stochastic process. Therefore, both the averaged value, μ_GD, and the standard deviation, σ_GD, need to be determined.

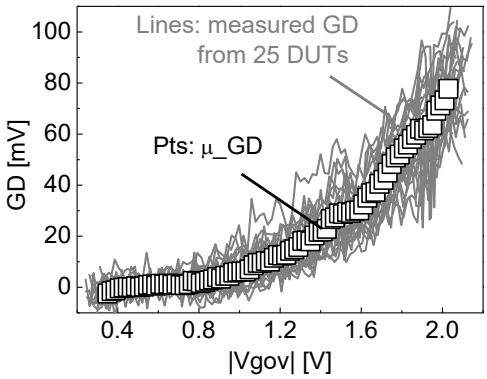

Fig. 7 The measured GDs from all 25 tested devices. The points show its average value.

We first concentrate on the average value, μ_GD ('□' in **Fig.7**) μ_GD follows the power law in eq. (1) and it has been reported that the time exponent, n, of GD is independent of device geometry [25]. The n=0.2 extracted from large device will be applied to the nano-scaled device. Once n is known, the same analysis procedure as described in section III.B can be applied to the μ_GD for extracting the model parameter g0 and m, as shown in **Fig.8a&b**.

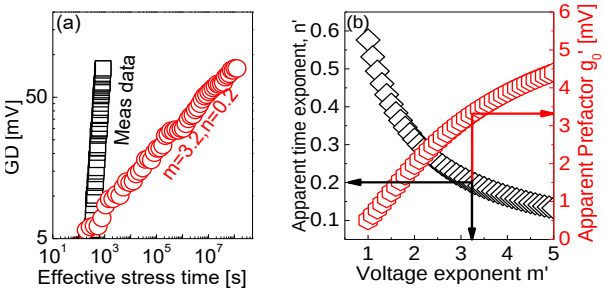

Fig. 8 (a) The aveage GD is ploted against real stress time ('□') and effective stress time ('o'), defined by Eqn (2) which is a function of voltage exponent m. m is selected to give a time exponent of 0.2. **(b)** The apperaent time exponent, n', prefactor, g0' under any given voltage expoenet, m'. The real m and g0' value can be determined when the apparent n' equals to 0.2, which is the real time exponent extracted from big device.

What is worth noting is small devices have larger g0 and smaller m, when compared with big devices, indicating higher trap density with stronger coupling (m/n). This leads to higher degradation compared with large devices. This difference has also been observed and reported [25,26]. One potential reason is that the edge-related processing effect: i.e. the degradation at the edge is larger than the middle part of the device and therefore with length scaling, the weight of edges get enhanced [26].

The distributions of GD under different Vg_ov are given in **Fig.9a**. A higher |Vgov| not only increases μ_GD, but also broadens of the distribution, resulting in larger σ_GD. The relationship for the extracted σ_GD and μ_GD is shown in **Fig. 9b**. It can be described by the power law with K2~0.5:

$$\sigma(GD) = K1 \times \mu(GD)^{K2} \qquad (3)$$

C. Statistical GD modelling

The line in **Fig.9b** has a K2=0.5, as predicted by the defect-centric model [2,3], which assumes a Poisson distribution for the DDV of GDs. The average ΔVth per trap, η, and the mean number of traps per device, N, is related to μ_GD and σ_GD:

$$\eta = \frac{\sigma(GD)^2}{2\mu(GD)} \qquad (4) \qquad N = \frac{2\mu(GD)^2}{\sigma(GD)^2} \qquad (5)$$

A η_GD = 3.12 mV is extracted from the slope of the line in **Fig.9b**. By normalizing to the expected value based on charge-sheet approximation η0=q*EOT/WL, we found that η/η0 extracted from our GD component (η/η0=2.84) is larger than the value from TDDS technique (η/η0=1.47) in which AHT dominates [27]. What is worth noting is that the recent study using charge pumping technique also observed the increase of η_GD with interface states generation [12]. It is speculated that, compared with AHT, GD is more likely located above the current percolation path due to channel-carrier assisting defect generation process.

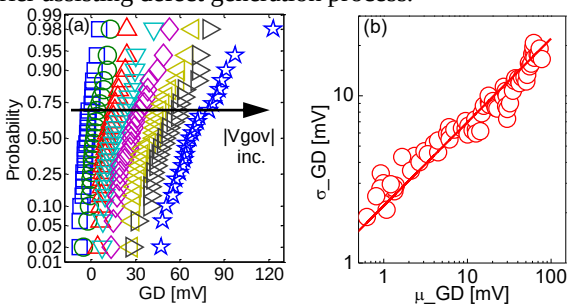

Fig. 9 (a) The statistical device-to-device distribution of GD component under different Vgov. Each point is the average of 100 measurements on one device. **(b)** The Relatiosnhip between the average and standard deviation of GD compoennt.

The procedure for the statistical simulation of GDs is illustrated in **Fig. 10**. With the experimentally determined g0, m, n, and η as the inputs, $\mu\_\Delta Vth_{GD}$ and μ_N_{GD} at any Vgov and t can be calculated by eqs. (1) and (5), respectively. If one uses M devices for each stress time, the number of traps per device can be randomly assigned using the Poisson distribution of an average μ_N_{GD} and the impact of each trap on a device, δVth_{GD}, can be generated from the exponential distribution. The total GD for a device is obtained by summing δVth_{GD} of each trap. To simulate the aging kinetics under a given Vgov, the stress time can be varied with the procedure in **Fig. 10** repeated for each time. The required input parameters for the simulation is shown in **Table 1**. What is worth noting is that the information of capture and emission time distribution of AHTs is necessary to simulate their

dynamic behavior during operation [28]. However, it is not necessary for GD, whose charging is stable under a given use-Vg. In a real circuit, both GD and WDF should be modelled, but this is out of the scope of this work.

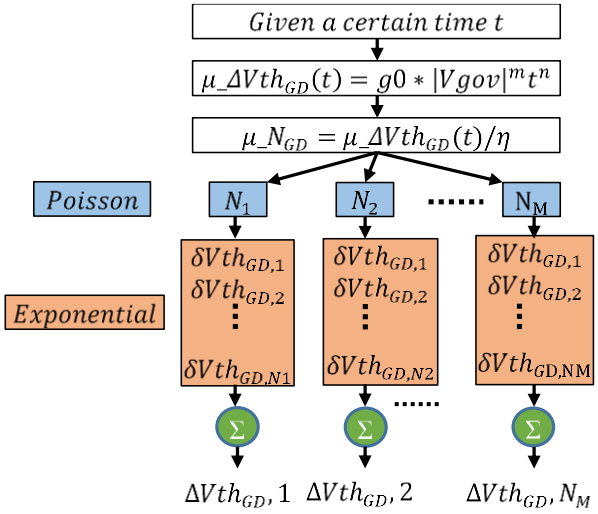

Fig. 10 Simulation procedure for generating ΔVth_GD.

g0 [mV]	m	n	η [mV]
3.31	3.24	0.2	3.125

Table I The input parameters for GD simulation

One example under Vgov = -1.5V is given in **Fig.11a** where each '+' represents one device and 3,000 devices were used. To verify the accuracy of the statistical simulation, μ_GD and σ_GD from the simulation is compared with the independently measured values in **Fig. 11b&c**, where the simulation result is shown as the red line. For the measurement, 20 devices were stressed under a constant Vgov=-1.5 V and their GDs were measured under constant Vgov and represented by the grey lines in **Fig. 11b**. The symbols in **Figs. 11b&c** represent the measured μ_GD and σ_GD, respectively. The prediction by the simulation agrees with the measurement. It should be pointed out that the test data in **Figs. 11b&c** were not used for fitting.

After verifying the model accuracy, we now use it to simulate the GD under Vgov=-0.5V, a typical overdrive voltage used in real circuits. As shown in the **Fig. 12**, the simulation starts from 1 sec and ends at 10 years, with 8 time points per decade and 3,000 devices for each time point. At 10 years, the average value is μ_GD=44mV. Although this is below the typical lifetime criterion of 50 mV, there are 1033 out of 3000 devices with GD>50 mV. This indicates that even though the RTN can be well controlled through process optimization [29], the circuit performance can still be deteriorated significantly by GD component in the long term. As a result, they need to be properly assessed during process qualification. We emphasize that it only takes less than one day for the proposed VSS-GD test to give the required statistical properties. This is similar to the test time when the conventional CVS is used for large device.

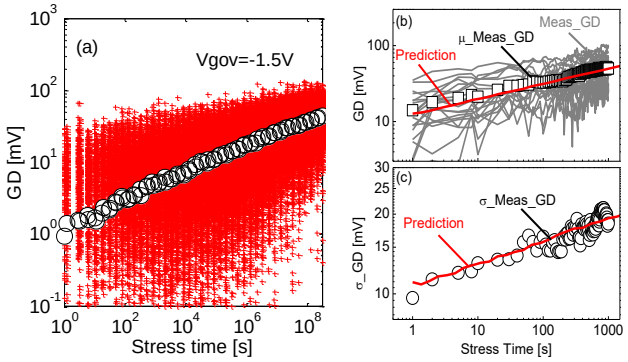

Fig. 11 (a) Simulated GD kinetics under Vgov=-1.5V. Each '+' represents one simulated device. The 'o' at each stress time is the average of 3000 devices. The comparison between the measurement and simulaton for **(b)** avearged GD, μ(GD) and **(c)** standard deviation, σ(GD). The simulation agrees with test data, which were independently obtained and were not used for model parameter extraction.

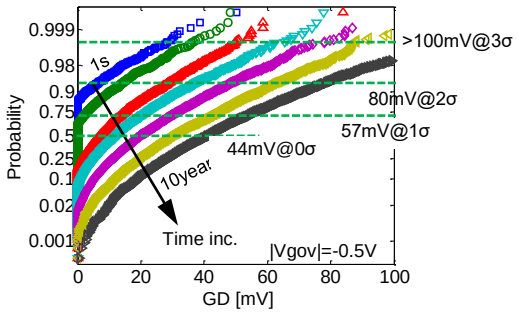

Fig. 12 The distributions under different time. the results is from 3000 Monto Carlo simulation similar to **Fig.11a** but under Vgov= -0.5V.

V. CONCLUSION

This work develops a VSS-GD technique for a fast and accurate characterization of the stochastic NBTI-generated defects in nano-scaled devices. The fast speed comes from the use of voltage step stress (VSS), instead of the conventional constant voltage stress, for extracting the voltage exponent. The accuracy is provided by capturing GDs without recovery, so that the extracted time exponent is independent of the measurement conditions. For the first time, we demonstrated that the applicability of VSS-GD to the nano-scaled devices for extracting the statistical properties, standard deviation and average value. Moreover, we verified that the accuracy of the statistical model with the extracted properties as input parameters against experimental data. The proposed method provides an effective solution for GD evaluation during process qualification. The total test-time is within one day, making it readily implementable in industrial test laboratories.

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