Chai, Z, Zhang, WD, Freitas, P, Hatem, F, Zhang, JF, Marsland, J, Govoreanu, B, Goux, L, Kar, GS, Hall, S, Chalker, P and Robertson, J

The over-reset phenomenon in Ta2O5 RRAM device investigated by the RTN-based defect probing technique

http://researchonline.ljmu.ac.uk/8673/

Article

Citation (please note it is advisable to refer to the publisher's version if you intend to cite from this work)


LJMU has developed LJMU Research Online for users to access the research output of the University more effectively. Copyright © and Moral Rights for the papers on this site are retained by the individual authors and/or other copyright owners. Users may download and/or print one copy of any article(s) in LJMU Research Online to facilitate their private study or for non-commercial research. You may not engage in further distribution of the material or use it for any profit-making activities or any commercial gain.

The version presented here may differ from the published version or from the version of the record. Please see the repository URL above for details on accessing the published version and note that access may require a subscription.

For more information please contact researchonline@ljmu.ac.uk

http://researchonline.ljmu.ac.uk/
The over-reset phenomenon in Ta$_2$O$_5$ RRAM device investigated by the RTN-based defect probing technique

Zheng Chai, Weidong Zhang, Pedro Freitas, Firas Hatem, Jian Fu Zhang, John Marsland, Bogdan Govoreanu, Ludovic Goux, Gouri Sankar Kar, Steve Hall, Paul Chalker and John Robertson

Abstract— Despite the tremendous efforts in the past decade devoted to the development of filamentary resistive-switching devices (RRAM), there is still a lack of in-depth understanding of its over-reset phenomenon. At higher reset stop voltages that exceed a certain threshold, the resistance at high resistance state reduces, leading to an irrecoverable window reduction. The over-reset phenomenon limits the maximum resistance that can be achieved by using a higher $V_{reset}$, which also degrades its potential in applications such as multi-level memory and neuromorphic synapses. In this work, the over-reset is investigated by cyclic reset operations with incremental stop voltages, and is explained by defect generation in the filament constriction region of Ta$_2$O$_5$ RRAM devices. This is supported by the statistical spatial defects profile obtained from the random telegraph noise based defect probing technique. The impact of forming compliance current on the over-reset is also evaluated.

Index Terms—Resistive switching, RRAM, over-reset, defect profile, random telegraph noise, Ta$_2$O$_5$, HfO$_2$.

Resistive-switching random access memories (RRAMs) have attracted extensive interest in the past decade as a promising candidate for future non-volatile memory applications [1-5]. RRAM devices can be categorized into either filamentary or non-filamentary [6,7] types. The filamentary type has a relatively longer development history and represents the current mainstream RRAM technology. Tremendous effort has been devoted to improving their performance such as endurance, retention, on/off window, etc. A large resistance window (RW) is always desirable for achieving better performance in applications such as multi-level memory [4] and neuromorphic synapses [8].

Resistive switching in filamentary devices has been attributed to the reversible migration of either metal ions in CBRAMs [9-11] or oxygen ions/vacancies in RRAMs [2-6]. A conductive filament is generated in RRAM during the forming through a field assisted and thermally activated hopping process. During alternate reset and set operations, the filament ruptures and restores repeatedly, leading to the high resistance state and low resistance state, respectively (HRS/LRS). It has been observed in RRAMs with various oxides such as HfO$_2$ and Ta$_2$O$_5$ [12, 13] that once $V_{reset}$ increases beyond a certain level, $R_{HRS}$ will start to decrease instead of further increase; it is difficult to recover from the consequent window reduction [12, 13]. This over-reset phenomenon will therefore limit the achievable RW by using a higher $V_{reset}$.

The over-reset phenomenon has been explained by the migration of defects near the bottom electrode (BE) moving back into the constriction region of the filament at higher reset voltages, which re-connects the defect-rich filamentary regions near the top electrode (TE) and BE. This effect leads to a reduced resistance at HRS [12]. An alternative explanation is by the horizontal out-diffusion of defects from the filament into the surrounding dielectrics which forms additional conduction paths, hence the higher conduction current and lower resistance [13]. However, there is a lack of direct experimental evidence to support either of the above assumptions. By using the random telegraph noise (RTN)-based defect probing technique (RDT) developed in our recent work [6, 7], we provide a novel microscopic insight into the defect’s spatial locations and compare the defect profiles after normal- and over- reset. The over-reset can be explained by defect generation in the filament constriction region at higher reset voltages. The impact of the compliance forming current on over-reset is also evaluated and discussed.

The Ta$_2$O$_5$ filamentary RRAM devices used in this work were fabricated in a cross-point structure with a size of 75 nm × 75 nm. The device consists of a Ti/Ta$_2$O$_5$/TaOx/TaN/TiN stack. The TiN BE was sputtered at room temperature and patterned, followed by the ALD deposition of a 4-nm-thick high-quality stoichiometric Ta$_2$O$_5$ layer. A nonstoichiometric 20-nm-thick TaOx film was then deposited by reactive DC magnetron sputtering using a Ta target in oxygen ambient. Without breaking the vacuum, a 10-nm-thick TaN capping layer was sputtered followed by a 30-nm-thick TiN film sputtering to form the TE. A long wire was patterned to connect the probe pad to the TE, enabling an integrated access resistance which effectively suppresses reset current overshoot [14]. We have also observed similar over-reset in other devices with either a Ti/Ta$_2$O$_4$ (15nm)/Pt stack [15] or a TiN/Hf(10nm)/HfO$_2$(5nm)/TiN stack [6].

DC electrical measurements were carried out by using a Keysight B1500A semiconductor parameter analyzer with the bias applied to the TE, and the BE at ground. A forming step using the positive voltage sweep in the fresh device activates the reversible resistive switching behavior, which is copped by a compliance current (Icc) to protect the device from hard breakdown. The device structure and its I-V characteristics are shown in Fig. 1(a). It is switched between LRS and HRS during the positive set and negative reset voltage sweeps, respectively. In our previous work [6, 7], RTN has been used as the electrical measurement technique to evaluate the defect profile, providing a defect-level explanation of switching mechanisms in filamentary [6] and non-filamentary
The over-reset phenomenon is investigated in this work by the RDT technique carried out in both normal-reset and over-reset devices for comparison. The origin of RTN is attributed to the random electron trapping/de-trapping process in a defect located in the oxide [16]. The spatial and energy location of defects can be extracted from the dependence of time constants on the TE bias. To obtain the statistical defect profile, the device was switched on and off repeatedly for 100 cycles under fixed conditions, and the RTN measurement was carried out after each reset. The accumulative occurrence of defects at HRS can therefore be used to evaluate the statistical defect profile. Details and discussion of this technique can be found in refs. [6, 7].

![Image](57x514 to 119x570)

**Fig. 1** (a) The structure (inset) and bipolar resistive switching characteristics of a 75 nm × 75 nm TaOx memory cell. (b) Comparison of normal reset (Vstop=-1.7V) and over-reset (Vstop=-2V) of the TaOx. The inset shows the over-reset phenomenon in HfOx RRAM devices (Vstop=3V).

The I-V characteristics of a normal reset at a stop voltage of -1.7 V and an over-reset at a stop voltage of -2 V are compared in Fig. 1(b). Both devices were formed with an Icc of 20 µA. It is clear that the currents overlap in a large part of the upward voltage sweep, suggesting that both devices start from the same LRS level, and the reset process is similar for the bias level up to -1.7 V. Since the over-reset stop voltage is higher, its current starts to increase from -1.7 V onward, and also becomes higher during the downward voltage sweep, leading to the over-reset, i.e., a lower resistance at HRS. As shown in the inset of Fig. 1(b), a similar over-reset phenomenon is also observed in HfOx RRAM devices, suggesting it is a universal issue for filamentary RRAM devices.

To further demonstrate the impact of over-reset on the HRS, the reset bias sweep cycle (0 V→Vstop→0 V) was repeated with the stop voltage incremented for each cycle, without invoking the set sweep in between. I-V curves during the reset and over-reset cycles, and the resistance read-out current after each reset cycle with no defect occurrence is observed at the center of the filament, as shown in Fig. 3(a). A similar RTN data are shown in Fig. 3(c). For the normal reset device, a region with no defect occurrence is observed at the center of the filament, as shown in Fig. 3(a). This result indicates that the filament constriction location is centered in the TaOx layer of our TiN/TaOx/TaOx/TiN device. Early work has reported that the filament in TaOx/TaOx dual-layer RRAM with Pt [17] or Ir [18, 19] metal electrodes ruptures in the TaOx layer near the TE interface, by the redox reaction of oxygen ions or vacancies. Since filament growth/dissolution dynamics is strongly dependent on the oxide and electrode materials and their combinations, the centered constriction location in our device is likely caused by the lower Schottky barrier and lesser scavenging power of the TiN electrode used in this work, and the similar oxygen scavenging power of the nonstoichiometric TaOx layer on top of the TaOx switching layer, which leads to a more symmetric hour-glass shaped filament in the TaOx layer [20]. In our previous work we have observed that in HfOx devices, the constriction is located near to, but not at, the BE [6]. This difference can be attributed to the Hf cap layer used under the TE in HfOx devices, which has stronger oxygen scavenging power.
than the TiN BE, so that more oxygen vacancies are generated near the HF cap, pushing the constriction region towards the BE.

In early work [12] the over-reset has been interpreted as the activation and movement of defects from the BE side into the constriction, subsequently moving further towards TE under a higher reset stop voltage. This results in the constriction being gradually narrowed and shifted. But this assumption cannot explain why this type of defect movement is not reversible. In another work [13], the assumption of horizontal out-diffusion of defects from the filament into the surrounding dielectrics, leading to additional conduction paths, has been used to explain the over-reset. Our results cannot completely rule out this possibility but do provide an alternative explanation supported with experimental evidence. Additional immobile defects are generated in the constriction under strong reset field during over-reset. These defects facilitate current conduction typically through trap-assisted-tunneling, leading to lower resistance at HRS. Meanwhile, their existence in the constriction leads to lower local electric field and makes the reset operation by normal defect movement less effective, even under the over-reset condition. This explains why the RW cannot be fully recovered.

Since the over-reset causes irreversible window reduction, it is desirable to alleviate this phenomenon. As shown in Fig. 3(d), devices formed under different Icc were tested to evaluate its impact, using the same incremental V_{reset, stop} method as shown in Fig. 2. The higher forming Icc leads to higher read-out current at LRS, due to the formation of a stronger filament. All devices reach the maximum HRS at around -1.7 V, with a steeper reset process at higher Icc. Interestingly, the extent of over-reset is reduced by using higher Icc, which can be explained as follows. The stronger filament formed at higher Icc can only be ruptured at higher V_{reset} leading to a more abrupt reset process. The conduction at HRS becomes less sensitive to the newly-generated defects in the constriction during over-reset, due to the overall larger effective filament cross section caused by higher Icc [4]. Using a higher Icc can alleviate, to some extent, but cannot completely avoid the over-reset problem, due to the defect generation in the filament constriction. A higher forming compliance current will lead to a number of side effects, such as higher power consumption, greater probability of device breakdown, larger resistance variation. The trade-off between higher Icc and lower level of over-reset should be carefully considered in practical application. It cannot be the ultimate solution for memory applications that primarily pursue low-current operation, therefore. Further efforts should be made to increase the critical reset voltage that causes the over-reset, potentially by using materials having lower defect generation rates and higher breakdown voltages.

In summary, the statistical defect profile in the conductive filament of TiN/TaOx/Ta2Ox/TiN RRAM devices has been analyzed using the RTN-based defect tracking technique. It is revealed that the constriction region is located at the center of the filament in the Ta2Ox layer. The irrecoverable over-reset is caused by the generation of immobile defects in the constriction region which facilitates current conduction at HRS and lowers the local field in following set/reset operations. It is also found that a higher forming compliance current can alleviate, to certain extent, the over-reset phenomenon. These findings provide valuable information for improving the on/off window in filamentary metal-oxide RRAM devices.
REFERENCES


