Cervone, A, Brando, G and Dordevic, O

Hybrid modulation technique with dc-bus voltage control for multiphase NPC converters

Hybrid Modulation Technique with DC-Bus Voltage Control for Multiphase NPC Converters

A. Cervone, *Student Member, IEEE*, G. Brando, and O. Dordevic, *Member, IEEE*

***Abstract* — The paper presents a novel Carrier-Based Pulse Width Modulation (CBPWM) technique for multiphase Neutral Point Clamped (NPC) converters. The technique is aimed to actively control the Neutral Point (NP) potential while supplying the desired set of line-to-line voltages to the load. Standard techniques are either based on the sole Common Mode Voltage Injection (CMI) or on the sole Multi-Step (MS) switching mode; contrarily, the proposed algorithm combines these two approaches to take advantage of their main benefits. The technique performs well for each number of phases, for each modulation index and for each type of load. It can control in closed-loop the NP voltage to any desirable value with a reduced number of switching transitions. The proposed approach has been experimentally validated and compared with other carrier-based algorithms.**

***Keywords* — Neutral Point Clamped, Multiphase Converters, Carrier Based, Pulse Width Modulation, Voltage Balancing.**

LIST OF SYMBOLS

M	Number of phases
v_{DC}	Total DC-bus voltage
$v_{DC,B};\ v_{DC,T}$	Bottom/Top DC-bus capacitor's voltage
$s_{B,k};\ s_{T,k}$	Bottom/Top device firing signal (*k*-th phase)
$d_{B,k};\ d_{T,k}$	Bottom/Top device duty-cycle (*k*-th phase)
$v_k;\ i_k$	NPC leg output voltage/current (*k*-th phase)
$i_{NP,k};\ i_{NP}$	Partial (*k*-th phase) / total NP current
$d_{NP,k};\ \alpha_k$	NP duty cycle / NP gain factor (*k*-th phase)
$d_{NP,\max,k}$	Maximum NP duty cycle value (*k*-th phase)
$d_{NP,\max}(v_k^*)$	Maximum NP duty cycle function
$\tilde{v}_k^*$	Output phase voltage reference (*k*-th phase)
v_0^*	Common mode voltage reference
$v_{0b,h}^*$	Clamping voltage (*h*-th breaking point)
$T_c;\ \sigma_c$	Modulation period / carrier signal
C	DC-bus capacitances

I. INTRODUCTION

Multilevel converters are, nowadays, an established and industrially accepted technology for high-voltage and high-power applications, both in the field of the electrical drives and for grid-connected interfaces [1-4]. Indeed, at the expense of a higher number of switching devices, they guarantee several benefits with respect to conventional two-levels converters, like higher output voltage capabilities, reduced output voltage harmonic content, lower switching losses and a better electromagnetic compatibility. Among the different architectures, the Diode Clamped Converter (DCC), first introduced in [5], is one of the most commonly used structures [1-2], especially in its three-level form, which is commonly named Neutral Point Clamped (NPC). Its basic leg circuit consists of four active switching devices (with their free-wheeling diodes) and two clamping diodes per leg. The DC bus is built of two series-connected capacitors with a Neutral Point (NP) rail. Given the presence of a common DC bus, the extension to a multiphase architecture is quite straightforward.

A key problem for NPC converters is to keep the DC-bus capacitors' voltages balanced, neutralizing the NP voltage drift and suppressing an undesired ripple [6-8]. Indeed, the current driven through the clamping diodes acts differently on the DC capacitors and, in some operating conditions, leads to low-frequency oscillations [6-8] or even to an unstable behaviour [7]. These phenomena stress both the capacitors and the switching devices, reducing the life-span of the entire structure.

The equalization task can be performed either through additional hardware circuits, specially developed for the voltage balancing [9-12], or through software approaches, by properly acting on the switching devices firing signals. This paper focuses on the software approaches.

Several Pulse Width Modulation (PWM) techniques have been proposed in the technical literature for the NPC converter. As in the two-level case, they can be classified into three main categories: Selective Harmonic Elimination (SHE), Space Vector (SV) and Carrier Based (CB), [13-14].

The SHE approaches compute the devices' switching instants with the aim to supply a set of voltages with a desired harmonic content. Based on the load currents, the switching instants can be properly conditioned to control the NP potential [15-16]. However, these strategies refer to the steady state behaviour of the converter and require a priori knowledge of the supplied load for the estimation of the effects of the currents on the DC-bus voltages. As a result, they lack robustness and are not suited when the load is often subject to transients.

Space vector approaches for NPC converters are usually related to three-phase case where the available output voltage combinations are classified into "zero", "small", "medium" and "large" vectors, according to their magnitude [13, 17-18]. Only the small and medium vectors have a direct effect on the NP potential and can be effectively exploited for equalization purposes, which is achieved by properly setting their dwell times [17-27]. To counteract the poor NP potential control capabilities in case of high modulation indexes, some authors proposed slightly different approaches based on the definition of a set of Virtual Space Vectors (VSVs) as proper linear combination of the original voltage vectors [28-30]. They allow

This work is an extension of the conference paper [52].

Manuscript received December 04, 2019; revised January 29, 2020 accepted April 20, 2020.

A. Cervone and G. Brando are with the Department of Electrical Engineering and Information Technology, University of Naples Federico II, 80125, Naples, Italy (e-mail: andrea.cervone@unina.it; gianluca.brando@unina.it)

O. Dordevic is with the Faculty of Engineering and Technology, Liverpool John Moores University, Liverpool L3 3AF, U.K. (e-mail: O.Dordevic@ljmu.ac.uk)

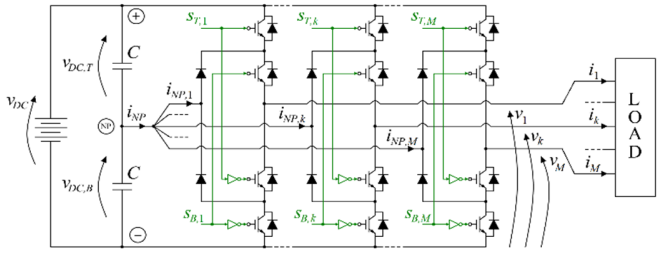

Fig. 1. Power circuit of an *M*-phase neutral point clamped converter.

full control of the NP potential but introduce more switching transitions in each modulation period. Nevertheless, SV techniques (including VSV-based ones) are usually not suited for multiphase converters, both due to the fast increase of the number of different output vectors with the increase of the number of phases and due to the appearance of the additional space vector planes [31-35]. Many different approaches have been proposed in the technical literature to simplify the SV implementation on digital controllers [34-35], but only few of them explicitly address the NP equalization at the same time.

Contrarily, CB approaches, by separately focusing on each converter's phase, can be easily extended from three-phase to multiphase converters without requiring any intensive computational effort [35].

Most of the standard CBPWM techniques developed for the NPC compute the switching signals for each phase through a single-reference/multi-carriers approach (i.e. by comparing a single duty-cycle per phase with two common triangular carrier signals) [13-14]. With this choice, in a single modulation period, the output node can either switch between the negative rail and the NP or between the NP and the positive rail, thus operating in Single-Step (SS) switching mode. This choice, despite minimizing the switching transitions rate, binds the top/bottom switching signals to the sole phase reference output voltage, thus lacking the control of the neutral point current.

To counteract this phenomenon, a proper Common Mode Injection (CMI) can be added to the reference leg voltages to condition the switching signals and regain control over the NP current [36-42]. This method is completely equivalent to the dwell-time adjustment with SV approaches [34-35] but, like the SV modulation techniques, it fails to guarantee the desired control in case of high modulation indexes, given the constraint on the common mode voltage which can be injected.

A different strategy is based on allowing the output voltage to switch between the positive, negative and NP nodes in the same modulation interval. This leads to an additional degree of freedom which can be exploited for the NP control [43-52]. This switching behaviour can be referred as Multi-Step (MS) mode and requires multiple reference signals for each phase, in order to separately control each switching device [45-46]. The extreme case is achieved by forcing the top and bottom device to switch at the same time. When it happens, the converter's leg acts as an equivalent two-level converter leg and this behaviour can be referred as Two-Level (TL) mode. However, all the MS based approaches, despite being generalizable to any number of phases and being able to completely control the NP current (thus, removing the NP voltage oscillations), by switching between more levels, lead to an increase of the losses [45].

This paper proposes a novel carrier-based modulation technique which, by properly combining the MS mode and an optimal CMI, is able to effectively exploit all the degrees of freedom offered by a multiphase NPC structure. It takes advantage of the main benefits of the two approaches, while at the same time neutralizing some of their main drawbacks.

This work is an extension of the hybrid technique proposed by the authors in [52], where the focus was on a three-phase NPC converter which allowed to establish a deterministic way to combine the CMI with the MS capability and to show that having only one leg working in MS mode is sufficient to guarantee the full NP voltage control. However, this property is not true for multiphase systems and, therefore, the generalization of the proposed hybrid technique to a multiphase converter requires a refined procedure to properly exploit all the degrees of freedom offered by the structure. The generalization to multiphase systems makes the proposed approach particularly suited for high-power/high-reliability applications, like for electric ship propulsion or wind turbines, where multiphase drives are more and more frequently adopted [31].

The paper is organized as follows. First, in Section II, the mathematical model of the converter's leg is obtained, with a special emphasis on the switching constraints to be respected; it is then expanded to a generic *M*-phases/*M*-wires system to highlight all the available degrees of freedom. In Section III, some different approaches are discussed. After addressing some CMI and MS based solutions already available in the technical literature, the proposed hybrid method is presented and discussed. Section IV shows the experimental validation of this technique, together with a proper comparison with some other approaches. The conclusions are given in Section V.

II. Mathematical Model

The considered architecture consists of an M-phase NPC converter, feeding a generic M-phases/M-wires load (Fig. 1). The neutral wire is absent and, consequently, the converter's common mode current is constrained to zero. The positive and the negative DC rails are connected to a DC source with an almost constant total voltage $v_{DC} = v_{DC,B} + v_{DC,T}$. The NP rail is connected to the NPC legs through the clamping diodes.

A. Mathematical Model of an NPC Converter's Leg

With reference to Fig. 1, the k-th converter leg (with $k = 1, \dots, M$) can be connected to the three DC-bus nodes through the active devices and the clamping diodes. Each top/bottom device can be controlled through the corresponding switching signal $s_{(T/B),k} \in \{0;1\}$, while its complementary device is controlled by the signal $(1 - s_{(T/B),k})$. The four possible switching states, together with the corresponding values of the obtained leg voltage v_k and NP current $i_{NP,k}$, are summarized in Table I. The state $\{1;0\}$ makes the output voltage dependent on the sign of the output current and, as a result, it is useless for control purposes. As can be seen from Table I, a simple way to avoid its exploitation is to guarantee $0 \le s_{T,k} \le s_{B,k} \le 1$.

TABLE I. NPC *k*-TH PHASE SWITCHING STATES

State	$s_{T,k}$	$s_{B,k}$	v_k	$i_{NP,k}$
{0,0}	0	0	0	0
{0,1}	0	1	$v_{DC,B}$	i_k
{1.0}	1	0	$v_{DC} \cdot (1 - \text{sign}(i_k))/2$	0
{1,1}	1	1	v_{DC}	0

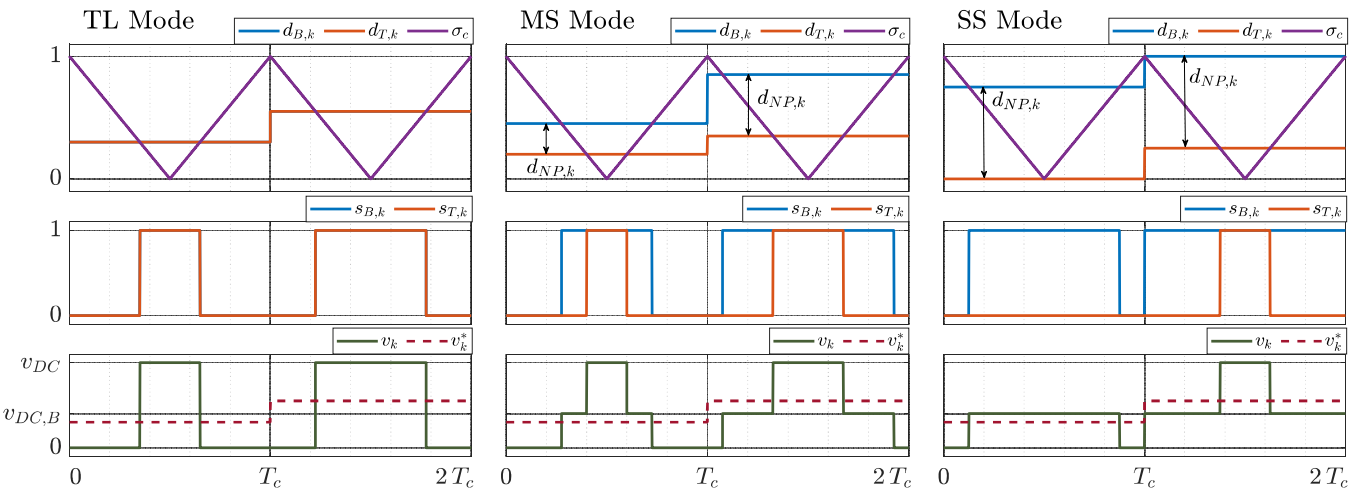

Fig. 2. Qualitative behavior of the different switching modes for the same leg output voltage reference v_k^* (left: Two-Level, middle: Multi-Step, right: Single-Step).

Further on, to take into account all the possible switching modes (SS, MS and TL), the switching signals are considered as obtained through a multi-references single-carrier PWM technique. This means that each $s_{(T/B),k}$ is computed through the comparison of a corresponding duty-cycle $d_{(T/B),k} \in [0;1]$ with a common triangular carrier σ_c, varying linearly in the same $[0;1]$ interval with period T_c. The different switching modes are exemplified in Fig. 2. Note that in Fig. 2, a general case is shown where the upper and the lower DC-bus capacitors have different voltages (i.e. $v_{DC,B} \neq v_{DC,T} \neq v_{DC}/2$).

As can be deduced from the graphical interpretation, the switching constraints $0 \leq s_{T,k} \leq s_{B,k} \leq 1$ are automatically met once the corresponding duty-cycles satisfy:

$$0 \leq d_{T,k} \leq d_{B,k} \leq 1 \tag{1}$$

Also, from Fig. 2 note that for SS and TL mode the duty cycles $d_{T,k}$ and $d_{B,k}$ are uniquely determined for a given leg reference voltage v_k^*. This is not the case for MS mode; the illustration in Fig. 2 is only one possible choice of $d_{T,k}$ and $d_{B,k}$.

By neglecting the voltage drops and the leakage currents in the semiconductor devices and by applying a standard averaging procedure over a T_c time interval, the average k-th converter's leg voltage and NP current are found to be:

$$\begin{aligned} \bar{v}_k &= d_{B,k} \cdot \bar{v}_{DC,B} + d_{T,k} \cdot \bar{v}_{DC,T} \\ \bar{i}_{NP,k} &= (d_{B,k} - d_{T,k}) \cdot \bar{i}_k = d_{NP,k} \cdot \bar{i}_k \end{aligned} \tag{2}$$

Overbar symbol denotes average value of the signal during T_c. To keep notation simple, the overbar will be omitted further on, meaning that all the variables will implicitly refer to their average values over a modulation period.

The difference $d_{NP,k} = d_{B,k} - d_{T,k}$, that appears in (2) for $i_{NP,k}$, is an important parameter. Based on (1) one can see that it is always a non-negative value and represents the fraction of the modulation period T_c for which the output of the k-th leg is connected to the NP. As mentioned, for MS mode the same reference voltage can be obtained by using different values of $d_{T,k}$ and $d_{B,k}$, thus by using different value of $d_{NP,k}$. Therefore, from the MS modulation perspective and based on (2), $d_{NP,k}$ can be considered as a degree of freedom for the NP current control.

The minimum value of $d_{NP,k}$ is zero and is obtained in TL mode (Fig. 2-left). The maximum value is obtained in SS mode (Fig. 2-right) and depends on the reference leg voltage v_k^*: if $v_k^* < v_{DC,B}$ (as in Fig. 2-right from 0 to T_c) then $d_{NP,\max,k} = v_k^*/v_{DC,B}$; if the reference is $v_k^* > v_{DC,B}$ (as in Fig. 2-right from T_c to $2T_c$) then $d_{NP,\max,k} = (v_{DC} - v_k^*)/v_{DC,T}$. Hence, the maximum NP duty-cycle of each leg can be expressed as a function of the corresponding leg voltage reference as:

$$d_{NP,\max,k} = d_{NP,\max}(v_k^*) = \min\left\{\frac{v_k^*}{v_{DC,B}}; \frac{v_{DC} - v_k^*}{v_{DC,T}}\right\} \tag{3}$$

The function $d_{NP,\max}(v_k^*)$ is the same for all M converter legs, but for each leg it should be evaluated in correspondence to its reference leg voltage v_k^* (which, in general, differs from leg to leg). From (3) one can see that $d_{NP,\max}(v_k^*)$ is a piece-wise linear function that linearly increases from 0 to 1 in the interval $0 \leq v_k^* \leq v_{DC,B}$ and linearly decreases from 1 to 0 in the interval $v_{DC,B} \leq v_k^* \leq v_{DC}$. All the intermediate values of $d_{NP,k}$ (between 0 and $d_{NP,\max,k}$) are the possible choices for MS mode (Fig. 2-middle). Thus, SS and TL mode can be also considered as special cases of MS mode.

Instead of dealing with $d_{NP,k}$ which is in range from 0 to $d_{NP,\max}(v_k^*)$ (and which is different for each leg), it is convenient to introduce the following normalization:

$$\alpha_k = d_{NP,k}/d_{NP,\max,k} = d_{NP,k}/d_{NP,\max}(v_k^*) \tag{4}$$

The parameter α_k is named gain factor and is in range from 0 to 1. It represents percentage of $d_{NP,\max,k}$ used in that switching period by the k-th NPC leg. The gain factor can be used to identify the switching mode of each leg ($\alpha_k = 0$: TL Mode; $0 < \alpha_k < 1$: MS Mode; $\alpha_k = 1$: SS Mode).

From (4) one can write $d_{B,k} - d_{T,k} = d_{NP,k} = \alpha_k \cdot d_{NP,\max}(v_k^*)$. Substituting this into (2), one can see that by properly adjusting α_k it is possible to vary the neutral point current $i_{NP,k}$ absorbed by the k-th converter leg in each switching period, while keeping the average value of the obtained leg voltage equal to the reference v_k^*. This capability of the MS mode can be conveniently exploited for the NP voltage control but, as a drawback, it introduces additional switching transitions comparing to the SS mode.

B. Multiphase NPC Mathematical Model

The average dynamic of the DC-bus capacitors' voltage unbalance can be found through superposition of each phase contribution to the average NP current (see Fig. 1):

$$C\frac{\mathrm{d}}{\mathrm{d}t}(v_{DC,T}-v_{DC,B}) = i_{NP} = \sum_{k=1}^{M} i_{NP,k} = \sum_{k=1}^{M} i_k \cdot \alpha_k \cdot d_{NP,\max}(v_k^*) \quad (5)$$

In absence of a neutral wire connection the converter's common mode voltage does not have any influence on the behaviour of the load (because the phase-to-phase voltages stay unchanged). A common mode voltage reference v_0^* can be therefore injected in the NPC leg voltages to influence the converter's behaviour (in this case the DC-bus voltages) without altering the voltages and currents of the supplied load. Each NPC reference leg voltage v_k^* can be expressed as a sum of the corresponding reference phase voltage $\tilde{v}_k^*$ and of the reference common mode voltage v_0^* as:

$$v_k^* = \tilde{v}_k^* + v_0^* \ , \quad \text{with} \quad v_0^* = (1/M)\cdot\sum_{k=1}^{M} v_k^* \quad (6)$$

By substituting (6) into (5) one gets:

$$C\frac{\mathrm{d}}{\mathrm{d}t}(v_{DC,T}-v_{DC,B}) = \sum_{k=1}^{M} i_k \cdot \alpha_k \cdot d_{NP,\max}(\tilde{v}_k^* + v_0^*) \quad (7)$$

This expression formulates the NP voltage dynamics in its most general way by highlighting all the involved parameters and allowing to separate the controllable ones (v_0^* and all α_k values) from the uncontrollable ones (all $\tilde{v}_k^*$ and i_k).

To analyse (7) first note that, since $0 \le v_k^* \le v_{DC}$ must be satisfied for all NPC legs, the value of v_0^* is constrained to be within the feasible interval, whose extremes are:

$$\begin{aligned} v_{0,\min}^* &= |\ \min_k\{\tilde{v}_k^*\}\ | = -\min_k\{\tilde{v}_k^*\} \\ v_{0,\max}^* &= v_{DC} - |\ \max_k\{\tilde{v}_k^*\}\ | = v_{DC} - \max_k\{\tilde{v}_k^*\} \end{aligned} \quad (8)$$

Going further, note that once a feasible set of reference phase voltages $\tilde{v}_k^*$ and of gain factors α_k are chosen, the neutral point current i_{NP} is a piece-wise linear function of the common mode voltage reference v_0^*. This is because $d_{NP,\max}(v_k^*)$ (as explained in section II-A) is a two-segment piecewise linear function and, from (7), i_{NP} is the sum of M of such functions (each of which has its own breaking points defined by the argument $v_k^* = \tilde{v}_k^* + v_0^*$ and is weighted by $i_k \cdot \alpha_k$). One example of i_{NP} as a function of v_0^* is shown in Fig. 3. The breaking points appear when one converter's leg voltage is clamped to one of the DC-bus nodes [38]. Since the conditions $v_k^* = 0$ and $v_k^* = v_{DC}$ are verified only when $v_0^* = v_{0,\min}^*$ and $v_0^* = v_{0,\max}^*$, while the condition $v_k^* = v_{DC,B}$ might be satisfied by any leg, there are at most $M+2$ different clamping voltages/breaking points (further on denoted as $v_{0b,1}^*, v_{0b,2}^*, \ldots$).

Finally, note that the above analysis is valid for any M-wire system, including non-linear and non-symmetrical loads.

III. Hybrid CMI - MS Modulation Strategy

Based on (7), to actively control the neutral point voltage, the NPC modulation strategy should be designed to achieve the full control of the current i_{NP}, which should be driven towards a desired reference i_{NP}^* (coming, for example, from a closed loop feedback controller). However, this capability should not interfere with the main converter purpose, which is to supply a desired set of phase voltages $\tilde{v}_k^*$. Similarly, the output currents i_k, depend on the supplied load, thus cannot be directly used for the NP voltage control. Therefore, as already stated, the available degrees of freedom are the common mode voltage reference v_0^* and the gain factors α_k . Depending on the exploited degrees of freedom, different strategies are defined.

A. Standard CBPWM

The standard CBPWM does not address the NP current control and all the converter's legs work in SS mode (i.e. all the gain factors are set to $\alpha_k = 1$ meaning that, in each modulation interval, the converter's legs are connected to the NP for the maximum available time). This is automatically achieved with most of the standard single-reference multi-carriers PWM techniques (like all the level-shifted methods). The common mode voltage is usually chosen to extend the linear modulation region, for example through a standard min-max injection [35]:

$$\begin{aligned} v_0^* &= v_{0,\text{avg}}^* = (v_{0,\min}^* + v_{0,\max}^*)/2 \\ &= v_{DC}/2 + (\ |\min_k\{\tilde{v}_k^*\}| - |\max_k\{\tilde{v}_k^*\}|\ )/2 \end{aligned} \quad (9)$$

B. Common Mode Injection Based Techniques

Some authors, as discussed in Section I, propose the exploitation of the sole common mode voltage v_0^* for the NP current control. The converter works in SS mode (i.e. all the $\alpha_k = 1$) and, again, the modulation can be realized through a single-reference multi-carriers comparison technique. The number of transitions per period is minimized and, together with it, also the corresponding switching losses [36-42].

In [37] and [38] the choice of the common mode reference voltage is performed by evaluating the neutral point current $i_{NP}(v_0^*)$ at the breaking points (as shown in Fig. 3) and then by selecting the clamping voltage $v_{0,opt,me}^*$ which minimizes the error $|i_{NP}(v_0^*) - i_{NP}^*|$ from the reference NP current:

$$v_0^* = v_{0,opt,me}^* = \text{argmin}_{v_{0b,h}^*}\{|i_{NP}(v_{0b,h}^*) - i_{NP}^*|\} \quad (10)$$

Since the breaking points $v_{0b,h}^*$ are obtained when one of the converter's legs is clamped to one of the DC-bus nodes, that means that this approach results in no switching in one phase during each modulation interval. Therefore, some discontinuous PWM techniques (DPWM), like the one of [42], can be interpreted as particular cases of this procedure.

A refined approach consists in choosing, when possible, the common mode voltage reference able to set the NP current exactly to the desired reference. If a zero-crossing of the error function $|i_{NP}(v_0^*) - i_{NP}^*|$ is detected between the h-th and $(h+1)$-th breaking point ($v_{0b,h}^*$ and $v_{0b,h+1}^*$), then the optimal

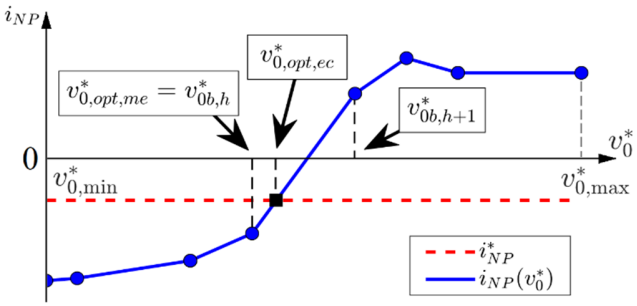

Fig. 3. Optimal common mode voltage reference with the minimum breaking point error ($v_{0,opt,me}^*$) and with the error cancellation ($v_{0,opt,ec}^*$).

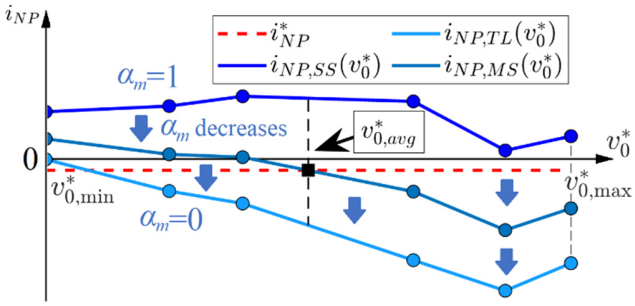

Fig. 4. Effect of the modification of the Current Gain Factor on a phase: $i_{NP,SS}$ (SS Mode), $i_{NP,TL}$ (TL Mode), $i_{NP,MS}$ (Optimal MS Mode).

v_0^* is easily obtained via linear interpolation as:

$$v_0^* = v_{0,opt,ec}^* = v_{0b,h}^* + (v_{0b,h+1}^* - v_{0b,h}^*) \cdot \frac{i_{NP}^* - i_{NP}(v_{0b,h}^*)}{i_{NP}(v_{0b,h+1}^*) - i_{NP}(v_{0b,h}^*)} \quad (11)$$

For the three-phase case, this coincides to the method proposed in [38] with the so-called "Precise Calculation Algorithm".

A qualitative picture of these two approaches is shown in Fig. 3, where the piece-wise linear function $i_{NP}(v_0^*)$ is compared with the desired reference i_{NP}^*. The common mode voltages selected by both (10) and (11) are clearly denoted.

The common mode injection based algorithms allow to keep number of switching transitions low and, therefore, the corresponding losses. However, from the NP voltage control perspective, they perform poorly in case of high modulation indexes, where the feasible common mode voltage injection interval $[v_{0,\min}^*, v_{0,\max}^*]$ is narrow. This effect is critical in case of low power factor operations (i.e. dominant reactive effect) [37-38] or for unbalanced loads [7].

C. *Multi-Step Switching Mode Based Techniques*

As discussed in Section I, a different approach involves the exploitation of the multi-step switching mode to control the NP voltage [43-50]. These techniques modify the gain factors α_k and require several modulation signals, corresponding to the duty-cycles of each device: therefore, standard single-reference multi-carriers approaches cannot be used. The choice of which phases to be used in the MS mode (i.e. which α_k to be different from 1) defines the different approaches. The common mode reference voltage v_0^* is not exploited for equalization purposes in these algorithms and is chosen by other criteria.

In [43] the common mode reference voltage is obtained by the min-max injection criterion given by (9). Then, a recursive method is performed to choose the minimum number of phases needed to switch in MS mode to get closer to the NP current reference (because more legs in MS mode means higher switching losses). In particular, by starting with all the legs in SS mode, the algorithm selects at each iteration one extra leg to switch in MS mode until either the corresponding NP current intersects the reference or it is able to affect the voltages in the desired direction with an acceptable slope (i.e. without exceeding the reference NP current magnitude).

The reduction of one or more gain factors (i.e. exploiting the MS mode) modifies the shape of the functional relation between the NP current and the common mode voltage. This can be graphically interpreted with the example given in Fig. 4. The original function (obtained with all legs in SS mode) $i_{NP,SS}(v_0^*)$ can be modified by reducing one gain factor α_m up to the function $i_{NP,TL}(v_0^*)$, obtained when the selected m-th NPC leg is in TL mode. The optimal gain factor is obtained when the function intersects the reference i_{NP}^* with the chosen voltage $v_0^* = v_{0,avg}^*$; the corresponding function is $i_{NP,MS}(v_0^*)$.

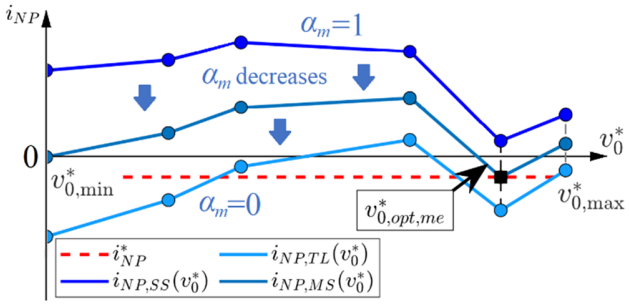

Fig. 5. Neutral point current modification through the proposed hybrid method: $i_{NP,SS}$ (SS Mode), $i_{NP,TL}$ (TL Mode), $i_{NP,MS}$ (Optimal MS Mode).

The MS based algorithms are always capable of guaranteeing the desired control over the NP voltage, but usually introduce many switching transitions, thus reducing the efficiency of the converter and worsening the output voltage harmonic content, especially for low power factor operations.

D. *Proposed Hybrid Technique*

A proper combination of a common mode voltage injection and multi-step operation can allow to take advantage of their main benefits, while partially neutralizing their respective drawbacks. The proposed hybrid technique, by controlling both v_0^* and α_k, is aimed to seek the desired reference NP current while keeping the average switching frequency low.

The proposed algorithm starts with all the legs in SS mode (i.e. $\alpha_k = 1$) and, by using the same reasoning as in [38], examines all the breaking points of $i_{NP}(v_0^*)$, looking for an intersection with the reference value i_{NP}^*. If an intersection is found, the optimal common mode voltage injection is found by applying (11), thus behaving like in Fig. 4. In case that there is no intersection, the algorithm evaluates the NP current function in correspondence to the clamping voltage $v_{0,opt,me}^*$ given by (10), which guarantees the minimum distance from the reference NP current i_{NP}^*. If the corresponding NP current $i_{NP,me} = i_{NP}(v_{0,opt,me}^*)$ affects the DC-bus voltages in the desired way and with an acceptable slope (i.e. when either $0 < i_{NP,me} \le i_{NP}^*$ or $i_{NP}^* \le i_{NP,me} < 0$), the algorithm identifies a *Natural Balancing Mechanism* and stops. If natural balancing is not identified, it is necessary to start modulating at least one leg in MS mode. As shown in [52], no more than one leg is needed to work in MS mode for a three-phase converter; neverthless this is not the case for a multiphase system. Therefore, an iterative algorithm is executed to identify the phases needed to be modulated in MS mode. Only one extra phase to be operated in MS mode is selected in each iteration and it is chosen according to the effect of the corresponding NP current on the DC-bus voltages:

- if the NP voltage is to evolve in the wrong direction (i.e. $i_{NP,me}$ and i_{NP}^* have the opposite sign), the selected phase is the most unbalancing one;
- if the NP voltage is to evolve in the correct direction, but with

an excessive slope (i.e. $i_{NP,me}$ and i^*_{NP} have the same sign, but $|i_{NP,me}| > |i^*_{NP}|$), the selected phase is the most balancing one.

The most balancing/unbalancing phase can be found from (7) by identifying the highest or lowest value among all the NP currents $i_{NP,k} = i_k \cdot d_{NP,\max}(\tilde{v}^*_k + v^*_{0,opt,me})$.

By denoting with m the leg selected to work in MS mode, the corresponding gain factor is found as:

$$\alpha_m = 1 - (i_{NP,me} - i^*_{NP})/i_{NP,m} \tag{12}$$

If $\alpha_m < 0$ in (12), it means that the choice of single leg to operate in MS mode is not enough to guarantee the desired current. Then, the algorithm sets α_m to 0 (i.e. the m-th phase works in TL mode) and the iterative procedure is repeated with a new search of the minimum error breaking point and with the selection of another phase to operate in MS mode. A qualitative effect of this method onto the $i_{NP}(v^*_0)$ waveform is shown in Fig. 5 to allow a graphical interpretation.

At the end of this procedure, the algorithm has selected both the common mode voltage reference v^*_0 and the gain factors α_k for all phases. Then, both the leg voltage reference v^*_k and the NP-duty cycle $d_{NP,k}$ are uniquely determined for each k-th NPC leg and the corresponding top/bottom device's duty-cycles are evaluated by substituting (4) and (6) in (2), resulting in:

$$\begin{aligned} d_{T,k} &= [(\tilde{v}^*_k + v^*_0) - v_{DC,B} \cdot \alpha_k \cdot d_{NP,\max}(\tilde{v}^*_k + v^*_0)]/v_{DC} \\ d_{B,k} &= [(\tilde{v}^*_k + v^*_0) + v_{DC,T} \cdot \alpha_k \cdot d_{NP,\max}(\tilde{v}^*_k + v^*_0)]/v_{DC} \end{aligned} \tag{13}$$

The flowchart of the proposed strategy is illustrated in Fig. 6. First, $v^*_{0,\min}$ and $v^*_{0,\max}$ are found by (8): they represent the extreme clamping voltages for v^*_0. Then, the internal clamping voltages are found by setting $v^*_k = \tilde{v}^*_k + v^*_0 = v_{DC,B}$ (for each k-th converter's leg) and by verifying that the resulting common mode voltage is included in $[v^*_{0,\min},\ v^*_{0,\max}]$. The gain factors α_k are initialized to 1 and NP current is evaluated via (7) and compared to the reference value i^*_{NP} for each breaking point. If an intersection is possible (i.e. the error function has at least one zero-crossing point), the optimal common mode voltage is found via (11), otherwise the MS iterative cycle is executed until either it is possible to impose $i_{NP} = i^*_{NP}$ (by reducing one or more gain factors α_k) or a natural balancing mechanism is recognized. Finally, the top/bottom devices' duty cycles are found by (13) and compared to the common triangular carrier signal σ_c (which is in range from 0 to 1). From the computational point of view, the NP current evaluation at the breaking points can be performed in a faster way by storing the NP current contributions $i_k \cdot d_{NP,\max}(\tilde{v}^*_k + v^*_{0b,h})$ in a $M \times (M+2)$ matrix at the beginning of each modulation interval.

With respect to the sole exploitation of the common mode voltage, the proposed technique can overcome the limitations existing in case of high modulation indexes. With respect to the sole exploitation of the multi-step switching mode, the automatic choice of the optimal common mode voltage can ensure faster control with less switching transitions.

Moreover, since $i_{NP}(v^*_0)$ is always a piece-wise linear function, when the MS mode is activated, the simultaneous common mode voltage injection automatically chooses v^*_0 among its breaking points, leading to a voltage clamping for one of the converter's legs. The clamped leg does not bring any switching transition and mitigates the increase of the switching losses caused by the MS mode. Given this property, some enhanced DPWM techniques can be conceived as special cases of the proposed approach. As an example, the technique proposed in [52] for three-phase converters can be obtained by discarding the error cancellation algorithm (11) in case of SS mode and by imposing $i^*_{NP} = 0$ for MS mode operations.

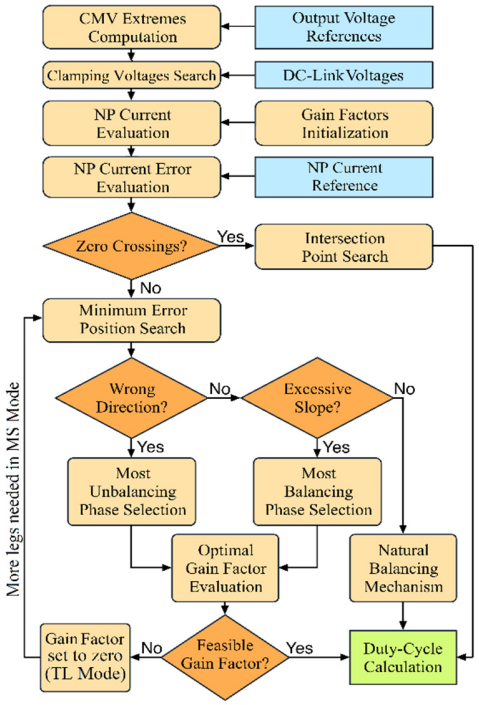

Fig. 6. Flowchart of the proposed hybrid modulation technique.

IV. Numerical and Experimental Results

The proposed modulation technique has been validated experimentally on a custom-made multiphase NPC prototype. To highlight its effectiveness, the approach has been compared with the modulation techniques proposed in [38] and in [43], (which can be respectively considered as the state-of-the-art techniques based on the sole CMI or on the sole MS mode) and with a standard carrier-based PWM (CBPWM) technique, which does not actively address the NP voltage control.

The converter is based on Semikron SKM50GB12T4 modules. The switching frequency has been chosen to be 2 kHz, while the dead time for the semiconductor switching transitions has been set in hardware to 6 µs. Both the top and the bottom DC capacitances have been set to 300 µF and realized through the parallel connection of three Kemet C4AE polypropylene capacitors. The overall converter DC voltage has been supplied through a Sorensen SGI 600/25 and stabilized to 300 V.

All the modulation techniques have been implemented on a dSpace ds1006 platform with a 2 kHz sampling rate, while the measurements have been recorded through a Tektronix DPO/MSO 2014 oscilloscope. As in [52], the NP current reference i^*_{NP} has been set through a feedback predictive controller acting on the voltage unbalance $(v_{DC,T} - v_{DC,B})$.

Several tests have been performed in different scenarios. For each test, the displayed waveforms are the bottom and the top DC-bus voltage ($v_{DC,B}$ and $v_{DC,T}$, in light blue and

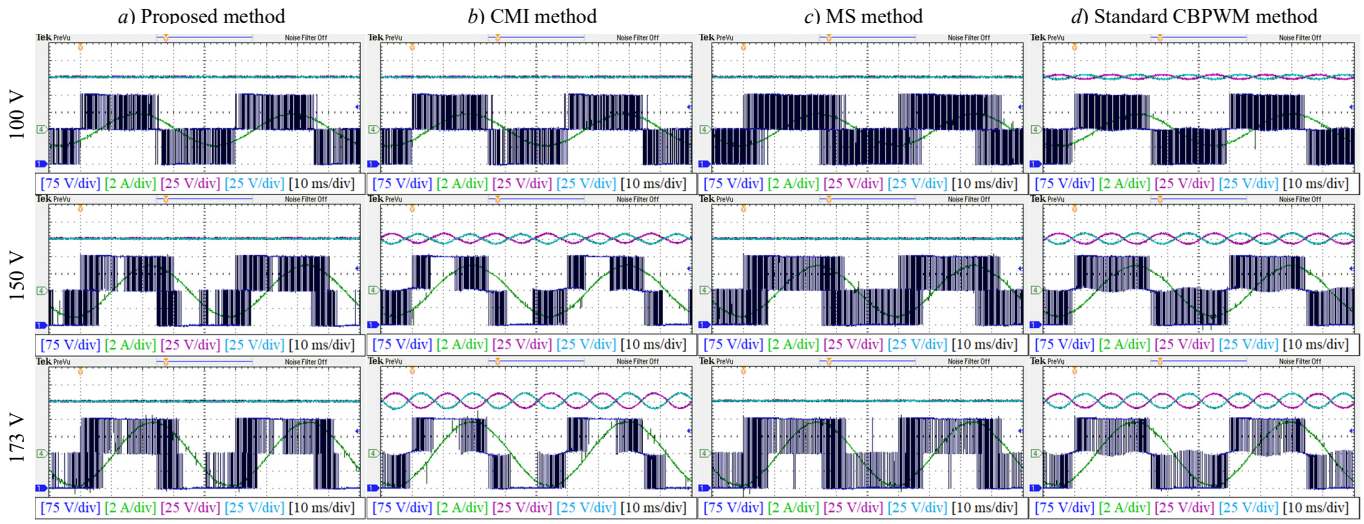

Fig. 7. Steady state results on the symmetrical three-phase system (RL load; 20 Hz).

magenta, respectively) and the 1st converter's leg voltage and current (v_1 and i_1, in dark blue and green, respectively).

A. Steady State Behavior for Three-Phase RL Load

The test has been performed by supplying a set of symmetrical and sinusoidal voltage references to a balanced three-phase ohmic-inductive load with $R \approx 20\ \Omega$ and $L \approx 360$ mH. To better highlight the NP voltage fluctuation the supply frequency has been set to 20 Hz. To consider different operating conditions the magnitude of the phase voltage references $\tilde{v}_k^*$ has been set to 100 V (i.e. below $v_{DC}/2$), to 150 V (i.e. equal to $v_{DC}/2$) and to 173.3 V (i.e. equal to $v_{DC}/\sqrt{3}$). By defining the modulation index M_{ind} as the ratio between the peak reference voltage and $v_{DC}/2$, the testing scenarios correspond to modulation index values of 0.66, 1.00 and 1.15. The results are shown in Fig. 7. Table II summarizes the average number of switching transitions per leg in one fundamental period.

For the test at 100 V it can be easily noted that all the techniques, with the only exception of the standard CBPWM, are able to suppress the NP voltage ripple. In this context, given the sufficient range of the v_0^* feasibility interval, the proposed approach does not need to operate in MS mode and applies the same leg output voltages as CMI method proposed in [38]. Both methods show fewer switching transitions than the pure MS based technique described in [43] (about 25% less, Table II).

When the reference voltage is 150 V, the feasibility interval for the CMI is narrow and the technique of [38] is unable to suppress the NP voltage fluctuation, whose magnitude is only slightly lower than the corresponding fluctuation obtained with the standard CBPWM method. On the other hand, the MS approaches (including the proposed one) are able to keep the DC-bus voltages equalized. It can be easily observed that, for the proposed approach, the CMI makes it possible to exploit the multi-step operation for reduced amount of time when compared to the pure MS based approach. Moreover, the clamping of the leg voltage to the DC rails further reduces the number of switching transitions (about 22% less, Table II).

A similar behaviour can be seen when the reference voltages are set to 173.3 V. Again, CBPWM and pure CMI based modulation perform poorly, while the proposed technique is able to suppress the NP voltage ripple with fewer transitions than the pure MS based approach (about 22% less, Table II).

A comparison of the estimated switching losses obtained with the proposed algorithm and with the MS based approach (which are the only methods always able to perform the NP voltage control) is shown in Fig. 8. The comparison is provided for different values of the modulation index M_{ind} and for different load power factor angles φ. The losses have been estimated through numerical simulations by assuming a linear evolution of the transistor's voltage and currents during each switching transition. Results have been averaged over 30 periods of the 20 Hz fundamental frequency.

TABLE II. AVERAGE NUMBER OF SWITCHING TRANSITIONS IN THE STEADY STATE TEST FOR THE THREE-PHASE RL LOAD

[V]/[Hz]	Proposed method	CMI method	MS method	Standard CBPWM
100/20	199	201	267	198
150/20	207	140	266	198
173/20	211	135	272	198

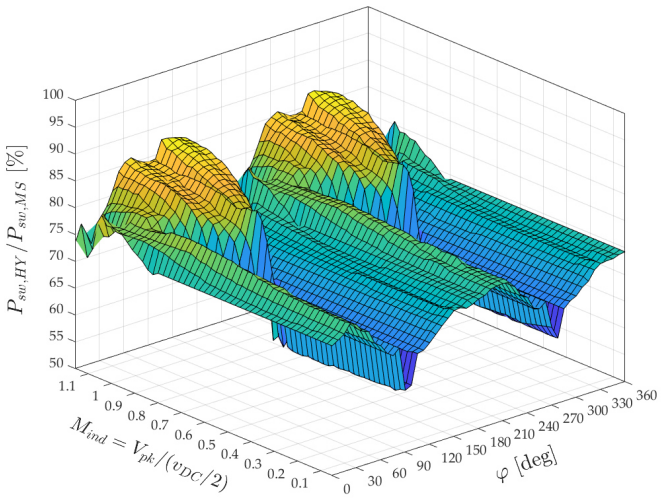

Fig. 8. Ratio between the estimated switching losses with the proposed hybrid algorithm and with the pure MS algorithm.

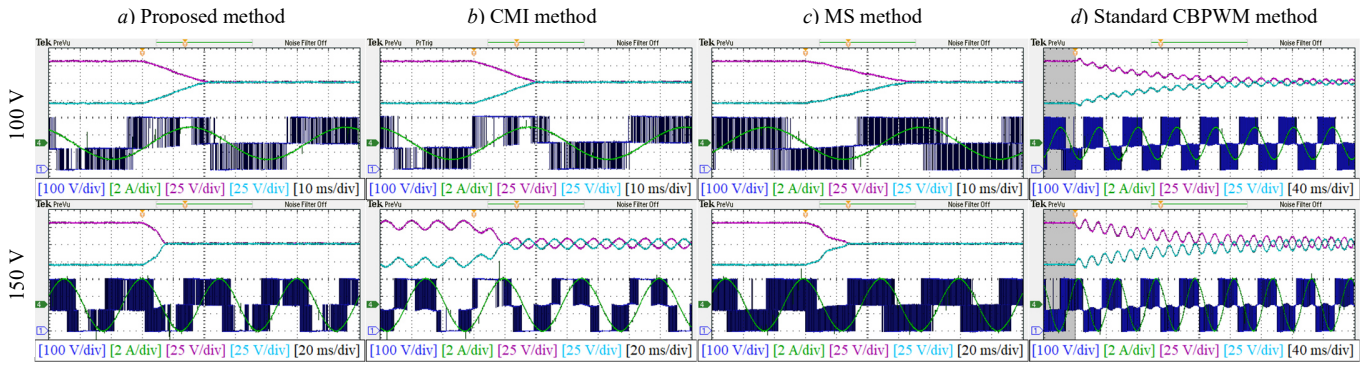

Fig. 9. Transient results on the symmetrical three-phase system (RL load; 20 Hz).

As can be noted, the estimated losses with the proposed algorithm are always lower than 90% of the ones obtained with the MS approach. For high power factor loads (i.e. when φ=0° and φ=180°) the losses ratio is around 75% for the whole range of M_{ind}. On the contrary, when the load is prevalently reactive (i.e. φ=90° and φ=270°) the losses have the lowest ratios for low modulation indexes (around 60% up to $M_{ind} = 0.6$) and the highest ratios for high modulation indexes (around 85%).

For the experimental results depicted in Fig. 7, the load power factor angle is always $\varphi \approx 66°$ and the power losses ratios have been found to be $P_{sw,HY}/P_{sw,MS} \approx 73\%$ for the 100 V test ($M_{ind} \approx 0.66$), $P_{sw,HY}/P_{sw,MS} \approx 84\%$ for the 150 V test ($M_{ind} \approx 1.00$) and $P_{sw,HY}/P_{sw,MS} \approx 83\%$ for the 173 V test ($M_{ind} \approx 1.15$), thus matching the numerical results.

B. *Transient Behavior for Three-Phase RL Load*

Again, the test has been performed by supplying a set of symmetrical and sinusoidal voltage references with both 100 V and 150 V peak amplitude to the balanced three-phase load of the previous test. Each controller is initially driven to set $v_{DC,B}$ to the 40% of the total DC-bus voltage and is then switched to the equalization mode. Since the standard CBPWM cannot control $v_{DC,B}$, the initial asymmetry is forced through the pure MS based approach of [43] (the grey shaded area in Fig. 9d). After 40 ms the mode is changed from MS to CBPWM. The results are shown in Fig. 9.

For the 100 V test it is easy to notice the similarity between the pure CMI based and the proposed method, which complete the equalization in a 20 ms time window. The pure MS based approach performs more slowly due to the natural balancing mechanism recognition, which tends to avoid the multi-step behaviour when it is not needed. The standard CBPWM evolves towards the equalized state in almost 360 ms and, as in the previous test, exhibits a superimposed NP ripple.

The 150 V test again highlights the main differences between the different approaches. As in the previous scenario, the pure CMI based technique suffers with NP voltage ripple, which is present both with the unbalanced and with the balanced DC-bus capacitors. This effect is completely absent in the other active balancing modulation techniques. The proposed approach is faster than the one given in [43] due to the exploitation of a proper CMI.

C. *Steady State Behavior for Five-Phase Induction Machine*

The test has been performed by supplying a set of symmetrical and sinusoidal voltage references to a custom-made five-phase induction machine working at no load. Its electrical parameters are summarized in Table III.

TABLE III. FIVE-PHASE INDUCTION MACHINE'S PARAMETERS

Parameter	*Symbol*	*Value*
No. of pole pairs	P	2
Stator resistance	R_s	0.75 Ω
Rotor resistance	R'_r	0.75 Ω
Stator leakage inductance	L_{ls}	11.25 mH
Rotor leakage inductance	L'_{lr}	3.75 mH
Magnetizing inductance	L_m	128.75 mH

TABLE IV. AVERAGE NUMBER OF SWITCHING TRANSITIONS IN THE STEADY STATE TEST FOR THE FIVE-PHASE INDUCTION MACHINE

[V]/[Hz]	Proposed method	CMI method	MS method	Standard CBPWM
100/33.3	110	112	138	120
150/50	81	64	98	83
158/52.5	77	63	84	76

The machine has been supplied in *V/f* mode in three different conditions. The results are depicted in Fig. 10 and the number of switching transitions per fundamental period of the examined converter leg are summarized in Table IV.

The presence of more phases in a symmetrical configuration contributes to a reduction of the NP voltage fluctuation with respect to the three-phase scenario (note that in Fig. 10 for DC-bus voltages, only the ripple is shown, and the scale is set to 1 V/div). Again, the peculiar properties of each method are evident from the leg voltage waveforms.

For the 100 V/33.3 Hz test the proposed method performs similarly to the CMI based one, while the effect of the multi-step behaviour of the technique proposed in [43] is evident in the leg voltage waveform. All the techniques are able to guarantee a NP peak-to-peak voltage ripple of about 1.5 V, but the MS approach has about 20% more transitions (Table IV). For both the 150 V/50 Hz and the 158 V/52.5 Hz scenarios, the pure CMI based technique shows a slightly higher fluctuation due to the reduced feasibility interval for v_0^*. The proposed approach introduces a MS behaviour and performs similarly to the technique proposed in [43], but with less switching transitions (about 17% and 8% less, respectively; Table IV). This is due to the simultaneous action of the CMI, which clamps the leg voltage to the negative DC-bus rail for a longer interval.

D. *Transient Behavior for Five-Phase Induction Machine*

This test has been performed for a single scenario, with the reference voltages set to 150 V (peak), 50 Hz. Similarly to the corresponding three-phase test, the control commences the equalization process starting from an unbalanced DC bus (with

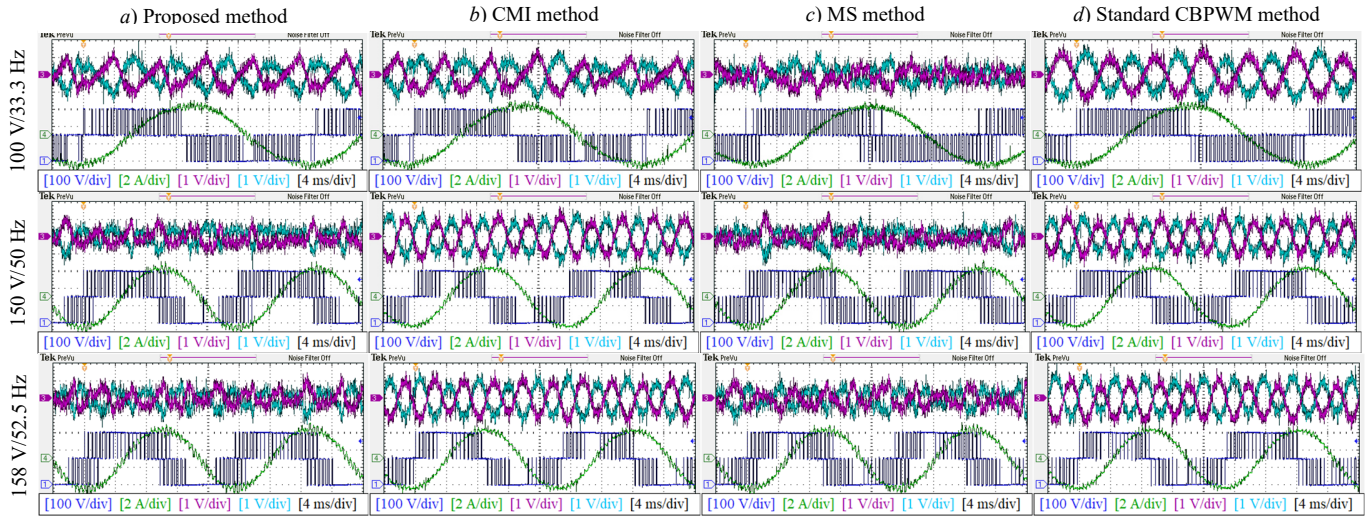

Fig. 10. Steady state results on the symmetrical five-phase system (induction machine; *V/f* control).

$v_{DC,B} = 40\% \cdot v_{DC}$). The results are depicted in Fig. 11.

As can be easily observed, both the proposed and the pure MS method are able to perform the equalization within 15 ms, while the pure CMI based technique needs almost 120 ms due to the narrow feasibility interval of v_0^*. Note the difference in the time scale in Fig. 10 sub-plots. Given the symmetrical load, the standard CBPWM naturally evolves towards the equalization, but in a longer time window (more than 1 s).

E. Steady State for Unbalanced Five-Phase Induction Machine

Finally, the capabilities of the methods have been studied for an asymmetrical load. To obtain the asymmetry an external 5 Ω resistor has been connected in series to the fifth phase, thus making the machine electrically unbalanced. The references were set again to 150 V/50 Hz. The results are shown in Fig. 12 and the corresponding average number of switching transitions per period are summarized in Table V.

As evident, this condition shows a significantly higher NP voltage fluctuation if compared to the balanced load (note that the scaling for $v_{DC,B}$ and $v_{DC,T}$ is now set to 5 V/div). Standard CBPWM shows the highest peak-to-peak voltage deviation (of about 10 V). The CMI based technique, given the high modulation index, is unable to suppress this ripple and behaves poorly. On the contrary, the other two approaches guarantee the equalization and, as expected, the proposed technique operates with fewer switching transitions (about 11% less, Table V) due to the leg voltage clamping allowed by v_0^*.

TABLE V. AVERAGE NUMBER OF SWITCHING TRANSITIONS IN THE STEADY STATE TEST FOR THE UNBALANCED FIVE-PHASE INDUCTION MACHINE

[V]/[Hz]	Proposed method	CMI method	MS method	Standard CBPWM
150/50	91	53	102	80

V. CONCLUSIONS

The paper presented a carrier-based pulse width modulation technique for multiphase neutral point clamped converters with the DC-bus NP voltage control capability. The proposed strategy exploits all the available degrees of freedom of the system and optimally combines two standard approaches for this kind of control. Those standard approaches are either based on the sole injection of a proper common mode signal into the leg voltage references or on the sole multi-step working principle. The proposed approach guarantees the desired control in all the converter's working conditions, including high modulation indexes and unbalanced loads. It follows an iterative procedure aimed to reduce the switching transition

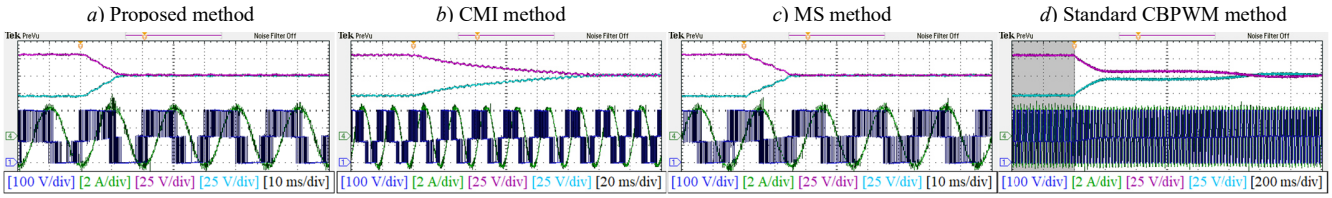

Fig. 11. Transient results on the symmetrical five-phase system (induction machine; 150 V / 50 Hz).

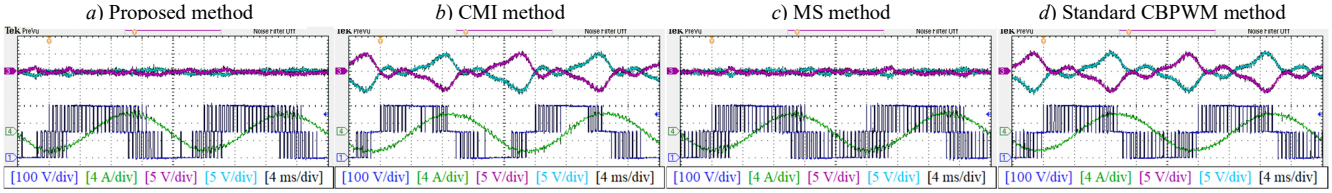

Fig. 12. Steady state results on the unbalanced five-phase system (induction machine with external resistor in phase 5; 150 V / 50 Hz).

rate, and hence the corresponding switching losses. The approach has been experimentally tested on a three-phase and on a five-phase test-bench and compared with some other techniques available in the technical literature. The results show satisfactory behaviour in all the testing scenarios and the proposed method is especially suited for high modulation indexes. It combines the benefits of both degrees of freedom for capacitors voltage balancing (CMI and MS operation) resulting in faster transient responses and in reduced transition rates.

REFERENCES

[1] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, Aug. 2002.

[2] S. Alepuz, S. Busquets-Monge, J. Bordonau, J. Gago, D. Gonzalez, and J. Balcells, "Interfacing renewable energy sources to the utility grid using a three-level inverter," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, Oct. 2006.

[3] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage,'' *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, Oct. 2006.

[4] G. Brando, A. Dannier, A. Del Pizzo, L. P. Di Noia, I. Spina, "Quick and high performance direct power control for multilevel voltage source rectifiers", *Electr. Pow. Sys. Res.*, vol. 121, Apr. 2015.

[5] A. Nabae, I. Takahashi and H. Akagi, "A New Neutral-Point-Clamped PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, Sep. 1981.

[6] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source PWM inverters," *IEEE Trans. Pow. Electron*., vol. 15, no. 2, Mar. 2000.

[7] J. Pou, D. Boroyevich and R. Pindado, "Effects of imbalances and nonlinear loads on the voltage balance of a neutral-point-clamped inverter," *IEEE Trans. Pow. Electron.*, vol. 20, no. 1, Jan. 2005.

[8] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: theory, design and operational limitations," IAS '97. *Thirty-Second IEEE Ind. Appl. Conf. (IAS '97)*, Oct. 1997.

[9] R. Stala, "A Natural DC-Link Voltage Balancing of Diode-Clamped Inverters in Parallel Systems," *IEEE Trans. Ind. Electron.*, vol. 60, no. 11, Nov. 2013.

[10] A. Ajami, H. Shokri and A. Mokhberdoran, "Parallel switch-based chopper circuit for DC capacitor voltage balancing in diode-clamped multilevel inverter," *IET Pow. Electron.*, vol. 7, no. 3, Mar. 2014.

[11] Z. Shu, X. He, Z. Wang, D. Qiu and Y. Jing, "Voltage Balancing Approaches for Diode-Clamped Multilevel Converters Using Auxiliary Capacitor-Based Circuits," *IEEE Trans. Pow. Electron.*, vol. 28, no. 5, May 2013.

[12] R. Stala, "Application of Balancing Circuit for DC-Link Voltages Balance in a Single-Phase Diode-Clamped Inverter With Two Three-Level Legs," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, Sep. 2011.

[13] B. Wu, "High-Power Inverters and AC Drives", John Wiley & sons, Inc., NJ, USA, 2006.

[14] S. A. Gonzalez, S. A. Verne, M. I. Valla, "Multilevel converters for industrial applications", CRC Press, 2013.

[15] M. Sharifzadeh, H. Vahedi, A. Sheikholeslami, P. Labbé and K. Al-Haddad, "Hybrid SHM–SHE Modulation Technique for a Four-Leg NPC Inverter With DC Capacitor Self-Voltage Balancing," *IEEE Trans. Ind. Electron.*, vol. 62, no. 8, Aug. 2015.

[16] X. Zhang and W. Yue, "Neutral point potential balance algorithm for three-level NPC inverter based on SHEPWM," *Electron. Letters*, vol. 53, no. 23, Nov. 2017.

[17] P. Kant and B. Singh, "Multi-pulse AC–DC converter fed SVM controlled NPC inverter based VCIMD," *IET Pow. Electron.*, vol. 11, no. 14, Nov. 2018.

[18] L. Lin, Y. Zou, Z. Wang and H. Jin, "Modeling and Control of Neutral-point Voltage Balancing Problem in Three-level NPC PWM Inverters," *IEEE 36-th Pow. Electron. Specialists Conf. (PESC 2005)*, Jun. 2005.

[19] F. Sebaaly, H. Vahedi, H. Y. Kanaan, N. Moubayed and K. Al-Haddad, "Design and Implementation of Space Vector Modulation-Based Sliding Mode Control for Grid-Connected 3L-NPC Inverter," *IEEE Trans. Ind. Electron.*, vol. 63, no. 12, Dec. 2016.

[20] Z. Ye, Y. Xu, X. Wu, G. Tan, X. Deng and Z. Wang, "A Simplified PWM Strategy for a Neutral-Point-Clamped (NPC) Three-Level Converter with Unbalanced DC Links," *IEEE Trans. Pow. Electron.*, vol. 31, no. 4, Apr. 2016.

[21] H. Zhang, S. Jon Finney, A. Massoud and B. Wayne Williams, "An SVM Algorithm to Balance the Capacitor Voltages of the Three-Level NPC Active Power Filter," *IEEE Trans. Pow. Electron.*, vol. 23, no. 6, Nov. 2008.

[22] Z. Wang, J. Chen, M. Cheng and Na Ren, "Vector space decomposition based control of neutral-point-clamping (NPC) three-level inverters fed dual three-phase PMSM drives," *42nd Annual Conf. of the IEEE Ind. Electron. Soc. (IECON 2016)*, Oct. 2016.

[23] Y. Jiao, F. C. Lee and S. Lu, "Space Vector Modulation for Three-Level NPC Converter With Neutral Point Voltage Balance and Switching Loss Reduction," *IEEE Trans. Pow. Electron.*, vol. 29, no. 10, Oct. 2014.

[24] D. Zhou and D. G. Rouaud, "Experimental comparisons of space vector neutral point balancing strategies for three-level topology," *IEEE Trans. Pow. Electron.*, vol. 16, no. 6, Nov. 2001.

[25] A. Choudhury, P. Pillay and S. S. Williamson, "DC-Link Voltage Balancing for a Three-Level Electric Vehicle Traction Inverter Using an Innovative Switching Sequence Control Scheme," *IEEE Journal of Emerging and Selected Topics in Pow. Electr.,* vol. 2, no. 2, Jun. 2014.

[26] H. Vahedi, P. Labbe and K. Al-Haddad, "Balancing three-level neutral point clamped inverter DC bus using closed-loop space vector modulation: real-time implementation and investigation," *IET Pow. Electron.*, vol. 9, no. 10, Aug. 2016.

[27] L. Gao and J. E. Fletcher, "A Space Vector Switching Strategy for Three-Level Five-Phase Inverter Drives," *IEEE Trans. Ind. Electron*., vol. 57, no. 7, pp. 2332-2343, July 2010.

[28] S. Busquets-Monge, J. Bordonau, D. Boroyevich and S. Somavilla, "The nearest three virtual space vector PWM - a modulation for the comprehensive neutral-point balancing in the three-level NPC inverter," *IEEE Pow. Electr. Letters*, vol. 2, no. 1, pp. 11-15, March 2004.

[29] S. Busquets Monge, S. Somavilla, J. Bordonau and D. Boroyevich, "Capacitor Voltage Balance for the Neutral-Point- Clamped Converter using the Virtual Space Vector Concept With Optimized Spectral Performance," *IEEE Trans. Pow. Electron.*, vol. 22, no. 4, pp. 1128-1135, July 2007.

[30] X. Wu, G. Tan, Z. Ye, G. Yao, Z. Liu and G. Liu, "Virtual-Space-Vector PWM for a Three-Level Neutral-Point-Clamped Inverter With Unbalanced DC-Links," *IEEE Trans. Pow. Electron.*, vol. 33, no. 3, pp. 2630-2642, March 2018.

[31] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. Ind. Electron*., vol. 55, no. 5, May 2008.

[32] G. Grandi, G. Serra, and A. Tani, "General analysis of multi-phase system based on space vector approach," *Pow. Electron. and Motion Control Conf. (EPE-PEMC 2006)*, Aug. 2006.

[33] M. Jones, O. Dordevic, N. Bodo, and E. Levi, "PWM algorithms for multilevel inverter supplied multiphase variable-speed drives," *Electronics*, vol. 16, no. 1, Jun. 2012.

[34] O. Dordevic, E. Levi, and M. Jones, "A vector space decomposition based space vector PWMalgorithm for a three-level seven-phase voltage source inverter," *IEEE Trans. Ind. Electron.*, vol. 28, no. 2, Feb. 2013.

[35] O. Dordevic, M. Jones and E. Levi, "A Comparison of Carrier-Based and Space Vector PWM Techniques for Three-Level Five-Phase Voltage Source Inverters," *IEEE Trans. Ind. Informatics*, vol. 9, no. 2, May 2013.

[36] J. Pou, J. Zaragoza, S. Ceballos, M. Saeedifard and D. Boroyevich, "A Carrier-Based PWM Strategy With Zero-Sequence Voltage Injection for a Three-Level Neutral-Point-Clamped Converter," *IEEE Trans. Pow. Electron.*, vol. 27, no. 2, Feb. 2012.

[37] I. López, S. Ceballos, J. Pou, J. Zaragoza, J. Andreu, E. Ibarra and G. Konstantinou, "Generalized PWM-Based Method for Multiphase Neutral-Point-Clamped Converters With Capacitor Voltage Balance Capability," *IEEE Trans. Pow. Electron.*, vol. 32, no. 6, Jun. 2017

[38] C. Wang and Y. Li, "Analysis and Calculation of Zero-Sequence Voltage Considering Neutral-Point Potential Balancing in Three-Level NPC Converters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, Jul. 2010.

[39] J. Chivite-Zabalza, P. Izurza-Moreno, D. Madariaga, G. Calvo and M. A. Rodríguez, "Voltage Balancing control in 3-Level Neutral-Point Clamped Inverters Using Triangular Carrier PWM Modulation for FACTS Applications," *IEEE Trans. Pow. Electron.*, vol. 28, no. 10, Oct. 2013.

[40] H. Akagi and T. Hatada, "Voltage Balancing Control for a Three-Level Diode-Clamped Converter in a Medium-Voltage Transformerless Hybrid Active Filter," *IEEE Trans. Pow. Electron.*, vol. 24, no. 3, Mar. 2009.

[41] H. Akagi and R. Kondo, "A Transformerless Hybrid Active Filter Using a Three-Level Pulsewidth Modulation (PWM) Converter for a Medium-Voltage Motor Drive," *IEEE Trans. Pow. Electron.*, vol. 25, no. 6, Jun. 2010.

[42] J. Lee, S. Yoo and K. Lee, "Novel Discontinuous PWM Method of a Three-Level Inverter for Neutral-Point Voltage Ripple Reduction," in *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3344-3354, June 2016.

[43] I. López, S. Ceballos, J. Pou, J. Zaragoza, J. Andreu, I. Kortabarria and V. G. Agelidis, "Modulation Strategy for Multiphase Neutral-Point-Clamped Converters," *IEEE Trans. Pow. Electron.*, vol. 31, no. 2, Feb. 2016

[44] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, C. Jaen and M. Corbalan, "Voltage-Balance Compensator for a Carrier-Based Modulation in the Neutral-Point-Clamped Converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, Feb. 2009.

[45] J. Zaragoza, J. Pou, S. Ceballos, E. Robles, P. Ibanez, and J. Villate, "A comprehensive study of a hybrid modulation technique for the neutralpoint-clamped converter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 2, Feb. 2009.

[46] J. Pou, J. Zaragoza, P. Rodriguez, S. Ceballos, V. M. Sala, R. P. Burgos and D. Boroyevich, "Fast-Processing Modulation Strategy for the Neutral-Point-Clamped Converter With Total Elimination of Low-Frequency Voltage Oscillations in the Neutral Point," *IEEE Trans. Ind. Electron.*, vol. 54, no. 4, Aug. 2007.

[47] C. Wang, Z. Li, X. Si and H. Xin, "Control of neutral-point voltage in three-phase four-wire three-level NPC inverter based on the disassembly of zero level," *IEEE Energy Conv. Congr. and Exp. (ECCE 2016)*, Sep. 2016.

[48] H. Chen, M. Tsai, Y. Wang and P. Cheng, "A novel neutral point potential control for the three-level neutral-point-clamped converter," *IEEE Energy Conv. Congr. and Exp. (ECCE 2016)*, Sep. 2016.

[49] F. Luo, K. Loo and Y. Lai, "Simple carrier-based pulse-width modulation scheme for three-phase four-wire neutral-point-clamped inverters with neutral-point balancing," *IET Pow. Electron.,* vol. 9, no. 2, Feb. 2016.

[50] W. Jiang, X. Huang, J. Wang, J. Wang and J. Li, "A Carrier-Based PWM Strategy Providing Neutral-Point Voltage Oscillation Elimination for Multi-Phase Neutral Point Clamped 3-Level Inverter," *IEEE Access*, vol. 7, pp. 124066-124076, 2019.

[51] K. Chen, W. Jiang and P. Wang, "An Extended DPWM Strategy With Unconditional Balanced Neutral Point Voltage for Neutral Point Clamped Three-Level Converter," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8402-8413, Nov. 2019.

[52] A. Cervone, G. Brando and O. Dordevic, "A Hybrid Modulation Technique for the DC-Bus Voltage Balancing in a Three-Phase NPC Converter," *45th Ann. Conf. of IEEE Ind. Electron. Soc. (IECON 2019)*, Oct. 2019

Andrea Cervone (Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering in 2014 and 2017, respectively, from the University of Naples Federico II, Naples, Italy, where he is currently working toward the Ph.D. degree in electrical engineering. His research interests include multilevel converters and electrical drives.

Gianluca Brando received the M.S. (cum laude) and Ph.D. degrees in electrical engineering from the University of Naples Federico II, Naples, Italy, in 2000 and 2004. From 2000 to 2012, he was a Postdoctoral Research Fellow with the Department of Electrical Engineering, University of Naples Federico II. Since 2012, he is an Assistant Professor of Electrical Machines and Drives with the Department of Electrical Engineering and Information Technology, University of Naples Federico II. He has authored several scientific papers published in international journals and conference proceedings. His research interests include control strategies for power converters and electrical drives.

Obrad Dordevic (S'11, M'13) received his Dipl. Ing. degree in Electronic Engineering from the University of Belgrade, Serbia, in 2008. He joined Liverpool John Moores University in December 2009 as a PhD student. Dr. Dordevic received his PhD degree in April 2013 and was appointed as a Lecturer at the Liverpool John Moores University in May 2013. In 2018 he was promoted to a Reader in Power Electronics. His main research interests are in the areas of power electronics, electrostatic precipitators, and advanced variable speed multiphase drive systems.