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Investigation Into How the Floor Plan Layout of a Manufactured PCB Influences Flip-Chip Susceptibility to Vibration

Kangkana Baishya, David Mark Harvey, Guangming Zhang, and Derek Richard Braden

***Abstract*— This article investigates how floor plan layout of a printed circuit board (PCB) influences the reliability of the component's solder joint connections when operated in a vibrating environment. A random vibration profile as seen in an automotive environment was used in full lifetime tests. An industry-standard FR4 PCB with electroless nickel immersion gold (ENIG) surface finish was manufactured with double-sided component placement including 14 flip chips, eight on the top side and six on the bottom side. Ultrasound scans were used as a nondestructive test to assess the integrity of solder joints from manufacture to failure. This enabled monitoring of the important interface between solder joints and flip chip where failure mostly occurs. The initial failure pattern was found by experiment where 86 cycles of random vibration caused all flip chips to mechanically fail. Failure followed a Weibull probability with a value of $\beta = 1.297$, indicating that failure rates increase with time. The results show that the reliability of a flip chip varies with its position on a PCB with some marked differences to component lifetimes. The results also show that for two-sided flip-chip placements on a PCB, back-to-back, overlapped, and single-sided orientations have subtle effects on flip-chip lifetimes. Similarly, reliability varied with solder joint positions since joints on the sides of a flip chip nearest the PCB edges were less reliable than those on sides on a flip chip furthest away. Finally, design guidelines are offered to effect the most reliable flip-chip placement on a two-sided PCB when operated in a vibrating environment.**

***Index Terms*— Flip chip, floor plan layout, solder joint, vibration.**

I. Introduction

SOLDER joint fatigue failure under vibration loading has always been a great concern in the microelectronics industry. In automotive, aerospace, and military applications, electronic systems should be able to undergo various dynamic loads and vibration frequencies during their operation [1]–[4]. Vibration was identified to be one of the most important causes of electronic failure by the U.S. Air force [5] and solder interconnects usually are the weakest link in terms of product reliability [6]. Therefore, solder joint reliability testing is necessary to understand the effects of high-frequency vibration, particularly for any manufactured electronics that are prone to encounter harsh environments in practice [7]. Liu and Meng [8] studied the lead-free solder joint behavior of ball grid array (BGA) packages under different random vibration loadings and results showed that the corresponding failure modes were converted from ductile fracture to brittle fracture with the increase of vibration intensity. Wong [9] presented a methodology to characterize and predict fatigue failure of BGA package solder joints under vibration loading based on board strain versus number-of-cycles-to-failure (or *S–N*) curve. The comparison of SnAgCu and SnPb solders in fatigue curves clearly indicated the better performance of SnAgCu solder system under high-cycle fatigue test, while this trend was reversed in low-cycle fatigue where SnPb solder has superior fatigue resistance. Che and Pang [10] carried out some sinusoidal vibration reliability tests for flip-chip solder joints and applied a linear cumulative damage analysis method (Miner's rule) to predict the life of solder joints. However, none of these studies attempted to conduct real-time vibration tests or were able to monitor the exact dynamics of manufactured solder joint reliability. Solder joint reliability, which is greatly affected by the component's floor plan, the thickness of the printed circuit board (PCB), and the influence of the surrounding components [6], has never been fully studied before. A previous article has investigated the effects of floor plan layout on through-life PCB reliability when considering thermal cycling effects [11]. This article investigates the reliability of solder joints in flip chips through real-time vibration and a nondestructive solder joint health monitoring system using acoustic microimaging (AMI/C-SAM) that detects the changes in mechanical integrity in the solder joints in terms of the mean intensity of reflected ultrasound signals from a solder joint [12]. Finally, PCB floor plan design guidelines for the most secure flip-chip placement for systems working in a vibration environment are proposed, which will ensure better reliability and improved lifetimes of PCBs in a vibration environment.

II. Experimental Design

An industry-standard FR4 PCB of 0.8-mm board thickness (see Fig. 1) and a surface finish of electroless nickel immersion

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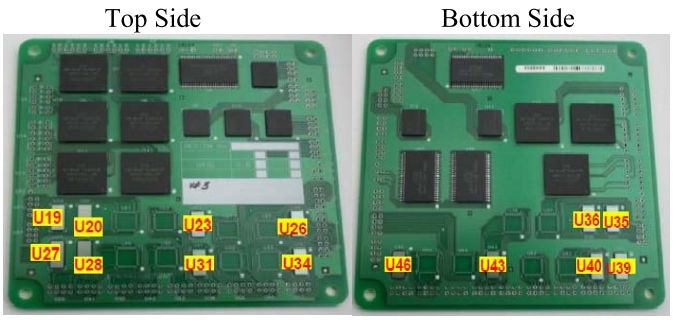

Fig. 1. Generic board layout with flip-chip numbers [19].

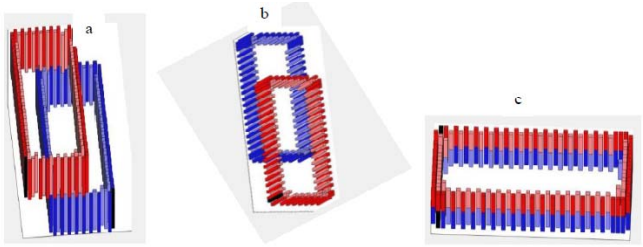

Fig. 2. Different flip-chip orientations. (a) Flip chip with back-to-back connection and offset along the breadth. (b) Flip chips with back-to-back connection with offset along the length. (c) Flip chips with back-to-back connections with no offset [19].

gold (ENIG) with various area array packages was designed at Delphi, Krakow, for the experiment. The 10-cm square manufactured PCB has a range of BGA and other area components populated carefully on both sides. One side of the PCB has eight flip chips, whereas the other side has six, making a total of 14 flip chips, numbered as shown in Fig. 1. Each flip chip has 109 solder joints. Table I shows more detailed information on the flip chips [13]. All the flip chips are placed in different positions on the PCB and also have different orientations relative to each other, as shown in Fig. 2. Flip chips U23 and U26 are stand-alone flip chips with no back-to-back connections. U19–U35 and U20–U36 pairs are placed back-to-back with an offset along the breath [see Fig. 2(a)]. U27–U39 and U28–U40 pairs are placed back-to-back with an offset along the length [see Fig. 2(b)]. U34–U46 and U31–U43 pairs are placed back-to-back with no offset [see Fig. 2(c)]. An aluminum test fixture was also designed at Delphi, Krakow, for the experiment that can accommodate four test boards at a time within a 4–5-mm recessed support for each board, as shown in Fig. 3. Each PCB is secured to the test fixture by a screw torqued to 1 N · m at its four corners. A random vibration profile used for the experiment is shown in Fig. 4. This profile was conceived with the help of automotive vibration experts in Delphi. The profile was designed to be a representation of the vibration loading experienced by many automobiles in real life. The setup is tabulated in Table II, with a level G rms = 9.5 g. A vibration shaker in Delphi, Liverpool, was programmed with this profile and used for the experiments, as shown in Fig. 5. Ultrasound C-scan images used for solder joint through life monitoring were obtained using the Sonoscan Gen6 C-Mode Scanning

TABLE I
INFORMATION ABOUT THE FLIP CHIPS [13]

Flip chip	
Die X	3948μm
Die Y	8898μm
Die Z	725μm
Poisson's ratio	0.22 to 0.28
CTE flip chip	2.6 ppm/K
UBM material	UBM stack is Al, Ni and Cu with Cu being on the top of stack.
UBM pad size	102μm
Level 1 interconnects (Solder joint)	
Solder bump diameter (middle)	140μm
Solder Bump height	125μm
Solder Joint height after assembly	90μm ±5μm
Solder material	Sn=52.9%, Pb=45.9%, Cu= 1.2%
Substrate	
Material	FR-4
Thickness	0.8mm or 1.6mm
Substrate x dimension	100mm, 5mm radius to corners
Substrate y dimension	100mm, 5mm radius to corners
CTE - PCB (ppm/K)	z=35x10-6, x=11x10-6, y=13x10-6, (in/in/c)
Pad thickness	35 - 42 microns
Pad material	Cu with HASL orENIG surface finish
Underfill	No underfill

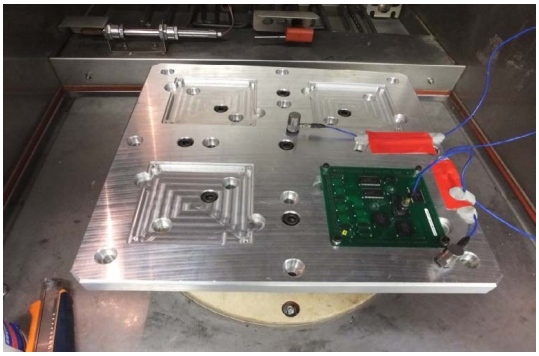

Fig. 3. Aluminum test fixture with one PCB and three empty slots [19].

Acoustic Microscope in the LJMU Laboratory, as shown in Fig. 6. A schematic of how the 109 solder joints was labeled to help with analysis along with an ultrasound C-Scan of the solder joints in a flip chip is shown in Figs. 7 and 8, respectively. A resolution of 3 μm was found to be optimal for the acoustic scanning after initial tests.

The PCB was mounted in the vibration shaker and vibrated according to the random profile obtained from Delphi, Krakow. As the total time to complete the mechanical failure of all the flip chips in the PCB was unknown, a pretest was conducted to help determine the maximum test time. All the flip chips were found to have reached complete failure after 86 vibration cycles, where each cycle was 4 min. Based on the pretest data, nine flip chips were selected according to their positions and

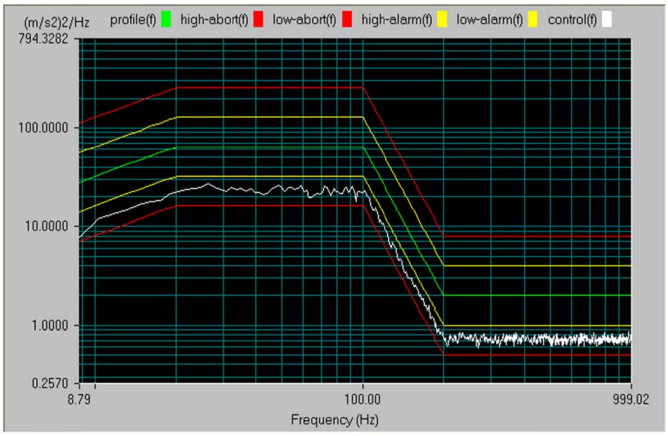

Fig. 4. Proposed random profile for the experiment (green trace) [19].

TABLE II
RANDOM VIBRATION PROFILE

Frequency (Hz)	10	20	50	100	200	300	400	500	750	1000
PSD $((m/s^2)^2/Hz)$	32	64	64	64	2	2	2	2	2	2

Fig. 5. Vibration chamber in Delphi, Liverpool, U.K.

relative orientations in the PCB to be monitored by acoustic scanning at different scan intervals based on their pretest results, as shown in Table III. This through lifetime data collected as an acoustic image was then processed and used for further analysis using MATLAB.

Table IV shows the failure time and pattern of the flip chips.

III. RESULTS AND DISCUSSION

A. Weibull Analysis

The Weibull distribution is one of the most widely used lifetime distributions in reliability engineering. The equation for the probability density function (pdf) $f(t)$ of a Weibull distribution is given by [13]

$$f(t) = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} \quad (1)$$

where $f(t) \geq 0, t \geq 0$ or $\gamma, \beta > 0, \eta > 0, -\infty < \gamma < \infty$.

Fig. 6. Sonoscan Gen6 C-Mode Acoustic Microscopy System (image courtesy of Sonoscan Inc.).

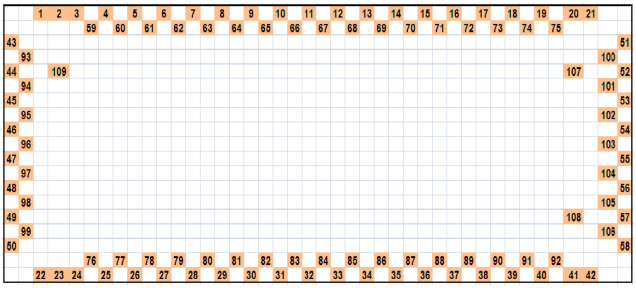

Fig. 7. Labeling scheme for 109 solder joints [16].

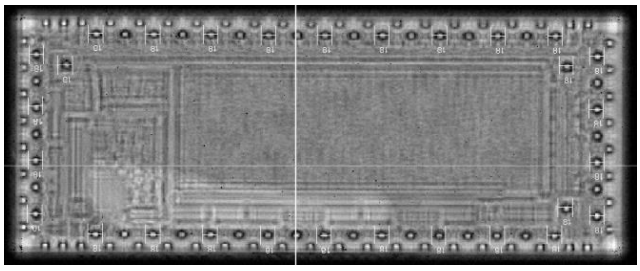

Fig. 8. C-scan of a target flip chip scanned at 3-μm resolution.

TABLE III
SCAN INTERVALS FOR DIFFERENT FLIP CHIPS FOR 0.8-MM ENIG

0.8mm ENIG	Scan interval
U23	1 scan/cycle
U26	1 scan/ 2 cycles
U27	1 scan/5 cycles
U34	1 scan/5 cycles
U19	1 scan/5 cycles
U28	1 scan/10 cycles
U20	1 scan/10 cycles
U35	1 scan/5 cycles
U40	1 scan/5 cycles

The parameters β, η, and γ control the scale, shape, and location of the pdf function. The scale parameter η defines where the bulk of the distribution lies. The shape parameter β

TABLE IV
FLIP CHIP FAILURE PATTERN FOR 0.8-MM ENIG

0.8mm ENIG flip chip no.	Cycles to failure 1 cycle = 4 minutes	Failure time in hours
U23	3	0.2
U26	14	0.933
U35	21	1.4
U39	23	1.533
U46	24	1.6
U34	29	1.933
U36	34	2.267
U27	45	3
U43	48	3.2
U20	53	3.533
U31	55	3.667
U40	57	3.8
U19	68	4.533
U28	86	5.733

TABLE V
RELIABILITY BASED COLOR CODING SCHEME

Color code	Criteria (% cycles to failure, say X)
Red: least reliable	X≤25
Yellow: medium reliability	25 <X≤ 50
Blue: most reliable	X>50

defines the shape of the distribution, and the location parameter γ defines the location of the distribution in time.

The Weibull distribution can take on the characteristics of other types of distribution based on the value of its shape parameter β. The Weibull shape parameter β, also known as the slope, is equal to the slope of the regressed line in a probability plot. The value of β has a marked effect on the failure rate of the Weibull distribution. Inferences can be drawn about a population's failure characteristics just by considering whether the value of β is less than, equal to, or greater than one. Populations with $\beta < 1$ exhibit a failure rate that decreases with time, populations with $\beta = 1$ have a constant failure rate that is consistent with an exponential distribution, and populations with $\beta > 1$ have a failure rate that increases with time. Fig. 9 shows the Weibull probability plot of the 0.8-mm ENIG-based PCB from the observations of Table IV.

The shape parameter β [15] has been calculated to be $\beta = 1.297$, which, being greater than 1, indicates that the ENIG PCB material set has a failure rate that increases with time. The fact that the data set closely follows the predicted Weibull distribution indicates the validity of the experimental data set.

B. Reliability Analysis Based on Flip-Chip Position

Upon close observation of the failure (Table IV), one can argue that the flip chips in the PCB can be classified into three categories based on their reliability performance. If we consider 86 cycles as the total expected lifetime of a flip chip,

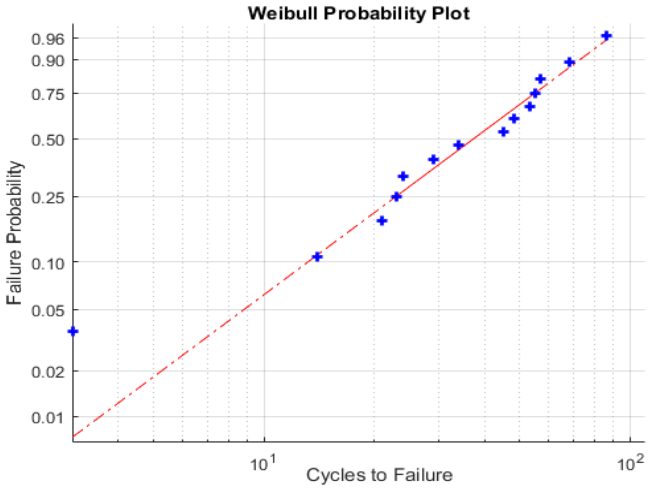

Fig. 9. Weibull plot for 0.8-mm ENIG PC.

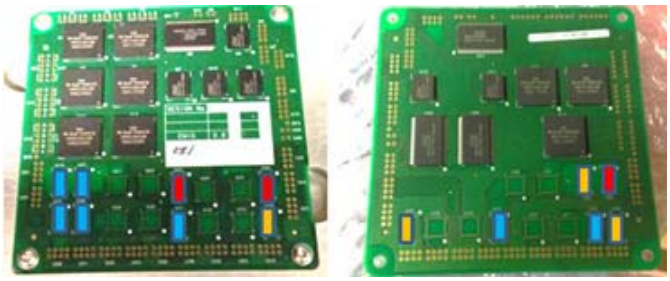

Fig. 10. 0.8-mm ENIG board layout with color-coded flip-chip positions based on reliability.

then flip chips with a lifetime of less than 25% of expected lifetime will be considered as the least reliable, those above 50% will be considered as the most reliable, and those in between 25% and 50% will have medium reliability. In order to visualize this classification, color coding was introduced as detailed in Table V and implemented in Fig. 10. Fig. 1 shows the nomenclature of the flip chips, whereas Fig. 10 shows their respective reliability.

Now, from Table IV, it can be seen that the most reliable positions are those of flip-chip pairs U31–U43 and U40–U28. Of these flip chips U31–U43 is a pair with back-to-back connection and no offset, while U40 is back-to-back connected with offset along the length. On the other hand, the least reliable flip chips are U23 and U26. They were the first two flip chips to fail within the first few vibration cycles in the test boards. Both these flip chips are stand-alone and have no back-to-back connections. Considering then together U23 that is placed near the center of the PCB has lower reliability than U26. Hence, it can be safely concluded that in a PCB, flip chips with back-to-back connections with no offset are the most reliable, while standalone flip chips with no back-to-back connections, especially the ones placed near the center of the PCB, are the least reliable when considering their susceptibility to vibration cycling.

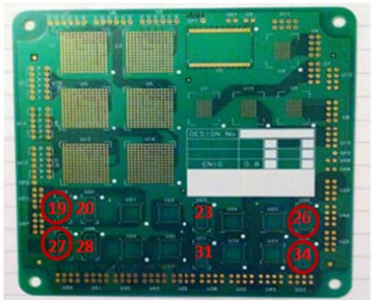

Fig. 11. Positions of the flip chips selected for analysis on the PCB.

C. Reliability Analysis Based on Flip-Chip Orientation and Solder Joint Position on PCB

In order to determine which of the solder joints fail first depending on the orientations and positions of the flip chip on the board, an in-depth analysis was done on selected flip chips U19, U26, U27, and U34, each of which belongs to a specific orientation.

1) *U34:* Back-to-back with no offset, near the board edge at the corner.
2) *U19:* Back-to-back with breath offset, near the board edge next to the corner.
3) *U27:* Back-to-back with length offset, near the board edge near the corner.
4) *U26:* Single sided near the board edge next to the corner.

Fig. 11 shows the flip-chip placement positions on the bare PCB in red circles. For the purpose of brevity and to avoid repetition, only the detailed analysis results for flip chip U34 will be discussed. Full details are available in [19].

In order to witness the behavior of the solder joints in each of the flip chips based on their orientations and positions, a 3-D plot of the mean intensity of the 51 solder joints in the inner region of each of the flip chips was generated. The mean intensity represents the reflected ultrasound wave strength from the solder bump to the flip-chip interface. As this connection cracks during vibration testing, the mean intensity grows in line with the crack size, giving a useful parameter through which to assess solder joint failure. The reason for dealing with only the inner 51 joints is to eliminate an ultrasound imaging edge effects. Yang [16] in his thesis concluded that because of an acoustic edge effect witnessed at the imaging of the outer row of solder joints in these particular flip chips, getting an accurate measure of their image parameters is very difficult. When an ultrasound signal strikes the edge of a material, the signal is scattered away that results in a drop of the required information from the solder joint [17], [18]. This effect can be reduced by custom transducer design but cannot be eliminated entirely due to the intrinsic properties of ultrasound. Hence, in order to get a more accurate picture of the behavior of the solder joints in a vibration environment based on the positions and orientations of the flip chips, only the inner periphery of 51 solder joints was selected to be analyzed, as shown in Fig. 12.

From the detailed mean intensity analysis of each of the solder joints in flip chips of various reliabilities in the PCB using

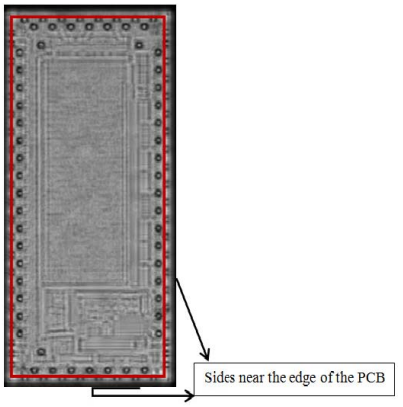

Fig. 12. C-scan image of U34 showing the solder joints to be examined within the red box.

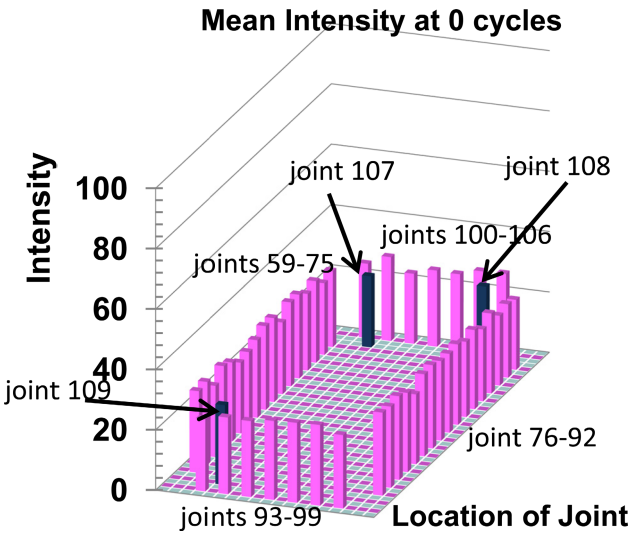

Fig. 13. 3-D plot of the mean intensity of joints 59–109 of U34 at cycle 0.

MATLAB [19], it was found that for all types of joints in a flip chip, the first trigger point occurs at around 35%–40% cycling and second change occurs at around 80%–85% cycling [19]. Thus, the failure pattern of any solder joint can be loosely said to fall into regions. The region between zero cycles and first trigger point where the crack initiates, the region between the first and second trigger point where the crack propagates, and finally the region after the second trigger point where the crack formed reaches its peak and finally the flip chip fails. Consequently, for flip chip U34 that has a total vibration cycling time of 29 cycles, the first trigger point of change or crack initiation should occur at around ten cycles, whereas the second trigger point should be at around 25 cycles. Hence, the solder joints at scan intervals of 0, 10, 20, and 25 cycles will be analyzed in detail. The reason for analyzing the scan at 20 cycles is because 20 cycles represent a point between the first and second trigger points and hence will provide valuable information on the crack propagation. Figs. 13–16 show the 3-D plots of the mean intensity of the solder joints of U34 at cycles 0, 10, 20, and 25, respectively.

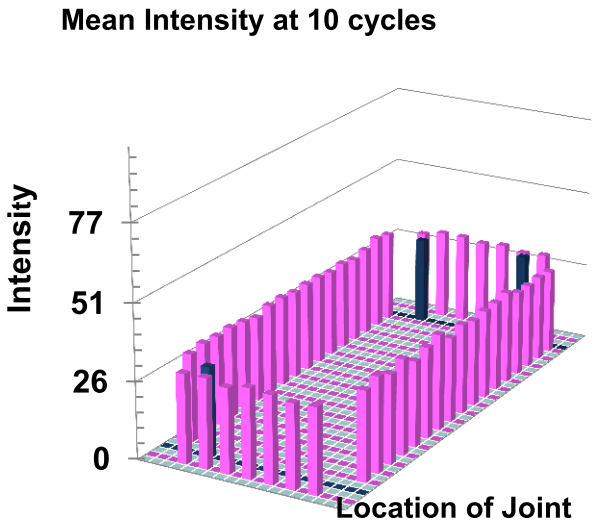

Fig. 14. 3-D plot of the mean intensity of joints 59–109 of U34 at ten cycles.

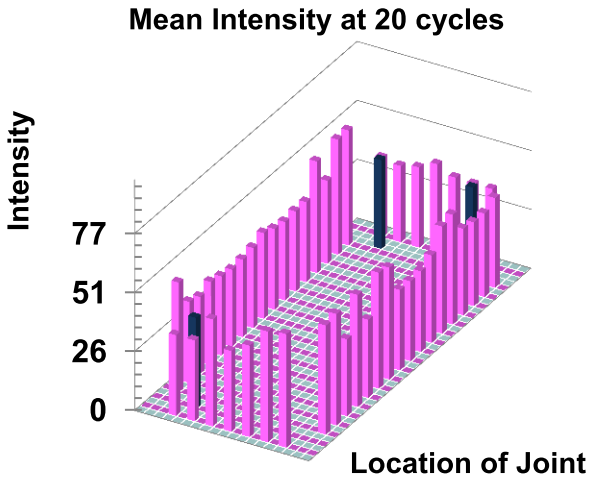

Fig. 15. 3-D plot of the mean intensity of joints 59–109 of U34 at 20 cycles.

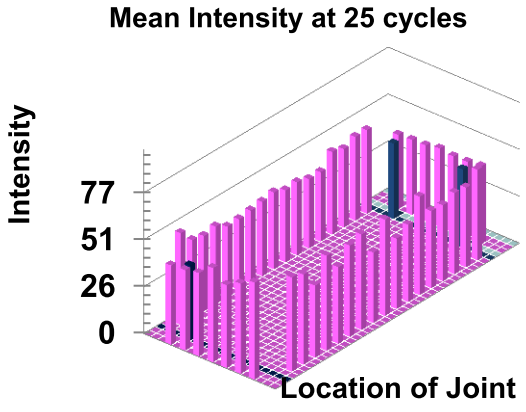

Fig. 16. 3-D plot of the mean intensity of joints 59–109 of U34 at 25 cycles.

For a clearer visualization, the graphs in Figs. 17–21 show the intensity change of all the 51 joints at cycle 25. It should be kept in mind that all the joints had a mean intensity of around 20–25 at cycle 0, as shown from Fig. 13.

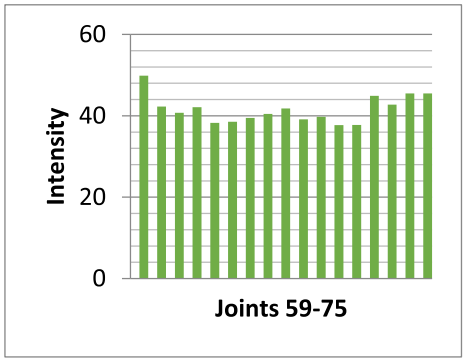

Fig. 17. Intensity of solder joints 59–75 (away from the PCB edge) at cycle 25.

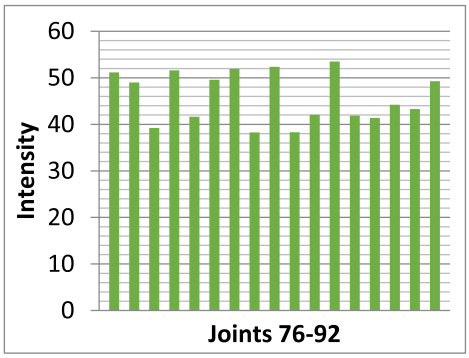

Fig. 18. Intensity of solder joints 76–92 (near the PCB edge) at cycle 25.

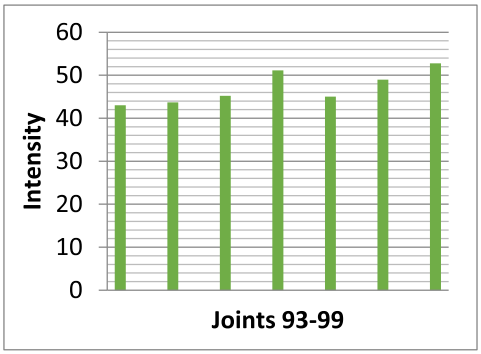

Fig. 19. Intensity of solders joint 93–99 (near the PCB edge) at cycle 25.

From the 3-D plots, it can be clearly seen that at cycle 0, all the solder joints have a mean intensity of around 20–25. However, after 25 cycles, joints 76–92 that are located near the edge of the board start showing more intensity change with an average intensity value of 45.8 compared with joints 59–75 that are located away from the edge and have an average intensity value of 41.2. Similarly, joints 93–99 that are located near the edge of the board start showing more intensity change with an average intensity value of 47.1 compared with joints 100–106 that are located away from the edge and have an average intensity value of 41.0. Joints 107–109 show a similar intensity change, but the intensity change of joint 109 that is located nearer the board edge is very slightly more than 107 and 108.

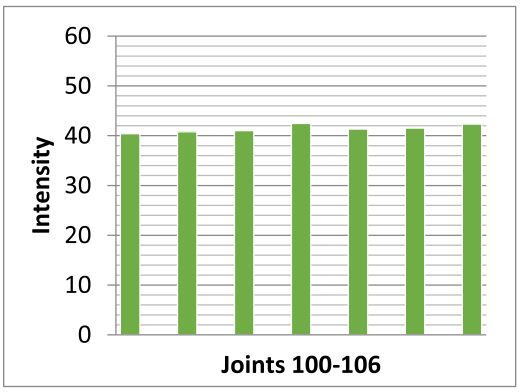

Fig. 20. Intensity of solders joint 100–106 (away from the PCB edge) at cycle 25.

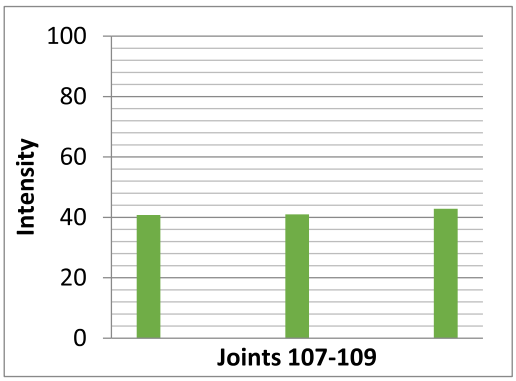

Fig. 21. Intensity of solder joints 107–109 at cycle 25 (joint 109 is nearest the edge).

A similar pattern in the behavior of solder joints was observed in the case of the rest of the flip chips as well. In the case of U19, the solder joints near the edge of the board, namely 59–75, showed more damage compared with the joints at the side away from the edge, namely 76–92. The overlapping joints 95–99 and 103–106 show average damage, but joints 103–106 near the board edge have slightly more damage compared with joints 95–99. In the case of U27, the solder joints near the edge of the board, namely, 59–75, show more damage compared to the side away from the edge, namely 76–92. The overlapping joints 59–67 and 76–84 show average damage, but joints 59–67 near the board edge have slightly more damage compared with joints 76–84. Solder joints 68–75 have more damage compared with joints 59–67 and 76–92, whereas joints 85–92 have more damage than joints 76–84. Finally, in the case of U26, the solder joints near the edge of the board, namely 59–75 show more damage compared to the joints at the sides away from the edge, namely 76–109.

From all the earlier observations, it can be concluded that in the case of vibration loading, the solder joints near the board edges start failing first. Thus, the farther away from the edge a solder joint is, the better the reliability. Solder joints with back-to-back connections are more reliable than the ones placed in one-sided orientation. However, solder joints with back-to-back connections but located near the board edges are less reliable compared with the ones located away from the board edges.

D. Design Guidelines for Floor Plan Layout in a PCB

Based on all the observations mentioned in Sections III-B and III-C, certain design guidelines can be loosely suggested to ensure better reliability of solder joints and flip chips and improve their susceptibility to PCBs operated in a vibration environment.

1) Single-sided flip-chip placements should be avoided.
2) Back-to-back connections should be made where possible.
3) Placement of flip chips at the center of the PCB should be avoided.
4) Placement of flip chips very close to the edges of the PCB should be avoided.
5) Back-to-back connection with no offset is the most reliable orientation for flip chips in PCBs subjected to vibration.
6) Back-to-back connection with length offset is the second most reliable orientation for flip chips in PCBs subjected to vibration.
7) Finally, back-to-back connection with breath offset is the least reliable of the three offsets, but it is more reliable than a stand-alone single-sided connection.

IV. Conclusion

In this article, the effects of vibration cycling on the reliability of flip chips of different positions and relative orientations in an industry-grade PCB were evaluated. Nondestructive testing in the form of AMI was used for data collection and MATLAB was used for data analysis. It was found that in the case of vibration cycling in a 10-cm square PCB attached by screws at each corner, flip chips with back-to-back connections with no offset are the most reliable, while stand-alone flip chips with no back-to-back connections, especially the ones placed near the center of the PCB, are the least reliable. A detailed 3-D mean intensity analysis of the degradation of individual solder joints in a flip chip was also done to study the failure patterns of individual solder joints in a flip chip based on their location and orientation on a PCB. It was found that in the case of vibration loading, the solder joints near the board edges start to fail first. Solder joints with back-to-back connections were more reliable than the ones placed in the one-sided orientation. However, solder joints with back-to-back connections but located near the board edges were still less reliable compared with the ones located away from the board edges. Thus, the farther away from the PCB edge a solder joint was, the better the reliability. Based on all these observations, a few design guidelines for the floor plan layout of flip chips in a PCB were proposed from this article.

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