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$SrTiO_3$ for sub-20 nm DRAM technology nodes—characterization and modeling

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Abstract

The electrical properties of Ru/SrTiO/Ru capacitors have been investigated. EOT of 0.38 nm at V_G = 0 V and $J_G \sim 10^{-7}$ Acm^{-2} at V_G = ±1V and temperature T = 25 °C meet sub-20 nm DRAM requirements. Relaxation measurements were performed, indicating acceptable charge loss. Modeling of defects based on multi-phonon trap-assisted-tunneling SrTiO can quantitavely well describe leakage and capacitance behavior.

Keywords: Metal-Insulator-Metal Capacitor; Strontium Titanium Oxide; Traps

1. Introduction

Modern operating systems and applications are designed to rely heavily on large amounts of Dynamic RAM (DRAM) memory. To cope with this demand, high-density DRAM components demand Metal-Insulator-Metal (MIM) capacitors with high storage charge density (i.e., low Equivalent Oxide Thickness EOT) and sufficient charge retention, determined by leakage and relaxation of the dielectric [1]. Completing the list of constraining requirements, high-density 3D integration schemes also stipulate maximum physical thickness of the dielectric [2].

The defects incorporated in the dielectric by processing inevitably influence the electrical characteristics of the MIM capacitor. Specifically, in $SrTiO_3$ (STO) films under development for sub-20 nm DRAM technology nodes [3], a defect band ~1 eV below CBM has been previously reported [4]. *Here we perform detailed modeling of defects in the dielectric to self-consistently explain both J-V and C-V characteristics. We furthermore measure the dielectric relaxation in this material and compare it with previously reported DRAM dielectrics candidates.*

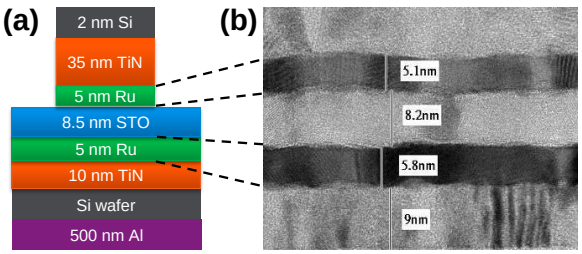

Fig. 1. (a) Schematic cross-section of a STO MIM capacitor with (b) a transmission electron micrograph.

2. Experimental

The structure of a process-of-reference STO MIM capacitor is shown in Fig. 1 [3]. Bottom and top electrodes (BE and TE) are Ru to provide good match with the $SrTiO_3$ dielectric, which is ALD-deposited by alternating TiO_2 and Si-

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rich SrTiO layers. Intermixing of the layers during crystallization then results in SrTiO film with higher Ti-content, which in turn yields favorable material and electrical parameters, such as favorable microstructure and a smaller lattice parameter, high dielectric constant *k*, and reduced leakage [3]. The physical thickness of the film t_{ox} is ~8.5 nm. Capping 2nm Si layer reduces oxidation of the top TiN electrode. Capacitors of different sizes are patterned by etching the TE.

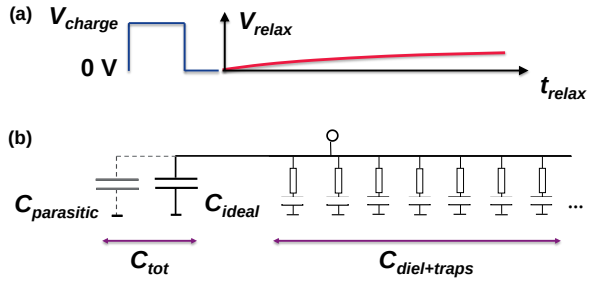

Fig. 2. (a) Schematic of relaxation measurement and (b) the equivalent electrical circuit of a MIM capacitor.

Electrical measurements were performed at wafer level. Off-the-shelf characterization equipment was used for the measurements of *C-V*, *J-V*, and *J-t*. Measuring relaxation current decreasing reciprocally with time over multiple decades is however quite problematic. Relaxation measurements were therefore done using a custom-built instrumentation. The microcontroller-controlled instrument charges the MIM capacitor with a short pulse (64 ms) at V_{charge}, followed by 0.75 µs discharge (Fig. 2a). Fig. 2b shows the equivalent circuit of the MIM capacitor, consisting of the ideal capacitor C_{ideal} and a RC element ladder with widely distributed times, representing the response of the dielectric and traps. After the discharge the instrument goes into high-impedance mode and voltage V_{relax} is measured as a function of time. V_{relax} starts developing on the floating capacitor C_{tot} due to charge flowing from $C_{diel+traps}$ (Fig. 2b). Correct evaluation of the relaxation requires considering the parasitic capacitance of the instrumentation $C_{parasitic}$ (Fig. 2b). The relaxation current can then be evaluated using

$$J_{relax}(t) = \frac{C_{tot}}{A}\,\frac{dV_{relax(t)}}{dt}\,, \qquad (2)$$

where *A* is the area of the tested capacitors, typically 100×100 µm^2. The relative charge loss, often used in DRAM capacitor benchmarking, is then

$$Q_{loss,relative}(t) = \frac{1}{CV_{charge}}\int_{t_0}^{t} J_{relax}(t')dt' = \frac{C_{tot}}{C_{ideal}V_{charge}}\left[V_{relax}(t) - V_{relax}(t_0)\right], \qquad (3)$$

where $C_{ideal}V_{charge}$ is the charge on the ideal capacitor, and t_0 is typically 10^{-8} s [Kiyotoshi?].

3. Results and discussion

Figs. 3 and 4 give the *J-V*, *C-V*, and *G-V* characteristics of the capacitor. EOT of 0.38 nm (at V_G = 0 V) and J_G ~ 10^{-7} Acm^{-2} at V_G = ±1V and temperature *T* = 25 °C meet sub-20 nm DRAM requirements. AC capacitance in Fig. 4a is seen to decrease with increasing magnitude of the electric field in the dielectric $E_{STO} = V_G / t_{ox}$, as observed previously [5], in agreement with Johnson's relation [6]

$$\varepsilon(E_{STO}) = \frac{\varepsilon_{max}}{\left(1+\Lambda E_{STO}{}^2\right)^{1/3}}\,, \qquad (4)$$

where ε_{max} the permittivity at 0 V and $\Lambda > 0$ a simplified scaling parameter. Capacitance further decreases with increasing frequency as ~ f^{n-1}, n ~ 0.997, due to dielectric relaxation [1]. The value of n decreases at increasing T (not shown). The intrinsic *G-V* characteristic in Fig. 4b is bordered by leakage at higher fields and lower *f*'s and series resistance at higher *f*'s, also noticeable at higher *f*'s in Fig. 4a.

In the departure from Eq. 4 above, constant or even slightly increasing capacitance is observed in the -0.5 to +0.5 V voltage range in Fig. 4a. For some investigated processing options the *C-V*'s even show two distinct peaks, cf. Fig. 5a. Because of the strong hysteresis of the *C-V* characteristics following large voltage range sweep in Fig. 5b, we conclude these additional *C-V* features can be also ascribed to defects in the dielectric.

J-V, *C-V*, and *G-V* curves are simulated by considering the defect distribution shown in Fig. 6. A defect band 0.9—1.2 eV below CBM with 10^{19} cm^{-3} density is introduced in compliance with previous observations [4]. The high defect density ~3×10^{20} cm^{-3} close to the interface is assumed due to reaction of STO with electrodes, consistently with [7]. Charge trapping/emission is modeled in the framework of the multi-phonon trap-assisted-tunneling model [8], which accounts for electron-phonon coupling and lattice relaxation. Note that *charge in the dielectric will locally change the electric field, which in turn changes* $\varepsilon(E_{STO})$ (cf. Eq. 4), requiring a fully self-consistent solution [9]. For this reason the "background" fixed positive charge (Fig. 4), introduced following [10], results in lower *measured* ε*;* we, however, find it is not strictly necessary to explain our observations.

At low biases, the high-density states close to the interface align with the electrode Fermi level (Fig. 6) and contribute to the peaks in *C-V* in Fig. 5a [11, 12]. The G/ω value of ~10^{-7} Scm^{-2}Hz^{-1} observed in Fig. 4b is also reproduced (not shown). Permanent charging of states is then assumed at high biases, resulting in excellent reproduction of the hysteresis in Fig. 5b. The same configuration correctly reproduces the *J-V* curves and their *T* dependence in Fig. 3.

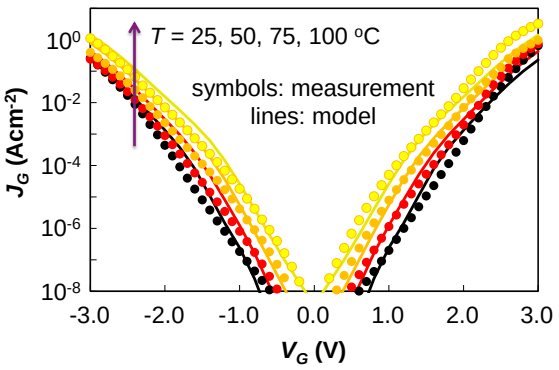

Fig. 3. MIM cap *J-V* characteristic is excellently reproduced by model assuming a defect band ~1 eV below the STO CBM [4].

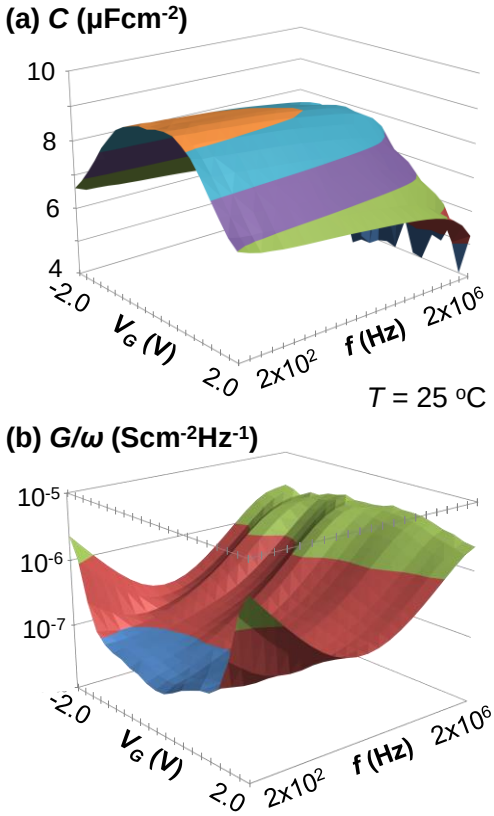

Fig. 4. STO MIM cap *C-V-f* and *G-V-f* characteristics (each *C-f* measured at constant V_G on a fresh cap). (a) The *C-V* decrease at higher electric field is described by Eq. 1. The decrease of *C* with *f* is due to dielectric relaxation. (b) The *G-V* characteristic is bordered by leakage at lower *f*'s and higher fields and series resistance at higher *f*'s (also noticeable at higher *f*'s in (a)).

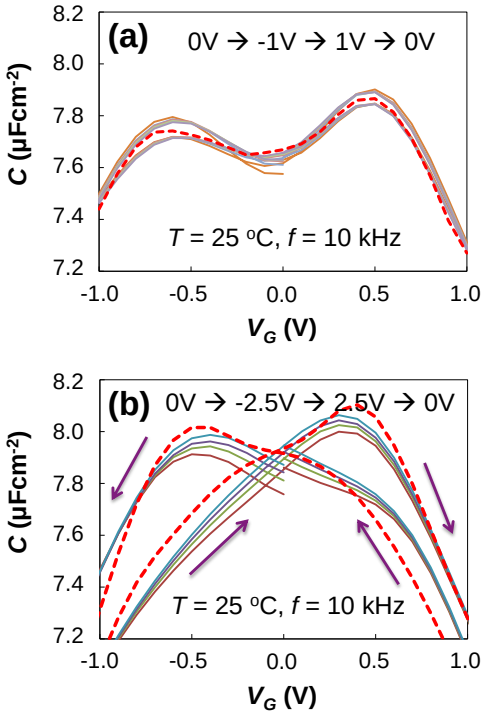

Fig. 5. (a) In some STO films the *C-V* characteristics show two distinct peaks, in addition to the overall *C-V* behavior shown in Fig. 3a. Weak hysteresis is also visible. (b) When higher voltages are applied, strong hysteresis appears and the peak weight shifts depending on the sweep sense. Solid lines: 5 subsequent measurements on same capacitor. Thick dashed lines: model fit.

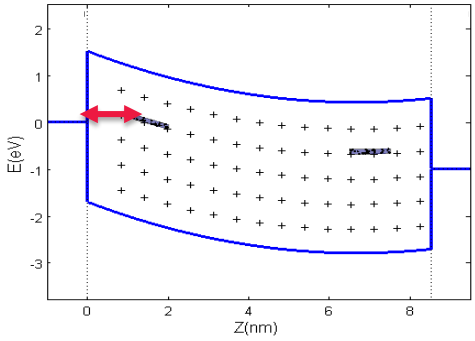

Fig. 6. Model assuming high density of defect states closer to interface (low density band not visible). At low biases, these states align with electrode Fermi level and contribute to *C* (Fig. 5a). Permanent charging of states at high V_G's results in hysteresis (Fig. 5b).

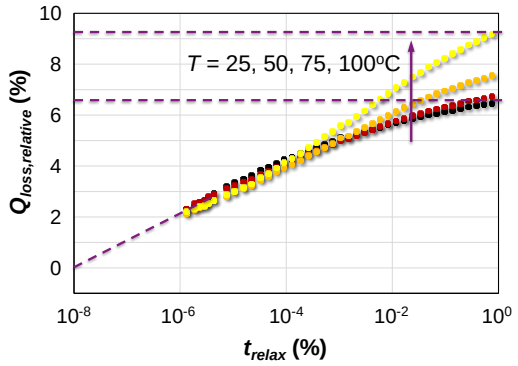

Fig. 7. Voltage relaxation measurement recalculated into charge loss Q_{loss}, normalized to $C_{ideal}V_{charge}$. Measurement back-extrapolated to t_0 = 10 ns as per DRAM specification. Temperature dependence indicates trap contribution.

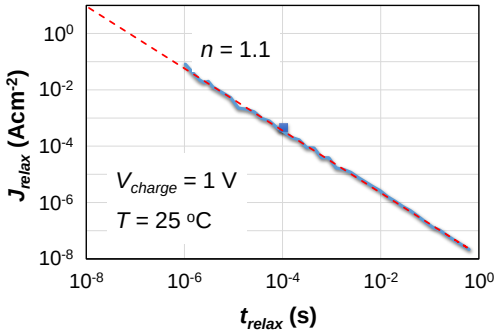

Fig. 8. Voltage relaxation measurement in Fig. 7 recalculated to *J-t* (solid line). Dashed line: fit with t^{-n}. The value of *n* decreases with increasing *T* (not shown). Symbol: Direct measurement of *J* at 10^{-4} s excellently matches the recalculated *J-t* data.

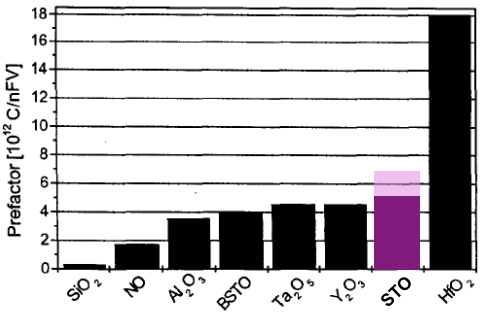

Fig. 9. Comparison of relaxation in different materials through prefactor *a* [13]. STO relaxation properties are adequate for DRAM operation.

The voltage relaxation measurements at different *T*'s are shown as charge loss on the MIM cap electrodes in Fig. 7. The *T* dependence again indicates trap contribution. In Fig. 8, the data are recalculated to current relaxation, following

$$J_{relax}(t) = aPt^{-n}\,, \qquad (5)$$

where *P* is dielectric polarization [13], *a* is a prefactor, and *n* = 1.1 close to the value obtained from *C-f* in Fig. 4a. It also favorably compares with direct *J-t* measurement (symbol in Fig. 8), which, however, is complicated in the full 6 dec time range. Finally, *J* / *P* obtained for our STO films in the studied *T* range of 25—100 °C is compared in Fig. 9 with other materials [13], indicating STO is a viable DRAM dielectrics candidate.

4. Conclusions

The electrical properties of Ru/SrTiO/Ru capacitors have been investigated. EOT of 0.38 nm at V_G = 0 V and $J_G \sim 10^{-7}$ Acm^{-2} at V_G = ±1V and temperature *T* = 25 °C meet sub-20 nm DRAM requirements. Relaxation measurements were performed, indicating acceptable charge loss. Modeling of defects based on multi-phonon trap-assisted-tunneling SrTiO can quantitavely well describe leakage and capacitance behavior.

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