Performance Comparison of Two Four-level Five-phase Open-end Winding Drives

M. Darijevic, M. Jones, E. Levi
Liverpool John Moores University
Liverpool L3 3AF, U.K.

A. Iqbal
Qatar University
2713 Doha, Qatar

H. Abu-Rub
Texas A&M University at Qatar
23874 Doha, Qatar

***Abstract* – Two four-level five-phase open-end winding drives are analysed in this paper, and their performances compared. The first topology consists of two two-level voltage source inverters (VSI) supplying a five-phase machine with open-end windings (OeW). The second topology comprises one three-level and one two-level VSI to supply the five-phase OeW machine. In both cases, two VSIs are supplied from isolated dc-sources, with voltages in a ratio 2:1. As a consequence, the output phase-voltage waveforms are equivalent to those produced by a four-level five-phase VSI. The paper shows that the considered topologies exhibit significantly different operating characteristics.**

I. INTRODUCTION

In the last two decades, open-end winding drives are considered as an alternative approach for multiphase drives construction [1-4]. This specific topology employs two VSIs, in order to supply OeW drive from both ends of its windings. Three-phase OeW drives have been a research focus for medium- and high-power applications [3, 4]. These pioneering research efforts demonstrated that OeW drives have advantages over conventional multilevel single-sided topologies. Namely, the OeW topology effectively splits the drive supply into two parts, which leads to a modular structure comprising standard off-the-shelf two-level (or multilevel) power electronic modules, while enabling multilevel phase voltage waveforms. Thus, various problems that exist with multilevel single-sided VSIs are eliminated, simply by using machine with windings open on both sides, instead of forming neutral point(s) on one side.

At the same time, another school of thought proposed multiphase drives, mainly in conjunction with two-level inverters [5-10]. The reported benefits are numerous [1, 6]. Usage of multiphase machines opens a possibility to increase the overall drive power, by splitting the current between more than three inverter legs. Secondly, an increased capability to operate under faulted conditions has been demonstrated [8, 9, 11], which seems to be of a great interest for automotive and traction applications. More recently, research merging multilevel OeW and multiphase drive concepts has been conducted [1, 10-17]. This work shows that the individual benefits of both concepts can be combined.

Regardless of the number of phases, it can be shown that when two two-level VSIs are used to supply an OeW machine (2L-OeW-2L), multilevel output waveforms can be obtained. This is due to the phase voltage being formed as the voltage difference between two VSI leg voltages connected to the same machine phase. In other words, the VSIs individual voltage levels are augmented and the final phase voltage waveform will be equivalent to that of a three- or four-level single-sided supply [1, 10-14]. The number of equivalent voltage levels depends not only on the number of levels of the two VSIs, but also on the dc-link voltage ratio [12-14]. It has been shown in [12] that, if two two-level inverters are supplied with equal dc-link voltages, the resulting phase voltage waveforms are equivalent to those obtained using a three-level neutral point clamped (NPC) or flying capacitor (FC) converter. On the other hand, if any other ratio of dc-links voltages is used, four-level output waveforms will be obtained.

In [13, 14] the VSIs are supplied with dc-link voltages in a ratio 2:1, which results in four equidistant voltage levels. A level shifted carrier based (CB) pulse width modulation (PWM) strategy is used and some issues are reported. The process explained in [14] is responsible for the presence of so-called dead-time spikes. Although this drawback has very weak influence on phase voltage harmonic performance, the presence of dead-time spikes may lead to increased EMI. Furthermore, it is shown that this phenomenon causes a larger number of levels in the common mode voltage (CMV) ac components, which may lead to several unwanted effects [13, 14]. The solution, presented in [14], effectively eliminates the issues related to dead-time spikes; however, this is achieved at the cost of a more sophisticated control method, which requires accurate phase current measurements. Also, the presented spike removal algorithm (SRA) may in some cases lead to increased low-order current harmonics, although spikes in the phase voltage waveform are fully eliminated.

A further drawback of the 2L-OeW-2L configuration with unequal dc-link voltages is discussed in [16, 17] where it is demonstrated that this topology requires at least one fully controllable bidirectional dc source, since the lower dc-link voltage capacitor can be overcharged, depending on the modulation index. In essence, overcharging of the capacitor belonging to the lower dc-link voltage side can be understood as a consequence of unbalanced power transfer between the two inverters. This problem can be solved using one of two approaches, either changing the modulation strategy (software solution) or reconfiguring the hardware. The first method represents a trade-off between quality of output phase voltage waveforms, CMV waveforms and lower dc-link voltage capacitor balancing. It has been shown in [16] that the unequal reference sharing (URS) modulation strategy [15] naturally eliminates the capacitor overcharging problem. Unfortunately, URS method produces waveforms that are not optimal regarding phase voltage harmonic distortion. Hence, the benefits expected from unequal and isolated dc-link voltages are not fully utilised.

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There are three possibilities to tackle this problem using a hardware based approach. The least efficient way is to dissipate the energy that leads to capacitor overcharging using the brake resistor. Since this is required during regular drive operation, it inevitably decreases the overall efficiency and requires a large resistor. Alternatively, one could direct the excess of energy towards the higher dc-link voltage side. This solution would require additional complex bidirectional and isolated dc-dc converters, which are still not in regular use for high-power applications. Finally, instead of intervention in dc-dc conversion stage, one can change the way dc-ac conversion is performed. This can be realised by replacing one two-level inverter with a three-level NPC VSI, making a 3L-OeW-2L drive. This becomes an attractive option with regard to recent progress in the semiconductor industry, where novel NPC power modules are now available as off-the-shelf solutions for three-level converters. At the same time, a further power increment is possible, since dc-link voltage on three-level inverter side can be increased further. This novel topology does not require simultaneous switching in two VSI legs connected to the same machine phase, which is the direct cause of dead-time spikes in phase voltage waveform in the 2L-OeW-2L configuration [14]. Additionally, it will be shown further that the 3L-OeW-2L drive naturally balances the dc-links capacitor voltages.

Both 2L-OeW-2L and 3L-OeW-2L topologies are described in the next section, for the five-phase drive case. It is shown that a dc-link voltage ratio 2:1 in both cases results in four-level operation. Suitable modulation techniques are described for each configuration and the different performances are compared using detailed simulations. In order to isolate the drive performance from the dc-link overcharging problem, the first set of results contains steady-state waveforms for the case when the VSIs are supplied using controllable four-quadrant dc sources. Next, the dc-link overcharging problem is analysed, observing the behaviour when dc-link voltages are formed using three-phase diode rectifiers.

II. Topology Analysis

The two topologies under investigation are depicted in Figs. 1 and 2. The dc-link voltages (V_{dc1}, V_{dc2}) are isolated so the OeW drive has overall dc-link of $V_{dc} = V_{dc1} + V_{dc2}$, which is set to be 600 V. This results in $V_{dc1} = 400$ V and $V_{dc2} = 200$ V.

To simplify the analysis of the drives characteristics, the single-phase equivalent (boxed red dashed line in Figs. 1 and 2) is considered. Disregarding the rest of the drive and under the assumption that $v_{n1} = v_{n2} = 0$ V, analysis of a so-called equivalent model shows how the phase voltage levels are formed. All possible switching states and their relationship with leg and phase voltages are given in Tables I and II, for 2L-OeW-2L and 3L-OeW-2L drives, respectively. Complementary switches in two-level inverters (VSI_1 and VSI_2 in Fig. 1 and VSI_2 in Fig. 2) for k^{th} drive phase are marked with S_{up2k} and S_{dn2k}. VSI_1 in Fig. 2 is a three-level NPC inverter and it contains two complementary pairs of power switches, per drive phase. These are marked with superscripts "*a*" and "*b*" (S^a_{up1k} and S^a_{dn1k}, S^b_{up1k} and S^b_{dn1k}) for the k^{th} drive phase. Common rule is that complementary switches with the indices "*up*" and "*dn*" cannot be turned on at the same time, in order to prevent dc-link rail short-circuiting. Having this in mind, in order to simplify the analysis, switching states can be defined for complementary pairs instead of analysing separate switches:

- $S_{1k} = 1$, if S_{up1k} or D_{up1k} is turned on, otherwise $S_{1k} = 0$.
- $S_{2k} = 1$, if S_{up2k} or D_{up2k} is turned on, otherwise $S_{2k} = 0$.
- $S^a_{1k} = 1$, if S^a_{up1k} or D^a_{up1k} is turned on, otherwise $S^a_{1k} = 0$.
- $S^b_{1k} = 1$, if S^b_{up1k} or D^b_{up1k} is turned on, otherwise $S^b_{1k} = 0$.

In this way, dead-time can be disregarded in order to simplify the analysis. Although the 2L-OeW-2L configuration has four switching combinations, while the 3L-OeW-2L has eight, it is clear from Tables I and II that both topologies have four, i.e. exactly the same, equivalent phase voltage levels (400 V, 200 V, 0 and -200 V). This is a consequence of the chosen dc-link voltage ratio, resulting in the mid-point voltage of VSI_1 in Fig. 2 to be equal to $v_{mp} = V_{dc1}/2 = V_{dc2}$. Hence, two switching combinations in Table II ($N = 2$ and 5) produce the same equivalent phase voltage level of 200 V, while 0 voltage level can be produced with $N = 6$ and 7. States that are not used are marked with "*Z*" in Table II. These states are not in use, since NPC VSI leg voltage for these switching combinations is not determined by modulation strategy, but with phase current sign and conduction of antiparallel diodes. On the other hand, Table I shows that in the case of 2L-OeW-2L only one switching combination corresponds with the single equivalent voltage level. As a result, the two topologies have different operating properties.

TABLE I. Relationship between switching states, leg and equivalent voltages for the 2L-OeW-2L drive.

N	S_{11}	S_{21}	v_{11} [V]	v_{21} [V]	Equivalent v_1 [V]
1	1	1	V_{dc1}	V_{dc2}	$1/3V_{dc}$
2	1	0	V_{dc1}	0	$2/3V_{dc}$
3	0	1	0	V_{dc2}	$-1/3V_{dc}$
4	0	0	0	0	0

TABLE II. Relationship between switching states, leg and equivalent voltages for the 3L-OeW-2L drive.

N	S^a_{11}	S^b_{11}	S_{21}	v_{11} [V]	v_{21} [V]	Equivalent v_1 [V]
1	1	1	0	V_{dc1}	0	$2/3V_{dc}$
2	1	1	1	V_{dc1}	V_{dc2}	$1/3V_{dc}$
3	1	0	0	Z	0	Z
4	1	0	1	Z	V_{dc2}	Z
5	0	1	0	$V_{dc1}/2$	0	$1/3V_{dc}$
6	0	1	1	$V_{dc1}/2$	V_{dc2}	0
7	0	0	0	0	0	0
8	0	0	1	0	V_{dc2}	$-1/3V_{dc}$

III. Modulation Strategy

Since both drives have four equidistant voltage levels, level shifted carrier based modulation strategies are analysed. Two carrier arrangements are investigated, with carriers in in-phase disposition (PD) and with alternate phase disposition (APOD), as shown in Fig. 3. During one fundamental period, phase voltage reference instantaneous value is always situated within one of three so-called reference zones, bordered with voltage levels (horizontal black lines in Fig. 3). In each zone

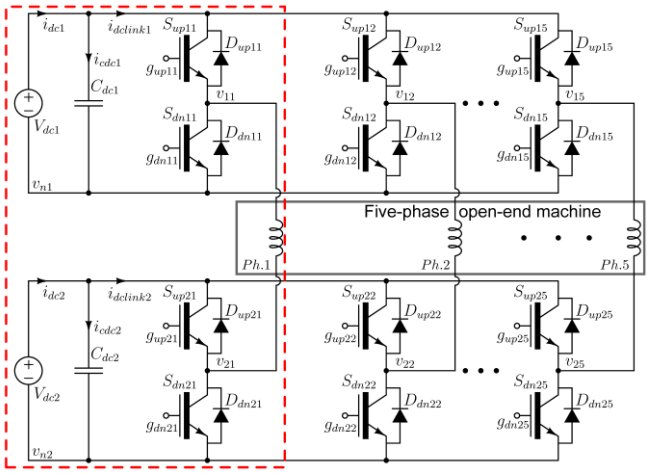


Fig. 1. Four-level five-phase OeW drive with two two-level VSIs (2L-OeW-2L).

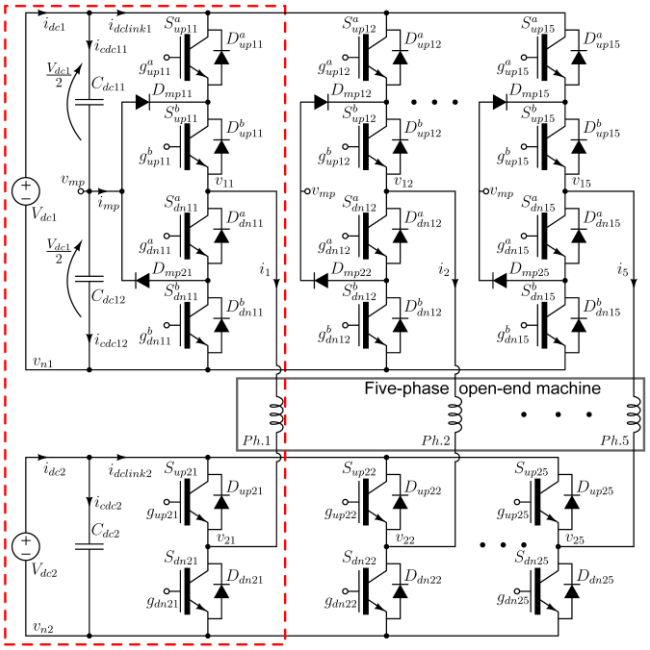


Fig. 2. Four-level five-phase OeW drive with one three- and one two-level inverter (3L-OeW-2L).

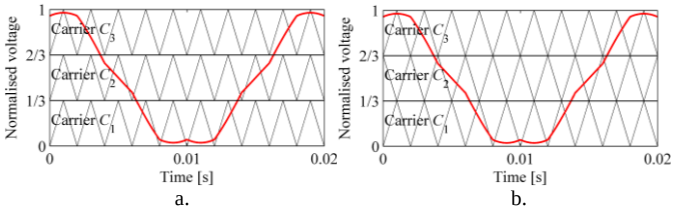


Fig. 3: One phase voltage reference (red line) and carrier signals for PD (a) and APOD (b) PWM during one fundamental period. Reference is with min-max injection.

a reference is compared with a single carrier. Clearly, as long as the reference is in the same zone, comparison with remaining two carrier signals always gives the same result (0 or 1). To determine the relationships between references, carriers and switching states, it is helpful to define:

$$A_{ik} = \begin{cases} \text{if } v_k^* > C_i & \text{then } 1 \\ \text{if } v_k^* < C_i & \text{then } 0 \end{cases} \qquad (1)$$

where v_k^* is the phase voltage reference for the k^{th} phase, while i can be equal to 1, 2 or 3. Since 2L-OeW-2L drive contains two complementary switch pairs per one drive phase (one per VSI), determination of switching states from A_{ik}, requires some additional calculations, as explained in [13, 14]:

$$S_{1k} = A_{2k}, \qquad S_{2k} = \overline{A_{1k}} + A_{2k} \cdot \overline{A_{3k}}, \qquad (2)$$

Resulting VSI_1 and VSI_2 operation is summarised in Table III. As emphasised in [14], both inverters are in PWM mode in the reference zone 2. In other two zones, VSI_1 holds one voltage level, while inverter with lower dc-link voltage performs PWM.

On the other hand, 3L-OeW-2L topology has much simpler switching pattern, due to the existence of one additional complementary switch pair in the VSI_1. Using the same rules as for the 2L-OeW-2L case, the governing relationships are:

$$S_{1k}^a = A_{1k}, \qquad S_{1k}^b = A_{3k}, \qquad S_{2k} = \overline{A_{2k}} \qquad (3)$$

Operation of two VSIs in the case of 3L-OeW-2L drive is summarised in Table IV. VSI_1 in the first reference zone performs PWM operation between 0 and its mind-point voltage ($V_{dc1}/2$), while in the reference zone 3 the same inverter operates between $V_{dc1}/2$ and its full dc-link voltage. This symmetry leads to natural NPC VSI's dc-link capacitor voltage balancing using either PD PWM or APOD PWM.

The final gating signals are derived from (2) and (3) and the relationships given in the previous section, but with dead-time included.

TABLE III. VSI OPERATION VS. REFERENCE ZONE (2L-OEW-2L DRIVE).

Ref. zone	Range in Fig. 3	VSI_1	VSI_2
1	0 to 1/3	holds 0	PWM
2	1/3 to 2/3	PWM	PWM
3	2/3 to 1	holds V_{dc1}	PWM

TABLE IV. VSI OPERATION VS. REFERENCE ZONE (3L-OEW-2L DRIVE).

Ref. zone	Range in Fig. 3	VSI_1	VSI_2
1	0 to 1/3	PWM (0 and $V_{dc1}/2$)	holds V_{dc2}
2	1/3 to 2/3	holds $V_{dc1}/2$	PWM
3	2/3 to 1	PWM ($V_{dc1}/2$ and V_{dc1})	holds 0

IV. SIMULATION RESULTS FOR THE CASE OF CONTROLLABLE DC-LINK VOLTAGE SOURCES

Numerical simulation of the two topologies is performed using Matlab/Simulink. The VSIs are modelled with a dead-time of 6 μs and PWM switching frequency of 2 kHz. The five-phase induction machine parameters are given in [13]. The first set of simulation results is obtained using ideal dc-sources for dc-link voltage formation in order to prevent dc-link capacitor overcharging. Waveforms for 2L-OeW-2L are shown in Figs. 4 and 5 for modulation index (M) equal to 1 and 0.5, which is defined as a ratio between the reference amplitude and $V_{dc}/2$. Phase voltage waveforms in Fig. 4 are the same as in [14], showing presence of voltage spikes since SRA is not implemented. The same phenomenon, but less visible due to naturally higher ripple, is present in Fig. 5, for APOD PWM. It should be noted that the phase voltage

waveforms produced when SRA [14] is implemented are much finer, since dead-time spikes are eliminated. In this case the phase voltage looks exactly the same as in corresponding cases for 3L-OeW-2L, depicted in Figs. 6 and 7. However, SRA increases the control complexity and requires current measurement, even for open-loop *V/f* control [14].

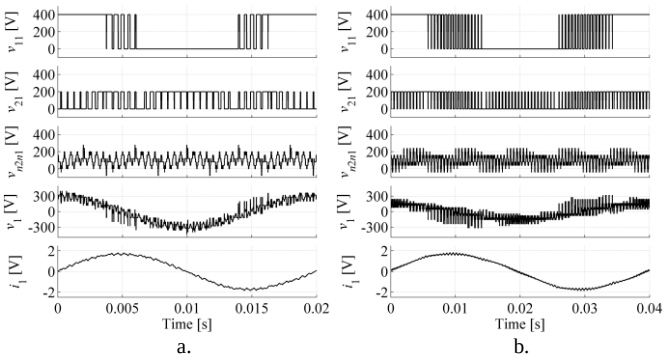


Fig. 4. Simulation results for 2L-OeW-2L PD, $M = 1$ (a), $M = 0.5$ (b).

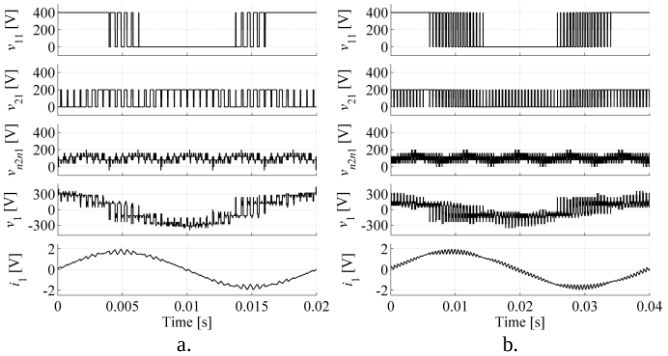


Fig. 5. Simulation results for 2L-OeW-2L APOD, $M = 1$ (a), $M = 0.5$ (b).

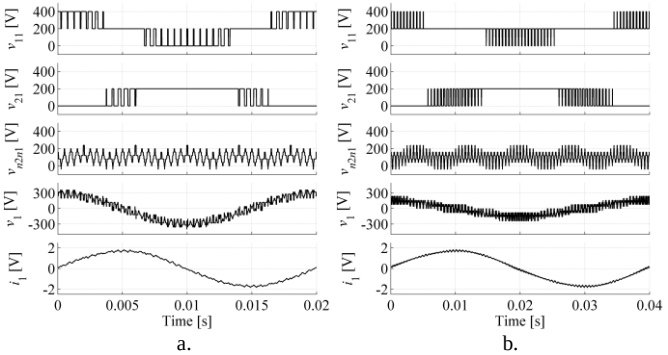


Fig. 6. Simulation results for 3L-OeW-2L PD PWM, $M = 1$ (a), $M = 0.5$ (b).

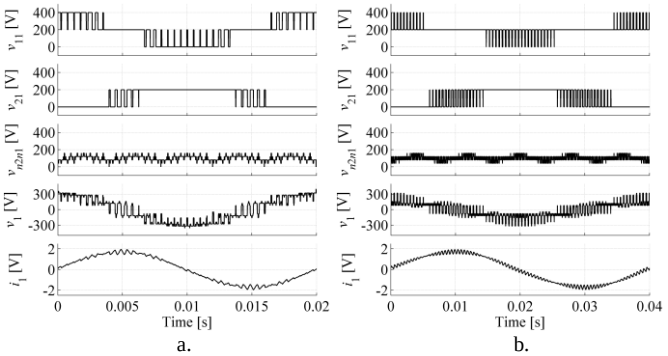


Fig. 7. Simulation results for 3L-OeW-2L APOD, $M = 1$ (a), $M = 0.5$ (b).

As explained in [13, 14], the 2L-OeW-2L drive naturally operates in two-level mode when $M < 0.35$. Alternatively, this modulation can be performed using only VSI_2, which eliminates dead-time induced spikes [14]. Differences in the two types of two-level output waveforms are visible in Fig. 8.

Similarly, the 3L-OeW-2L drive naturally performs two-level modulation for $M < 0.35$. It is also capable of working in three-level mode, for $M < 0.7$. This can be achieved by a simple modification of the modulation strategy in such a way that only VSI_1 operates in PWM mode, while VSI_2 connects all its output leg voltages to the same dc-link rail, forming a star connection on that OeW side. Waveforms for this case are given in Fig. 9. Although this modification does not improve harmonic performance, it can be used to reduce the switching losses. In general, both drives are capable of operating with variable number of voltage levels (depending on M) by simple modifications of modulation strategies, as summarised in Table V.

The phase voltage and stator current total harmonic distortions (THDs) are plotted against modulation index in Figs. 10 and 11 for the considered topologies. As explained in [14] for the 2L-OeW-2L drive, the dead-time spikes are responsible for harmonic distortion when the drive operates in the low and medium modulation index range ($M < 0.7$). This is especially dominant for two-level operation ($M < 0.35$), (black line in Fig. 10), since the entire phase voltage reference is located in zone 2, where spikes occur. However, if only VSI_2 is used for $M < 0.35$ (blue '+' in Fig. 10), the THD is significantly reduced. Three-level operation with 2L-OeW-2L is based on reference comparison with two carrier signals (C_1 and C_2, or C_2 and C_3), which means that in one reference zone only VSI_2 is in PWM mode, while in zone 2 (associated with C_2) both inverters operate. This asymmetry increases the dead-time influence on low-order current harmonics. Hence, this operation mode does not meet expectations.

TABLE V. VSI OPERATION FOR DIFFERENT OPERATING MODES.

Number of levels	*M* range	VSIs PWM operation	
		2L-OeW-2L	3L-OeW-2L
2	0 – 0.35	VSI_1 and VSI_2	VSI_2
		VSI_2	
	0 – 0.7	VSI_1	n/a
3	0 – 0.7	VSI_1 and VSI_2	VSI_1
4	0.35 – 1.05	VSI_1 and VSI_2	VSI_1 and VSI_2

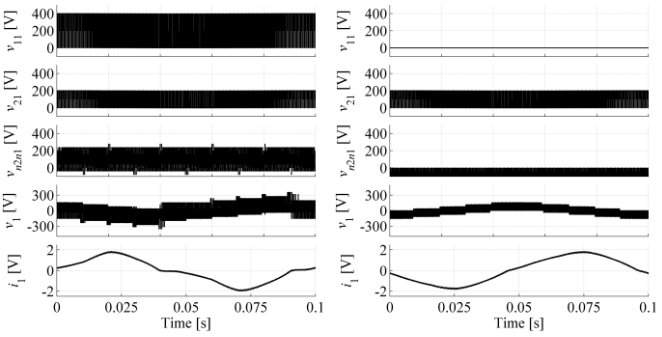
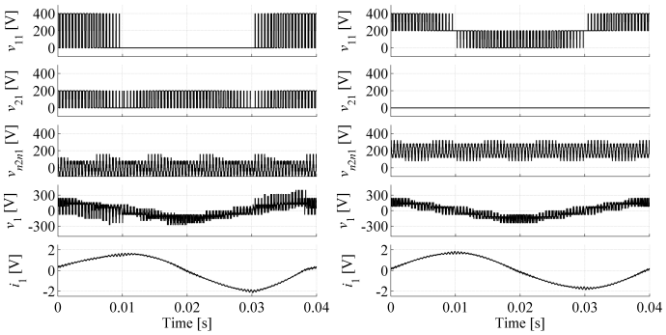
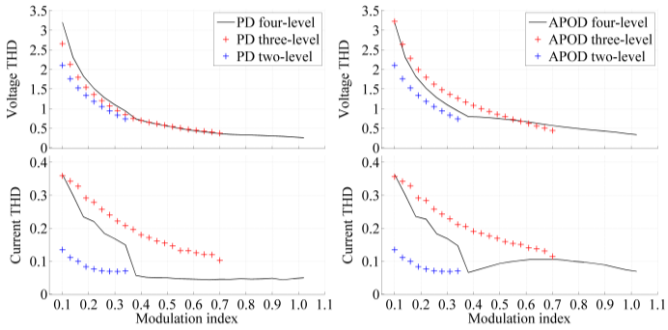


Fig. 8. Two-level operation and $M = 0.2$: 2L-OeW-2L with both inverters in PWM mode (a) and with only VSI_2 in PWM mode (b).



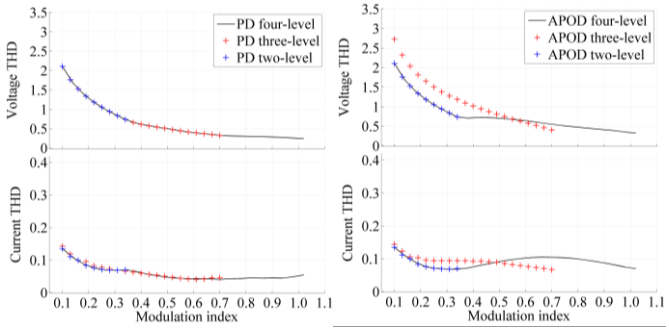
a. b.

Fig. 9. Three-level operation with PD PWM and M = 0.5: 2L-OeW-2L with both inverters in PWM mode (a) and for 3L-OeW-2L with only VSI_1 in PWM mode (b).



a. b.

Fig. 10. Phase voltage and stator current THD against M for 2L-OeW-2L drive, with PD (a) and APOD (b) PWM.



a. b.

Fig. 11. Phase voltage and stator current THD against M for 3L-OeW-2L drive, with PD (a) and APOD (b) PWM.

In contrast to this, 3L-OeW-2L topology has identical performance for both open-end mode and the equivalent of single-sided two-level operation mode (Fig. 11). Furthermore, three-level single-sided operation results in approximately the same harmonic performance as the OeW four-level drive for $M < 0.7$. This feature can be used to reduce the drive switching losses.

V. Simulation Results for the Case of Uncontrollable Dc-link Voltage Sources

Analysis of dc-link capacitor overcharging problem requires detailed discussion of the dc-link current flow. From Figs. 1 and 2, capacitor currents are determined with:

$$\begin{aligned} i_{cdc1} &= i_{dc1} - i_{dclink1} \\ i_{cdc2} &= i_{dc2} - i_{dclink2} \end{aligned} \tag{5}$$

$$\begin{aligned} i_{cdc11} &= i_{dc1} - i_{dclink1} \\ i_{cdc12} &= i_{dc1} - i_{dclink1} - i_{mp} \\ i_{cdc2} &= i_{dc2} - i_{dclink2} \end{aligned} \tag{6}$$

Equation (5) describes dc-link capacitor balancing for the 2L-OeW-2L drive, while (6) gives corresponding system of equations for the 3L-OeW-2L topology. Detailed analysis of the dc-link charging problem requires analysis of inverter's operation and conductance of each semiconductor device, in order to determine $i_{dclink1}$ and $i_{dclink2}$ currents. However, having in mind relationship between capacitor voltage and current:

$$v_c(t_1) = \frac{1}{C}\int_{t0}^{t1} i_c dt + v_c(t_0) \tag{7}$$

where $v_c(t_1)$ is capacitor voltage at $t = t_0$ and C is capacitance value, it is clear that $i_c < 0$ will lead to reduction of capacitor voltage, while $i_c > 0$ will increase v_c (with regard to the $v_c(t_0)$). The second important conclusion for this analysis comes from energy flow analysis. Namely, since all dc-link voltages are constant and positive, it is clear that dc voltage sources V_{dc1} and V_{dc2} (Figs. 1 and 2) should always have positive current in order to source power to the rest of the drive. Therefore, current unidirectional voltage sources for dc-link formation are usually used. The simplest circuitry, suitable for this application in medium and high-power range, is three-phase diode rectifier with suppressed output voltage [18]. Due to diode characteristics, current can flow only from diode rectifier ac to its dc side. In other words, currents i_{dc1} and i_{dc2} in (5) and (6) are never negative. If so, when for some reason $i_{dclink1}$ and $i_{dclink2}$ are negative, some charge might be added to the capacitor, even for i_{dc1} and/or i_{dc2} equal to 0. Similar, well-known overcharging mechanism is related to the drive braking process, where axillary circuit is usually used for energy dissipation. Power loss during braking process is undesired, but it takes a small part in drive operation, making losses tolerably small. However, it is shown in [16, 17] that 2L-OeW-2L drive suffers from overcharging problem during regular drive operation, making the energy dissipated in the resistor drastically higher.

In order to consider this problem in more detail, another simulation is performed. Three-phase diode rectifier models are included in simulation, together with large dc-link capacitors (of 1.5 mF). Figs. 12a and 12b show the dc-link voltages of each inverter for the 2L-OeW-2L and 3L-Oew-2L topologies, respectively. Once steady state is reached (at t = 0.5 s), the dc-link voltage supplies are changed from controllable to uncontrollable mode. In the case of the 2L-OeW-2L drive, Fig. 12a shows that the lower dc-link voltage capacitor is over-charged, while Fig. 12b shows that the 3L-OeW-2L does not have this issue. The reason for the dc-link voltage increase in the 2L-OeW-2L case can be found in the different switching operation of the two VSIs, leading to a different power flow. Namely, the 2L-OeW-2L drive in reference zone 3 holds VSI_1 leg output high (400 V, $S_{1k} = 1$, Table III), while VSI_2 works in PWM mode. It follows that, every time $S_{2k} = 1$, k^{th} drive phase is connected between 400 V and 200 V. Positive phase current in that case flows

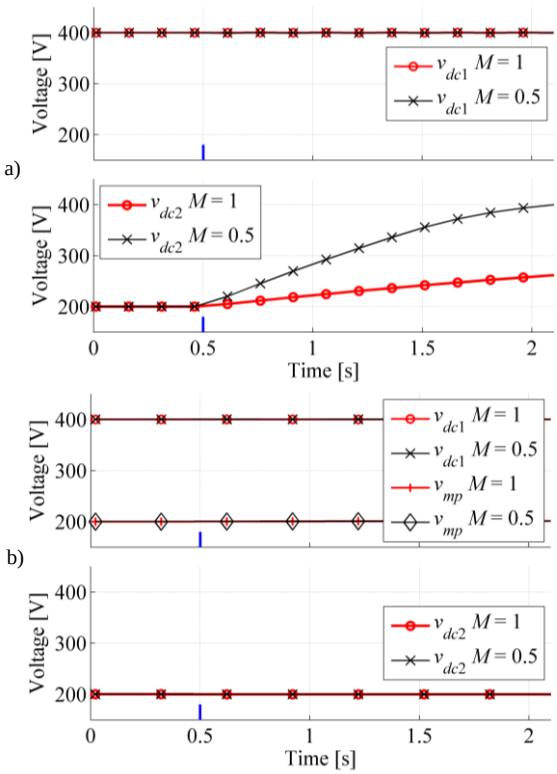


Fig. 12. Dc-link voltages for 2L-OeW-2L (a) and 3L-OeW-2L (b).

through D_{up2k}, which increases dc-link voltage. This state is symmetrical with the state $S_{1k} = 0$, $S_{2k} = 1$, when the same k^{th} drive phase is connected between 0 and 200 V in zone 1. In this case the capacitor will be discharged through S_{up2k} for $i_k < 0$. However, since phase angle between v_k and i_k is different from 90°, symmetry exists only in terms of switching state triggering, but not in the conduction of D_{up2k} and S_{up2k}, which directly leads to capacitor overcharging issue. Combined with simultaneous dead-time intervals in zone 2, influence of M, and the fact that phase angle depends not only on the machine parameters, but also on the machine load, it is clear that this problem has complex nature (which is beyond the scope of this paper) and balancing between sinking and sourcing power is hard to achieve in practice. The 3L-OeW-2L topology always sinks power from all of its dc-links, which means that the overcharging issue does not exist in this topology, as demonstrated in Fig. 12b.

VI. Conclusion

Two four-level five-phase OeW drives are analysed and compared in this paper. The first drive topology consists of a five-phase induction machine and two two-level inverters (2L-OeW-2L), supplied from unequal and isolated dc-link voltages, in the ratio 2:1. Unfortunately, several drawbacks seriously affect the drive performance and its feasibility for high power applications. The most serious one is the dc-link capacitor overcharging on the lower dc-link voltage side, which leads to a fully controllable dc-source requirement.

The paper demonstrates that these problems are completely eliminated by replacing high dc-link voltage side's two-level inverter with three-level NPC VSI, while dc-link voltage ratio is kept the same. This novel topology (3L-OeW-2L) also provides four-level phase voltage waveform. Performance of both drives is examined by numerical simulation. Comparison of the results shows that 3L-OeW-2L drive has a superior performance. However, it has to be noted that this improvement is associated with higher hardware complexity.

References

[1] E. Levi, "Multiphase electric machines for variable-speed applications," *IEEE Trans. on Ind. Electronics*, vol. 55, no. 5, pp. 1893-1909, 2008.

[2] Y. Wang, T. A. Lipo, and D. Pan, "Robust operation of double-output AC machine drive," in *Proc. Int. Conf. Power Electronics ICPE & ECCE Asia*, Jeju, Korea, pp. 140-144, 2011.

[3] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverter drives," in *Proc. European Power Electronics and Applications Conf. EPE*, Brighton, UK, pp. 7-14, 1993.

[4] K. Corzine, S. Sudhoff, and C. Whitcomb, "Performance characteristics of a cascaded two-level converter," *IEEE Trans. on Energy Conv.*, vol. 14, no. 3, pp. 433-439, 1999.

[5] H. Toliyat, and H. Xu, "A novel direct torque control (DTC) method for five-phase induction machines," in *Proc. IEEE Applied Power Electronics Conf. and Expo. APEC*, New Orleans, USA, pp. 162-168, 2000.

[6] E. Levi, R. Bojoi, F. Profumo, H. Toliyat, and S. Williamson, "Multiphase induction motor drives–a technology status review," *IET Electric Power Applications*, vol. 1, no. 4, pp. 489-516, 2007.

[7] M. Jones, S. N. Vukosavic, D. Dujic, and E. Levi, "A synchronous current control scheme for multiphase induction motor drives," *IEEE Trans. on Energy Conv.*, vol. 24, no. 4, pp. 860-868, 2009.

[8] A. Mohammadpour, S. Sadeghi, and L. Parsa, "A generalized fault-tolerant control strategy for five-phase PM motor drives considering star, pentagon, and pentacle connections of stator windings," *IEEE Trans. on Ind. Electronics*, vol. 61, no. 1, pp. 63-75, 2014.

[9] H. Guzman, M. J. Duran, F. Barrero, B. Bogado, and S. Toral, "Speed control of five-phase induction motors with integrated open-phase fault operation using model-based predictive current control techniques," *IEEE Trans. on Ind. Electronics*, vol. 61, no. 9, pp. 4474-4484, 2014.

[10] L. Shuai and K. Corzine, "Multilevel multi-phase propulsion drives," in *Proc. IEEE Electric Ship Technologies Symp. ESTS*, Philadelphia, USA, pp. 363-370, 2005.

[11] G. Grandi, P. Sanjeevikumar, and D. Casadei, "Preliminary hardware implementation of a six-phase quad-inverter induction motor drive," in *Proc. European Power Electronics and Applications Conf. EPE*, Birmingham, UK, pp. 1-9, 2011.

[12] N. Bodo, E. Levi, and M. Jones, "Investigation of carrier-based PWM techniques for a five-phase open-end winding drive topology," *IEEE Trans. on Ind. Electronics*, vol. 60, no. 5, pp. 2054-2065, 2013.

[13] M. Darijevic, N. Bodo, M. Jones, and E. Levi, "Four-level five-phase open-end winding drive with unequal dc link voltages," in *Proc. European Power Electronics and Applications Conf. EPE*, Lille, France, pp. 1-10, 2013.

[14] M. Darijevic, M. Jones, and E. Levi, "Analysis of dead-time effects in a five-phase open-end drive with unequal dc link voltages," in *Proc. IEEE Ind. Elec. Soc. Annual Conf. IECON*, Vienna, Austria, pp. 5134-5139, 2013.

[15] E. Levi, I. N. W. Satiawan, N. Bodo, and M. Jones, "A space vector modulation scheme for multi-level open-end winding five-phase drives," *IEEE Trans. on Energy Conv.*, vol. 27, no. 1, pp. 1-10, 2012.

[16] M. Jones, M. Darijevic, and E. Levi, "Decoupled modulation techniques for a four-level five-phase open-end winding drive," in *Proc. IEEE Energy Conv. Congr. and Exhibition ECCE*, Pittsburgh, USA, pp. 178-186, 2014.

[17] B. V. Reddy and V. T. Somasekhar, "A dual inverter fed four-level open-end winding induction motor drive with a nested rectifier-inverter," *IEEE Trans. on Ind. Informatics*, vol. 9, no. 2, pp. 938-946, 2013.

[18] J. W. Kolar and H. Ertl, "Status of the techniques of three-phase rectifier systems with low effects on the mains," in *Proc. Int. Telecomm. Energy Conf. INTELEC*, Copenhagen, Denmark, pp. 1-16, 1999.