Darijevic, M, Jones, M and Levi, E

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An Open-end Winding Four-level Five-phase Drive

Milan Darijevic, *Student Member*, *IEEE*, Martin Jones, Emil Levi, *Fellow, IEEE*

Abstract–A four-level five-phase open-end winding (OeW) drive topology is introduced in the paper. The drive comprises a five-phase induction machine with open-end stator windings, supplied using two two-level voltage source inverters with isolated and unequal dc-link voltages, in the ratio 2:1. The topology offers the advantages of a modular structure with fewer semiconductor components and has a greater potential for fault tolerance, compared to an equivalent single-sided four-level drive. Due to the large number of switching states, development of a suitable space-vector pulse-width modulation (SVPWM) method can be challenging. Hence, this paper examines the implementation of two level-shifted carrier-based modulation (CBPWM) methods. The effect of dead time on the drive performance is discussed and it is shown that simultaneous PWM switching of both inverters can lead to degraded output phase voltage waveforms. Detailed analysis of this phenomenon is presented, a solution is proposed, and the modified modulation techniques are incorporated in an experimental set-up, at first in conjunction with *V/f* control. Once when the proof-of-concept has been provided, full field oriented control (FOC) is implemented in this OeW drive topology for the first time; detailed experimental testing is conducted and results are reported.

Index Terms–Multiphase drives, open-end winding, pulse width modulation, induction motor drives, field oriented control.

I. INTRODUCTION

Owing to the constraints of the current semiconductor technology multilevel converters are often regarded as a solution for high-power applications [1]. Multilevel inverters are a topology which enhances the quality of the output voltage waveform, reduces dv/dt and enables the construction of a high power converter without the problem of switching series-connected semiconductor devices. High power drives can be found in industrial sectors such as the mining, petrochemical, cement and marine industries [1]. Commonly employed multilevel converters are the neutral point clamped (NPC), the flying capacitor (FC) and the various cascaded converter topologies (CB) [2-4]. Commercially available NPC, FC and CB converters include the Converteam MV7000, the Alstom Alspa VDM 6000 and the Siemens Perfect Harmony range, respectively [1]. Multi-

phase drives are also considered as being well suited to medium- and high-power applications [5, 6]. Merging these two concepts seems natural, and several attempts have been reported recently [6-13].

The open-end winding (OeW) topology, originally described in [4], can be considered as an alternative approach to create multilevel phase voltage waveforms [14]. OeW drives offer some advantages over conventional multilevel drives. One advantage is the reduced component count [9, 14] compared to traditional equivalent NPC and FC converters. For example, a five-phase four-level NPC converter requires an additional 30 diodes and 10 switches while the equivalent FC converter requires an additional 10 capacitors, diodes and switches. Another advantage is the capability of the OeW topology to operate under faulted conditions [15, 16]. It has been suggested in the literature that such drives may offer an alternative supply solution in applications such as EVs/HEVs [17, 18], electric ship propulsion [19], rolling mills [20] and renewable electric energy systems [21].

One disadvantage of this topology is that two isolated dc power supplies are required to feed the inverters in order to eliminate a path for zero-sequence current flow. A second disadvantage is that, if the dc-link voltages are in a ratio 2:1, the switches in the higher voltage dc-link will need to tolerate twice the voltage than in the equivalent four-level NPC or FC converters [14]. For these reasons the configuration considered here is not suitable for high voltage applications, but may be an interesting solution for EV/HEV applications. The requirement for isolated dc-links does not present a problem in EV/HEV applications where the isolated supplies can be formed using batteries. In these applications, where the dc-link voltage is rather low and limited, a machine with a lower current rating can be utilized since the voltage across phases can be higher when two independent batteries are used instead of a single one [18]. Moreover, the multiphase structure offers further advantages such as a reduction of the per-phase current rating for a given machine power compared to the three-phase alternative, the possibility of increased torque density, increased fault tolerance [5, 6] and lower acoustic noise [22], all attractive attributes for EVs and HEVs. Furthermore, multiphase machines are under investigation in the framework of on-board integrated battery chargers [23, 24].

Application of two isolated two-level inverters with equal dc-link voltages enables drive operation with voltage waveform equivalent to that obtainable with a three-level voltage source inverter (VSI) in the single-sided supply mode [14]. Compared to the equal dc-link voltage topology, having different dc-link voltages can lead to more voltage levels, which can further improve drive performance [25]. Use of dc-link voltages in the ratio of 2:1 enables performance equivalent to the four-level VSI [14]. Until very recently [26, 27], dc links with unequal voltages have been

studied in relation to only three-phase drives [28-30] where the space vector modulation technique was used to control the inverters. The drive is able to produce 37 phase voltage space vector locations forming 54 equilateral triangular sectors [28]. The developed SVPWM algorithm requires large look-up tables in order to identify the sector the reference occupies and the switching sequences to be applied, making the scheme difficult to implement. A fractal based SVPWM method with low computational burden is proposed in [29]; it relies on the fact that a three-phase system produces simple triangular subsectors. This technique cannot be easily adapted to five-phase drives since the five-phase system does not produce such uniformly distributed subsectors and there is also more than one plane to consider.

The modulation strategies discussed so far consider both inverters as a single "coupled" entity. A decoupled SVPWM algorithm which views the inverters as individual two-level converters is discussed in [30]. The method is based on sharing the reference between two inverters in the same ratio as the dc-link voltages, i.e. 2:1, with both inverters having the same switching frequency. A second strategy utilizes switching of the two inverters using switching frequencies that are proportional to their dc-link voltage with respect to the overall dc-link voltage. Power losses that come from switching losses are equalized between inverters in this way.

In the case of multiphase multilevel drives the large number of switching states and voltage space vectors, combined with the requirement to consider several planes simultaneously in order to achieve optimum performance [5], means that carrier based PWM methods are preferable due to simplicity. Comparison of CBPWM and SVPWM methods shows that CBPWM is capable of achieving the same level of performance as the SVPWM method while requiring a much reduced computational burden [11]. It is for these reasons that CBPWM methods are analyzed here.

Two modulation strategies, with carriers having in-phase disposition (PD) and alternative phase opposition disposition (APOD) are developed and investigated using simulations in [26]. It is shown that the operating mode of the converter can be selected using a simple reference offset; hence the switching losses can be reduced when the drive operates at low speeds. In this paper these modulation methods are examined experimentally using a four-level five-phase OeW induction machine drive prototype for the first time. It is shown that, in this topology, the inverter dead time has a stronger influence on drive performance than in the configurations analyzed in the past. This is because of simultaneous dead-time intervals in two inverters, which causes triggering of unwanted voltage levels and additional distortion of the phase voltage waveforms. The paper experimentally investigates the dead-time spike phenomenon and a simple alteration to the PWM strategies, which minimizes the occurrence of so called dead-time spikes, is proposed and evaluated. There is no evidence in literature that application and implementation of carrier-based PWM and dead-time induced voltage spikes in four-level multiphase drive systems with an OeW configuration has been studied until now, except for the simulation study in [27], which is the starting point for this paper. It is demonstrated that the spike removal algorithm (SRA) is very effective and that closed-loop current control alone cannot mitigate the issue. The paper also investigates for the first time the performance of the four-level drive under field

oriented control (FOC). The current controllers in the x-y plane are synchronized to the dominant dead-time generated harmonics (i.e. the 3rd and 7th).

The paper builds on previous work reported in [26, 27]. It begins with a description of the topology, along with the impact of the dc-link voltage ratio, before describing the developed modulation methods. Next, the dead-time induced voltage spike phenomenon is described and a solution for the dead-time spikes removal is introduced. Experimental investigation of the problem follows, together with the experimental verification of the developed solution, using open-loop V/f control. Performance of the modulation techniques is thus not influenced by the current controllers. Finally, implementation of closed-loop current control in conjunction with FOC is described and a high-performance multilevel multiphase OeW drive is realized and experimentally tested for the first time.

II. MULTIPHASE OPEN-END WINDING TOPOLOGY WITH DUAL INVERTER SUPPLY AND UNEQUAL DC-LINK VOLTAGES

The drive consists of a five-phase induction machine, supplied via two isolated two-level PWM voltage source inverters (VSI), as shown in Fig. 1, where VSI$_1$ is supplied from V_{dc1}, and VSI$_2$ is supplied from V_{dc2}. Leg voltages of two VSIs, v_{1i} and v_{2i}, are defined with respect to the inverters' lower dc-link rails, denoted with $N1$ and $N2$ in Fig. 1. Actual phase voltage can be calculated as:

$$v_i = v_{1i} - v_{2i} - v_{N2N1} \tag{1}$$

where v_{N2N1} represents the potential difference between two bottom rails of VSI$_1$ and VSI$_2$ dc links, that is, common mode voltage. However, in order to establish correlation between this topology and an equivalent drive with single-sided supply, one can use an equivalent drive model, as explained in [26], which represents a single-phase equivalent open-end configuration (denoted with dashed box in Fig. 1), suitable for comparison with multilevel inverters. In this case, voltage potentials of $N1$ and $N2$ are equal, and phase voltage in the equivalent model can be compared with leg outputs of single-sided multilevel inverters.

Let us define next the switching states S_{ji}, which correspond to the jth inverter and i^{th} phase in Fig. 1. Switching state is equal to the state of upper switch, 1 if S_{upij} is turned on, and 0 otherwise. Clearly, there are 4 possible combinations in the equivalent model, as listed in Table I. For each of them, leg voltage outputs are defined with regard to the dc-link voltage ratio r:

$$r = \frac{V_{dc1}}{V_{dc2}} = \frac{V_{dc} - V_{dc2}}{V_{dc2}} \tag{2}$$

where $V_{dc1} \geq V_{dc2}$ and V_{dc} represents the dc-link voltage of the equivalent single-sided supply ($V_{dc} = V_{dc1} + V_{dc2}$). Setting $r = 1$, results in an OeW drive which is equivalent to the three-level single-sided topology. In that case states with $N = 1$ and $N = 4$ in Table I result in the same equivalent phase voltage level. This case is analyzed in detail in [12, 13]. For $r > 1$ the number of phase voltage levels will be four, and the number of space vectors will increase. The first important consequence of $r > 1$ is absence of redundant switching states that exist in the case of equal dc-link voltages, meaning that each switching state results in a different equivalent voltage level. In general, three out of four equivalent phase voltage levels are actually dependent

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on r. Therefore, it is important to determine the influence of the dc-link voltage ratio on the drive properties.

In order to allow easier comparison with other solutions, the drive properties are initially analyzed using the vector space decomposition approach [5]. Since the drive comprises two two-level five-phase inverters, overall number of switching states is $2^5 \times 2^5 = 1024$. The influence of the dc-link voltage ratio on the space vector magnitudes is illustrated in Fig. 2, where circular lines apply to the first sector, and radial lines apply to the ninth sector. Phase voltage space vectors for $r = 1.5$ and 3 are more clustered, while $r = 2$ provides a more homogeneous vector distribution. Table I shows that only $r = 2$ provides equidistant phase voltage levels. In this case, 781 voltage space vectors are generated, of the same values as in the case of a single-sided four-level inverter. When $r = 1$, 211 voltage space vectors are available [12]; hence, from this point of view, better performance can be expected in the case when $r = 2$.

III. DEVELOPED MODULATION TECHNIQUES

Setting $r = 2$ and using the overall dc-link voltage $V_{dc} = 600$ V, results in $V_{dc1} = 400$ V and $V_{dc2} = 200$ V. Since four switching combinations of two inverters in one drive phase are possible (Table I), four different equivalent phase voltage levels, -200 V, 0, 200 V and 400 V, result. Consequently, three carrier signals are required. Reference voltage of one phase, with min-max injection [8] and carriers for both PD and APOD PWM, are shown in Fig. 3, where all signals are normalized with V_{dc} and zero per-unit value corresponds to the lowest voltage level (-200 V). Modulation index (M) is defined as a ratio between the reference amplitude and one half of the total dc-link voltage $V_{dc}/2$. Hence, assuming zero-sequence (min-max) injection, the modulation index spans 0 to 1.05 range.

Comparison of the reference and carriers (Fig. 3) produces three logic variables A_{1i}, A_{2i} and A_{3i}:

$$A_{ki} = \begin{cases} \text{if } v_i^* > C_k & \text{then 1} \\ \text{if } v_i^* < C_k & \text{then 0} \end{cases} \tag{3}$$

where v_i^* is the reference voltage for the ith phase, while C_k is a carrier. Since there are two inverters and three carrier signals, the inverter switching states, S_{ji}, cannot be obtained directly from variables A_{1i}, A_{2i} and A_{3i}. Table II shows the Karnaugh maps that are used to derive the simplest conversion from logic variables A_{ki} to switching signals S_{ji}. The sum-of-product form was chosen, which provides relations:

$$S_{1i} = A_{2i}$$
$$S_{2i} = \overline{A}_{3i} \cdot A_{2i} + \overline{A}_{1i} \tag{4}$$

These apply to both PD and APOD PWM. Table II shows that there are "don't care states", marked with "X". These states represent logic states (A_{1i}, A_{2i}, A_{3i}) which cannot occur. For example $A_{1i} = 0$, $A_{2i} = 1$, $A_{3i} = 0$ is not possible since the reference (v_i^*) cannot be less than C_1 while at the same time being greater than C_2 or C_3. From Fig. 3, it can be concluded that the instantaneous reference value can belong to one of the three so-called reference zones, defined with voltage levels. This is summarized in Table III, together with operation mode in each of the zones of the two VSIs.

Since two dc-link voltages are isolated and unequal, one additional parameter is introduced. Reference offset (R_{offset}) represents a harmless dc component in the common mode

TABLE I. RELATIONSHIP BETWEEN SWITCHING STATES, LEG AND EQUIVALENT PHASE VOLTAGES IN GENERAL FORM.

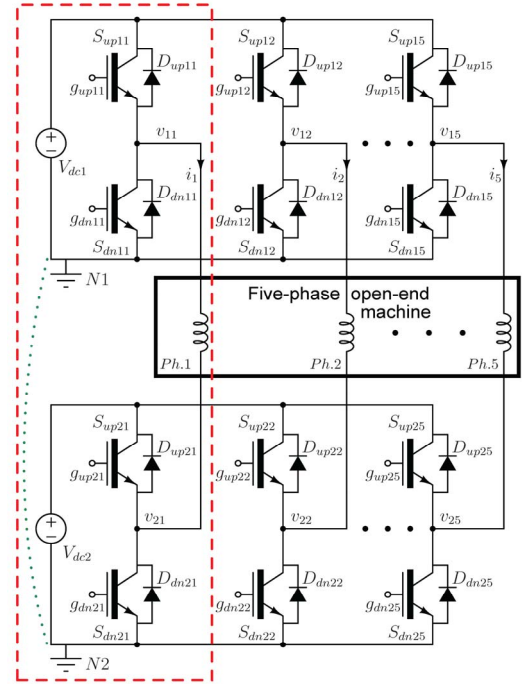| N	S_{1i}	S_{2i}	v_{1i} [V]	v_{2i} [V]	Equivalent v_i [V]
1	1	1	$r \cdot V_{dc}/(r+1)$	$V_{dc}/(r+1)$	$(r-1) \cdot V_{dc}/(r+1)$
2	1	0	$r \cdot V_{dc}/(r+1)$	0	$r \cdot V_{dc}/(r+1)$
3	0	1	0	$V_{dc}/(r+1)$	$-V_{dc}/(r+1)$
4	0	0	0	0	0

Fig. 1. Open-end winding n-phase topology with dual two-level inverter supply. One drive's phase that represents equivalent drive model is boxed within the dashed line.

Fig. 2. Phase voltage space vectors for $r = 1$ (a), 1.5 (b), 2 (c) and 3 (d).

voltage (CMV) v_{N2N1} (Fig. 1), which can be used for selecting different operating modes [26]. In Fig. 3, $R_{offset} = 1/2$ is used, since full dc-link voltage utilization is needed for modulation indices higher than 0.7, for the case when min-max injection is applied. This reference offset value leads to two-level operation in low modulation index range ($0 < M \le 0.35$), since reference will be completely in the second reference zone (Fig. 3, Table III). For $M > 0.35$, the same reference offset leads to four-level operation. It can

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be seen that two-level operation, which is used in low modulation index range, is formed with simultaneous switching in two VSIs, since both inverters operate in PWM mode in reference zone 2 (Table III). This leads to additional switching losses. Therefore, two-level operation can be utilized by setting $R_{offset} = 1/6$ or $5/6$. In these two cases, common mode voltage dc component will be different, but only VSI$_2$ will operate in PWM mode, while all leg voltages of the VSI$_1$ will be on the same voltage potential. Consequently, VSI$_1$ forms star connection between stator windings, for $M \leq 0.35$. R_{offset} influence on the number of voltage levels is depicted in Fig. 4.

Reference offset can be used to achieve three-level operation. This could be done, for low ($M \leq 0.35$) and medium modulation index range ($0.35 < M < 0.7$), by setting R_{offset} to either $1/3$ or $2/3$. In these cases the phase voltage reference will pass through two reference zones (Fig. 4, Table III), leading to different switching behavior depending on the reference zone. For example, when R_{offset} is $1/3$, both inverters will operate in PWM mode when reference passes through 2nd reference zone, while only VSI$_2$ will operate in the reference zone 1. This asymmetrical operation leads to increased low order harmonic content in phase voltage and current spectra. Therefore, in the proposed solution the drive will operate as two-level drive with only one VSI in PWM mode for $M \leq 0.35$, while for the rest of the modulation index range four-level operation will be utilized.

IV. DEAD-TIME INDUCED VOLTAGE SPIKES

In general, during dead-time intervals, output voltages of the VSIs are determined by the load current, which flows through antiparallel diodes. As a result, there are two possible scenarios [27]:

- In scenario 1, the phase voltage during dead time takes the value equal to one of the two voltage levels between which the transition is to be done.

TABLE II. MAPPING OF LOGIC VARIABLES (A_{ki}) AND INVERTER SWITCHING SIGNALS (S_{1i} (a) and S_{2i} (b))

(a) S_{1i}

A_{3i} ╲ A_{1i} A_{2i}	0 0	0 1	1 1	1 0
0	0	X	X	X
1	0	1	1	X

(b) S_{2i}

A_{3i} ╲ A_{1i} A_{2i}	0 0	0 1	1 1	1 0
0	1	X	X	X
1	0	1	0	X

TABLE III. OPERATION MODE OF VSIS VS. REFERENCE ZONE.

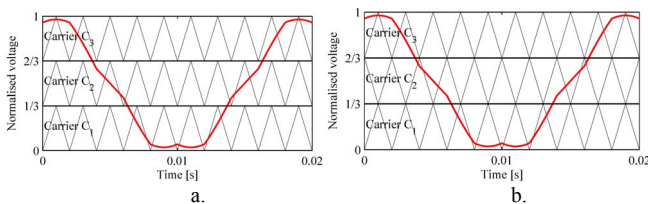| Ref. zone (k)	Range in Fig. 3	VSI$_1$	VSI$_2$
1	0 to $1/3 V_{dc}$	holds 0	PWM
2	$1/3 V_{dc}$ to $2/3 V_{dc}$	PWM	PWM
3	$2/3 V_{dc}$ to 1	holds V$_{dc1}$	PWM

Fig. 3. Reference voltage of one phase and carrier signals for PD PWM (a) and APOD PWM (b), for $M = 1$. Carrier frequency is 500 Hz, for better visualization.
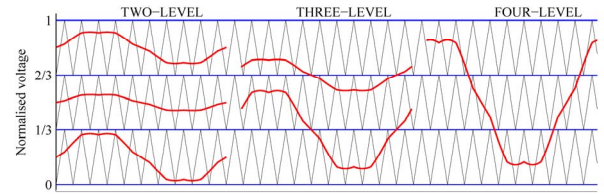

Fig. 4. Selection of different PWM modes using R_{offset}. Phase voltage reference for four-level operation is shown, for different modulation index and reference offset parameters.

- In scenario 2, the phase voltage during dead time takes the value which is different from both initial and final voltage level between which the transition is to be done.

As far as single-sided supplied drives are concerned, only scenario 1 is possible. For example, in a four-level NPC inverter [31], only one complementary switch pair in the leg will change state during transition between adjacent leg voltage levels. On the other hand, in a four-level open-end winding drive the voltage is formed as a difference of corresponding leg voltages of the two inverters. Scenario 1 will occur when transition from one phase voltage level to the adjacent voltage level is to be accomplished by switching one inverter only, while leg voltage of the second inverter in that phase remains unchanged.

When leg voltages in both inverters must be changed in order to make phase voltage transition between adjacent levels, scenario 2 will take place. This causes an unwanted phase voltage level during dead-time intervals. The direction of this voltage level is determined by the sign of the phase current. This phenomenon is explained in detail in [27] and is addressed here with the help of Fig. 1 and Fig. 5. Semiconductor states in the first phase, during the nth switching period ($T_S = 500$ µs), are shown in Fig. 5, for negative phase current and phase voltage reference in zone 2. For the purpose of discussion, dead time is set to 15 µs. The switch state is 1 when corresponding power transistor or diode conduct, otherwise it is 0. Since the phase current is negative in the whole switching period (with respect to notation in Fig. 1), diodes D_{up11} and D_{dn21} will conduct, while diodes D_{dn11} and D_{up21} will be turned off. Having in mind data in Table I, in the time instant $t = (n\text{-}1) \cdot T_S$ S_{up11} and S_{up21} should be turned on, which will result in equivalent phase voltage of $1/3 V_{dc}$. However, since the current i_1 is negative, S_{up11} will not conduct. Instead, antiparallel diode D_{up11} will be turned on, while complementary transistors, S_{dn11} and S_{dn21} are off. So the current will flow through S_{up21} and D_{up11}. This continues until $t = t_1$, when the first transition occurs. The equivalent voltage should change from $1/3 V_{dc}$ to 0 at t_1, however the dead-time interval will start in both inverter legs. End of the dead-time interval is marked with t_2. It follows that the phase voltage during interval $t_1 < t < t_2$ will not be determined by switches in this phase, but with phase current sign, which means that diodes D_{up11} and D_{dn21} will conduct and equivalent voltage level will be $2/3 V_{dc}$ rather than 0. The consequence of this transition is an unwanted voltage level (200 V) in the phase voltage (v_1), as shown in Fig 5. Similarly, at time instant determined with the second reference intersection with carrier signal ($t = t_3$), another dead-time spike will occur (of duration $t_4 - t_3$), with the same direction and amplitude.

From the control point of view, it is important to notice that both PWM strategies lead to the simultaneous switching of the VSIs (S_{1i} and S_{2i}). As a consequence, dead-time
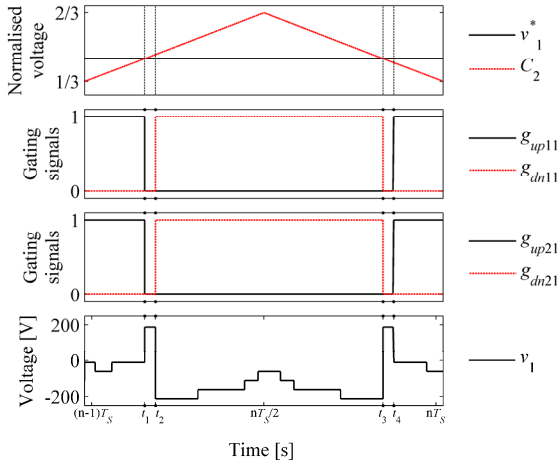
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Fig. 5. Example of gating signals formation based on phase voltage reference (v_1^*) and carrier C_2 comparison in the reference zone 2, for conventional PD PWM.
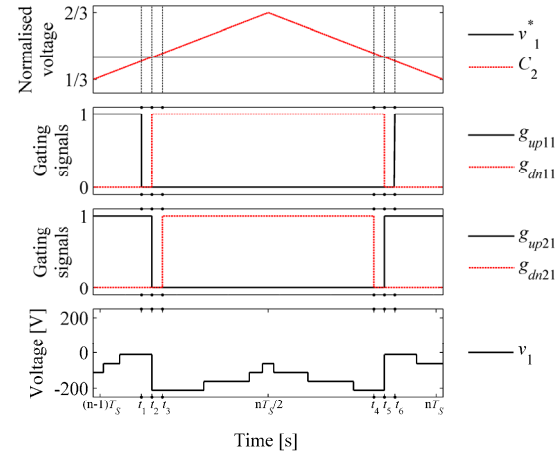

Fig. 6. Example of gating signals formation based on phase voltage reference (v_1^*) and carrier C_2 comparison in the reference zone 2, for PD PWM with implemented SRA.

intervals appear at the same time in both VSIs. Therefore, the dead-time spike elimination algorithm (SRA), proposed in [27], is based on reference shifting. This ensures that the gating signals are not changed at the same time. When this is applied to the situation described above, S_{up11} turns off followed by S_{up21}. Therefore, when S_{dn11} turns on the current flows through S_{dn11} and S_{up21} and the equivalent phase voltage is held at $1/3V_{dc}$. Next, S_{up21} switches off and the current flows through D_{dn21} and so the equivalent phase voltage is 0 as expected. This situation is shown in Fig. 6. The SRA results in a slightly asymmetrical phase voltage waveform. This does not lead to any significant harmonic distortion since similar waveforms, but with inverse asymmetry, will take place when the phase current changes its sign. Further details of the SRA follow in the next section along with analysis of the harmonic performance.

V. DEAD-TIME SPIKE ELIMINATION ALGORITHM

As described previously dead-time spikes can be eliminated by modification of the modulation strategy so that the dead-time intervals do not occur simultaneously in VS$_1$ and VSI$_2$ when the reference is in carrier zone 2. This can be achieved with addition or subtraction of a small reference offset, which will shift in time the reference intersection with the carrier signal. The reference offset should be set to:

$$\Delta r = (2/3)\Delta t \cdot f_s \cdot V_{dc} \tag{5}$$

where Δt is the dead-time duration. In this way, dead-time intervals in the same drive phase in two VSIs will take place one after another, rather than simultaneously. Although this is probably the simplest compensation method for dead-time spikes, it requires a different switching algorithm in the first and the second half of the switching period T_S (= $1/f_S$).

The algorithm is depicted in Fig. 7. For the nth switching period it can be summarized as follows:

- For $n \cdot T_S < t < (n + 0.5) \cdot T_S$ and $i_1 > 0$, reference will be increased by Δr in the case of VSI$_1$, while switching of the VSI$_2$ should be governed with the original reference value.
- For $(n + 0.5) \cdot T_S < t < (n + 1) \cdot T_S$ and $i_1 > 0$, reference for VSI$_1$ should remain unchanged, while switching of the VSI$_2$ should be determined with the reference value reduced by Δr.
- For $n \cdot T_S < t < (n + 0.5) \cdot T_S$ and $i_1 \leq 0$, only reference for VSI$_1$ should be reduced by Δr.
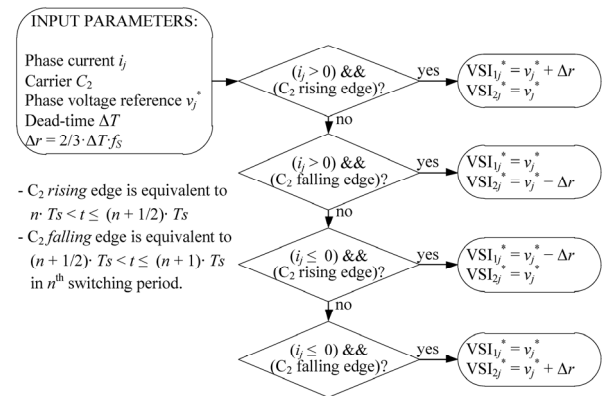

Fig. 7. Determination of the additional offset value that should be added to the voltage reference in zone 2 in order to eliminate dead-time spikes.

- For $(n + 0.5) \cdot T_S < t < (n + 1) \cdot T_S$ and $i_1 \leq 0$ only reference for VSI$_2$ should be increased by Δr.

As a result, dead-time interval will never coincide in the legs of two VSIs that are associated to the same phase. The modified PWM algorithm should be applied only when the reference is in zone 2. From the load perspective, this modification doubles the effective dead time, in comparison to the original PWM. This means that the antiparallel diodes will conduct twice longer and will either hold the current voltage level or switch to the next level, as in the scenario 1.

VI. EXPERIMENTAL RESULTS IN OPEN-LOOP V/f OPERATION

The results presented in this paper are obtained using the experimental system shown in Fig. 5. The control algorithms are developed and tested using dSPACE DS1006 processor board, while a DS5101 digital waveform output board is used for PWM generation. Two two-level VSIs are used to supply the five-phase induction machine. The machine parameters are provided in the Appendix. It is coupled to a dc machine and operated under no-load conditions, unless specified differently. The VSIs are supplied with unequal dc-link voltages of 400 V and 200 V. The higher dc-link voltage is obtained using a Sorensen SGI-600-25 dc supply. The lower dc-link voltage is obtained via a Spitzenberger controllable power supply. The carrier frequencies are 2 kHz and the semiconductor drivers have fixed dead time of 6 μs.

Firstly, the steady-state performance of the drive is investigated under open-loop V/f control for different modulation index values. This control method is used in

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order to determine the true performance of the CBPWM modulation techniques, without the inevitable influence of current controllers that will exist in FOC mode. Figs. 9-11 and Figs. 12-13 show oscilloscope recordings of the waveforms produced using APOD PWM and PD PWM without and with the spike removal algorithm, respectively. The leg voltages of VSI$_2$ and VSI$_1$, associated with the first drive phase (v_{11} and v_{21}), and the corresponding phase voltage (v_1) traces are given (channels 1, 2 and 3, respectively), together with the motor phase current (i_1, channel 4). The transient performance of the drive operating under FOC is investigated in the next section, where the results are recorded using the dSPACE system.

It has been shown that simultaneous switching in reference zone 2 leads to unwanted transitions in phase voltage, which are visible as unwanted voltage transitions (spikes). Therefore, spikes prevalence in produced phase voltage waveforms depends on how long phase voltage reference is in reference zone 2 per fundamental period. That is, for four-level operation, the occurrences of unwanted phase voltage levels are inversely proportional to M.

The phenomenon is illustrated in Figs. 9 and 10, during four-level operation with PD and APOD PWM methods. The waveforms show that dead-time spikes occur only when both VSIs are in PWM mode. The unwanted voltage levels (spikes) are less visible in the case of APOD PWM, since this modulation, under ideal conditions, already has higher voltage distortion than PD PWM. It is evident that the dead-time spikes are present only in the middle third of the phase voltage waveform, which corresponds to the reference crossing into the zone 2. It has to be noted that the VSI's leg voltages do not contain dead-time spikes, since they are a consequence of combining leg voltages during common dead-time intervals. Therefore, the erroneous voltage levels will not cause overvoltage damage to the VSI components, but may lead to high frequency EMI and acoustic noise. Two- level operation is shown in Fig. 11, which is the same for both PD and APOD PWM, since phase voltage reference is compared with the single carrier signal (since $R_{offset} = 1/6$, ref. zone 1). It is obvious that two-level operation does not lead to dead-time spikes if a suitable reference offset is selected causing only one inverter to switch.

Results of the spike removal algorithm (SRA) implementation in PD and APOD PWM are shown in figures 12 and 13, for $M = 1$ and 0.5, respectively. Waveforms for $M = 0.2$ are identical to those in Fig. 11, since only one inverter is in PWM mode, and reference is placed in zone 1, while SRA has effect on operation in zone 2 only.

Clearly, the dead-time spike elimination algorithm is very effective, but the non-ideal nature of the inverters leads to some practical limitations. Namely, SRA is conceptually
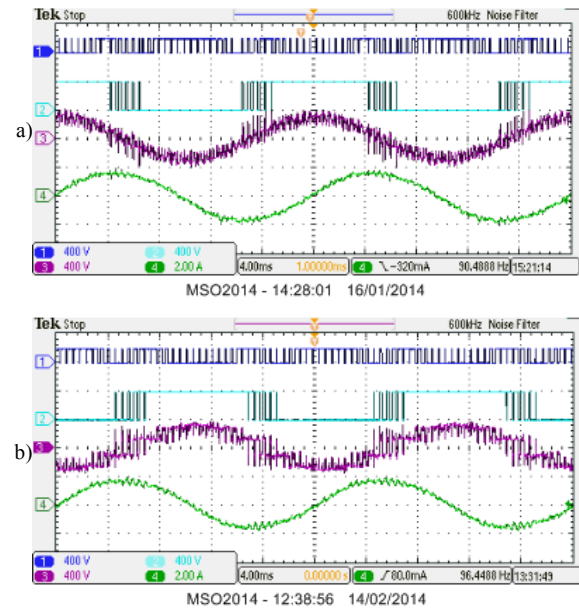

Fig. 8. Experimental set-up.

Fig. 9. Experimental results for conventional PD PWM (a) and APOD PWM (b), for $M = 1$ and $R_{offset} = 1/2$. Oscilloscope channels, from top to bottom: CH1 − v_{21}, CH2 − v_{11}, CH3 − v_1, and CH4 − i_1.

Fig. 10. Experimental results for conventional PD PWM (a) and APOD PWM (b), for $M = 0.5$ and $R_{offset} = 1/2$. Data acquisition and signal labels are the same as in Fig. 9.

Fig. 11. Experimental results for original PD and APOD PWM, for $M = 0.2$ and $R_{offset} = 1/6$. Data acquisition and signal labels are the same as in Fig. 9.

based on synchronization of leg voltage transitions of two leg outputs, connected to the same OeW phase. Due to different dynamic characteristic of IGBTs and antiparallel diodes, some minor spikes in phase voltage will exist even when gating synchronization of gating signals is almost

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Fig. 12. Experimental results for original PD PWM (a) and APOD PWM (b), with SRA, for $M = 1$ and $R_{offset} = 1/2$. Data acquisition and signal labels are the same as in Fig. 9.
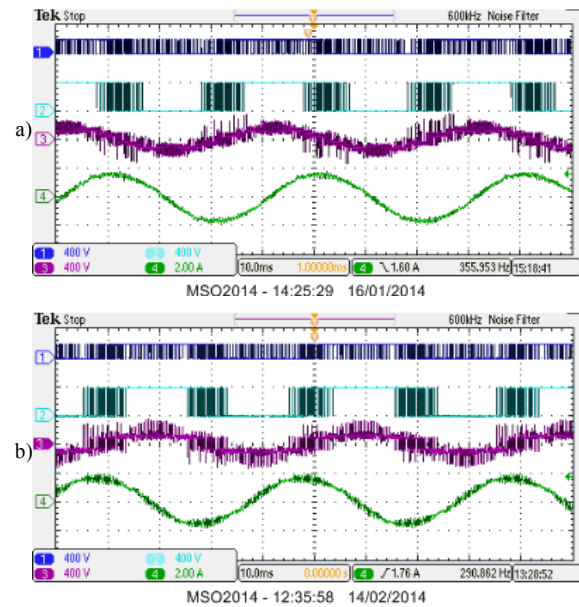

Fig. 13. Experimental results for original PD PWM (a) and APOD PWM (b), with SRA, for $M = 0.5$ and $R_{offset} = 1/2$. Data acquisition and signal labels are the same as in Fig. 9.
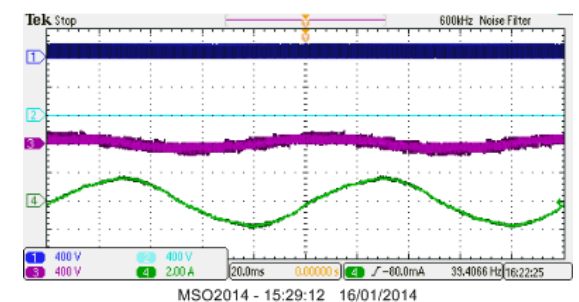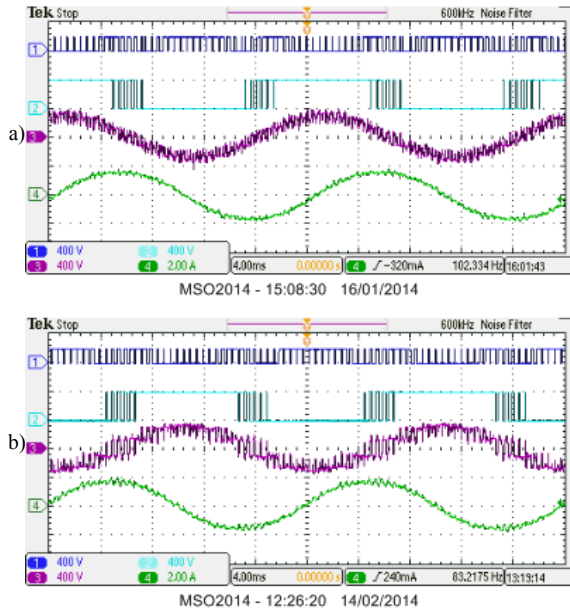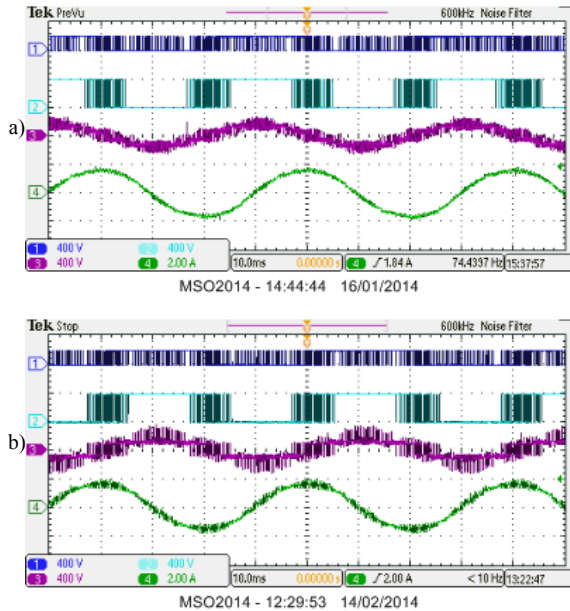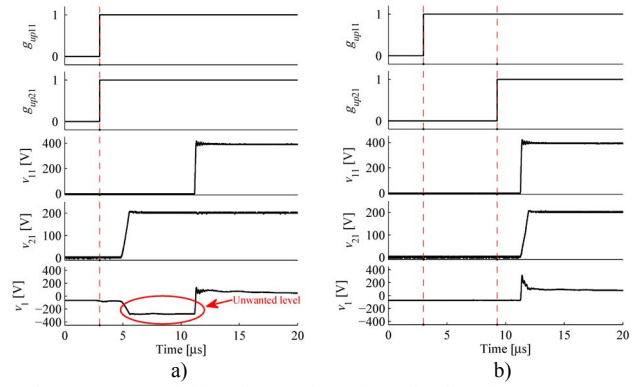

Fig. 14. Open-end drive phase voltage formation in reference zone 2: PD PWM without (a) and with (b) SRA. Data acquisition and signal labels are the same as in Fig. 1. Dashed line marks gating signal transitions.
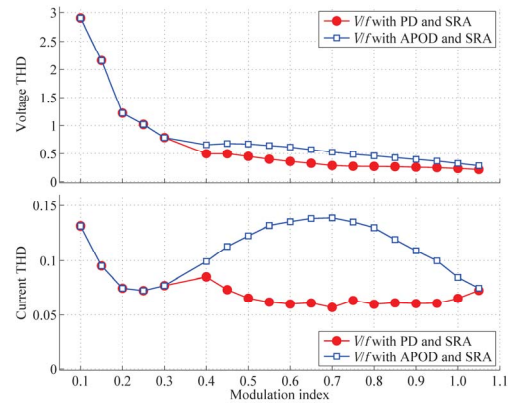

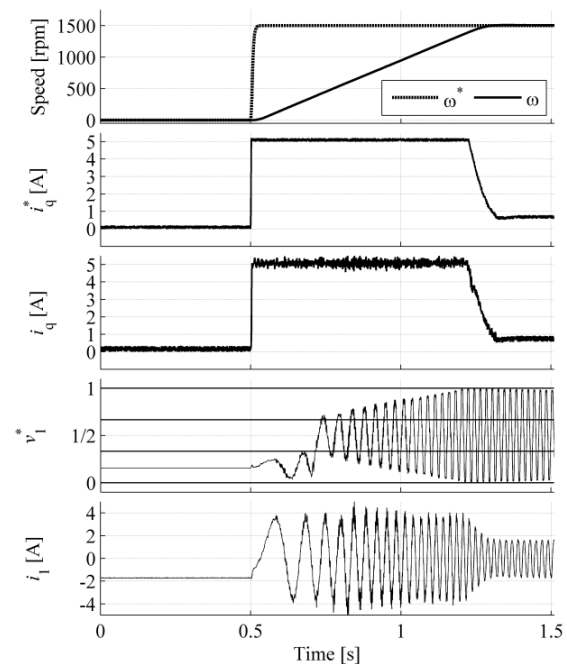Fig. 15. Phase voltage and current THD against M for the open-loop V/f control.

Here X_i is the RMS value of the ith harmonic, the fundamental is denoted with X_1 and K is set to 5000. The THD is calculated for modulation index ranging from 0.1 to 1.05 in 0.05 increments and is shown in Fig. 13. PD PWM offers superior performance; in particular, the current THD is significantly lower from $M = 0.4$ to $M = 1$. This is a consequence of the harmonic mapping, with APOD PWM generating slightly higher low order harmonics which map into the low-impedance x-y plane [26].

VII. CLOSED-LOOP CONTROL

High performance control of multiphase multilevel drives has been dealt with relatively rarely, a notable exception being [25]. Likewise, PWM algorithms for open-end winding drives cover only open-loop VSI control [26, 27]. This seems to be logical, since the number of levels and machine windings configuration (star-connected or open-end) influence the PWM algorithm only, while FOC of multiphase machines developed for two-level converters can be used without any modification. However, it seems important to demonstrate the performance of the considered topology under the closed-loop control, since that is nowadays a standard approach in industrial applications. Furthermore, the impact of the SRA on the dynamic performance of the drive under FOC should be evaluated. For these reasons this section discusses use of indirect rotor flux FOC to control the speed of the five-phase induction machine, as discussed in [5]. As with three-phase machines, only two current components (i_d, i_q) are required for independent torque and flux control if the multiphase machine has nearly sinusoidal magneto-motive force (MMF) distribution, as the case is here. On the other hand, the

ideal. This is depicted in Fig. 14, where only one switching transition is shown for PD PWM without and with SRA, for voltage reference in zone 2. Fig. 14a shows that, although the gating signals are synchronized, the leg voltages change at different times due to the dead time (implemented in the hardware) and therefore the resultant phase voltage switches, for a short time, to an unwanted voltage level. Fig. 14b shows that the SRA suppresses this phenomenon by shifting the gating signals so that the legs switch as required; however, a very small glitch can still be seen around 11.5 µs.

Next, the harmonic performance of the PD and APOD PWM methods is experimentally compared using the total harmonic distortion (THD) as a figure of merit:

$$THD = \sqrt{\sum_{i=2}^{K} \frac{X_i^2}{X_1^2}} \qquad (6)$$

existence of drive asymmetries, finite switching frequency and other non-ideal effects lead to the need for additional (*x-y*) current controllers if high efficiency is to be achieved [5].

The inverter dead-time effect can be represented as a simple square wave [32]. This can be resolved into a set of odd harmonics; since the fifth harmonic cannot flow in a five-phase machine, the dominant harmonics are the 3rd and 7th. These harmonics appear as ac components in the *x-y* plane where the machine's impedance is low, since it consists of stator's resistance and leakage inductance only. It is demonstrated in [33] that the dead-time caused harmonics can be suppressed using synchronous PI current controllers in the *x-y* plane. In this case the 3rd and 7th harmonics appear as the 4th and 6th harmonics, respectively. However, the PI controllers are unable to fully compensate ac components and require high bandwidth [34]. An alternative solution, used here, employs a multiple reference frame structure [35, 36] using PI controllers in several synchronous reference frames in parallel. The method is based on separate control of the most dominant current harmonics. This solution requires two pairs of PI controllers, in order to suppress *x* and *y* components that correspond to the 3rd and 7th harmonic. The current control structure is depicted in Fig. 16. Current components labelled with i_{x3}, i_{y3}, i_{x7} and i_{y7} are obtained with additional rotational transformations that rotate the second plane with $-3 \cdot \omega$ and $7 \cdot \omega$, where ω is rotor flux space vector electrical angular speed. In this way, obtained i_{x3}, i_{y3}, i_{x7} and i_{y7} are dc and almost constant, with a small ripple that comes from switching harmonics, which have amplitudes much lower than the original 3rd and 7th harmonics. It should be noted that this current control scheme, while easy to understand, requires several transformations and PI controllers. A less computationally demanding solution, using resonant controllers, is given in [37] for any phase number. However, since a five-phase machine is considered here and only two harmonics are of interest, the computational saving would be small [38].

The performance of the current control scheme, presented in Fig. 16, is examined using the experimental set-up shown in Fig. 8. The PI controller parameters are provided in the Appendix. The PD PWM method is selected since it has been shown to be superior to APOD (Fig. 15). The current spectra shown in Fig. 17 demonstrate that the PD PWM with closed-loop current control and the SRA is capable of achieving sinusoidal currents containing negligible low order harmonic content. Fig. 17 shows that the closed-loop current control system effectively suppresses the dead-time induced low order harmonics, in contrast to the open-loop *V/f* control. The dynamic performance of the FOC with the SRA is presented in Figs. 19-21.

Fig. 17. Low-order phase current harmonics for closed-loop current control with PI controllers, for $M = 1$ and $M = 0.5$. Harmonics are normalized with respect to the fundamental component.

Fig. 18. Low-order harmonics for two modulation index values with FOC (closed-loop current control is used) and with open-loop *V/f*.

Fig. 19. FOC response under no-load conditions to speed reference stepping from 0 rpm to 1500 rpm. Top to bottom: speed (rpm), *q*-axis current reference, actual *q*-axis current, normalized voltage reference, and stator phase "1" current.

Firstly, in Fig. 19, the speed reference is stepped from zero to 1500 rpm. As expected, the *q*-axis current reference (i_q^*) almost immediately steps to its maximum value and remains there until the reference speed has been met. The measured *q*-axis current (i_q) tracks the reference closely. The power invariant transformation is used. This means that the magnitude of the stator current space vector will be $\sqrt{5}$ greater than the RMS value. The voltage reference v_1^* can be seen to cross into different reference zones without any discernable impact on the dynamic performance of the drive.

Fig. 16. Indirect FOC with closed-loop current control with four-level five-phase open-end winding drive (power invariant transformation is used).

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During the transient (at approx. 0.7 s), the reference offset changes from 1/6 to 1/2 and so the operating mode changes from two- to four-level. This transition leads to a change of common mode voltage dc component, from -100 V to 100 V; however, this has no effect on the drive performance, since the two dc sources are fully isolated. It has been noticed that parasitic capacitance between the VSIs' bottom rails can lead to a short spike in i_q during changes in R_{offset}; this effect is reduced by limiting the rate-of-change of the reference offset, meaning that the transition of reference offset from 1/6 to 1/2 is ramped rather than instantaneous. The transition of reference offset lasts for two switching periods. This has no impact on the FOC dynamic performance.
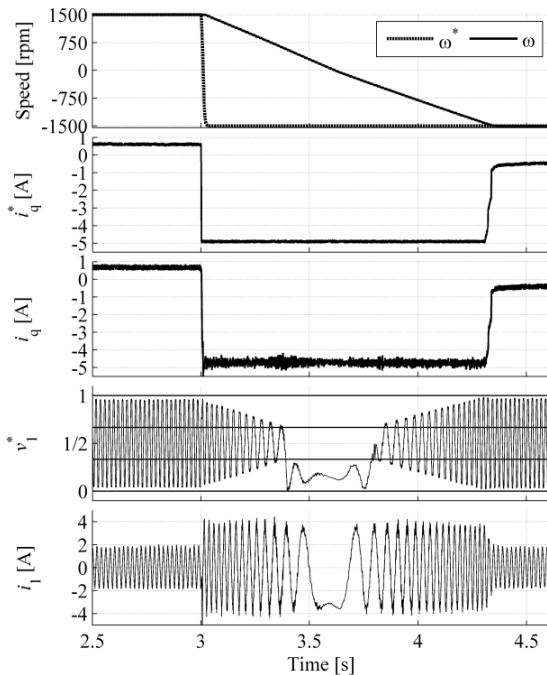
Next, a speed reversal transient is examined. Fig. 20 shows the commanded speed stepping from 1500 rpm to -1500 rpm at $t = 3$ s. Again, the dynamic performance of the drive is excellent with the q-axis current tracking the reference as expected. Lastly, the response of the drive during step loading and unloading is given in Fig. 21. Once again a typical FOC response is observed with the dynamic performance being largely influenced by the speed PI controller tuning.

As the final experimental set of results, Figs. 22 and 23 illustrate phase voltage waveform under FOC with and without use of the spike removal algorithm. They demonstrate that closed-loop current control alone is not capable of suppressing unwanted voltage transitions, as can be seen from Fig. 22. Hence the SRA should be implemented in conjunction with FOC and closed-loop current control in both planes, in order to ensure removal of the dead-time induced spikes, Fig. 23.

Fig. 20. FOC response under no-load conditions for speed reversal from 1500 rpm to −1500 rpm. Traces as in Fig. 19.

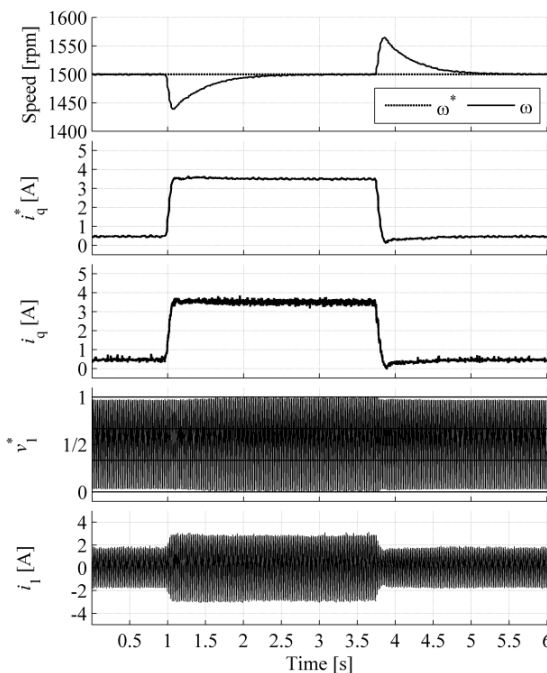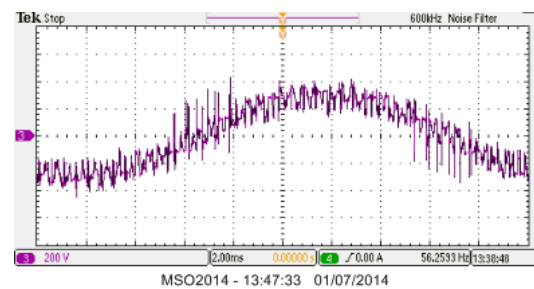Fig. 22. Phase voltage under FOC without SRA ($M = 1$, PD PWM).

Fig. 23. Phase voltage under FOC with SRA ($M = 1$, PD PWM).

Fig. 21. FOC response to step load application and unloading at the speed of 1500 rpm. Traces as in Fig. 19.

VIII. CONCLUSION

The paper presents a four-level five-phase drive constructed using two two-level inverters and a five-phase induction machine with open-end windings. Inverter dc links are isolated in order to eliminate the path for zero sequence current circulation. Presented analysis shows that equal dc-link voltages will lead to a three-level drive equivalent, while any unequal dc-link voltage ratio will lead to a four-level operation. Analysis of space vector distribution shows that the dc-link voltage ratio 2:1 leads to the most homogenous distribution of space vectors in both planes and this ratio is therefore chosen. Two carrier based modulation strategies (PD and APOD PWM) are developed for this drive in conjunction with the dc-link voltage ratio 2:1. The paper shows that the inverter dead time can lead to the triggering of unwanted voltage levels in the phase voltages. A simple solution is proposed and the performance of the CBPWM techniques is verified experimentally for the first time. It is shown that the PD-PWM method offers better overall performance compared to the APOD PWM.

The dynamic performance of the drive is investigated using indirect field oriented control in conjunction with

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closed-loop current control. Along with PI controllers operating on the fundamental, the current control scheme incorporates PI controllers in multiple reference frames synchronized to the 3rd and 7th harmonic, the aim being to suppress the most dominant dead-time induced current harmonics in the second plane, since the impedance presented to these harmonics is low. It has been demonstrated that the spike removal algorithm has negligible impact on the dynamic performance of the drive and is expected to lead to reduced EMI. The presented experimental results demonstrate that this topology offers potential for EV/HEV applications where the dc-link voltages are low and isolation of the supplies is easier to achieve. Naturally, any merits/demerits of using the four-level OeW drive will depend on EV/HEV configuration, i.e. the dc-dc converter structure, battery packs, and the charging topology, and will need to be evaluated on a case-by-case basis.

APPENDIX

Five-phase induction motor: 50 Hz, 4-pole
Motor parameters:
$R_s = R_r = 3$ Ω, $L_{ls} = 45$ mH, $L_{lr} = 15$ mH, $L_m = 545$ mH.

TABLE A1. PI CONTROLLER PARAMETERS

Parameter	Value
K_{p_speed}	0.205
K_{i_speed}	0.500
$K_{p\_cc-\alpha\beta}$	25
$K_{i\_cc-\alpha\beta}$	6000
K_{p_cc-xy}	40
K_{i_cc-xy}	200

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Milan Darijevic (S'10) received BSc and MSc degrees in Electrical Engineering, from the University of Belgrade, Serbia, in 2010 and 2011, respectively. In May 2012 he joined Electric Machines and Drives Group at Liverpool John Moores University, UK, as a PhD student. His research interests are related to power electronics for high power applications, including both control strategies and hardware design.

Martin Jones received his BEng degree (First Class Honours) in Electrical Engineering from the Liverpool John Moores University, UK in 2001. He was a research student at the Liverpool John Moores University from September 2001 till Spring 2005, when he received his PhD degree in Electrical Engineering. Dr Jones was a recipient of the IEE Robinson Research Scholarship for his PhD studies and is currently with Liverpool John Moores University as a Reader. His research is in the area of high performance ac drives.

Emil Levi (S'89, M'92, SM'99, F'09) received his MSc and the PhD degrees in Electrical Engineering from the University of Belgrade, Yugoslavia in 1986 and 1990, respectively. From 1982 till 1992 he was with the Dept. of Elec. Engineering, University of Novi Sad. He joined Liverpool John Moores University, UK in May 1992 and is since September 2000 Professor of Electric Machines and Drives. He served as a Co-Editor-in-Chief of the IEEE Trans. on Industrial Electronics in the 2009-2013 period and is currently Editor-in-Chief of the IET Electric Power Applications and an Editor of the IEEE Trans. on Energy Conversion. He is the recipient of the Cyril Veinott award of the IEEE Power and Energy Society for 2009 and the Best Paper award of the IEEE Trans. on Industrial Electronics for 2008. In 2014 he received the "Outstanding Achievement Award" from the European Power Electronics (EPE) Association.

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