Identify the critical regions and switching/failure mechanisms in non-filamentary RRAM (a-VMCO) by RTN and CVS techniques for memory window improvement

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Abstract Non-filamentary RRAM is a promising technology that features self-rectifying, forming/compliance-free, tight resistance distributions at both high and low resistance states (HRS/LRS). Direct experimental evidence for its physical switching & failure mechanisms, however, is still missing, due to the lack of suitable characterization techniques. In this work, a novel method combining the random-telegraph-noise (RTN), constant-voltage-stress (CVS) and time-to-failure Weibull plot is developed to investigate these mechanisms in the non-filamentary RRAM cell based on amorphous-Si/TiO_2. For the first time, the following key advances have been achieved: i) Switching mechanism by defect profile modulation in a critical interfacial region has been identified from defect locations extracted by RTN; ii) Defect profile in this region plays a critical role in device failure, leading to different Weibull distributions during negative (LRS) and positive (HRS) CVS; iii) Progressive formation of a conductive percolation path during electrical stress is directly observed due to defect generation in addition to pre-existing defect movement; iv) Optimizing the critical interfacial region significantly improves memory window and failure margin. This provides a useful tool for advancing the non-filamentary RRAM technology.

I. Introduction

Resistive switching memories (RRAM) attracted extensive attentions as an emerging memory technology. There are two types of oxygen ion/vacancy based RRAMs: (1) filamentary RRAM: Switching is through the modification of a conductive filament, which leads to long HRS/LRS retention tails (e.g. HfO_2, [1-2]) (**Fig.1a&c**); (2) Non-filamentary RRAM: It features self-rectifying, forming/compliance-free, low μA operation, tighter HRS/LRS distributions with little tail-bits shifting issues (e.g. TiO_2/TaO_x [3], a-VMCO [4,5]). It has been proposed that its switching is through the uniform defect profile modulation (**Fig.1b&d**) [4], however, direct experimental evidence is still missing and its failure mechanism is not known. *In this work, a novel method has been developed combining RTN, CVS and Weibull plot, which, for the first time, enables the identification of its switching and failure mechanisms at defect level by directly observing the profile modulation of pre-existing defects and the progressive formation of a conductive percolation path by the addition of generated defects. The unique failure characteristics of a-VMCO can be explained by a proposed model. Identifying the key roles of the critical interfacial region in switching/failure provides guidance for further improving non-filamentary RRAM.*

II. Device and operation

A TEM image of the device structure and the DC I-V curves are shown in **Fig.1e&f**, respectively [4]. Device details are given in Table 1. The a-VMCO cell features analog switching behavior. It RESETs at a positive top electrode (TE) voltage and SETs at a negative bias. Increasing Vreset is desirable for enhancing the memory window, but this will soon cause breakdown in devices with unoptimized process (W1). *By improving the critical regions responsible for switching/failure through process optimization (W2&W3), we will demonstrate that the memory window and failure margin can be significantly improved (**Fig.1g**).*

III. RTN & CVS Characterization

A. RTN and defect profile modulation by switching

In our earlier work [2], RTN in HfO_2 RRAM has been used to extract the profile of defect's spatial and energy locations, X_T & E_T, from its mean capture/emission time constant dependence on the applied bias [6-8]. By adapting this method to a-VMCO, RTN can be clearly observed and defects are detected in both TiO_2 and a-Si layers (**Fig.2**). Defects profiles in the vertical direction extracted after switching to LRS (o) and HRS (o) are compared in **Fig.3a&b**. At HRS, there is a defect-'less' region at each side of the a-Si/TiO_2 interface (IL). At LRS, however, it is not observed at the TiO_2 side; hence this is where the defect profile modulation occurs predominantly. The total width of defect-'less' regions is closely correlated with resistance, as it becomes wider at HRS and narrower at LRS, providing, for the first time, direct experimental evidence for the proposed switching mechanism (**Fig.1b**) [4-5]. Note that this defect profile modulation is caused by the movement of pre-existing defects, which have uniform spatial distribution in the lateral direction (**Fig.1b**), because of its forming-free and area-dependent non-filamentary switching characteristics as shown in refs. [4, 5].

B. Time-to-failure during CVS and its Weibull plot

In order to characterize the device failure, CVS is applied on TE and time-to-breakdown, t_{BD}, is examined with Weibull plot. It exhibits a single slope for positive CVS at V_{BD}=+6.6V (**Fig. 4a**), but a bimodal behavior with two slopes for negative CVS at a much smaller V_{BD}=-3.5V (**Fig.4b**). This significant polarity-dependence of V_{BD} and Weibull slopes have not been observed for high-k dielectric stacks used in MIM capacitor or MOSFETs (e.g. **Fig.5**) [9-13]. The cell current is also monitored against stress time during CVS, showing two stages before reaching breakdown: in 1st stage, current reduces at positive CVS (**Fig.6a**), but is stable at negative CVS (**Fig.6b**). Large fluctuations are observed in 2nd stage in both cases. In order to explain these differences, defect profiles during CVS will be obtained next by combining RTN and CVS measurements.

C. Combination of RTN and CVS

RTN measurements are inserted at certain intervals during CVS (**Fig.7**) to monitor the gradual changes in defect profiles at different CVS stages. RTNs with only small amplitudes (<5%) are observed in 1st CVS stage (also in fresh devices after switching to either HRS or LRS, not shown), whilst both small and large RTNs (>10%) are observed in 2nd CVS stage (**Fig.8a-d**). This suggests that in addition to the profile modulation of pre-existing defects during set/reset and in 1st stage, additional defects are generated by stress in 2nd stage, leading to the large amplitude of RTN and

current fluctuations, and breakdown. The same defects can be detected by immediately repeated RTN measurements in both 1st and 2nd stages, confirming the effectiveness of the measurement (**Fig.9**). In the following, defect profiles during 1st and 2nd stages of both CVS polarities will be examined, and a physical model for the failure mechanism will be proposed.

IV. Failure mechanisms

A. Defect profile during positive CVS

The positive CVS bias resets a-VMCO to HRS. As shown in **Fig.1b&3b**, switching to HRS is associated with two pre-existing defect-'less' regions, one at a-Si side and the other at TiO_2 side of IL. Profile of pre-existing defects extracted during the 1st stage of positive CVS (**Fig.3b**) is shown as the orange-color background in **Fig.10a-c**. The current reduction in 1st stage (**Fig.6a**) is caused by deeper reset under the positive CVS. Defects extracted from the large RTN signals (●) in 2nd CVS stage are observed in the pre-existing defect-'less' (white) region in TiO_2 at early 2nd stage, gradually reaching the TiO_2/IL interface (**Fig.10a-c**), confirming that they are caused by defects generation as they are absent in this region during normal switching. Defects generation is also observed in a-Si approaching its pre-existing defect-'less' region. This result suggests that the defect-'less' interfacial region plays a key role as the 'last-to-break' region. The wider pre-existing defect-'less' regions at HRS (**Fig.1b & 10d**) result in a higher positive V_{BD} with the potential drop across the TiO_2/a-Si stack $V_{stack}=V_{CVS}-V_{FB}=5.6V$ (**Fig. 2)**.

B. Defect profile during negative CVS

The negative CVS bias sets a-VMCO to LRS, and the TiO_2 side of IL is occupied by the pre-existing defects (**Fig.1b&3**). Profile of the pre-existing defects extracted during the 1st stage of negative CVS (**Fig.3b**) is shown as the light-blue background in **Fig.11a-c**. Defects causing large RTNs in 2nd stage evolve in a way similar to that under positive CVS: they are observed in TiO_2 gradually approaching the TiO_2/IL interface, and also in a-Si approaching the pre-existing defect-'less' region. This eventually leads to the formation of a percolation path across the TiO_2/a-Si stack, as can be seen clearly in the case after device soft BD (**Fig.12**). The narrower defect-'less' IL/a-Si region leads to a smaller negative V_{BD} with the potential drop across the TiO_2/a-Si stack $V_{stack}= V_{CVS}-V_{FB}=-4.5V$. Moreover, these devices are in the region 1 of its bimodal Weibull plot (**Fig.4b**).

Devices in region 2 of the bimodal Weibull plot for -CVS shows a stepper distribution at short t_{BD} (**Fig.4b**). Defect profiles in these devices are also extracted (**Fig.13**), and a percolation path is formed after short stress times, leading to their early failure. It should be emphasized that there is no device breakdown observed when stressed under +CVS at $V_{stack}= 4.5V$ for 10ks, suggesting the interfacial region becomes significantly more robust at HRS.

C. Physical model for the failure mechanism

Based on the above results and analysis, we propose a device failure model as illustrated in **Fig.14a&b**. The failure of a-VMCO cell is a combined result of three factors: (1) the profile of pre-existing defects that can be modulated in the RRAM dielectric stack between HRS and LRS, unlike that in the classical gate dielectric of MOSFETs; (2) the conductive percolation path formed by defect generation during stress, which is affected by the pre-existing defects modulation; (3) quality of the TiO_2/a-Si interfacial region.

The two-slope bimodal distribution was also reported for some small-area high-k/SiON stacks in MOSFETs at both bias polarities and has been explained by the substantially higher defect generation rates (DGR) in either the high-k layer [9] or its grain boundary (GD) [11,13]. DGR can also explain the bimodal distribution in **Fig.4b**: the TiO_2 side of IL is occupied by pre-existing defects under –CVS at LRS (**Fig.3b**), and has much higher DGR than the defect-'less' IL/a-Si region. The polarity dependence of the pre-existing defect distribution in **Fig.14a&b**, however, is unique to the TiO_2 layer in a-VMCO. The removal of pre-existing defects in the TiO_2/IL region under +CVS at HRS reduces its DGR and the smaller difference in DGR for the two layers leads to the single slope in **Fig.4a**. To support this explanation, the Weibull plot of the Metal/a-Si/Metal devices [14] shows that the single a-Si layer has a similar single slope when the TiO_2 layer was absent (**Fig.15**).

V. Memory window improved by critical IL regions

According to the above failure model, improving IL quality should reduce the DGR in the critical IL region, leading to better device performance. Indeed, an improved overall processing condition for both TiO_2 and a-Si in W2/P2 lead to larger memory windows and failure margins as shown in **Fig.1g&16.** This is consistent with t_{BD} improvement of W2 under both ±CVS (**Fig. 17a&b)**. Interestingly, further improvement of TiO_2/IL by a specific treatment prior to TiO_2 deposition in W3 leads to a further improvement only in region 2 under -CVS (**Fig.17b)**, supporting that the higher DGR in the TiO_2 side of IL [9,11] under –CVS at LRS is responsible for region 2. This is further supported in **Fig.18**. W1&2&3 have similar current fluctuation generation and failure path formation process, but at much longer stress times in W2 and W3 due to the lower DGR in TiO_2/IL region with better quality, suggesting that exploring new IL material/process may facilitate even further improvement.

VI. Conclusions

A novel method combining RTN, CVS and Weibull plot has been developed for non-filamentary RRAM device. For the first time, its defect profiles have been extracted by RTN, which are clearly correlated to resistance switching and to different time-to-failure Weibull distributions. Identification of defect generation during CVS enables the observation of progressive formation of the conductive percolation path leading to breakdown. This work provides insights for further improving the performance of non-filamentary RRAM through identifying the roles of specific critical IL regions, assisting in advancing the RRAM technology.

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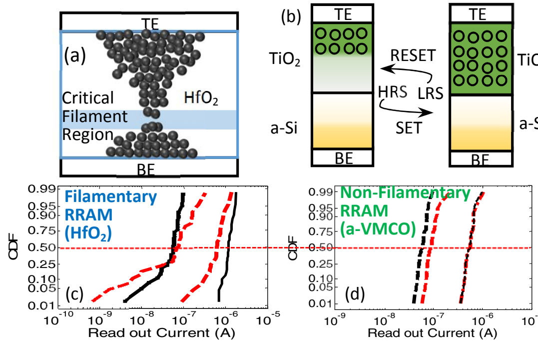

Fig.1 RRAM: (a) filamentary (HfO_2); (b) non-filamentary (a-VMCO); (c) & (d) Read current distributions before (black) and after (red) the retention test for (a) & (b), respectively [4].

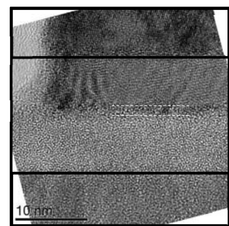

Fig.1 (e) TEM of a-VMCO RRAM, a ~1-nm SiO_x interfacial layer (IL) is formed between amorphous Si and anatase-phase TiO_2 by the end of process [4,5].

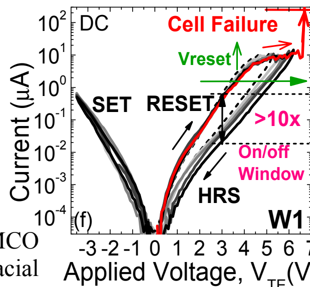

Fig.1 (f) DC I-V curves of a-VMCO cell (W1) at different Vreset. (g) Improved IL quality in W2 and W3 can enhance the memory window (Iread@3V) and failure margin significantly.

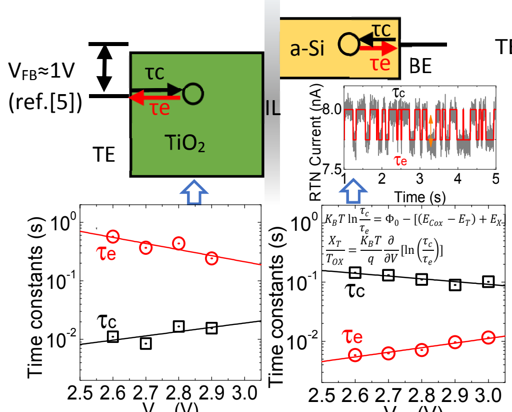

Fig.2 Defect location is extracted from the dependence of RTN's mean time constants on bias V_{TE} [2, 6-8]. Defects can be found in both TiO_2 and a-Si.

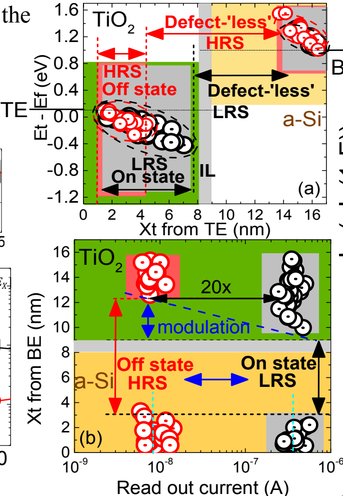

Fig.3 Extracted defect profiles at LRS/HRS (a) vs. distance from TE, and (b) vs. Iread. Note that this defect profile does not provide information on the actual defect density [2].

Defect profile modulation predominantly occurs in a critical region in TiO_2 near IL.

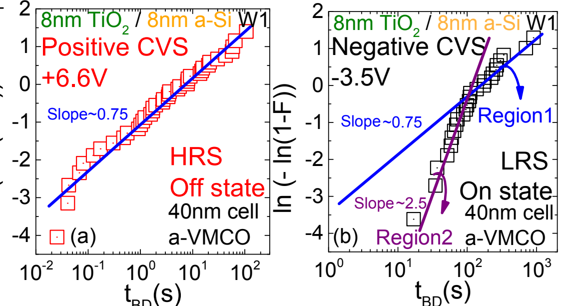

Fig.4 (a) t_{BD} Weibull plot for the dual layer a-VMCO (a) single-slope at positive CVS. (b) Two slopes at negative CVS. V_{BD} appears much higher at positive CVS.

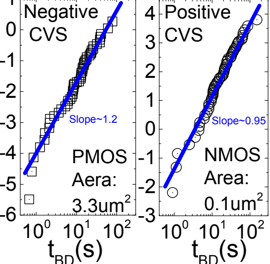

Fig5. t_{BD} Weibull plot for SiO_2/HfO_2 in CMOS device [9], similar distribution is observed at negative & positive CVS.

Table 1: Devices

Sample	#	Process	
a-VMCO RRAM	W1	8nmTiO2/	P1
	W2	8nm a-Si	P2
	W3	40x40nm	P3
a-Si MSM	W4	8nm a-Si 40x40nm	P1

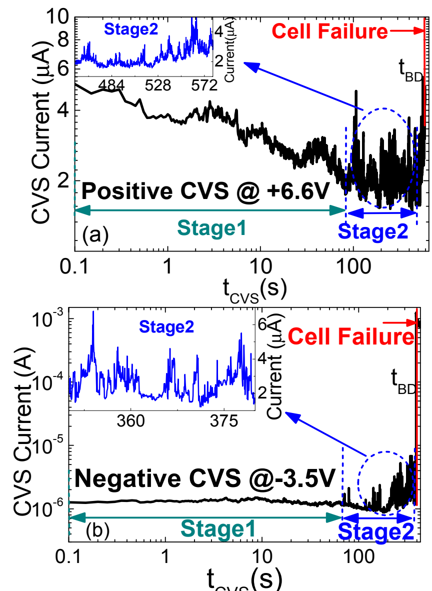

Fig.6 I-t plots during (a) positive CVS after reset at +6.6V and (b) negative CVS after set at -3.5V. **Stage 1** and **Stage 2** are observed in both cases before device failure. CVS current reduction during 1st stage in (a) is due to deeper reset under positive CVS. It is not observed in (b) due to the faster SET speed in a-VMCO [4].

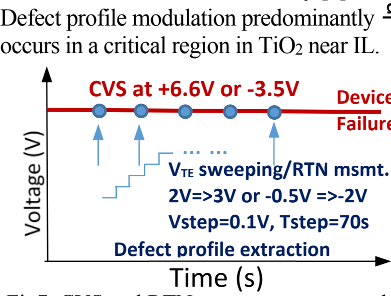

Fig7. CVS and RTN measurement procedure for defect profile extraction. V_{TE} during the RTN sweeping has the same polarity as CVS stress.

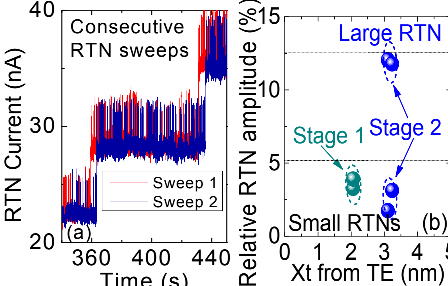

Fig.9 Same defects are measured by consecutive RTN sweeps as shown by (a) similar RTN signals, and (b) same defect locations and RTN amplitude in both **Stage 1** and **Stage 2**.

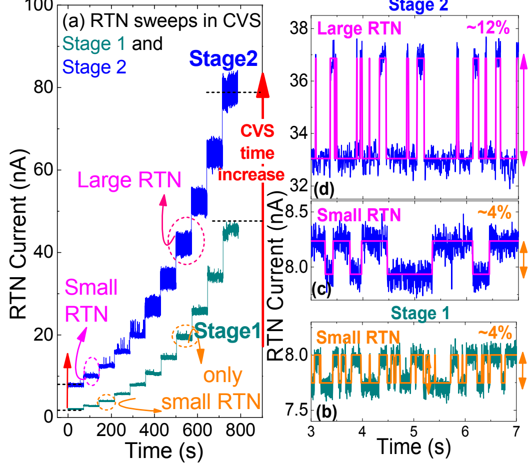

Fig.8 (a) I-V sweeps during RTN measurements in CVS **Stage 1** & **Stage 2** as shown in Fig.6. (b) Only small RTNs in **Stage 1**. Both (c) small and (d) large RTNs in **Stage 2**. Large RTNs are caused by (or related to) defects generation in the percolation path.

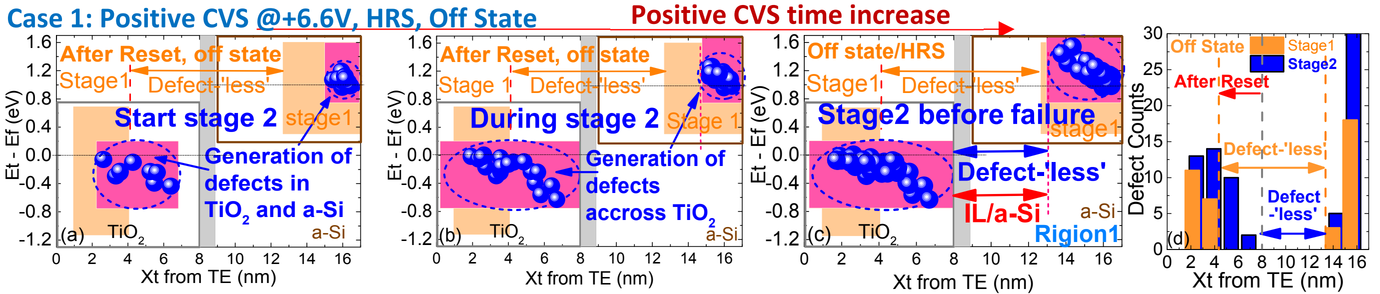

Fig10 Progressive percolation path formation by defects generation at the (a) start, (b) middle, (c) end of 2nd stage during positive CVS, in addition to pre-existing defects observed during Stage 1. (d) The narrower defect-'less' region in 2nd stage is the most robust region observed before BD.

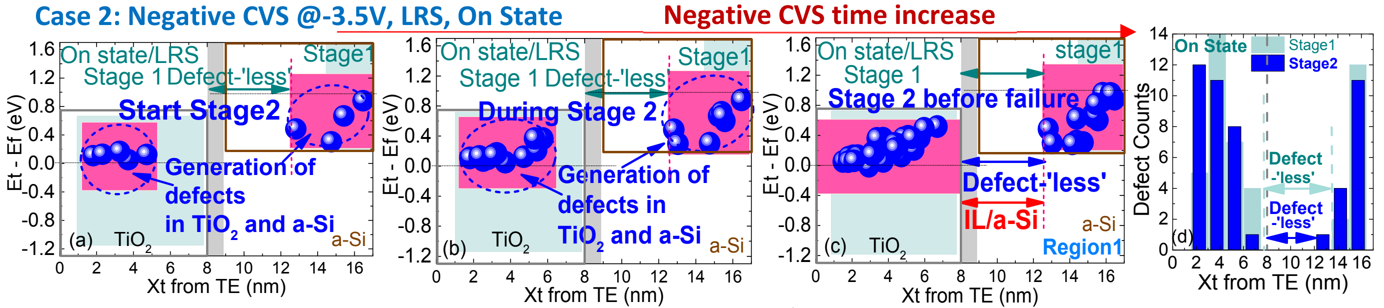

Fig11 (a-c) Progressive percolation path formation by defects generation during 2nd stage of negative CVS, in addition to pre-existing defects observed during Stage 1. (d) Defects generation in the most robust defect-'less' IL/a-Si region can be observed after the soft BD as shown in Fig.12.

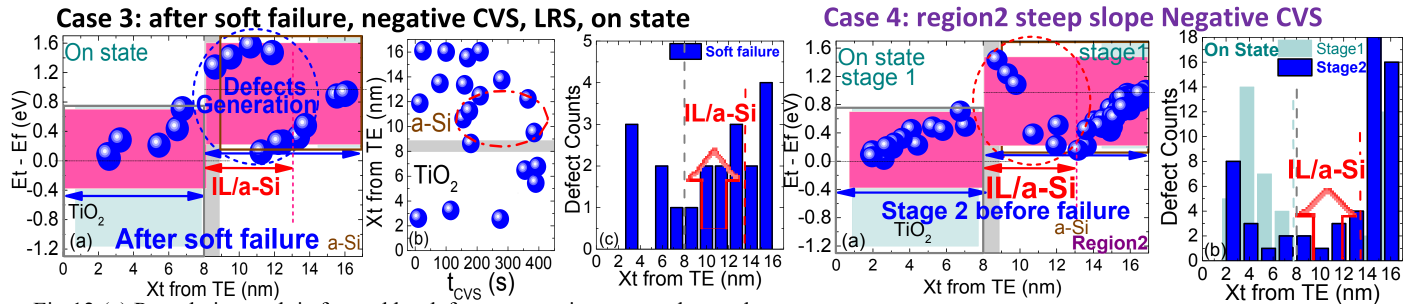

Fig.12 (a) Percolation path is formed by defects generation across the stack after soft BD at Negative CVS. (b&c) Defects generation found near IL/a-Si.

Fig.13 (a) Defects distribution before failure at short t_{BD} in devices in Region 2 (steep slope) of negative CVS (Fig.4b). (b) Defects generation found near IL/a-Si at short stress times.

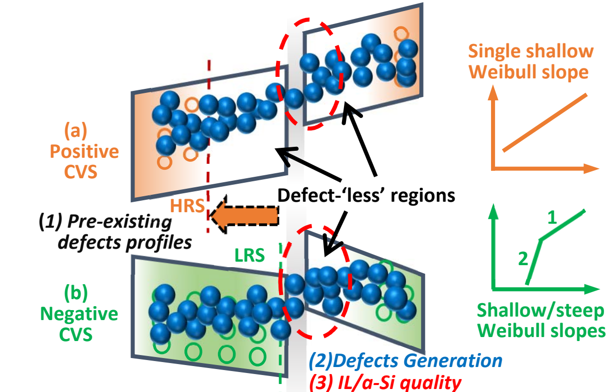

Fig14. Illustration of the switching and failure model.

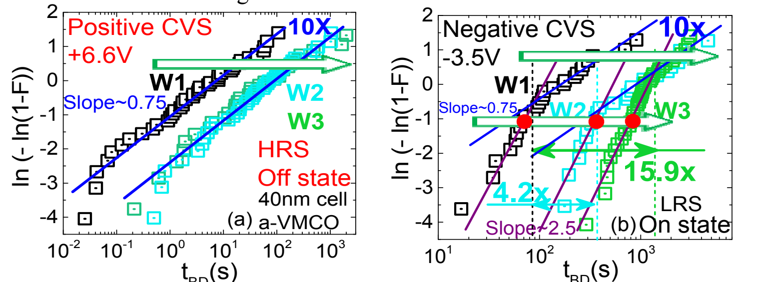

Fig.17 t_{BD} improvement in W2&3 under (a) positive and (b) negative CVS. W2 has 10x larger t_{BD} failure margins than W1 under both ±CVS. Further improvement in region 2 under -CVS is observed in W3 due to improved TiO_2/IL quality.

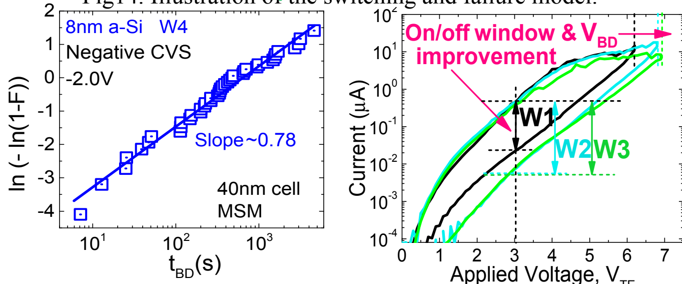
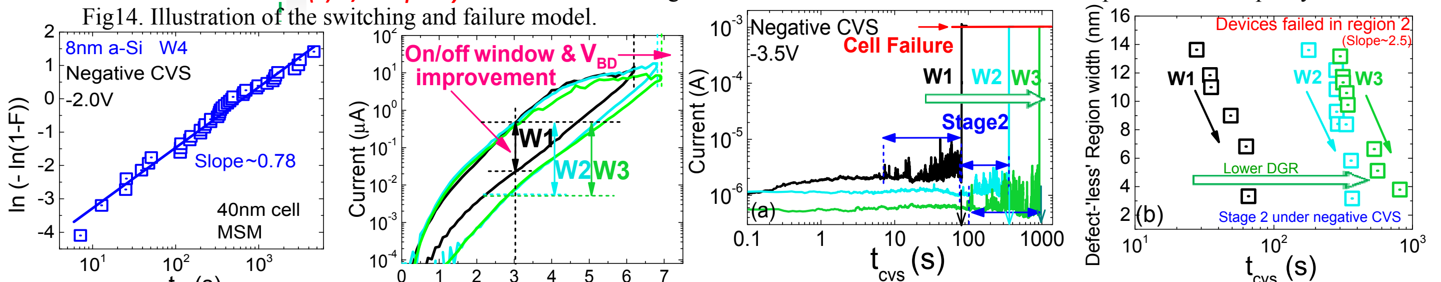

Fig15. t_{BD} Weibull distribution of single amorphous Si layer (MSM).

Fig.16 Memory window and V_{BD} enhancement in W2&3.

Fig18. Comparison of (a) occurrence time of stage 2 under - CVS in W1&2&3. (b) Progressive reduction of the generated defect-'less' region width against stress time in devices failed in region 2 as indicated by '●'symbols in Fig.17b.