DEFECTS AND LIFETIME PREDICTION OF GERMANIUM MOSFETS

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To my family

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Abstract

To continue improving device speed, much effort has been made to replace Si by high mobility semiconductors. Ge is considered as a strong candidate for pMOSFETs due to the high hole mobility. Two approaches have been demonstrated: high-k/Si-cap/Ge and high-k/GeO_2/Ge. Negative Bias Temperature Instability (NBTI) is still one of the main reliability issues, limiting the device lifetime. In this project, it is found that the conventional lifetime prediction method developed for Si is inapplicable to Ge devices and defect properties in Ge and Si MOSFETs are different.

The threshold voltage degradation in Ge can be nearly 100% recovered under a much lower temperature than that in Si devices. The defect losses observed in Si devices were absent in Ge/GeO_2/Al_2O_3. The generation of interface states is insignificant and the positive charges in GeO_2/Al_2O_3 on Ge dominate the NBTI. These positive charges do not follow the same model as those in SiON/Si and an energy-alternating model has been proposed: there are a spread of energy levels of neutral hole traps below Ev and they lift up after charging, and return below Ev after neutralization.

The energy distribution of positive charges in the Al_2O_3/GeO_2/Ge gate stack was studied by the Discharge-based Multi-pulse (DMP) Technique. The different stress-time dependence of defects below Ev and around Ec indicates that they originate from different defects. Quantization effect, Fermi level pinning, and discharge voltage step were considered. The defect differences in terms of the energy level were investigated

by using the DMP technique and the energy alternating model is verified by the defect energy distribution.

Based on the understanding of different defect behavior, a new NBTI lifetime prediction method was developed for Ge MOSFETs. Energy alternating defects were separated from as-grown hole traps (AHT), which enables to restore the power law for NBTI kinetics with a constant power exponent. The newly developed Ge method was applicable for NBTI lifetime prediction of the state-of-the-art Si-cap/Ge and GeO_2/Ge MOSFETs. When compared with SiON/Si, the optimized Si-cap/Ge shows superior reliability, while GeO_2/Ge is inferior and needs further optimization. Preliminary characterization was also carried out to investigate the impacts of energy levels and characteristic times of different defects on the frequency and duty factor dependence of AC NBTI degradation.

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List of Abbreviations

Abbreviation	***Signification***
GeO_2	Germanium dioxide
High-k	High dielectric constant/permittivity
SiON	Silicon Oxide Nitride
HfO_2	Hafnium dioxide
Al_2O_3	Aluminum oxide
NBTI	Negative Bias Temperature Instability
PBTI	Positive Bias Temperature Instability
TDDB	Time Dependent Dielectric Breakdown
HC	Hot Carrier
PCs	Positive Charges
EOT	Equivalent Oxide Thickness
CP	Charge Pumping
TC	Transfer Curve
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
TaN	Tantalum Nitride
TiN	Titanium Nitride
DMP	Discharge-based Multi-Pulse
CNL	Charge Neutrality Level
FLP	Fermi Level Pinning

CCS	Capture Cross Section
AHT	As-grown Hole Traps
CPC	Cyclic Positive Charge
ANPC	Anti-Neutralized Hole Traps

List of Symbols

Symbol	***Description***	***Unit***
Nc	Effective density of states in conduction band	cm^{-3}
Nv	Effective density of states in valence band	cm^{-3}
σ_i	Capture cross section	cm^2
C_{ox}	Oxide capacitance	F
C_{lf}	Low-frequency substrate capacitance	F
Cs	Semiconductor capacitance	F
f	Frequency	Hz
E_f	Fermi level	eV
Eox	Oxide electric field	MV/cm
Ev	Valence band	eV
Ec	Conduction band	eV
g_m, G_m	Transconductance	S
I_d	Drain current	A
I_g	Gate current	A
Is	Source current	A
Icp	Charge pumping current	A
L	Gate channel length	μm
W	Gate channel width	μm
D_{it}	Interface trap density	$eV^{-1}cm^{-2}$

N_{it}	Interface trap density	cm^{-2}
q	One electron charge	C
R	Feedback resistance	Ω
G	Conductance	S
Φs	Surface potential	
V_d	Drain voltage	V
V_{out}	Output voltage	V
T	Temperature	^oC
n	Power exponent	
m	Time-to-failure exponent	
γ	Voltage acceleration exponent	
t_m	Measurement time	sec
ts	Stress time	sec
$V_{discharge}$	Gate voltage applied during discharge	V
V_{fb}	Flat band voltage	V
V_g	Voltage applied on the gate	V
V_{ov}	Overdrive voltage	V
V_{th}	Threshold voltage	V
V_{th0}	Fresh threshold voltage	V
ΔV_{th}	Threshold voltage shift	V
V_{gst}	Stress voltage applied on the gate	V
V_{g_rec}	Recovery voltage applied on the gate	V

1 Introduction of the project

1.1 Research concerns and rationale

The downscaling of Si MOSFETs is approaching its end since the device is running out of atoms and its leakage and variability are becoming intolerable [1-6]. To continue improving device speed, much effort has been made to replace Si by high mobility semiconductors [1-4]. Ge is a strong candidate, especially for pMOSFETs because its intrinsic hole mobility is about 4 times of that for Si. Promising results have already been demonstrated for Ge pMOSFETs through two approaches: high-k/Si-cap/Ge [1, 2, 4] and high-k/GeO_2/Ge [2, 3, 7-9]. Interface states can be as low as that for SiO_2/Si [7, 8, 10] and the potential for fabricating Ge nMOSFETs has been demonstrated [7, 11, 12]. The process for fabricating Ge MOSFETs is becoming sufficiently mature and reproducible to warrant research into their reliability [13-15]. Good TDDB data were obtained [14], but electron trapping is high [16], similar to that in the early stage of developing high-k/SiON stack for Si [17-20]. For Si-based CMOS technologies, the negative bias temperature instability (NBTI) is the most severe reliability issue, since it results in a lifetime of pMOSFETs shorter than that of nMOSFETs [21, 22]. With Si-capped Ge MOSFETs, it has been reported that NBTI can be lower than its Si counterpart [2, 14, 15, 23]. For the Ge pMOSFETs without a Si-cap layer, however, there is little information available on the NBTI and the properties of defects responsible

for it. The works for NBTI in Si devices report that there are three types of positive charges: AHT (As-grown Hole Trap), ANPC (Anti-Neutralization Positive Charge), and CPC (Cyclic Positive Charge) [17-20]. For the purpose of comparison, the initial NBTI characterization is carried out on Ge MOSFETs as referred to the framework of defects in Si MOSFETs.

Efforts were made to extract the energy distribution of PCs [24, 25], but they used the slow quasi-DC measurement, hence did not capture the defects that discharged rapidly. Moreover, they only provide distribution within the bandgap. As a result, two types of PCs, AHT and ANPC, were not covered by these early works [24, 25]. A discharge-based multiple pulse (DMP) technique has been developed recently to evaluate the different types PCs in Si device [26]. Attempts have also been made in high mobility channel devices, however, only energy distribution of the interface traps [27] and PBTI induced border traps [28] were characterized. There is little information on the PCs induced by NBTI in $Al_2O_3/GeO_2/Ge$ pMOSFETs. To assist in the understanding and further minimization, it is desirable to know their energy distribution, which also provides the PC density at a given surface potential needed for simulating the NBTI impact on devices and circuits in the future.

It has been found out that traditional lifetime prediction method with DC measurement cannot be applied to Ge with Al_2O_3/GeO_2 gate stack, due to the non-constant power exponent under different stress conditions [29]. The reason was unknown at that time. It was reported that Si-cap/Ge device has superior reliability, but NBTI degradation in Si-

cap Ge devices by DC measurement cannot be described by power law [30]. Its lifetime, τ, cannot be predicted by power law extrapolation, either [30, 31]. This holds for both Si-cap and GeO_2 based gate stacks in Ge devices, albeit NBTI for GeO_2/Ge is higher [32]. Reproducible results can be achieved for the state-of-art Germanium process, but little is known about the defects. When measured by the fast pulse technique, the existing NBTI prediction method is inapplicable for both Si-cap/Ge and Al_2O_3/GeO_2/Ge, preventing reliable lifetime prediction. It is essential to develop a new lifetime prediction method for Ge devices, to assist in further process and device optimization.

1.2 Objectives of the project

To understand the properties of defects responsible for NBTI in Ge MOSFETs, the initial characterization compares the NBTI of Ge and Si devices, including the impact of stress electric field and stress temperature, the effects of annealing and measurement temperature and defect losses. Contribution of interface states generation will be estimated by using charge pumping technique. An energy alternating model will be proposed to explain the differences.

The second objective is to study the energy distribution of positive charges in the Al_2O_3/GeO_2/Ge gate stack. Discharge-based Multi-pulse (DMP) Technique will be adapted to characterize the impact of stress time on the energy distribution. Quantization effect, Fermi level pinning effect and discharge voltage step will be further evaluated for

the DMP application on Ge devices. The energy alternating model will be verified by the defect energy distribution.

Finally, with the knowledge of trap energy level, the behavior of different defects during DC and AC NBTI stress in Ge device will be investigated, which enables us to develop a new NBTI lifetime prediction method for Ge MOSFETs. Energy alternating defects will be separated from as-grown hole traps (AHT) to restore power law for NBTI kinetics with constant power exponents. The NBTI lifetime of the state-of-the-art Si-cap/Ge will be predicted by the newly developed Ge method with power law extrapolation. Three CMOS technology systems, consisting of SiO_2/Si, GeO_2/Ge and Si-cap/Ge, will be further evaluated, which shows process and device optimization needed. Impacts of energy levels and characteristic times of different defects on the frequency and duty factor dependence of AC NBTI degradation will be examined.

1.3 Novelty and originality of the research

1) For the first time, a detailed and systematic NBTI characterization was carried out and compared with Si device, focusing on the defect properties in Ge MOSFETs.
2) The energy distribution of hole traps in Ge MOSFETs was extracted by adapting the Discharge-based Multi-pulse (DMP) Technique.
3) An energy alternating defect model is proposed and verified from both slow and fast measurements for Ge NBTI.

4) A new NBTI lifetime prediction method is developed for Ge devices, based on the understanding of differences from the generated defects in Si.
5) This method is applied to Si-cap/Ge devices and NBTI Lifetime in SiO_2/Si, GeO_2/Ge and Si-cap/Ge is compared to show the process improvement achieved and further device optimization needed.
6) For the first time, the impact of energy levels and characteristic times of defects on the AC NBTI in Ge MOSFETs is investigated.

1.4 Organization of the thesis

The thesis is organized as follows:

Chapter 2 gives a review of CMOS technology and challenges in advanced Germanium MOSFETs. The fundamental properties of Germanium are compared with Si and III-V devices. Ge surface passivation and defects are discussed in two main Ge structures: high-k/GeO_2/Ge and high-k/SiO_2/Si-cap/Ge. Reliability issues are introduced in Ge MOSFETs, such as Positive charges (PCs) in oxide, Negative bias temperature instability (NBTI), Positive bias temperature instability (PBTI) and Hot carrier (HC) degradation. NBTI models, including Reaction-Diffusion Model, Hole Trapping Model, Two Stage Model, As-grown Generation (A-G) Model are discussed individually in this chapter.

Chapter 3 introduces the experimental system and techniques for characterizing Ge pMOSFETs. Conventional techniques consist of the DC Id-Vg Technique, Charge Pumping (CP) Technique, Capacitance Voltage (C-V) Technique and Conductance Technique. Limitations of conventional techniques application for Ge MOSFET are reviewed. The advantages of the advanced techniques in characterizing Ge devices are discussed, including the Pulse Id-Vg (Pulsed I-V) Technique, Ultra-Fast Pulsed (UFP) Technique, Ultra-Fast On-The-Fly (OTF) Technique and Discharge-based Multi-Pulse (DMP) Technique.

Chapter 4 presents the initial characterization of NBTI for $Ge/GeO_2/Al_2O_3$ and its comparison with Si samples. Similar to Si samples, NBTI is activated both electrically and thermally for $Ge/GeO_2/Al_2O_3$. Similarities and differences are discussed, including the impact of stress electric field and stress temperature, the effects of anneal and measurement temperature and defect losses. Contributions of interface states generation are estimated by using charge pumping technique and confirmed further by Id-Vg measurement. An energy alternating model is proposed to explain the defect differentces between Ge and Si devices.

Chapter 5 studies the energy distribution of PCs in the $Al_2O_3/GeO_2/Ge$ gate stack characterized by Discharge-based Multi-pulse (DMP) Technique. Principle of DMP techniques is described and the charge polarity of hole traps is explained. Disturbance from the trapping/detrapping during the measurement is discussed. Energy distribution of PCs in the $Al_2O_3/GeO_2/Ge$ gate stack is characterized. The contribution of interface

states and effects of stress time were further discussed. Quantization effect, Fermi level pinning effect and discharge voltage step are further evaluated for the DMP application on Ge devices. Energy alternating defects are verified though their energy distribution.

Chapter 6 further demonstrates that the defects behave differently in Ge and Si devices. Energy alternating defects exist in Ge devices, which were separated from as-grown hole traps (AHT) to restore power law NBTI kinetics with constant power exponents. The developed Ge method was applicable in Si-cap/Ge devices. NBTI Lifetime is predicted with power low extrapolation for three CMOS technologies to show improvement achieved and the further process/device optimization needed. Si-cap/Ge shows superior reliability while GeO_2/Ge needs further optimization. Also, the impact of defects on the AC NBTI in Ge MOSFETs is evaluated.

Chapter 7 summarizes the thesis and draws conclusions. The topics and direction for future works are discussed.

2 A review of Germanium MOSFETs and challenges in advanced CMOS technology

2.1 Historical overview

Germanium was the semiconductor material used to develop the first transistor by J. Bardeen and W.H. Brattain at Bell Laboratories in 1947 [33], as shown in Fig. 2.1. This invention created a large number of novel solid state electron device applications thereafter, dominating the markets in 1950s to 1970s. From early 1970s, silicon started to replace germanium after high quality silicon wafer were made available, and also because SiO_2 provided a highly stable and naturally high quality interface with silicon substrate in MOSFET structures.

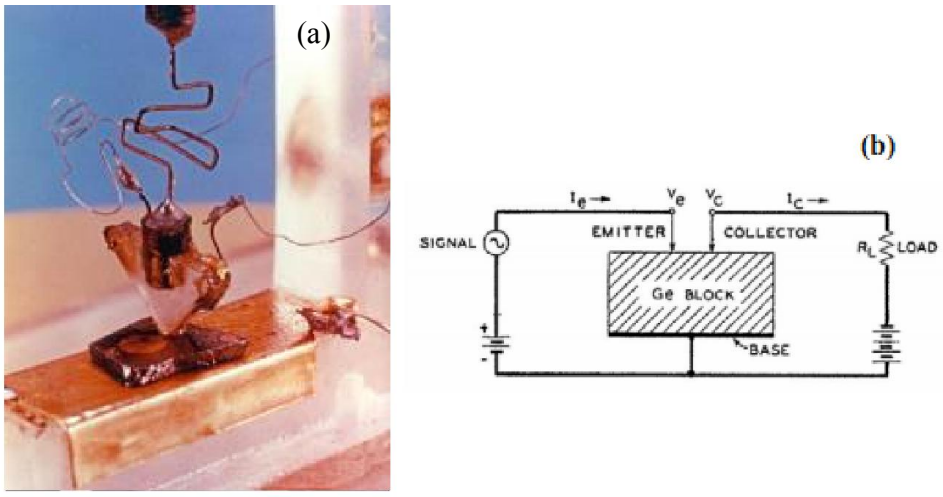

Fig. 2.1 (a) The first point contact Ge amplifier [34] and (b) schematic of semiconductor triode [33]

In 1959, the first integrated circuit was invented by Jack Kilby at Texas Instruments [35] and Robert Noyce at Fairchild Semiconductor [36], which allowed the integration of multiple devices in one chip. The mass production is then enabled after the development of processes for complementary metal–oxide–semiconductor (CMOS) integration technology by Frank Wanlass in 1963 [37]. Since then, ultra large scale integration (ULSI) chips with high speed, high density integration and low power consumption have been achieved by shrinking the feature sizes of transistors over the past fifty years.

The downscaling trend was first described by Moore's Law in 1965 [38], which is the observation that the number of transistors in the integrated circuit doubles in about every two years. This exponential improvement has been the driving force to enhance the performance and reduce the cost, which provides the incentive for semiconductor industry to keep pursuing the down-scaling. In order to further scale down beyond the 45 nm technology nodes following the Moore's law, SiO_2, which had already reached its minimum physical thickness of 1~2 nm for preventing excessively large leakage current, was no longer viable and had been combined with the high-k dielectric at 45nm technology node by Intel in 2007 [39]. For technology beyond the 20 nm node, there are a number of physical limitations to be overcome for achieving higher performance on the Si CMOS. This has become increasingly difficult so that equivalent scaling cycle has slowed down to three years rather than two. Using novel device structures and materials is becoming more and more important for further boosting the performance.

In order to gain adequate drive current for highly scaled MOSFETs, channel materials

with high charge carrier mobility, such as III-V or germanium, are needed. Implementation of non-classical CMOS channel materials is planned to replace Si from 2021 to 2028 according to the International Technology Roadmap for Semiconductor (ITRS) [40]. This has motivated extensive revisits of germanium as an alternative semiconductor material to be integrated with the silicon CMOS platform for building transistors with enhanced performance [40, 41]. Fig. 2.2 shows logic device roadmap in IMEC, highlighting the research underway down to 5nm node. Power was a concern in high performance logic devices and efforts have been made to lower the power supply V_{dd}. For the 7nm node, it is believed that the channel will need to be replaced by high mobility material, Ge for pMOSFETs and InGaAs for nMOSFETs [42].

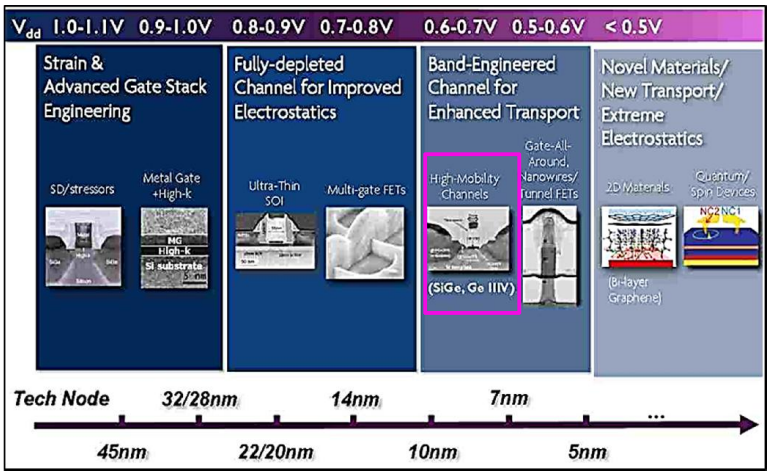

Fig. 2.2 Logic device Roadmap in IMEC 2014 [42]. It highlights the research future down to 5 nm node.

2.2 The properties of Germanium

Germanium has fundamental advantages over Si, as shown by the physical properties listed in Table 2.1 [43]. The mobility, band gap and dielectric constant are also

compared between group IV and III-V semiconductors in Table 2.2. It shows that the electron and hole mobility of Ge is higher than that of Si by a factor of about two and four, respectively. Electron mobility in III-V is more than six times higher than that in Si. It is considered that the III-V nMOSFETs and Ge pMOSFETs are the best combination in terms of achieving the highest mobility. However, practical challenges still remain for the process integration of III-V material with the Si CMOS platform [44]. Germanium, on the other hand, has the advantage of better compatibility with Si. It has been reported that SiGe devices are able to offer superior performance and better reliability than Si for logic circuit applications [15, 45, 46].

Table 2.1 The physical properties of Ge, SiGe and Ge [43]

Properties	**Ge**	**$Si_{0.5}Ge_{0.5}$**	**Si**	**Units**
Atoms	4.42×10^{22}	4.61×10^{22}	5.0×10^{22}	$/cm^3$
Atomic weight	72.60	50.345	28.09	
Breakdown field	$\sim10^5$	2×10^5	$\sim3\times10^5$	V/cm
Crystal structure	Diamond	Diamond	Diamond	
Density	5.3267	3.827	2.328	g/cm^3
Effective density of states in conduction band, Nc	1.04×10^{19}		2.8×10^{19}	$/cm^3$
Effective density of states in valence band, Nv	6.0×10^{18}		1.04×10^{19}	$/cm^3$

Effective mass, m^*/m_0 **Electrons** **Holes**	m^*_l=1.64 m^*_t=0.082 m^*_{lh}=0.044 m^*_{hh}=0.28		m^*_l=0.98 m^*_t=0.19 m^*_{lh}=0.16 m^*_{hh}=0.49	
Electron affinity	4.0		4.05	
Intrinsic carrier concentration	2.4×10^{13}	1.2×10^{13}	1.45×10^{10}	
Intrinsic Debye length	0.68	12.34	24	μm
Lattice constant	5.6575	5.5373	5.4310	A
Minority carrier lifetime	1×10^{-3}	1.75×10^{-3}	2.5×10^{-3}	s

Table 2.2 Comparison of group IV and III-V semiconductors

	Si	**Ge**	**GaAs**	**InAs**	**InSb**
Electron mobility (cm^2/Vs)	1600	3900	9200	40000	77000
Hole mobility (cm^2/Vs)	430	1900	400	500	850
Band gap (eV)	1.12	0.66	1.42	0.36	0.17
Dielectric constant	11.8	16	12.4	14.8	17.7

2.3 Ge surface passivation and defects

The water soluble nature of Ge oxides is one of the major challenges for Ge CMOS process. Although there were early efforts to investigate Ge MOSFETs by utilizing different MOS gate dielectric and junction formation technologies [47-59], significant

progress has only been achieved recently, among which two main approaches have been applied to overcome this problem [60-62]. One is the high-k/GeO_2/Ge structure [60, 61] and the other one is the high-k/SiO_2/Si/Ge structure with a Si capping layer on top of the Ge substrate [62].

2.3.1 High-k/GeO_2/Ge structure

Poor quality of the dielectric/Ge interface and strong Fermi level pinning (FLP) have been the major challenges for achieving high performance for Ge CMOSFETs [63]. It was found by the density functional theory simulation [64] and experiments [63] that the charge neutrality level (CNL) is located at ~0.1eV above the Ge valence band edge. It is very different from Si, in which the CNL is considered to be located at the midgap. Experiments also showed that CNL is responsible for the degraded Pt/HfO_2/Ge nMOSFETs performance at operational conditions, due to the negative charges built up with the Fermi level locating above the CNL [63].

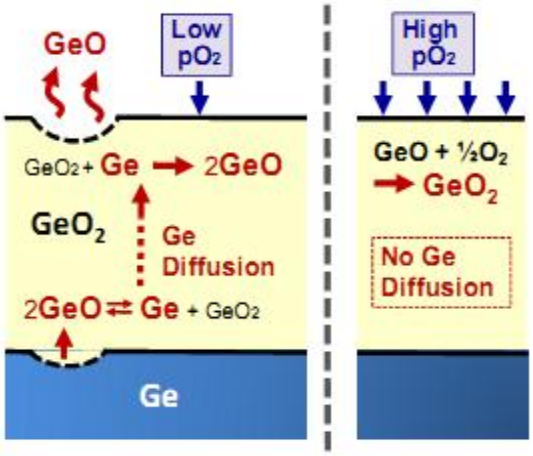

Fig. 2.3 Mechanism of Ge diffusion into GeO_2 and GeO desorption from GeO_2/Ge stack [65].

Fig. 2.3 shows that Ge can diffuse into GeO_2 through GeO desorption ($2GeO <=> GeO_2 + Ge$) under low-pressure O_2 (Low pO_2) ambient and GeO can evaporate away, which deteriorates the GeO_2/Ge interface and the GeO_2 dielectric. High-pressure O_2 (High PO_2) ambient effectively suppressed the GeO generation by $GeO + ½ O_2 => GeO_2$, which could help stop the Ge diffusion [65].

Adding a HfO_2 layer on top of GeO_2, has not been effective in preventing this problem [66]. Latest studies showed that Al_2O_3 can effectively suppress Ge diffusion [61]. High performance Al_2O_3/GeO_2/Ge pMOSFETs was reported by employing novel plasma post oxidation method, with both low density of interface states (Dit) $<10^{11}$ $cm^{-2}eV^{-1}$ and thin equivalent oxide thickness (EOT) around 1nm [67]. Ultra-thin EOT ~0.7nm was achieved by using $HfO_2/Al_2O_3/GeO_2$/Ge gate stacks, in which Al_2O_3 can prevent HfO_2-GeO_2 from intermixing [68]. EOT of 0.5 nm with $HfON/GeO_2$ gate stack has been reported [69]. $HfGeO_4$ and La_2GeO_5 are well bonded at interface as suggested by First principle (FP) calculation [70]. Experimental results confirmed their effective prevention of the Ge diffusion and improvement of interfacial properties [71, 72].

There have been early investigations on the defects in GeO_2/Ge gate stack [65, 73]. Water-related GeO_2/Ge was considered as free of any dangling bonds (DBs), including the GeOx transition region [73]. The energy position of interfacial defects at GeO_2/Ge interface can be either near the conduction band minimum (CBM) or valence band maximum (VBM) [74], verified by using different states of dangling bonds (DBs) with the first-principle study. Oxygen vacancies near GeO_2/Ge interface are the possible

origin of various interfacial states [65]. The fast trapping through interface states is possibly responsible for poor mobility in Ge nMOSFETs [75]. Slow trapping through GeO_2/Al_2O_3 border traps and parasitic S/D series resistance can also cause degradation in Ge nMOSFETs [76].

Recent study shows promising results for GeO_2/Ge pMOSFETs [2, 3, 7-9]. It has been reported that the interface states can be as low as that for SiO_2/Si [7, 8, 10]. This approach also offers the potential for fabricating Ge nMOSFETs [7, 11, 12]. The record hole mobility for this structure can be as high as 596 cm^2/Vs, achieved simultaneously with sub-nm EOT and low Dit of 10^{11} $cm^{-2}eV^{-1}$ [68].

2.3.2 High-k/SiO_2/Si-cap/Ge structure

Many attempts have been made with different high-k materials including HfO_2 [77], ZrO_2 [78], $LaAlO_3$ [79] to find a suitable dielectric for Ge. Efforts have been made also to engineer the Ge interface [80-86]. However, the direct deposition of high-k layer on Ge does not produce the required interfacial characteristics due to large lattice mismatch. The insertion of a Si/SiO_2 layer between Ge and high-k gate stacks can improve the interface quality significantly [23]. Progresses have been made for Ge surface passivation with the growth of a Si-capping layer deposited at 500 °C [4]. A maximum I_{ON} of 350 μA/μm was achieved with 8 mono layer Si-cap and Vth control is optimal for thin passivation layer. However tradeoff is needed between these two, i.e. Ion & Vth. Epitaxial growth of silicon at lower temperature (350 °C) for gate dielectric was proposed as a solution to reduce the Equivalent Oxide Thickness (EOT) [86, 87], as

low-temperature (350 °C) Si deposition shows lower Ge peak at Si surface in the SIMS signal in Fig. 2.4 [88], leading to a lower Dit than high temperature processes. In addition, EOT can be scaled down to 0.8 nm when combined with a reduced HfO_2 layer [89].

The optimized Si capping thickness is found around 6 monolayers [84, 90]. The maximum critical thickness for plastic relaxation of the Si cap grown on Ge has been determined to be 12 MLs [91]. For thicker layer, relaxation defects were determined, whatever the Si growth process used. Thinner Si caps are considered as free of the relaxation defects [92].

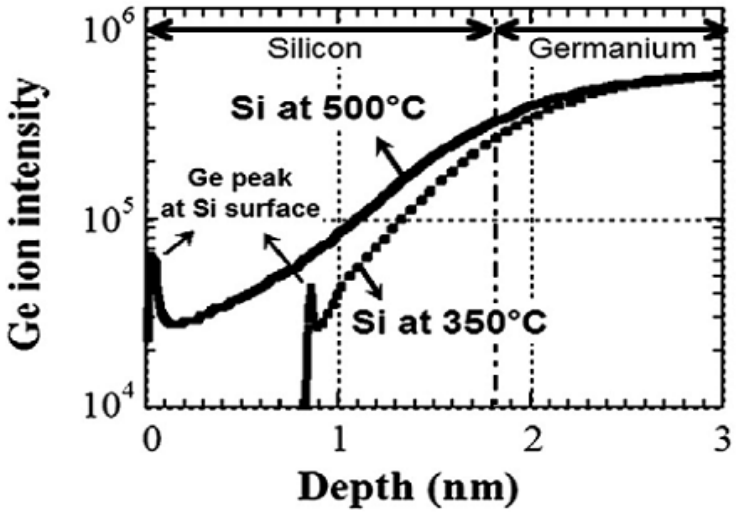

Fig. 2.4 SIMS signal of Ge ion at different temperature [88]. Ge peak at Si surface is lowered at 350 °C deposition.

Possible physical origin of mobility enhancement was examined on Si-cap/Ge [93]. At low effective field (Eeff), the density of coulomb scattering is reduced due to the

separation of mobile charges from SiO_2/Si interface, and at high Eeff, the reduction of surface roughness is due to the channel region moving from SiO_2/Si to Si/Ge at high Eeff. The inserting of thin Si-cap layer plays an important role [93].

Promising results have been reported for Ge with Si-capping layer on top [4]. A record performance of Ion/Ioff: 478μA/μm and 37nA/μm is obtained at Vdd=-1 V with 1 nm EOT on a 65 nm Ge pMOSFET [4].

2.4 Reliability issues in Ge MOSFETs

The quality of Ge MOSFETs has become good enough for their reliability study. As demonstrated in the state-of-the-art Ge-based pMOSFETs, interface states and oxide traps are the main causes of the Vth instability. Negative bias temperature instability (NBTI), positive bias temperature instability (PBTI) and Hot Carrier (HC) degradation are reviewed below.

2.4.1 Positive charges (PCs) in oxide

Extensive works have been done on positive oxide charges in Si dioxide [94-97]. Various names have been used to describe the traps in the oxide, at the SiO_2/Si or Gate/SiO_2 interface, as summarized in Fig. 2.5 [98]. To explain the complex dependence of PCs on biases, time, and temperature, it has been proposed that there are three different types of PCs: AHT (As-grown Hole Trap), ANPC (Anti-Neutralization

Positive Charge), CPC (Cyclic Positive Charge) [94, 99, 100]. AHT has energy levels below the top edge of silicon valence band, i.e. Ev, making them easy to neutralize, but hard to charge. In contrast, ANPC has energy level above the bottom edge of silicon conduction band, i.e. Ec, making them hard to neutralize, but easy to charge. CPC is energetically located within the bandgap and can be repeatedly charged and discharged by alternating gate bias polarity.

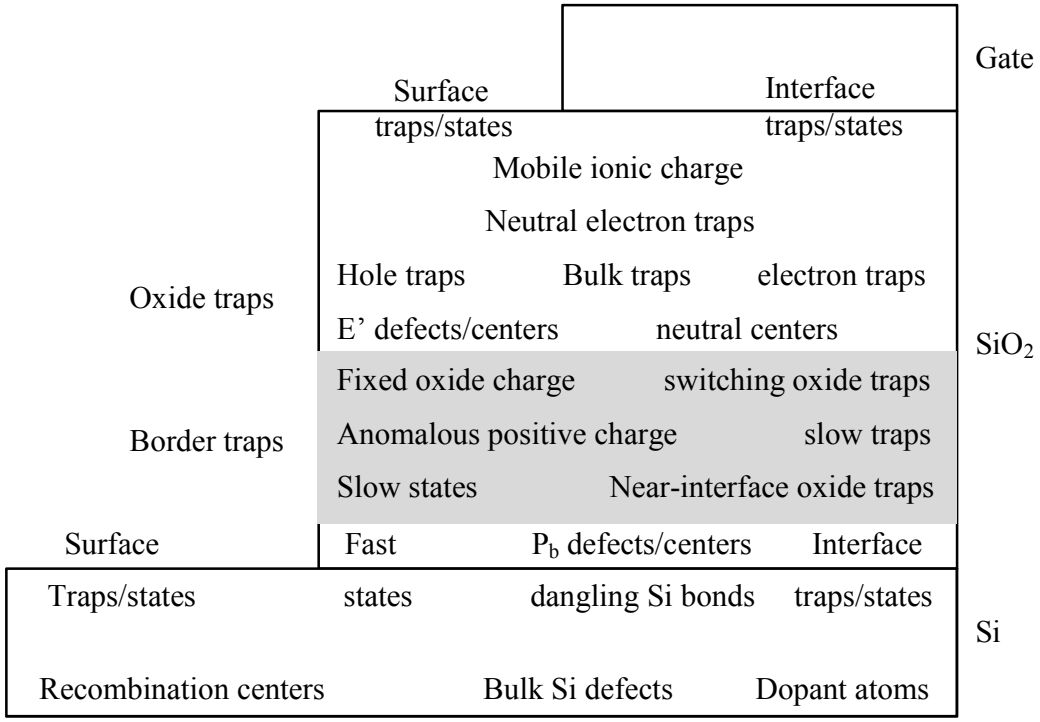

Fig. 2.5 Summary of various names for different types of traps at interface or in the bulk of SiO_2/Si [98].

2.4.2 Negative bias temperature instability (NBTI)

Negative bias temperature instability has been discovered in the early days of MOSFET development by Miura and Matukura in 1966 [101], as shown in Fig. 2.6. It has the highest impact in p-channel MOSFETs, which leads to severe degradation after stress.

The stress conditions for NBTI with thick gate dielectric stacks typically lie below the oxide electric field of 6 MV/cm under temperature from 100 to 300 ºC, but can exceed 10 MV/cm in deeply scaled modern CMOS technology with thin gate stacks. One of the most important parameters for MOSFET, threshold voltage (Vth), is degraded with an increasing absolute Vth value due to NBTI.

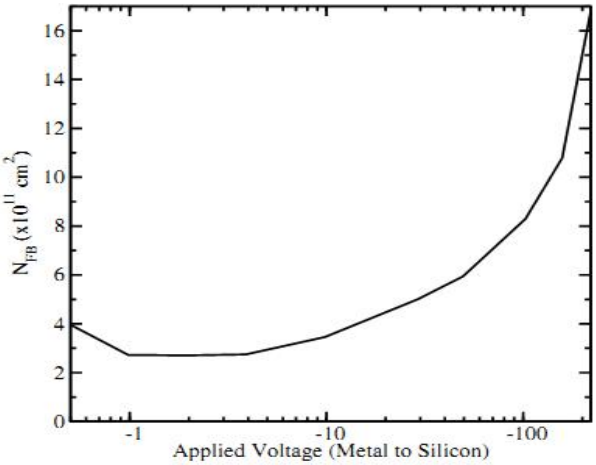

Fig. 2.6 The first report of NBTI effect by Miura and Matukura in 1966 [101]. It shows saturated value of the accumulated electron density at flat-band conditions N_{FB} for different stress voltages.

NBTI has become one of the biggest reliability threats to modern CMOS technologies [102, 103], as the equivalent oxide thickness keeps scaling down, and the oxide electric field becomes higher [64]. It is commonly observed that pMOSEFTs suffer NBTI during the "high" state logic in an inverter, which leads to higher Vth, lower driving current, and longer delay, potentially causing failure of logic circuits [103].

State-of-the-art Ge-based pMOSFETs also suffers NBTI [30]. It has been observed that NBTI of Si-capped Ge pMOSFETs is smaller than their Si counterparts [15, 23]. This

improvement corresponds to the increasing tunneling barrier for holes formed in the Ge channel [40, 41]. Lowering the temperature of epitaxial Si using Si_3H_8 as a precursor is detrimental for Vth stability and hole mobility for thick Si film, but seems beneficial for achieving thinner EOT, lower interface states density, better Vth control and higher mobility for ultra-thin Si-cap layer [4]. Despite the fact that the initial interface state density of Si-cap/Ge was about 2 orders of magnitude higher than the typical values obtained on the Si/SiO_2 interface, the degradation due to NBTI stress remains within acceptable limits.

2.4.3 Positive bias temperature instability (PBTI)

For conventional SiON gate stack, NBTI has larger impact on pMOSFETs, and PBTI can be dominant in nMOSFETs, especially with high-k gate stacks. After stressed at positive bias, a large amount of electrons can be injected into and trapped in the dielectric, leading to Vth shift, which is a severe constraint for reliability of Hf-based CMOS application [104].

Unlike the NBTI, very few PBTI works have been performed on pMOSFETs. However, it has been demonstrated that at the circuit level, PBTI affects both the n- and p-MOSFET in a digital inverter [105]. In analog circuits, the PBTI can also be a regular stress condition for pMOSFETs when the circuit is at the power-down-mode [106].

An important parameter of traps is the capture cross section (CCS), which can be used for modeling leakage, breakdown and device variability. In the first order model, it is

assumed that the traps may have multiple-capture cross sections. The areal density of the trapped electrons, N, is described by,

$$N = \sum_{i=1}^{M} N_i \cdot \left[1 - exp\left(\frac{-\sigma_i \cdot Jt}{q}\right)\right] \quad (2.1)$$

where M is the number of measurable electron capture cross sections, and N_i is the saturation density of traps with a capture cross section of σ_i.

A substantial electron trapping has been reported when the Si-cap/Ge device is stressed under a positive gate bias with two capture cross sections by measuring the transient gate current [16]. The larger one can reach ~10^{-12} cm^2 and reduces for higher Vgs, a signature of columbic attractive trap. This large trap was absent in Si samples with the HfO_2/SiO_2 gate stack. The small one is ~10^{-14} cm^2 and acceptor-like, similar to that found in SiO_2 [107] and HfO_2 [20, 108, 109] in Si MOSFETs.

2.4.4 Hot carrier (HC) degradation

Hot carriers are the electrons or holes that gain high kinetic energy accelerated by high electric field. They are of great concern as these energetic particles can be injected into the oxide, forming oxide charges. These defects can cause threshold voltage shifts and gate leakage current. Hot carrier injection is significant when drain voltage (Vds) is equal to or even larger than gate voltage (Vgs), which will lead to impact ionization near drain region. These hot carriers degrade device performance, as shown in Fig. 2.7.

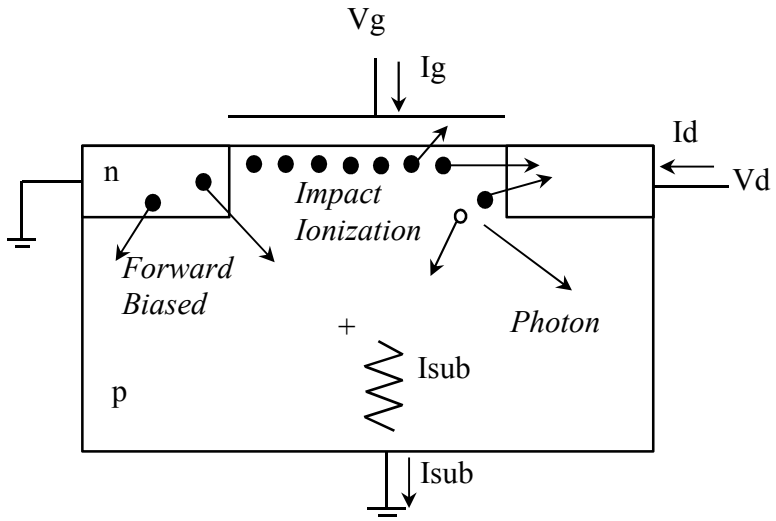

Fig. 2.7 Effect of hot electron near the drain of MOSFETs. The impact ionization leads to hot electron-hole pairs.

HC degradation was confirmed to be highly detrimental for Si-cap/Ge devices, affecting their reliability [110]. A two orders of magnitude higher impact ionization rate is observed in Ge devices, when compared with their Si counterparts. By increasing the Si-passivation thickness, it is possible to improve the device performance in terms of mobility and subthreshold slope [66]. HC degradation can be significantly reduced and meet the required lifetime projections [111]. These results are promising for ensuring sufficient reliability performance of the Ge pMOSFET.

2.5 NBTI models

Various NBTI models have been proposed for Si MOSFETs, although little information

is available for Ge MOSFETs. A review is given below on the Reaction–Diffusion (R–D) model, Hole Trapping Model, Two Stage Model, and As-grown-Generation (A-G) Model.

2.5.1 Reaction-Diffusion Model

The reaction-diffusion(R-D) model was first proposed by Jeppson and Svensson in 1977 [112] to describe the NBTI phenomenon. Two processes are included to model the device degradation, as illustrated in Fig. 2.8.

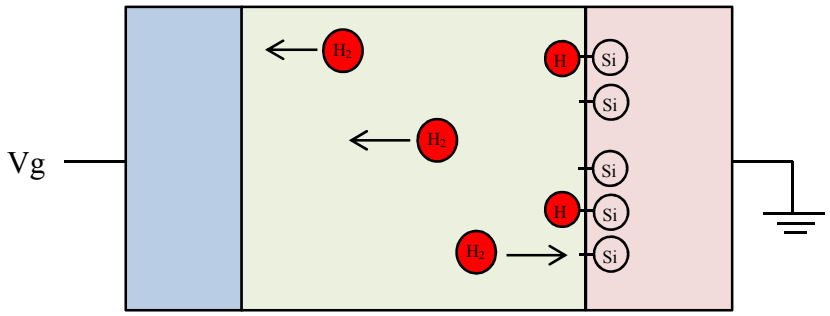

Fig. 2.8 Schematic presentation of the reaction-diffusion (R-D) model proposed by Jeppson and Svensson [112].

One process is the electrochemical reaction at the Si/SiO_2 interface, which breaks the Si-H bond to form the dangling $Si^{\bullet}$ bond, an electrically active interface state and active hydrogen species $H^{\bullet}$,

$$Si - H = Si^{\bullet} + H^{\bullet}. \quad (2.2)$$

The other process is the transport or diffusion of the hydrogen related species from the interface into the oxide bulk or poly-Si gate,

$$H^{\bullet} \text{ (interface)} \rightarrow H^{*}\text{(Bulk)} \tag{2.3}$$

In the standard R-D formulation, the diffusion kinetics is assumed as,

$$\frac{\partial N_{it}}{\partial t} = K_F(N_0 - N_{it}) - K_R N_{it}(N_{H^*})^{1/a} \tag{2.4}$$

where x =0 is the location at the interface of Si/SiO_2 and x > 0 is in the oxide, N_{it} is the number of interface states generated at any given time during stress, N_0 is the initial Si-H bonds and $N_H^{\bullet}$ is the $H^{\bullet}$ concentration at the interface. The forward dissociation rate (K_F) and the re-passivation rate (K_R) are controlled by temperature and oxide electric field. a is the order of reaction. If a =1, neutral atomic H_0 is assumed to be the species during diffusion process, a =2 for the molecular hydrogen diffusion, H_2. For each generated interface state, the number of hydrogen released should be equal to that diffused into oxide, thus

$$N_{it}(t) = \int_0^{\infty} N_{H^*}(x,t)dx \tag{2.5}$$

The recent R-D model is applied only to the interface state generation but oxide charges are also generated in the dielectric [113].

2.5.2 Hole Trapping Model

The hole trapping model is based on the fact that there are trapped charges in the oxide, contributing to the NBTI [113]. The R-D model had been modified recently to include hole trapping in order to simulate the recovery kinetics and dynamic stress [114, 115].

One of the hole trapping models was proposed in 2005 [116]. The basic processes for hole trapping are shown in Fig. 2.9 [95].

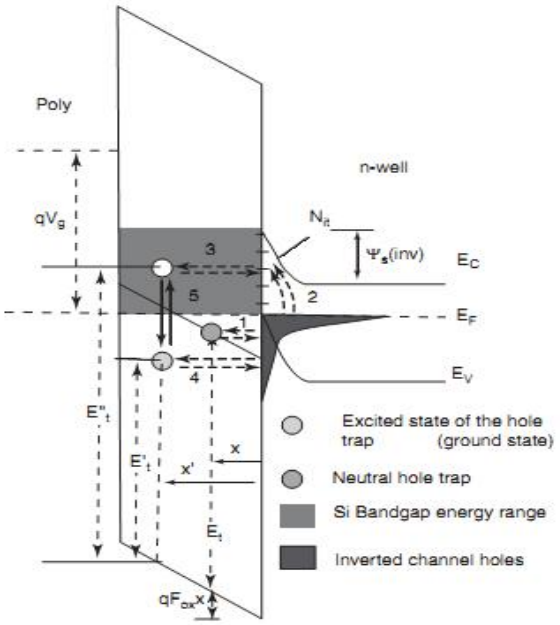

Fig. 2.9 Description of three possible mechanisms for Hole trapping [95]. Traps are positively charged when occupied by a hole and are neutral when empty.

Hole traps are positively charged when occupied by a hole and are neutral when empty. In thermal equilibrium, hole traps with energy below the Fermi level Ef are neutral and become charged when it is above Ef, contributing to the Vth instability. When the device is working in inversion, the energy level of the oxide trap at a distance x from SiO_2/Si interface is given as,

$$E = E_t + q \cdot E_{ox} \cdot x, \tag{2.6}$$

where E_t is the energy level of the traps and E_{ox} is the oxide electric field. Thermal equilibrium is achieved by two types of charge exchange mechanism. Trap below Si

valence band (Ev) is able to be charged and discharged through elastic hole tunneling at the same energy level (path 1). Hole traps at x' above Ev get activated by two different mechanisms. First, path 2 and 3 form a two-step process, as the channel hole could interact with interface states (2), which exchange charge with oxide traps at Et'' by direct tunneling (3). Secondly, a channel hole could tunnel elastically to the excited energy level Et' at x' (4) and then relax to the ground state Et'' by multi-phonon assisted processes (5).

Distribution of the time constant has to be considered for different processes and the total time constant associated with the hole trapping is given by

$$\frac{1}{\tau} = \frac{1}{\tau_1} + \frac{1}{\tau_{23}} + \frac{1}{\tau_{45}} \tag{2.7}$$

2.5.3 Two Stage Model

The two stage model [117] is based on the multiphonon-field-assisted tunneling (MPFAT) [118, 119] and Harry-Diamond-Laboratories (HDL) model [120], which is initially developed for the emission of particles from deep traps and switching oxide traps, respectively.

In the first stage, holes can be trapped into oxygen vacancies near interface by the MPFAT mechanism. The defect transforms into a positively charged E' center after the hole capture. In this configuration, hole can be charged and discharged repeatedly. But only in neutral state 3, the E' center can be fully recovered. In the second stage, the

increased hole concentration enhances the creation of slowly recoverable defects, probably Pb-centers in SiO_2. It is assumed that the transition of hydrogen is much slower than the hole capture or emission process.

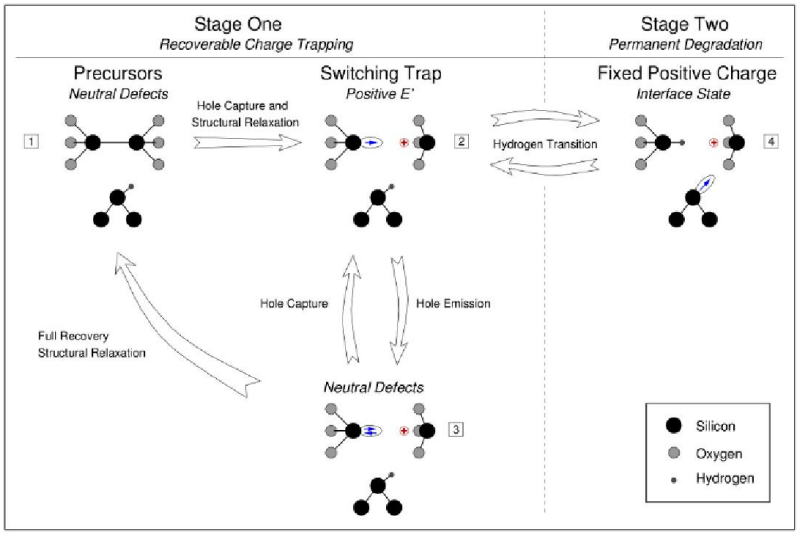

Fig. 2.10 The two stages for the trapping dynamics [117]. Stage one, the recoverable charge trapping and stage two, the permanent degradation.

2.5.4 As-grown-Generation (A-G) Model

Although extensive studies have been carried out on NBTI models [96, 117], an agreement has not been reached. It was reported that the R-D model contradicted with the experimental data for the recovery kinetics, suggesting a non-diffusion-limited process [96]. On the other hand, the two stage model has too many adjustable fitting parameters [97]. Stress acceleration is widely used to assess device lifetime in the semiconductor industry. A model must have prediction ability.

Three different types of positive charges in the dielectric have been discussed in Section 2.4.1: anti-neutralization positive charges (ANPC), cyclic positive charges (CPC), and as-grown hole trapping (AHT), as shown in Fig. 2.11. AHT is as-grown defects, while CPC and ANPC are generally considered as defects generated in Si MOSFETs. For the thin oxide MOSFETs, power law empirical model was proposed [121] and supported by early works with slow DC measurement [121-123], which was dominated by generation of defects.

$$\Delta V_{th} = C * |V_{ov}|^{\gamma} t^{n} \ , \tag{2.8}$$

And the charging of AHT generally follows the first order reaction model [124],

$$\Delta N_{ot} = N\left[1 - exp\left(-\sigma Q_{inj}\right)\right] \ , \tag{2.9}$$

where ΔNot is trap charge density, Qinj is hole injection level and σ is the capture cross section.

As-grown Generation (A-G) Model [125] was proposed to explain data with fast Pulse measurement by combining these two and has been evaluated based on the understanding of different positive charges by researchers at LJMU

$$\Delta \mathrm{V_{th}} = \mathrm{At^{n}} + \mathrm{B}[1 - \exp(-t/t^{*})] \tag{2.10}$$

where 'A', 'n', 'c', and t* are constants and were obtained by fitting test data with a least square technique, for a given stress temperature and bias.

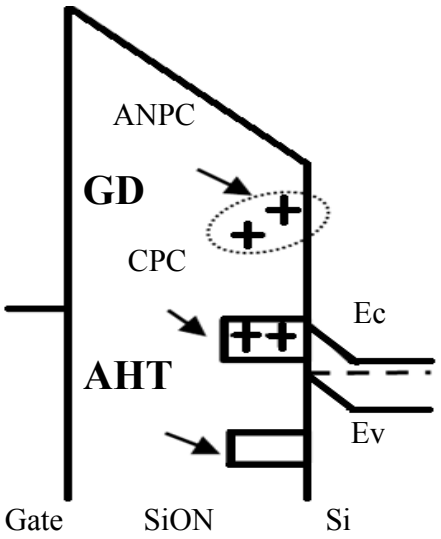

Fig. 2.11 Three types defects in SiON/Si device: As-grown Traps (AHT), Cyclic positive charges (CPC), and Generated traps (GD) in oxide

Reliable lifetime prediction method [126] has been proposed based on separating the generated from the As-grown defects. A-G Model and the lifetime prediction method are verified on devices with different processes, including SiON/Si and high-k/SiON/Si. A detailed understanding of the defects and the induced Vth instability in the advanced Ge MOSFETs will be investigated in this thesis.

2.6 Summary

In this chapter, the technology of MOSFETs and its historical development are reviewed. The properties of germanium material are discussed for its fundamental advantage over Si. Two structures, GeO_2/Ge and Si-cap/Ge, are further focused on its surface passivation and defects, which leads to the reliability issues in Ge MOSFETs, such as NBTI, PBTI and HC degradation. NBTI models for Si MOSFETs are discussed, including R-D model, hole trapping model, two stage model and A-G model.

3 Experimental Facilities and Characterization Techniques

3.1 Introduction

New measurement techniques and instrumentations have been developed for further understanding the reliability issues and new channel materials in the latest CMOS technologies. In this chapter, the experiment system and instruments used in this thesis are presented, focusing on their application for Ge pMOSFETs. Conventional techniques are reviewed, including the DC Id-Vg technique, Charge Pumping (CP) technique, Capacitance Voltage (C-V) technique and Conductance technique. Limitations of conventional techniques for Ge MOSFET application are discussed. Several advanced fast measurement techniques are also presented, including the Pulse Id-Vg (Pulsed I-V) technique, Ultra-Fast Pulsed (UFP) technique, Ultra-Fast On-The-Fly (OTF) technique and Discharge-based Multi-Pulse (DMP) technique.

3.2 System and Instrumentation

The DC characterization system includes the Agilent E5270 Parameter Analyzer and 81110A Pulse Generator. They are controlled by a GPIB card with an IEEE 488 port and data can be transported and saved into a personal computer. Agilent E5270 includes

4 Source Measure Units (SMUs), which allows accurate DC measurement down to 10^{-12} A. User interface was designed and written in visual basic language. Parameter analyzer and pulse generator are controlled by specifically designed programs to execute the Id-Vg and Charge Pumping measurements.

Keithley 4200 Semiconductor Characterization System contains the 4210-SMUs and 4210-CVU, 4225-PMUs (Pulse Measure Units), and 4225-RPM Remote Amplifier/Switch offering additional low current ranges down to tens of picoamps. All these modules are installed in one chassis which allows easy experiment operation, such as Id-Vg, Charge Pumping, C-V measurement. Program written in C language is used to control the hardware and it is flexible for users to implement applications using the KITE and KULT software within the system. Both the DC characterization system and K4200 system can be connected to the advanced Cascade 1200 Probe Station. Devices with feature sizes down to nanometer can be probed, using the system shown in Fig. 3.1.

Fig. 3.2 is a picture of the Pulse Characterization System. The system consists of a home-made current-to-voltage converter circuit (OPA657) with E3631 DC power supply, an Agilent MSO8104A Oscilloscope and a Pulse Generator (81150A). Pulse Generator is used to supply gate bias waveform and the circuit was designed to convert and amplify the current to voltage signal, which is captured by the oscilloscope.

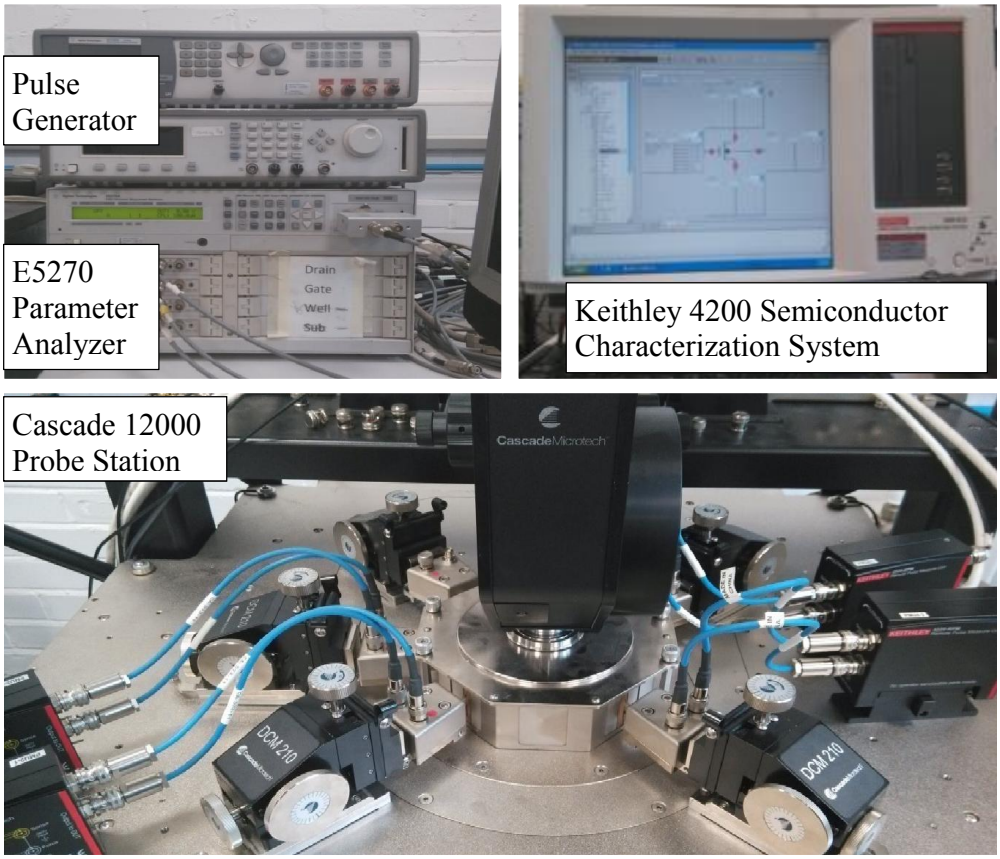

Fig. 3.1 Photograph of DC characterization systems, Keithley characterization system and Cascade 1200 Probe station used in the thesis.

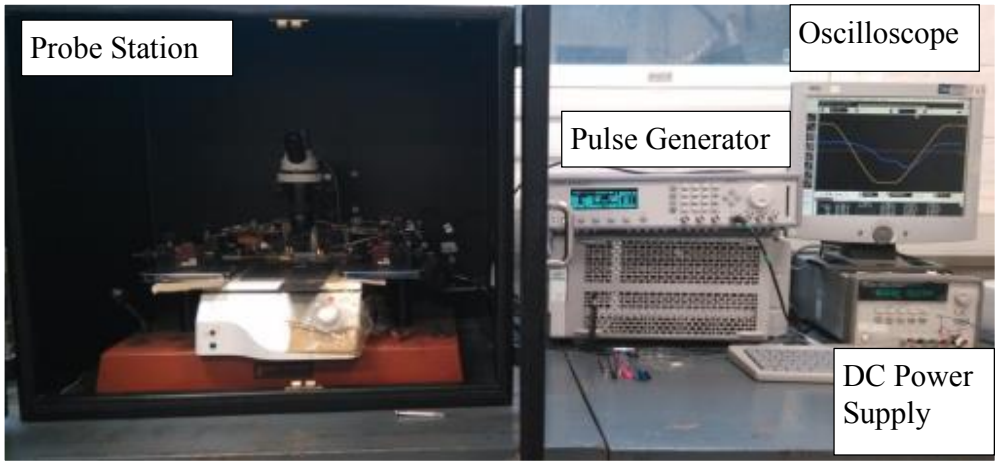

Fig. 3.2 Home-made Pulse Measurement System with converter circuit, pulse generator and Oscilloscope used in the thesis.

3.3 Layout of Ge samples

The testing samples used in this project were manufactured at the Interuniversity Microelectronics Research Centre (IMEC), Belgium. The advanced process technology and facilities at IMEC produced the state-of-the-art CMOS devices with industrial standards. The layout of Ge samples is shown in Fig. 3.3.

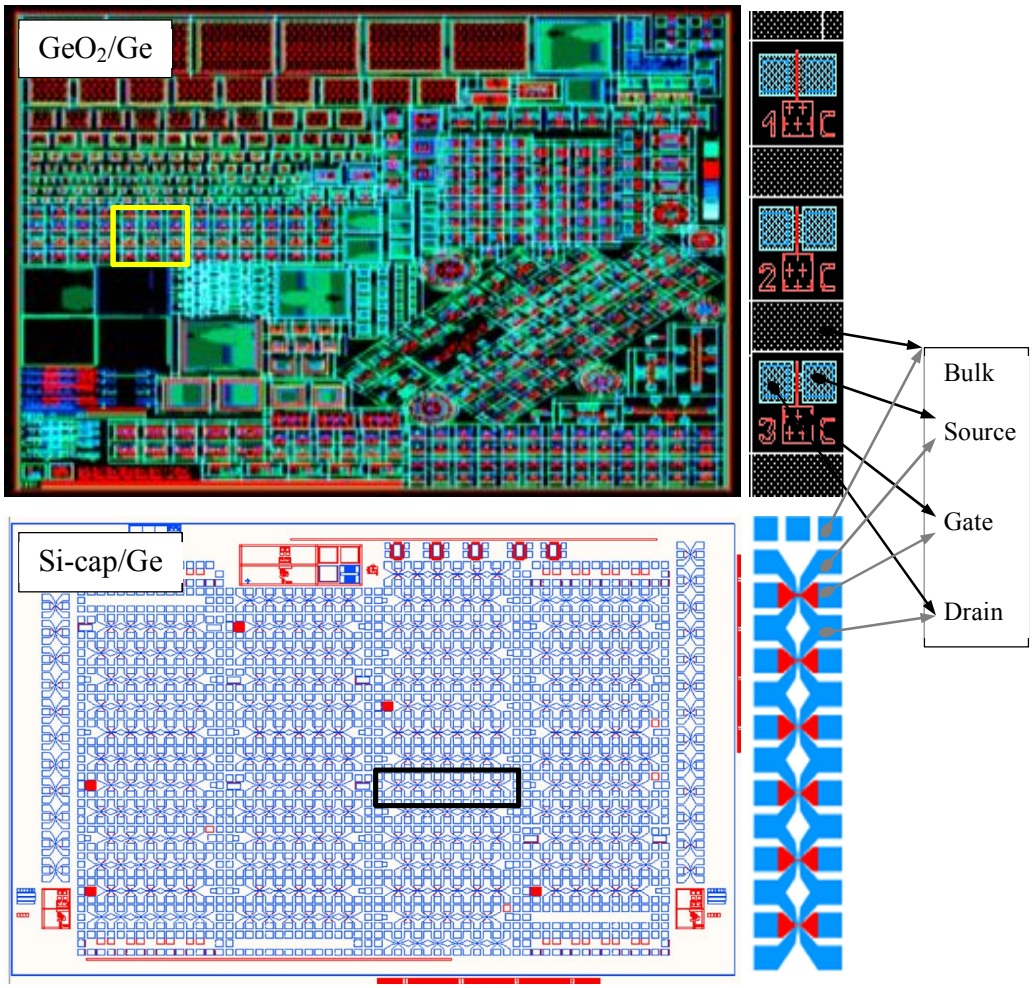

Fig. 3.3 Layout of advanced GeO_2/Ge and Si-cap/Ge devices and devices with different feature size are distributed in one block.

There are devices with different sizes in each block with a typical channel width / length of 50 μm / 1 μm for GeO_2/Ge and Si-cap/Ge devices. Source and Drain are designed with small active area in order to achieve lower leakage. Detailed process and sample information are given in the experiment descriptions.

3.4 Conventional Characterization Techniques

Threshold voltage is extracted by the Conventional Id-Vg (DC I-V) technique with either the extrapolation or constant current method. The interface characterization techniques include the Charging Pumping (CP) method, Capacitance Voltage (C-V) method, and Conductance method. To evaluate the passivation level of high traps density at the oxide semiconductor interface, further investigation has been carried out recently on Ge MOSFETs [9, 127].

3.4.1 Conventional Id-Vg (DC I-V) Technique

The threshold voltage (Vth) is an important parameter for MOSFETs [128], which can be extracted from the conventional DC Id-Vg measurement technique. The drain current, Id, is measured with gradually changed gate voltage Vg at a low drain voltage Vd, typically 25-100mV. In the linear operational region of a MOSFET, Id can be expressed by

$$I_d = \frac{W}{L_{eff}} \cdot \mu \cdot C_{ox} \cdot \left(V_{gs} - V_{th}\right) \cdot V_{ds} \tag{3.1}$$

where W is the channel width, L is the effective channel length, Cox is the oxide capacitance per unit area, μ is the effective free-carrier mobility, and Vgs and Vds are the intrinsic gate–source and drain–source voltages, respectively.

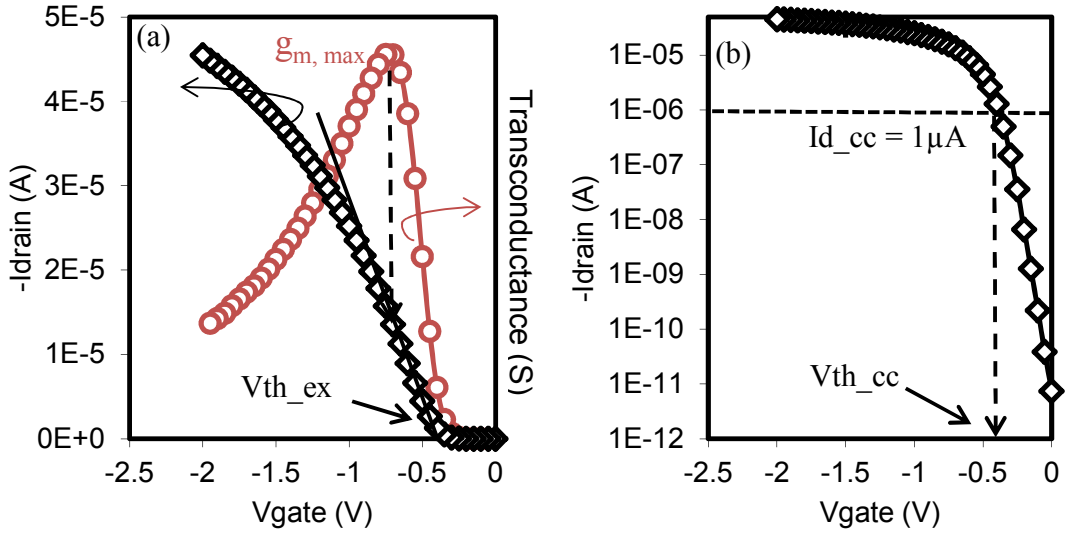

Fig. 3.4 Threshold voltage determined by the (a) Extrapolation Method and (b) Constant Current Method

Several extraction methods [128-130] have been proposed based on the transfer characteristics, among which the Extrapolation Method [131-134] and Constant Current Method [131-135] are widely used and accepted in industry, as shown in Fig. 3.4.

Extrapolation Method: It is a common practice to find the point of maximum transconductance, g_m, which is the first-order derivative (slope) of the Id-Vg curve. Vth is determined from a linear extrapolation of Id-Vg at this point with this slope.

Constant Current Method: The gate voltage at a specific threshold drain current is taken as the Vth. Typically, a constant current is chosen as (W / L) × 100 nA [136], where W and L are the channel width and length, respectively.

3.4.2 Charge Pumping (CP) Technique

Brugler and Jespers developed the CP technique in 1969 [137]. Various charge pumping techniques were further developed to achieve reliable measurement [138] and provide detailed information on interface states [139, 140], including the Frequency Modulated CP (FM-CP) [141, 142], On-The-Fly Charge-Pumping (OTF-CP) [143], Ultra-Fast Charge Pumping (UF-CP) [144, 145] and Single Pulse Charge Pumping (SP-CP) [146].

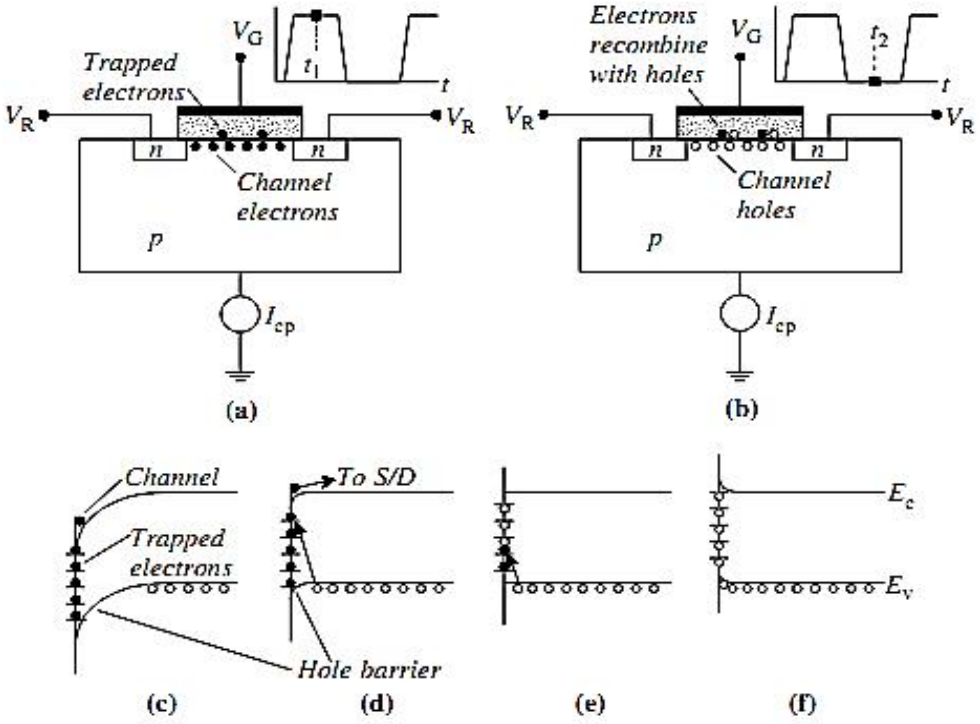

Fig. 3.5 Device cross-sections and energy diagrams for charge pumping at different bias [131].

The Charge Pumping Technique is explained with nMOSFET as an example in Fig. 3.5 below. In the inversion region, electrons are either in the channel or trapped in the dielectric, shown in Fig. 3.5(a)&(c). Most channel electrons are going into the source or drain when gate waveform sweep from positive to negative. Interface states near conduction band edge can be emitted and also drift to the source or drain (see Fig. 3.5 (d)), while the remaining stay charged due to insufficient emission time (see Fig. 3.5(e)).

During the transition from inversion to accumulation, holes start to flow into the channel and recombine with the electrons left in the band gap. The charge during the recombination process is given by,

$$Q_{ss} = A_G \cdot q \int D_{it}(E)\, dE \ , \tag{3.2}$$

It can also be expressed as,

$$Q_{ss} = A_G \cdot q^2 \cdot D_{it} \cdot \Delta\Phi s \ , \tag{3.3}$$

where A_G is the channel area of the transistor (cm^{-2}),

Dit (E) is the surface-state density at energy level E ($cm^{-2}eV^{-1}$),

Dit is the mean surface-state density, averaged over the energy levels swept by the Fermi level ($cm^{-2}eV^{-1}$),

$\Delta\Phi s$ is the total sweep of surface potential,

q is the electron charge ($1.6\times10^{-19}C$), and

ΔE is the total sweep of energy range.

When applying sweep gate pulses with frequency f, this charge Qss will also give rise to a substrate current, Icp, given by

$$I_{CP} = f \cdot Q_{ss} = f \cdot A_G \cdot q^2 \cdot D_{it} \cdot \Delta\Phi s \tag{3.4}$$

$$\Delta E = q \cdot \Delta\Phi s \approx E_g - KT\left[ln(\sigma_n v_{th} N_c/2f) + \left(ln\left(\sigma_p v_{th} N_v/2f\right)\right)\right] \tag{3.5}$$

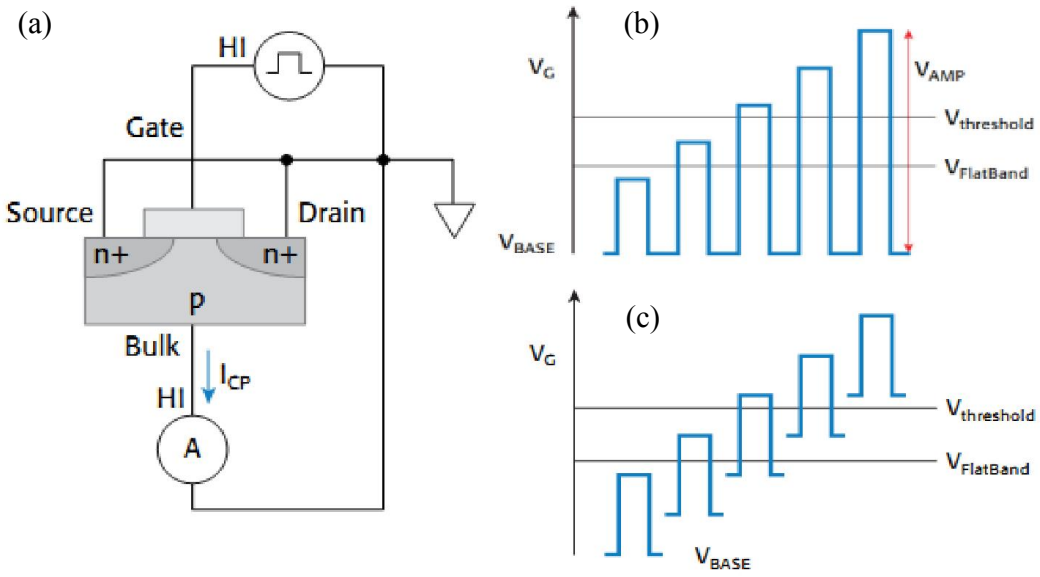

Fig. 3.6 (a) Basic charge pumping measurement setup. Applied pulse waveform for (b) fixed base voltage charge pumping and (c) fixed amplitude charge pumping technique.

Icp can be measured using either the fixed base voltage method or fixed amplitude method, and the pulse waveforms are shown in Fig. 3.6. Interface states density, Nit (cm^{-2}) and Dit ($cm^{-2}eV^{-1}$), can be calculated by

$$N_{it} = \frac{I_{cp}}{q \cdot f \cdot A_G} \tag{3.6}$$

$$D_{it} = \frac{I_{cp}}{q \cdot f \cdot A_G \cdot \Delta E} \tag{3.7}$$

Typical charge pumping measurement results on high-k/SiO_2/Si devices are shown in Fig. 3.7. Icp is plotted versus Vpeak (Vbase plus Vampl) for these two methods.

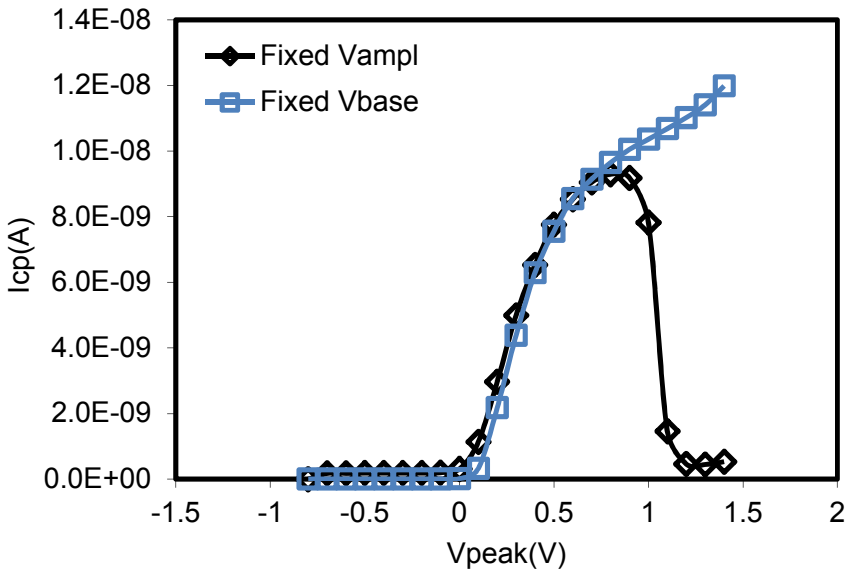

Fig. 3.7 Typical experimental results in High-k/SiO_2/Si device obtained by using fixed amplitude (1.2V) and fixed base voltage (-0.8V) charge pumping technique. Substrate currents were measured by using waveforms in Fig. 3.6, with 50% duty cycle, 20 ns edge time and 1 MHz frequency.

3.4.3 Conventional Capacitance Voltage (C-V) Technique

Capacitance is defined as the change in charge (Q) of one device that occurs when there is a change in voltage (V), as given by

$$C = \frac{\Delta Q}{\Delta V} \tag{3.8}$$

High Frequency CV (HF-CV): The HF-CV measurement is usually carried out at 10 kHz ~ 1 MHz and the simplified capacitance measurement circuit and configuration [147] are shown in Fig. 3.8.

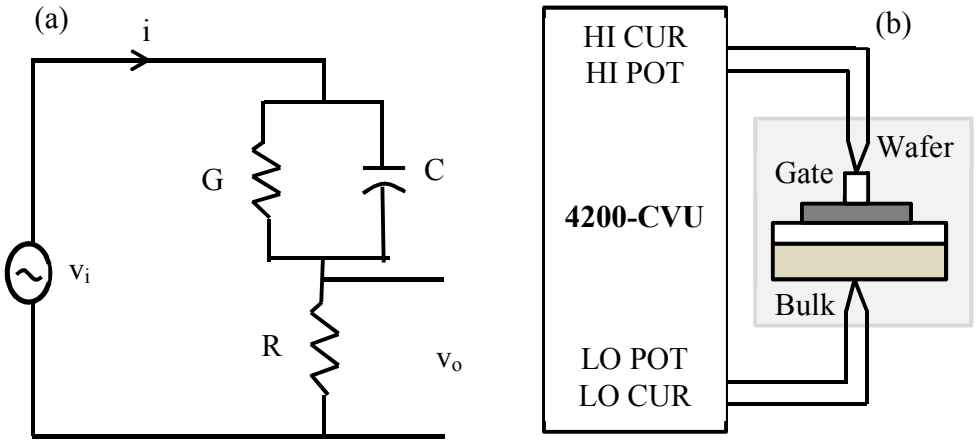

Fig. 3.8 Simplified circuit (a) and configuration of HF-CV test (b) in MOS capacitor by Keithley4200-CVU.

A small AC signal (typically 10~30 mV) is applied to the device under test (DUT) and the AC current *i* through the device and resistor can be measured as

$$v_0 = i \cdot R = \frac{R}{Z} \cdot v_i = \frac{R}{R + (G + jwC)^{-1}} \cdot v_i$$

$$= \frac{RG(1 + RG) + (\omega RC)^2 + j\omega RC}{(1 + RG)^2 + (\omega RC)^2} \cdot v_i \qquad (3.9)$$

where R is output resistor, G is the conductance and C is the capacitance. MOS device is represented by the parallel G/C circuit. For $RG \ll 1$ and $(\omega RC)^2 \ll RG$,

$$v_0 \approx (RG + j\omega RC) \cdot v_i \qquad (3.10)$$

Low Frequency (Quasi-static) CV (QS-CV): In the QS-CV measurement [148, 149] the current is measured in response to voltage change with a slow ramp, as shown in Fig. 3.9.

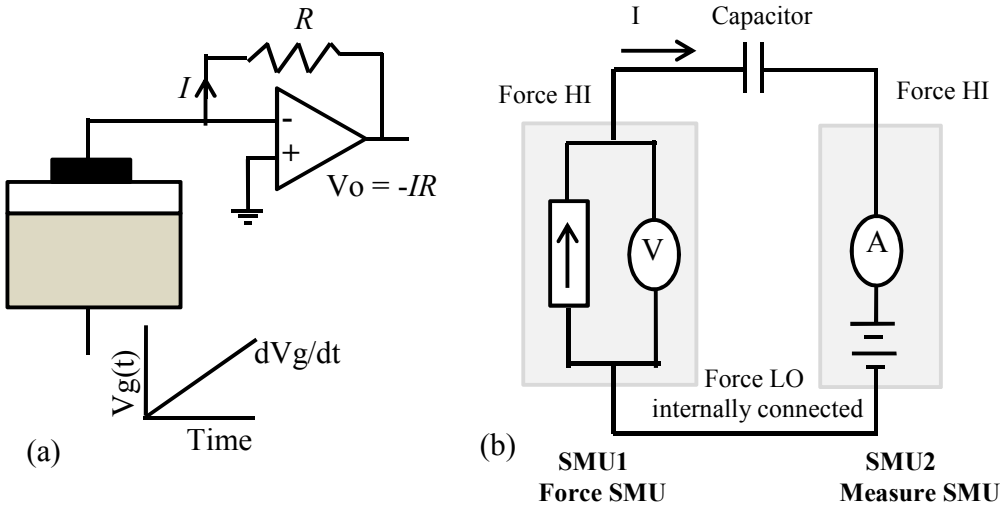

Fig. 3.9 Simplified circuit (a) and configuration of QS-CV (b) in MOS capacitor by Keithley4200-SMU.

The current measured from the amplifier circuit is expressed as

$$I = \frac{dQ}{dt} = \frac{dQ}{dV_g}\frac{dV_g}{dt} = C \cdot \frac{dV_g}{dt} \tag{3.11}$$

where dVg/dt is a constant Ramp Rate, I is proportional to C and QS-CV is obtained if the Ramp Rate is sufficiently low. Noise can be significant when the Ramp Rate is smaller than 0.1 V/s [149].

Interface States Response: HF-CV and QS-CV technique can be used to characterize interface states. High frequency CV method was developed by Terman to determine interface states density in 1966 [150] in which interface states at a high frequency cannot respond to the AC signals but can still follow the DC bias, causing the C-V curve to stretch out, as shown in Fig. 3.10.

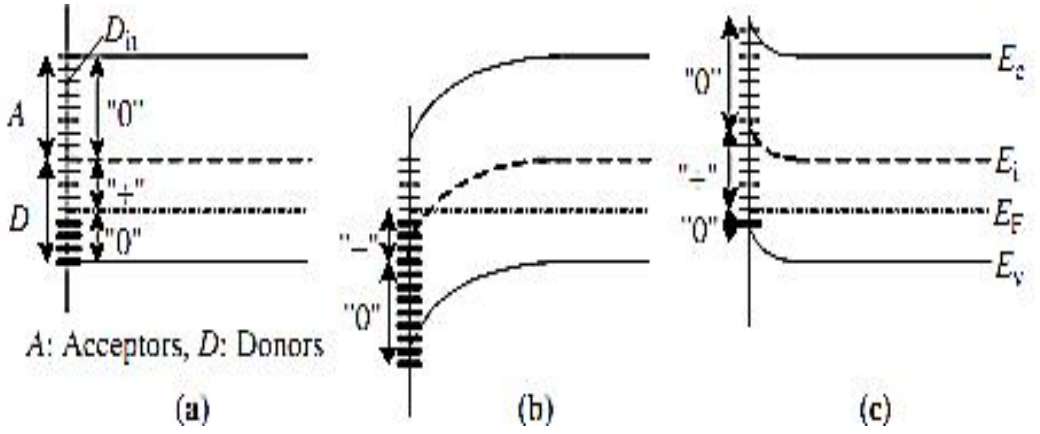

Fig. 3.10 Illustration of the effect of interface states (a) Vg = 0 (b) Vg > 0 and (c) Vg < 0. Electron-occupied interface states are indicated by the small horizontal heavy lines and unoccupied ones by the light lines. [131]

The effect of interface states is shown in Fig. 3.11. The C-V curve is stretched out along the voltage axis, due to the interface states contribution to the interface states capacitance, Cit. The occupancy of donor and acceptor interface states is changing with Ef at different energy level.

When interface states exist at a certain surface potential Φs, experimental Φs versus Vg curve is a stretched-out version of theoretical one. By comparing these two, the interface states density can be determined by

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_g}{d\Phi_s} - 1\right) - \frac{C_s}{q^2} = \frac{C_{ox}}{q^2} \cdot \frac{dV_g}{d\Phi_s} \tag{3.12}$$

where dVg = Vg (Dit ≠ 0) – Vg(Dit = 0) is the voltage shift.

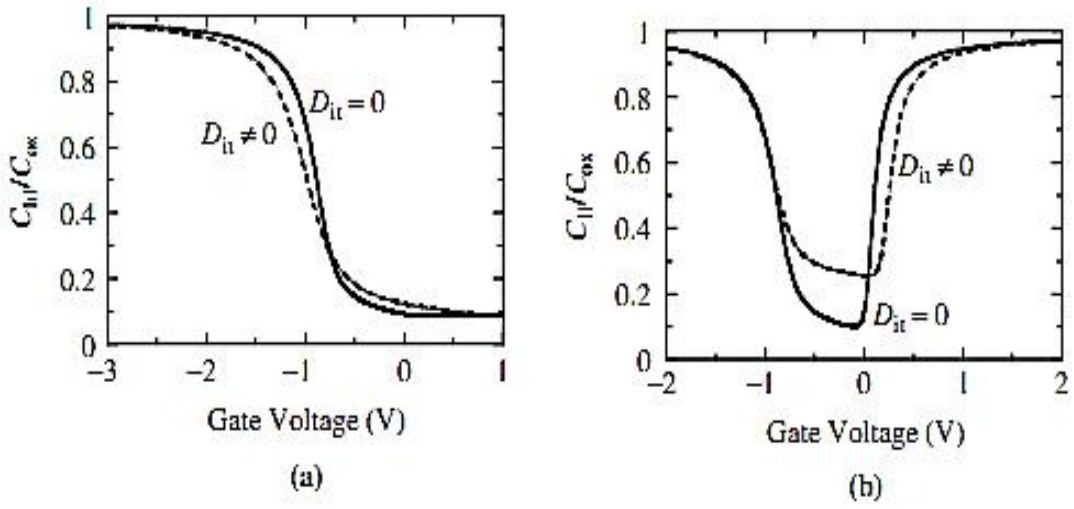

Fig. 3.11 Effect of Dit on (a) High and (b) Low Frequency Capacitance-Voltage characteristics [131].

Quasi-Static method was developed by Berglund [151] by comparing a low frequency C-V with theoretical curve, as shown in Fig. 3.11(b). The interface states density can be determined by

$$D_{it} = \frac{1}{q^2}\left(\frac{C_{ox}C_{lf}}{C_{ox}-C_{lf}} - C_s\right) \tag{3.13}$$

where Cs is theoretical semiconductor capacitance, Cox is the oxide capacitance, C_{lf} is measured capacitance at low frequency.

3.5 Limitation of conventional Techniques for Ge MOSFETs

DC Id-Vg Technique: Gate stacks with high-k layers show different charge trapping or detrapping behavior from that for the conventional SiO_2 interfacial layer. The time scale can vary from milliseconds to microseconds [152] and it strongly depends on gate

voltage and polarity, which make the conventional techniques too slow to capture the fast trapping/detrapping process.

Charging Pumping Technique: CP is capable of probing the interface states near mid band of the gap, which counts to a small part of the interface states in Ge MOSFETs [153], due to the smaller band gap and higher interface states density near the band edge in Ge devices. As an alternative, charge pumping measurement with transition time as short as 6 ns or at lower temperature (80 K) have been used to capture a larger range of interface states along the band gap, as demonstrated in Fig. 3.13 [153]. Therefore, interface states close to band edge of Ge require careful characterization.

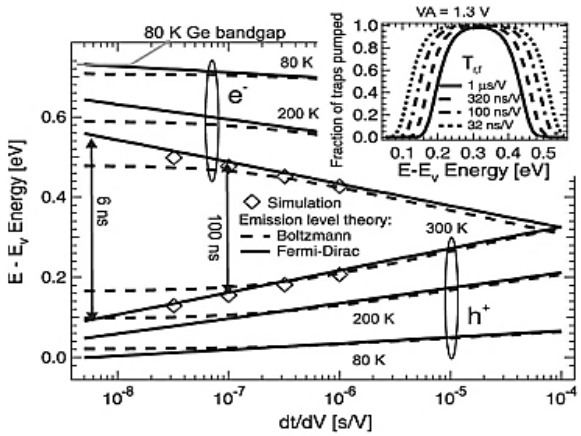

Fig. 3.12 Calculated electron and hole emission levels with Boltzmann and Fermi-Dirac statistics at different temperature of Germanium. (Inset) Simulation of the faction of traps probed with different rise/fall time at RT. Emission-level theory is compared with the other two calculations to prove the validity on Ge MOSFETs [29].

Capacitance Voltage Technique: The conventional CV was developed for MOS capacitors and requires the gate leakage current to be small when compared with the

capacitance current. The gate leakage increases exponentially as the oxide thickness reduces. This makes the conventional QS-CV inapplicable to thin oxides, since the low ramp rate required to maintain thermal equilibrium generally gives a displacement current lower than the leakage. When HF-CV was taken on Ge MOS capacitors, Fig. 3.13 shows frequency dispersion in inversion due to the faster response of minority carriers in low band gap semiconductor [154-156].

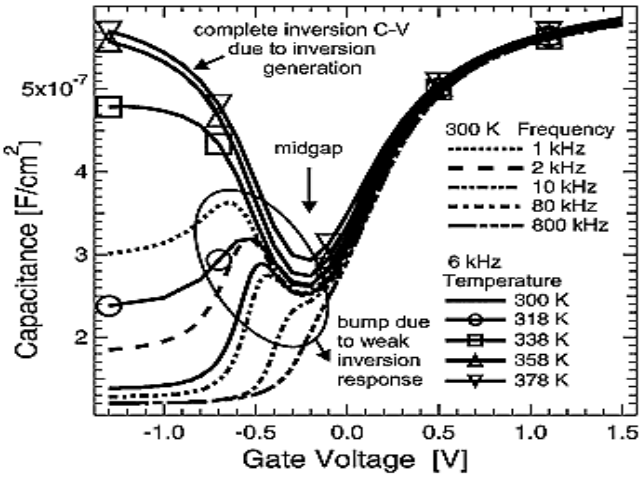

Fig. 3.13 Temperature and frequency dependence of C-V curve shows the effect of weak inversion response at lower frequency and temperature and the effect of generation causing complete inversion C-V in n-type GeOxNy/Ge device.

3.6 Stress-and-Sense Methodology

3.6.1 Typical Methodology

Stress-and-Sense Methodology has been commonly used for reliability verification. The typical NBTI experimental sequence is summarized in the flow chart of Fig. 3.14.

Devices were characterized before and after a certain time of aging, to assess the quality and understand the failure mechanism [157].

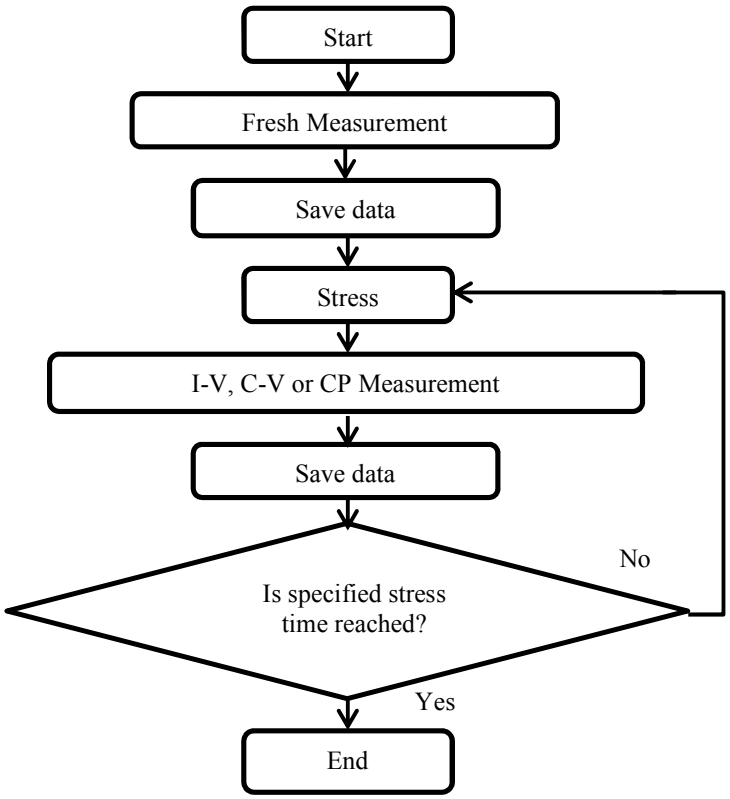

Fig. 3.14 Flow chart of typical Stress-and-Sense methodology, I-V, C-V or CP is measured periodically after stress.

3.6.2 Integration of multiple types of measurements

The integration of multiple types of measurements is desirable, as it is hard to compare measurement results under various conditions and with different measurement instrumentations. Multiple types of measurements have integrated into one configuration, as shown in Fig. 3.15 [158]. The remote amplifier/switches and the multi-measurement

performance cabling used to connect them to the probe manipulators on the wafer probe station are critical for integrating accurate Pulsed I-V, C-V, and precision DC I-V measurements into the same parametric analysis system.

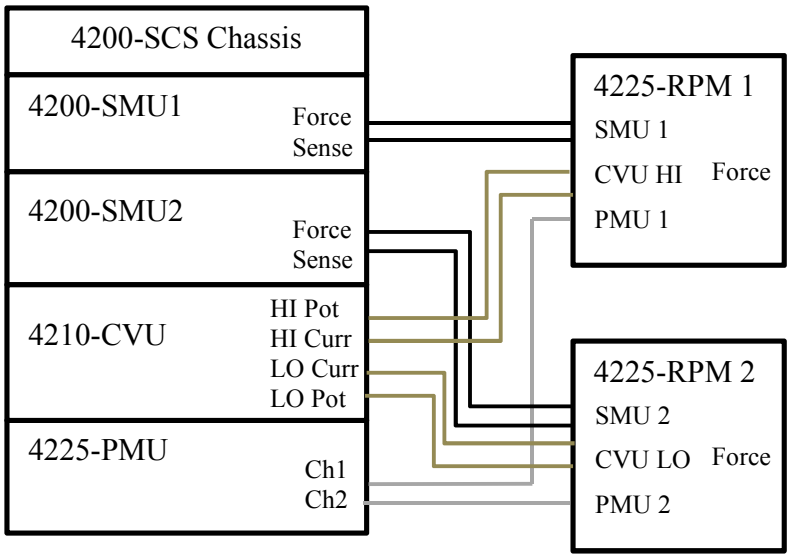

Fig. 3.15 Integration of Multiple Measurement Types, including DC I-V, C-V and Pulsed I-V measurement. Configuration is shown as an example with two RPMs, which can switch mode to the SMUs, the CVU or the PMU channels in Keithley 4200 system.

3.7 Advanced Characterization Techniques

3.7.1 Pulsed Id-Vg (Pulsed I-V) Technique

High-k gate dielectric, such as Al_2O_3, HfO_2, has been developed for advanced CMOS devices. Advanced techniques discussed below include the Pulsed Id-Vg (Pulsed I-V) Technique, Ultra-Fast Pulsed (UFP) Technique, Ultra-Fast On-The-Fly (OTF)

Technique and Discharge-based Multi-Pulse (DMP) Technique to overcome the fast charging/discharging issue [152].

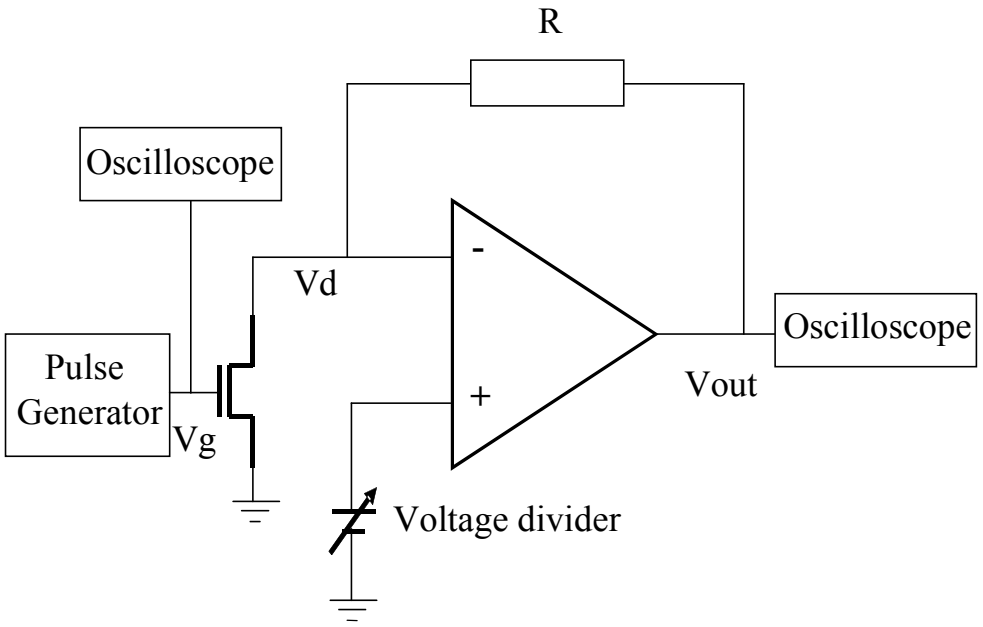

Fig. 3.16 The circuit used as a current to voltage convertor for Pulsed Id-Vg (Pulsed I-V) Technique.

The circuit designed for the Pulsed I-V measurement in the microelectronic reliability laboratory at Liverpool John Moores University [146] is shown in Fig. 3.16. Many works have been carried out based on this technique [146, 159-161].

A pulse generator is used to supply the gate waveform. Drain is biased with a small voltage, Vd (-0.1V), by a battery through a voltage divider. Source is grounded. Oscilloscope is used to capture the gate waveform and output voltage from the drain side of transistor through feedback resistor. Drain current, Id, is given as,

$$I_d = (V_{out} - V_d)/R \ , \tag{3.14}$$

where R is at range 1 ~ 10 kΩ. Typical results are shown in Fig. 3.17.

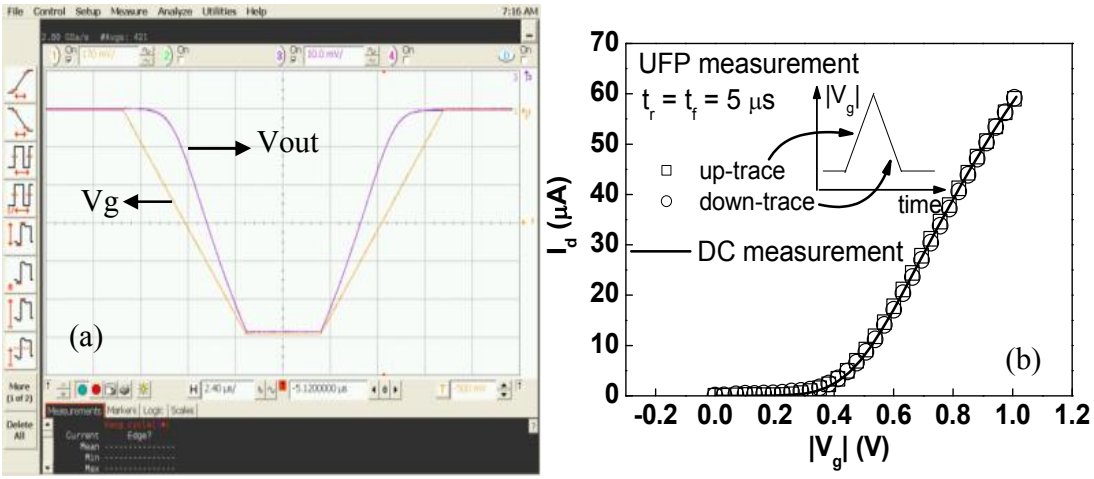

Fig. 3.17 A typical result measured with pulse technique. (a) A screenshot of Vg and Vout acquired by the oscilloscope. Vg was supplied by pulse generator. (b) The extracted Transfer Curve (TC) with 5 μs pulse edge time under Vd = 25mV; both up and down edges can be used to obtain Id-Vg curve [41].

3.7.2 Ultra-Fast Pulsed (UFP) Technique

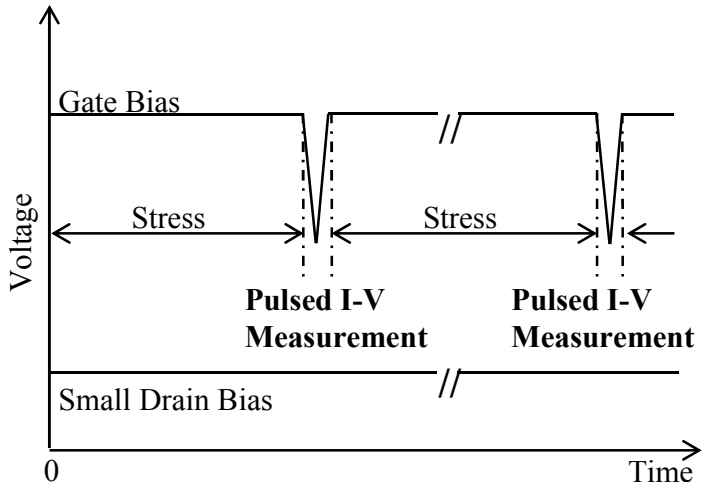

Fig. 3.18 Typical waveform of gate and drain terminals of Ultra-Fast Pulsed (UFP) Technique for NBTI characterization. Pulsed I-V was used to replace the conventional DC I-V measurement.

Ultra-Fast Pulsed (UFP) Technique [162] has been developed to suppress the fast recovery. Pulsed I-V measurement on the pulse edges was used to replace the conventional DC I-V measurement at pre-specified stress time. The methodology is the same as described in Section 3.6.1. Typical waveform is shown in Fig. 3.18.

3.7.3 Ultra-Fast On-The-Fly (OTF) Technique

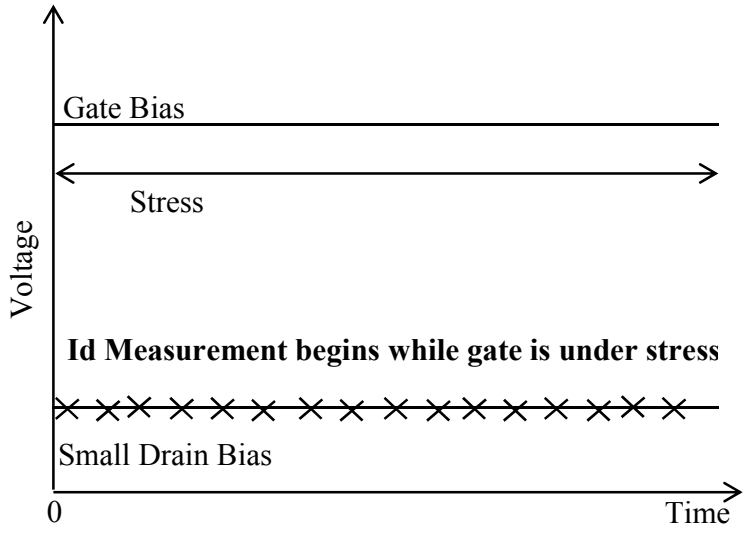

Fig. 3.19 The Id only OTF technique involves holding a small bias on the drain and sampling the drain current continuously, while the gate voltage is stressing the device.

The Ultra-Fast On-The-Fly (OTF) Technique was proposed , including variations such as Id Only OTF, OTF Single Point and OTF Vth Techniques [100, 162-164]. Fig. 3.19 shows the waveform used for OTF measurement. The obvious difference from the UFP Technique is that threshold voltage shift is evaluated under the same Vg as the stress condition, Vgst.

As shown in Fig. 3.20, different Vth extracted by UFP Technique, OTF and DC techniques have been well bridged by considering the recovery and the sensing Vg effect [22, 160].

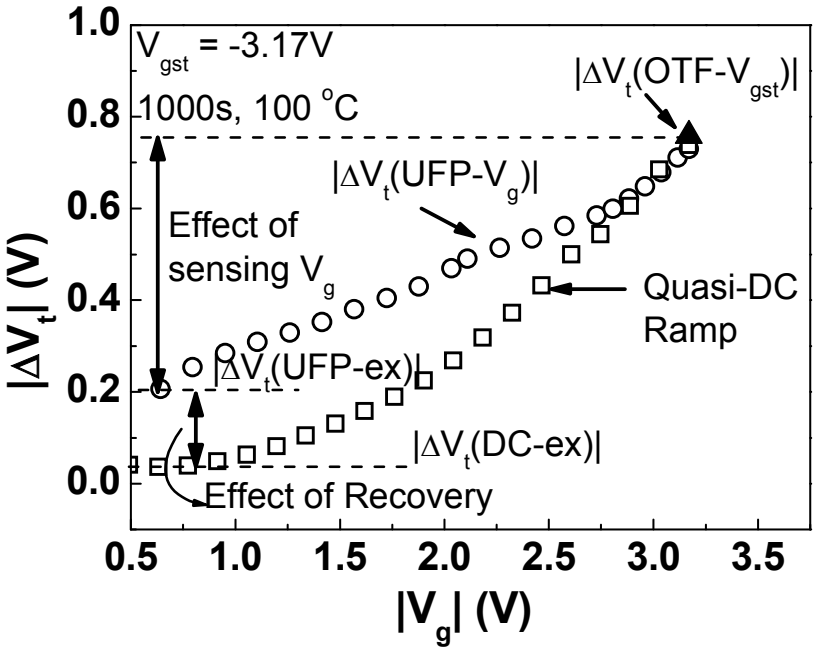

Fig. 3.20 Bridging the gap in ΔVt evaluated by different techniques. By taking both the recovery and sensing Vg effects into account, the new method successfully bridges the gap in OTF, UFP and DC Techniques.

3.7.4 Discharge-based Multi-Pulse (DMP) Technique

Discharge-based Multi-Pulse (DMP) Technique [165] was initially proposed to characterize the electron traps at various energy levels in Si nMOSFETs [166]. Only the electron traps with energy level higher than the silicon conduction band bottom can be discharged via tunneling [167], since there are few empty states in the silicon band gap.

Work has been done to adapt the DMP Technique to investigate hole traps in Si pMOSFETs [26]. Fig. 3.21 illustrates the principle of extracting the energy distribution of Positive Charges (PCs) in SiON/Si devices. As a first order approximation, following the early works [24, 25], we assumed that below the Fermi level, Ef, PCs throughout the thin oxide will be neutralized, if discharge time is sufficiently long. As Vdischarge increases towards positive for each discharging step, the energy level of PCs is lowered against the substrate, thus a shaded region is accommodated below Ef for discharging, as shown in Fig. 3.21.

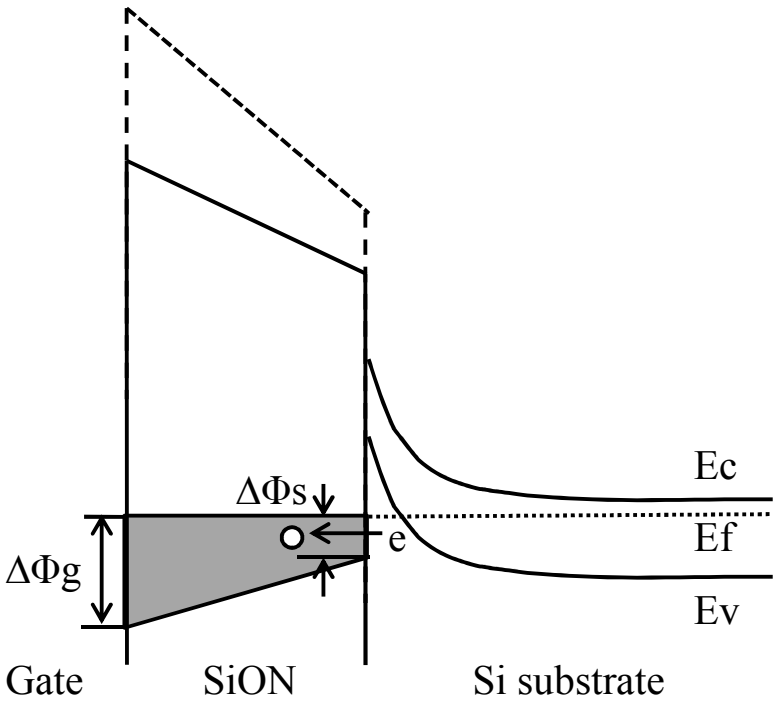

Fig. 3.21 An illustration of the principle for extracting the energy distribution of PCs in SiON/Si devices. When Vdischarge was stepped towards positive direction each time, a shaded area with an energy depth of ΔΦs at the interface falls below Ef and the PCs within it start discharging. By sweeping Vdischarge from the negative stress level to positive, Ef can be driven from below Ev to above Ec.

Ef can be swept over a wide energy range at the interface by varying Vdischarge over a sufficiently large range, including the region beyond bandgap at SiON/Si interface. Although PCs within SiON locates close to the substrate [124], it is worth to point out that they are not exactly at the Si/SiON interface and have a spatial distribution across the dielectric. As illustrated in Fig. 3.21, the vertical depth of the shaded area increases towards gate, $\Delta\Phi g > \Delta\Phi s$. For device and circuit simulation, it is of great use to know the change in PCs for a given $\Delta\Phi s$. Therefore, the energy level at the Si/SiON interface is used for their energy distribution, which is considered as an "effective" energy distribution in this sense.

3.8 Summary

In this chapter, experimental system and instruments for characterizing Ge pMOSFETs are presented and the principles are reviewed. Conventional techniques consist of the DC Id-Vg Technique, Charge Pumping (CP) Technique, Capacitance Voltage (C-V) Technique and Conductance Technique. Limitations of conventional techniques' application for Ge MOSFET are reviewed. Advanced techniques including the Pulse Id-Vg (Pulsed I-V) Technique, Ultra-Fast Pulsed (UFP) Technique, Ultra-Fast On-The-Fly (OTF) Technique and Discharge-based Multi-Pulse (DMP) Technique, and their advantages are discussed.

4 Initial NBTI Characterization and Defects Properties in Ge MOSFETs

4.1 Introduction

Two approaches have already been shown promising results for Ge MOSFETs. One is to use a few mono Si-cap layers [168]. It is compatible with existing Si processes with the same gate dielectric stack as that for Si. However, the interface states are relatively high, the Si-cap increases the separation between gate and channel, and Ge nMOSFETs is difficult to be made with good performance [168]. The other approach is depositing GeO_2/high-k stack directly on Ge substrate [169]. By suppressing the evaporation of GeO due to the interaction of GeO_2 with Ge, the interface states is reported as low as that for SiO_2/Si interface [169]. This approach can be potentially used for fabricating Ge nMOSFETs as well [169].

The fabrication process for Ge MOSFETs is becoming sufficiently mature and repeatable to guarantee to work on their reliability and encouraging results have been reported [170]. However, electron trapping is high [16], similar to high-k/SiON stack for Si developed in the early stage. The negative bias temperature instability (NBTI) is the most severe reliability issue for Si devices, since it results in a lifetime of pMOSFETs shorter than that of nMOSFETs [21, 22]. The NBTI of Si-cap/Ge MOSFETs has been

reported to be lower than its Si counterpart [30]. For the Ge pMOSFETs without a Si-cap layer, however, there is little investigation available on the NBTI.

4.2 Devices and Measurement Procedure

4.2.1 Device Process and Test Procedure

The gate dielectric stack used for the majority of tests in this chapter is shown in Fig. 4.1(a). The Ge layer is 700 nm and grown directly on Cz–Si wafers. To minimize interface states, a 1.2 nm GeO_2 was prepared by exposing clean Ge surface to an atomic oxygen flux at a low temperature of 150 °C for 20 min. A 4 nm Al_2O_3 was then produced by molecular beam deposition in the same chamber [171], resulting in a SiO_2 equivalent oxide thickness of 2.35 nm for the stack. Although Al_2O_3 has only a modest dielectric constant, it can suppress the evaporation of GeO and, in turn, the deterioration of GeO_2/Ge interface [65]. The device was annealed post-metallization in forming gas at 350 ºC for 20 mins.

The channel length used in this work is typically 1 μm and the width is 50 μm. The pMOSFETs have a 10 nm PVD TiN metal gate. For the purpose of comparison, other structures used include Ge/Si-cap/SiO_2/HfO_2, Si/SiON/High-k, and Si/SiON and their details are given in Table 4.1.

Table 4.1 Gate stack for Si and Ge Samples

(1) 2.3nm plasma-N **SiON/Si**
(2) 1.4nm plasma-N **SiON/Si**
(3) 2nm **HfO_2/SiON/Si**
(4) 0.5nm **AlO/** 1.2nm **HfO/** 0.4nm **SiON/Si**
(5) 4nm Al_2O_3/ 1.2nm **GeO_2/Ge**
(6) 4nmHfO_2/ 0.5nmSiO_2/**Si-cap/Ge**

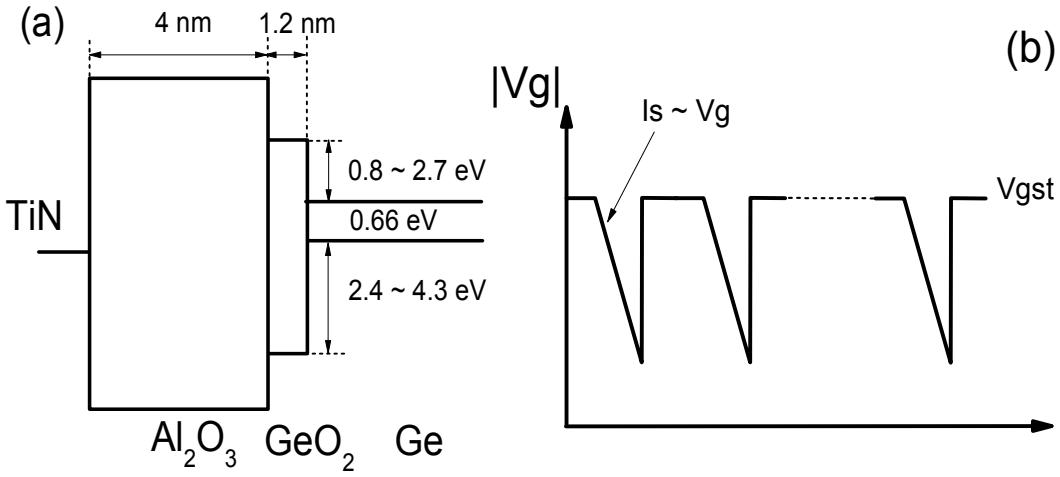

Fig. 4.1 (a) Schematic energy band diagram and structure of the used sample (b) The gate bias waveform used in tests. Vgst is the stress bias.

The test follows the standard 'stress-and-sense' procedure [125, 172] and a typical Vg waveform is given in Fig. 4.1(b). To monitor the threshold voltage shift, i.e. ΔVth, the stress was periodically interrupted and the source current, i.e. Is, instead of Id, versus Vg was recorded under a drain bias of Vd = -100 mV by using a Vg ramp to minimize the

impact of junction leakage. ΔVth was extracted from the Vg shift at a constant Is = 100 × W / L nA [173]. The temperature used is in the range of 20 ~ 125 °C and the stress and measurement were performed at the same temperature, unless otherwise specified.

4.2.2 Determination of Electric Field and Measurement Time (tm)

The electric field (Eox) over the interfacial GeO_2 layer was calculated from

$$Eox = (Vg - Vth) \times 3.9/(6 \times EOT) \quad (4.1)$$

where the EOT is the equivalent SiO_2 oxide thickness for the GeO_2/Al_2O_3 stack. Vg is the gate voltage and Vth is threshold voltage of fresh device.

Although SiO_2 was not present in the test structure, the equivalent SiO_2 thickness is used to follow the common practice and to make it easier for comparison with Si devices. The "3.9" and "6" in the formula above is used to take into account that GeO_2 and SiO_2 have a dielectric constant of 6 [174] and 3.9, respectively. The voltage drop across the semiconductor in inversion is taken into account by using Vg-Vth, which is an approximation widely used.

In order to check the accuracy of the Eox calculated from the equation (4.1), we also determined the Eox by using the 1D Poisson Simulator [175] and the CV method [176]. A reasonable agreement is obtained for these three methods. Comparison is shown in Fig. 4.2.

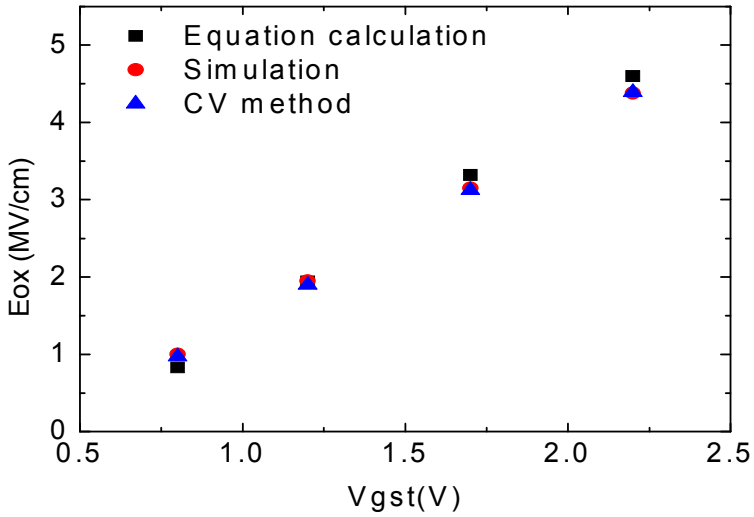

Fig. 4.2 Comparison of electric field calculated by equation, 1D simulation and CV methods. Good agreement is obtained.

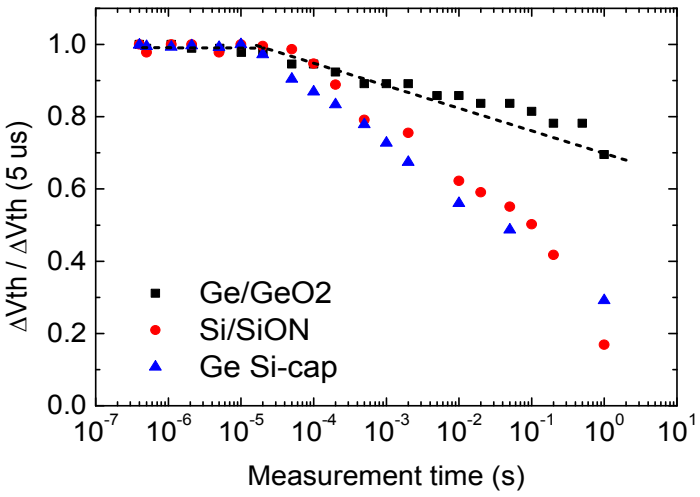

Fig. 4.3 Dependence of ΔVth on the measurement time for different samples. The stress field over the interfacial layer is 6.5 MV/cm for Ge/GeO_2 and 10 MV/cm for both Si/SiON and Si-capped Ge sample. The stress time is 1 ks and temperature is 20 ^{o}C. During the measurement period, Vg was kept negative and did not reach zero, as shown in Fig. 1(b).

The measurement time, tm, can be defined as the time for sweeping Vg from the stress level Vgst to the measurement Vg for Is = 100 × W / L nA (see the ramp in Fig. 4.1(b)). Reliable measurements were obtained only for tm > 0.4 μs and the recovery for shorter time could not be assessed. Fig. 4.3 shows that the recovery is negligible when tm increases from ~0.4 μs to ~10 μs and tm = 5 μs is used here to minimize recovery. The high temperature results show a similar behavior (not shown).When tm = 1 sec, recovery lowers ΔVth by 70~80% for Si/SiON and the Si-capped Ge sample, but only ~30% for Ge/GeO_2/Al_2O_3, so that ΔVth is relatively stable for the latter.

In this work, both tm = 5 μs [125, 160, 173, 174] and tm = 1 sec were used [94, 99, 177]. Although tm = 5 μs minimizes recovery, agreement has not been reached on the NBTI kinetics even for Si/SiON [96, 178, 179]. Under the conventional slow DC measurement of tm = 1 sec, however, it is widely accepted that ΔVth follows a power law and the Vg-accelerated lifetime prediction method is established [180] and some industrial researchers preferred tm = 1 s (e.g. [181]). It is of importance to find out whether this method is applicable for Ge/GeO_2/Al_2O_3.

4.3 Impact of Stress Electric Field on NBTI of GeO_2/Ge

4.3.1 Traditional Vg-accelerated Lifetime Prediction Method

The Vg-accelerated lifetime prediction method for Si/SiON requires the time exponent of ΔVth to be independent of the stress Vg [125, 180]. See Equation 2.8. When using this method, the stress bias, i.e. Vgst, typically does not change with time and tm is

~seconds. For example, it shows that |Eox| > 9MV/cm was used for Si MOSFETs [125, 182] in Fig. 4.4.

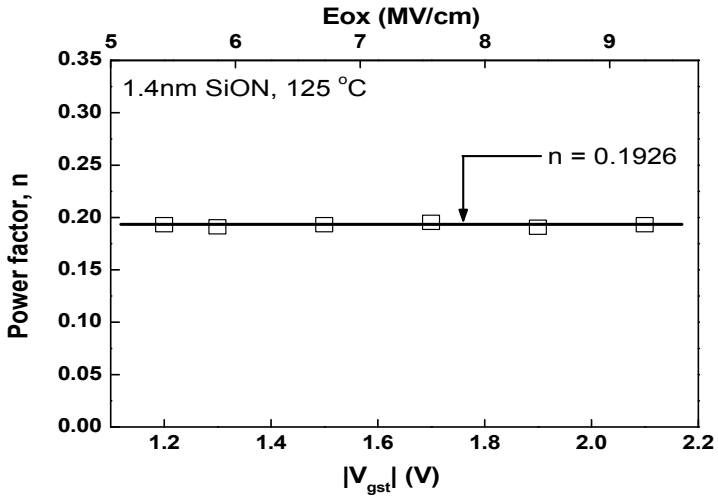

Fig. 4.4 Stress bias and Eox in the traditional Vg-acceleration for testing lifetime of Si MOSFETs [125].

4.3.2 NBTI under Different Stress Electric Field

We applied these test conditions first to the $Ge/GeO_2/Al_2O_3$ and Fig. 4.5(a) shows that ΔVth was substantial even under an operation bias level of -1.2 V (Eox=-2 MV/cm) and it is Vg-accelerated. The defect density in the current $Ge/GeO_2/Al_2O_3$ is clearly too high to meet the lifetime required for commercial application. It is of interest, however, to study their properties and dynamics, since the past experiences from high-k/SiON stack on Si show that the nature of the defects does not change when their density reduces substantially through process optimization [183, 184].

Fig. 4.5(a) appears similar to the conventional Si/SiON where ΔVth follows a power law against stress time [125]. log|ΔVth| versus log(time), however, is not a parallel shift

for different Vgst and the time exponent, n, reduces from 0.33 at Vgst = -0.8 V to 0.13 at Vgst = -2.2 V in Fig. 4.5(b), despite that the |Eox| ≤ 4.5 MV/cm used here is well within the range typically used for Si MOSFETs when observing a constant time exponent [125, 182].

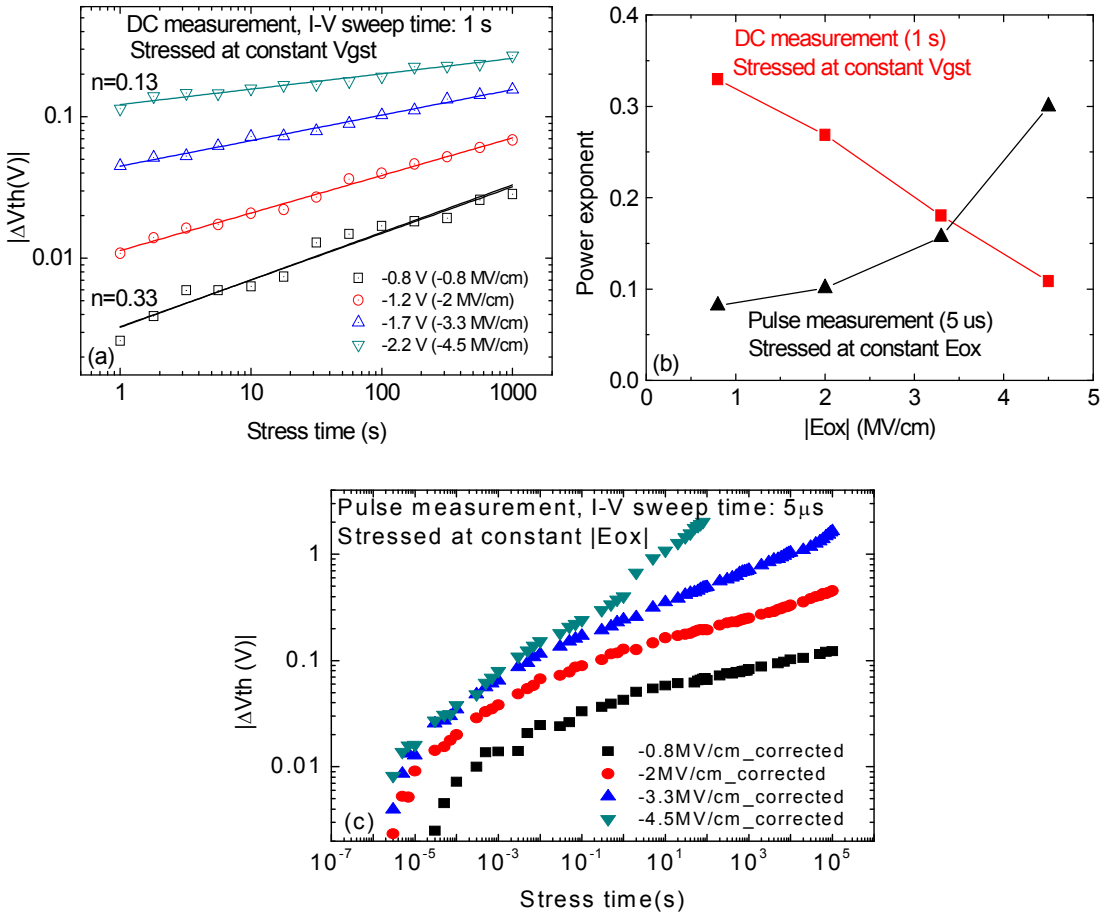

Fig. 4.5 (a) NBTI degradation kinetics under different stress biases at 20 °C measured by slow DC I-V of tm = 1 s. The solid lines were fitted with a power law. The stress Vg does not change with time and Eox in the legend is the field strength over GeO_2 at the start of stress. (b) The time exponent at different Vgst for DC and Eox for pulse measurement extracted within the time range of 1 s to 1000 s. (c) NBTI kinetics under constant stress Eox at 20 °C measured by pulse I-V of tm = 5μs. The stress |Vg| was increased with time to maintain a constant Eox here.

A possible explanation for the lower n at higher Vgst is that, when the stress was carried out under constant bias Vgst, the formation of positive charges lowers the |Eox| near the Ge/dielectric interface. At higher Vgst, there are more PCs, leading to a larger reduction in |Eox| near Ge, lowering |ΔVth| and in turn n. This PCs-induced |Eox| reduction can be corrected by increasing Vgst for a stress step i from the Vgst at the start of stress by ΔVth_{i-1}, so that the effective stress bias, (Vgst-Vth), and Eox are kept constant.

To suppress the recovery during measurement and the consequent underestimation of ΔVth, tm = 5 μs was used and Fig. 4.5(c) gives the result under constant stress Eox. The degradation does not follow a power law with a single exponent over the whole range of test time in Fig. 4.5(c), although data between 1 and 1000 sec can be fitted with a power law. The time exponent extracted between 1 and 1000 sec is given in Fig. 4.5(b), which increases for higher |Eox|. As a result, suppressing recovery during measurements and stressing under constant Eox do not lead to a constant time exponent and the conventional lifetime prediction method cannot be used for the $Ge/GeO_2/Al_2O_3$ used here.

4.4 Effects of Stress Temperature and Anneal

4.4.1 Effect of Stress Temperature

Fig. 4.6(a) shows the ΔVth under |Vgst-Vth0| = 0.75 V for different stress temperatures with tm = 1 s. As expected, the NBTI is thermally activated. Under a higher |Vgst-Vth0| = 2.35 V, however, Fig. 4.6(b) shows that ΔVth tends to become insensitive to

temperature as it rises. This leads to a reduction of the activation energy, Ea, for higher Vgst, as shown in Figs. 4.6(c) and (d).

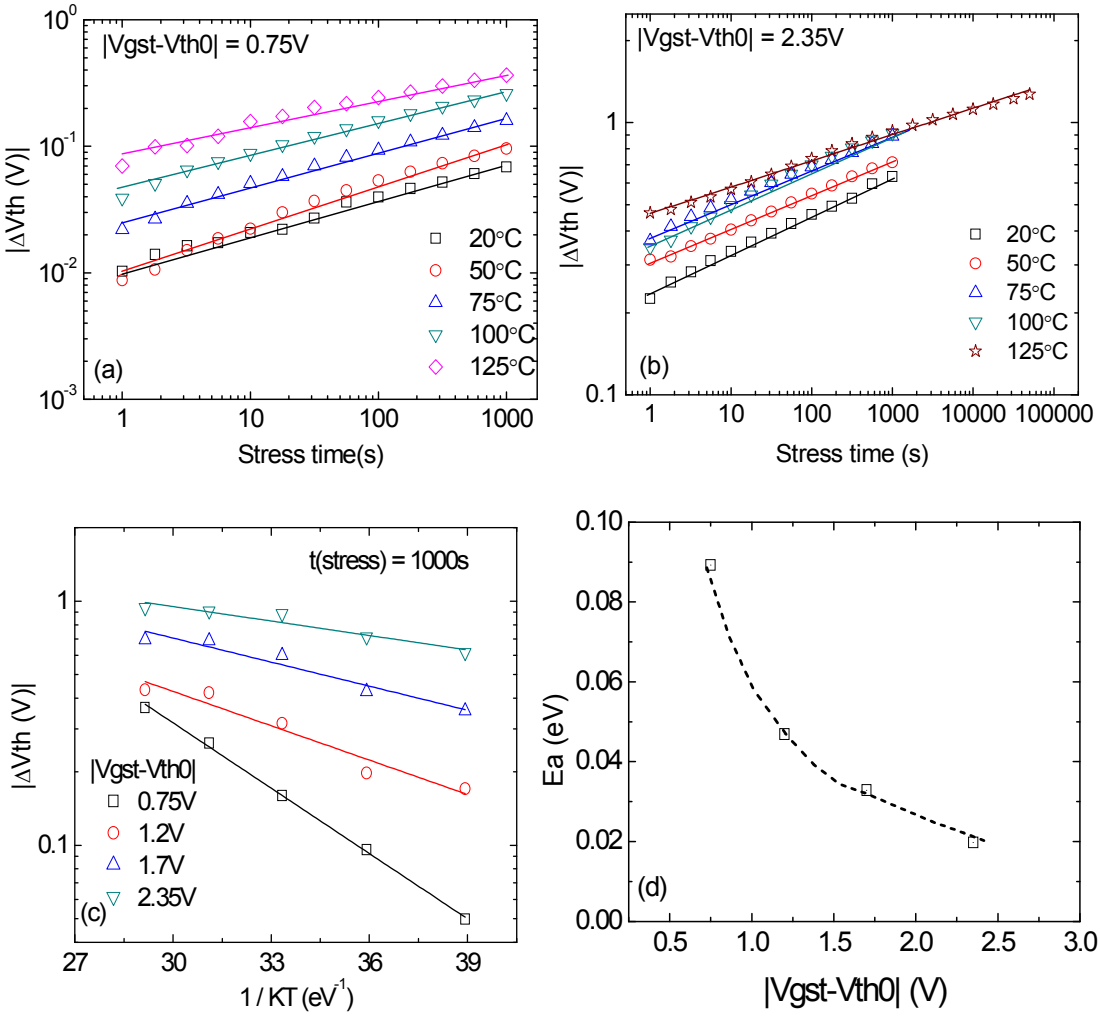

Fig. 4.6 NBTI kinetics under different stress temperatures, tm = 1 s, and |Vgst-Vth0| = 0.75 V (a) and 2.35V (b). (c) is the Arrhenius plot at 1000 sec. (d) gives the extracted apparent activation energy from (c) at different |Vgst-Vth0|.

Ea was extracted from the Arrhenius plot at 1000 sec in Fig. 4.6(c). It is an apparent activation energy with the measurement made at the stress temperature [185]. The

insensitivity of ΔVth to temperature over 75 ºC at |Vgst-Vth0| = 2.35 V in Fig. 4.6(b) is not caused by running out of defects, since the longer stress clearly shows that the degradation can be higher.

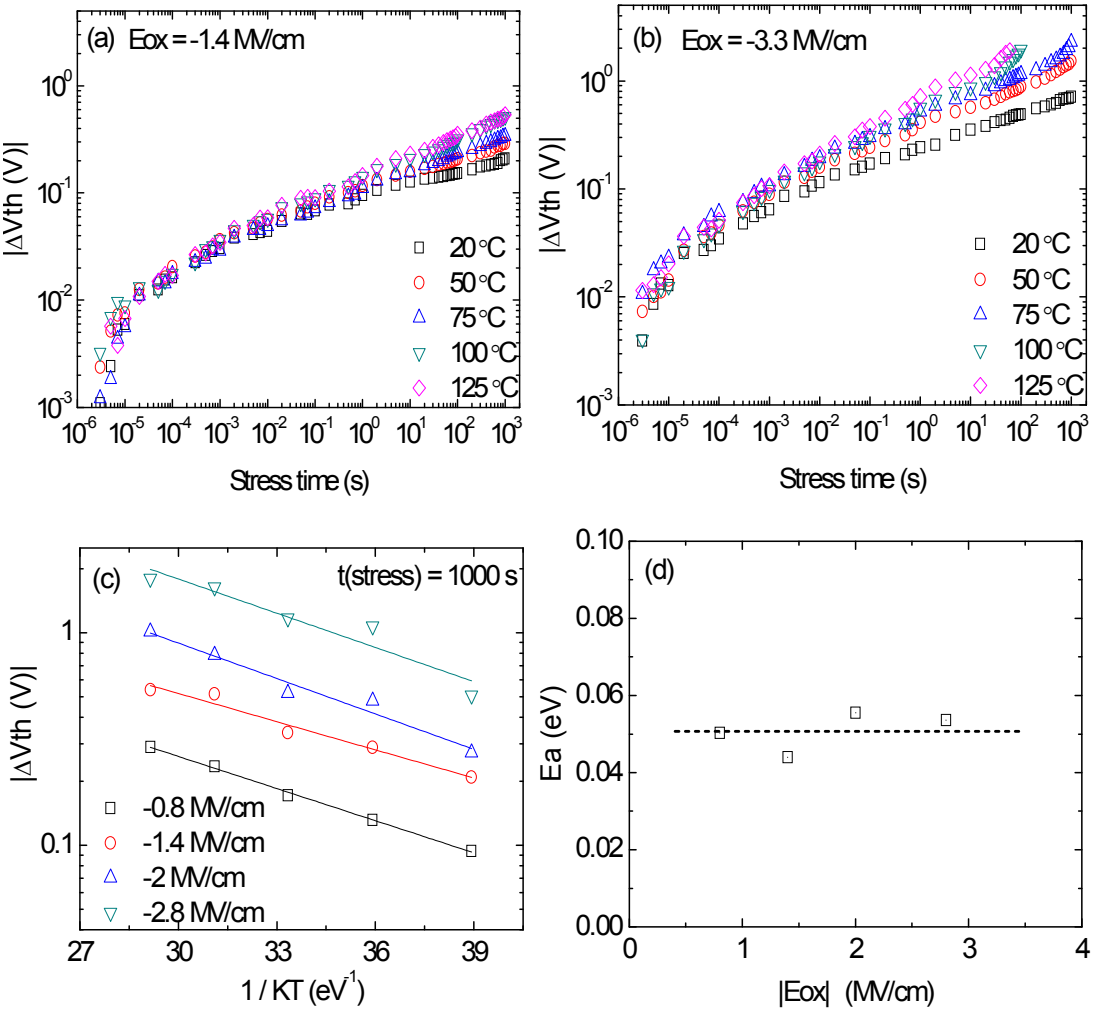

Fig. 4.7 NBTI kinetics under different stress temperatures with tm = 5 μs. The Eox during stress was kept at a constant of -1.4 MV/cm (a) and -3.3 MV/cm (b). (c) is the Arrhenius plot at 1000 sec. (d) gives the extracted apparent activation energy from (c) at different Eox.

The temperature-insensitivity of ΔVth at a stress time of 1000 sec has not been observed for Si/SiO_2 [112] and Si/SiON/High-k [186] and is worth of further exploring. One possibility is that the recovery during the 1 s measurement delay is also a thermally activated process, compensating the degradation. Figs. 4.7(a)-(d) give the results measured with tm = 5 μs that minimized the recovery. The ΔVth appears insensitive to temperature initially (e.g. < 1 ms) and the reason will be discussed in Chapter 6. For longer stress time, however, it is clearly thermally enhanced and the apparent Ea taken at 1000 sec is insensitive to Eox in Fig. 4.7(d).

4.4.2 Effect of Anneal

To study the anneal of PCs, a device was exposed to 150 °C after stressing at 20 °C. Fig. 4.8(a) shows that nearly all PCs can be neutralized in 1,800 sec. In comparison, the neutralization is less than half for Si/SiON under similar anneal conditions [187]. The following speculation is made to explain this difference.

It has been reported that the positive charges in SiO_2 can have energy levels above the bottom edge of the Si conduction band, i.e. Ec, making them difficult to reach by free electrons from Si substrate [17, 94, 99, 177]. The Ec offset between SiO_2 and Si is around 3.2 eV, so that these traps can be located well above the Si Ec. The Ec offset between GeO_2 and Ge, however, has been reported to be as low as 0.8 eV [188], so that the positive charge in GeO_2 should be closer to Ge Ec, making them relatively easier to neutralize at elevated temperature.

It is worth pointing out that the PCs in SiO_2 can only be fully neutralized when the anneal temperature reached 400 ºC [187-189]. After the anneal, the ΔVth in the subsequent stress becomes smaller than that before anneal, because of defect losses and slowdown in SiON [187-189]. To test if this is also the case for $Ge/GeO_2/Al_2O_3$, the device was re-stressed after anneal and Fig. 4.8(b) clearly shows that ΔVth has not been reduced for the re-stress, so that the defect losses and slowdown were not observed here.

The full anneal at 150 ^oC in Fig. 4.8 was observed after stress under Vgst=-2.8 V, which is much higher than the operation bias, say Vg=-1.2 V. To test whether the full anneal can also be achieved after stress under use bias, the anneal was performed also after stress under Vgst=-1.2 V. Fig. 4.9 confirms that the full anneal was also achieved.

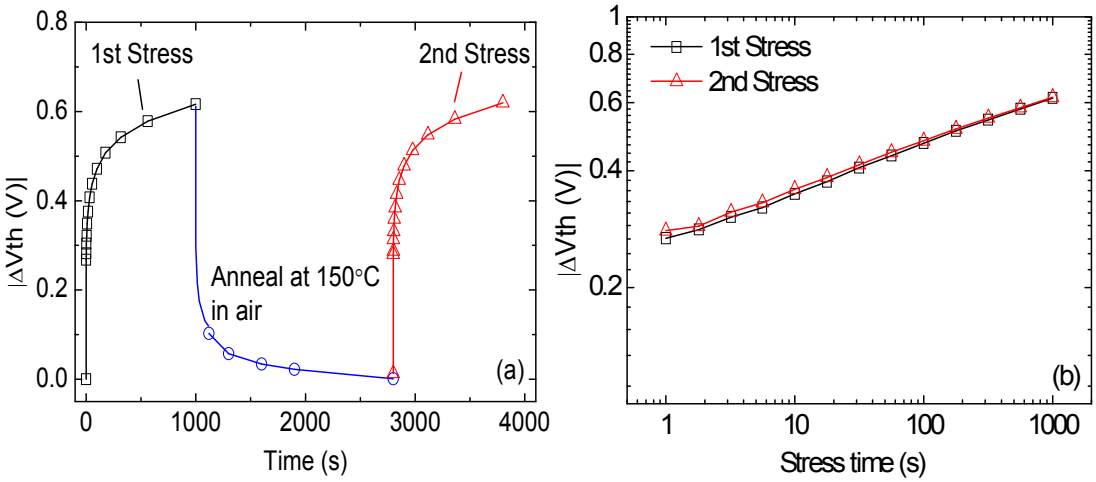

Fig. 4.8 (a) The 1st stress was under Vg = -2.8 V, 20 ^oC for 1000 s. The device was then annealed for 20 min at 150 °C in air with all terminals floating. The 2nd stress was under the same conditions as the 1st one. (b) compares the ΔVth for these two stresses by resetting the stress time to zero at the start of the 2nd stress. Tm = 1s.

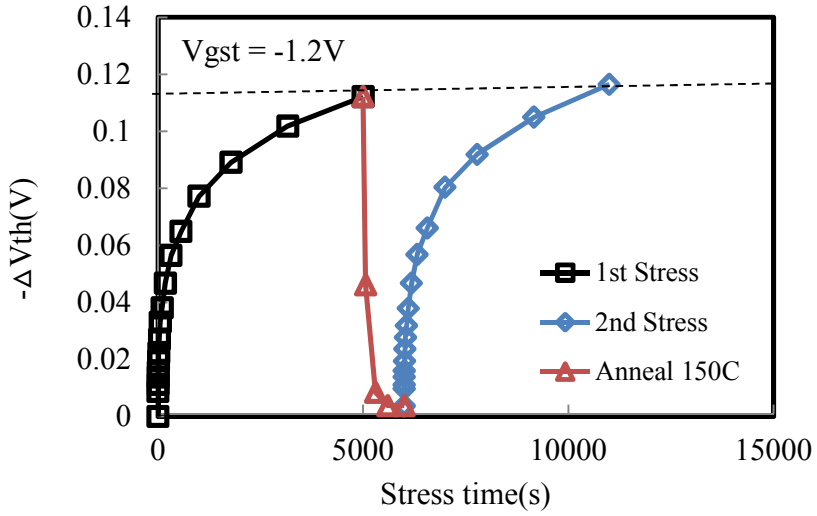

Fig. 4.9 After stress at Vgst = -1.2 V, degradation can be fully recovered by annealing at 150 °C.

4.5 Contribution of Interface States Generation

The positive charges responsible for NBTI can originate from both the bulk of gate oxide and the oxide/substrate interface [22, 112, 183, 190]. When NBTI was reported for thick SiO_2 (e.g. 95 nm) in early years, the stress Eox was relatively low and it was observed that PCs from the oxide and the interface were equally important [112]. For thin (< 3 nm) oxides, however, the stress Eox used is typically higher (e.g. 10 MV/cm) and hole injection occurs [22, 125]. The charging of hole traps leads to a larger contribution of PCs from oxides to ΔVth than that from generated interface states [22, 160, 191]. Nitridation introduces additional hole traps, further enhancing the contribution of PC from oxides to ΔVth [26, 192]. We now assess the relative importance of PCs from interface states for Ge pMOSFETs of a GeO_2/Al_2O_3 stack.

4.5.1 Charge Pumping Measurement

Fixed amplitude charge pumping is a widely-used method for characterizing the interface states [138, 153]. The fixed voltage base level charge pumping, on the other hand, can suffer from the interference from the trapping/detrapping of traps in the gate dielectric bulk as the pulse amplitude increases [138]. To demonstrate this, we carried out the fixed base voltage CP on the Ge samples and a Si sample with high level traps in dielectric bulk. The results are shown in Fig. 4.10. There is no clear saturation for both samples, because of the contribution from the charge trapping/detrapping in the dielectric to the charge pumping current. To confirm that the non-saturation of Icp for the fixed base voltage CP is not caused by gate leakage current, the leakage current also was measured and it is insignificant in both devices. Fixed amplitude CP is preferred in this work, therefore.

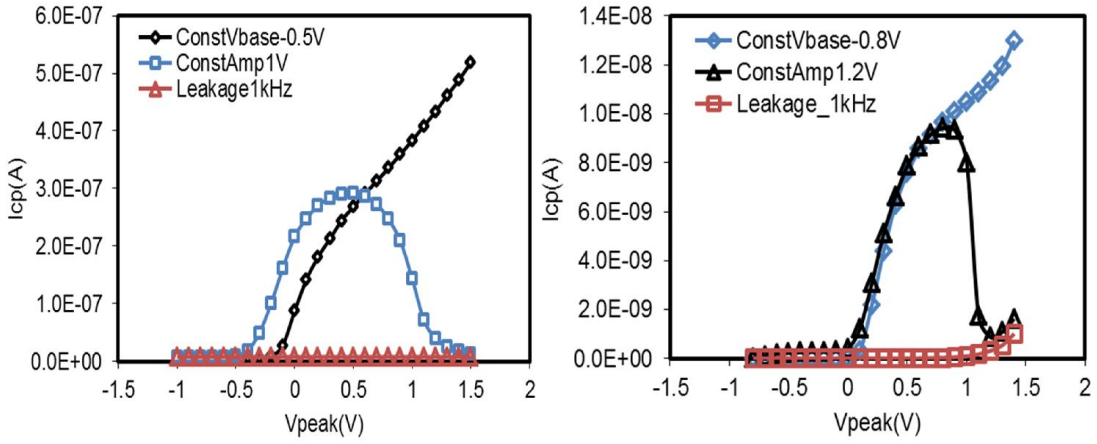

Fig. 4.10 Non-saturation Icp measured by using fixed base voltage CP for both (a) GeO_2/Ge pMOSFET (b) Si pMOSFET. The frequency is 1MHz. The fall/rise time is 20ns.

4.5.2 Estimation of Interface States Generation

Fig. 4.11(a) presents a typical result of charge pumping measurements before and after a stress. The generation of interface states clearly can be seen from the raised peak after stress, resulting in an increase of interface state density of $\Delta Dit = 1.88 \times 10^{11}$ $cm^{-2}eV^{-1}$. As a first order estimation of the contribution from ΔDit to ΔVth, we assume a uniform energy distribution of interface states. It has been reported that the charge neutrality level is in the lower half of the band gap for Ge [127], but, for simplicity, we assume that all states between the midgap and Ev are donor-like and contribute to positive charges. This gives rise to a positive charge of $\Delta Nit = 0.33 \times \Delta Dit = 6.20 \times 10^{10}$ cm^{-2} and a corresponding threshold voltage shift of $\Delta Vit = \Delta Nit \times q / Cox$ [193]. Fig. 4.11(b) compares the ΔVit with the measured ΔVth, showing that ΔVit is one order of magnitude smaller. The ΔDit measured by CP is the average value over an energy range of ± 0.22 eV centered at midgap in our case [194]. It has been reported that the interface state density rises substantially towards the band edge, so that an assumption of uniform energy distribution can underestimate the contribution of ΔDit.

As a second order approximation, we use the energy profile reported in earlier work [174] for Dit. As shown in Fig. 4.11(c), the solid curve was fitted with the test data by using an expression, $Dit = A \times \exp[-(E-Ev) / Eo] + C$, where A, Eo and C are constants. This function was then normalized to the measured ΔDit over the energy range from midgap to 0.22 eV below it, resulting in the dotted line in Fig. 4.11(c). The positive charges were estimated by integrating the dotted line between midgap and Ev, resulting in $\Delta Nit = 7.89 \times 10^{10}$ cm^{-2}. The corresponding ΔVit is also shown in Fig. 4.11(b) and its

contribution remains insignificant. Moreover, even if we use the highest Icp value measured by the fixed base voltage CP for evaluating Nit, it is still substantially less than the defect density for the total ΔVth. We conclude that the NBTI of $Ge/GeO_2/Al_2O_3$ is dominated by positive charges in the dielectric. The parameters used for the Nit calculation [43, 153, 195] are: thermal drift velocity (6×10^6 cm/s), capture cross-section (5×10^{-17} cm^{-2}) and intrinsic carrier density (2.4×10^{13} cm^{-3}).

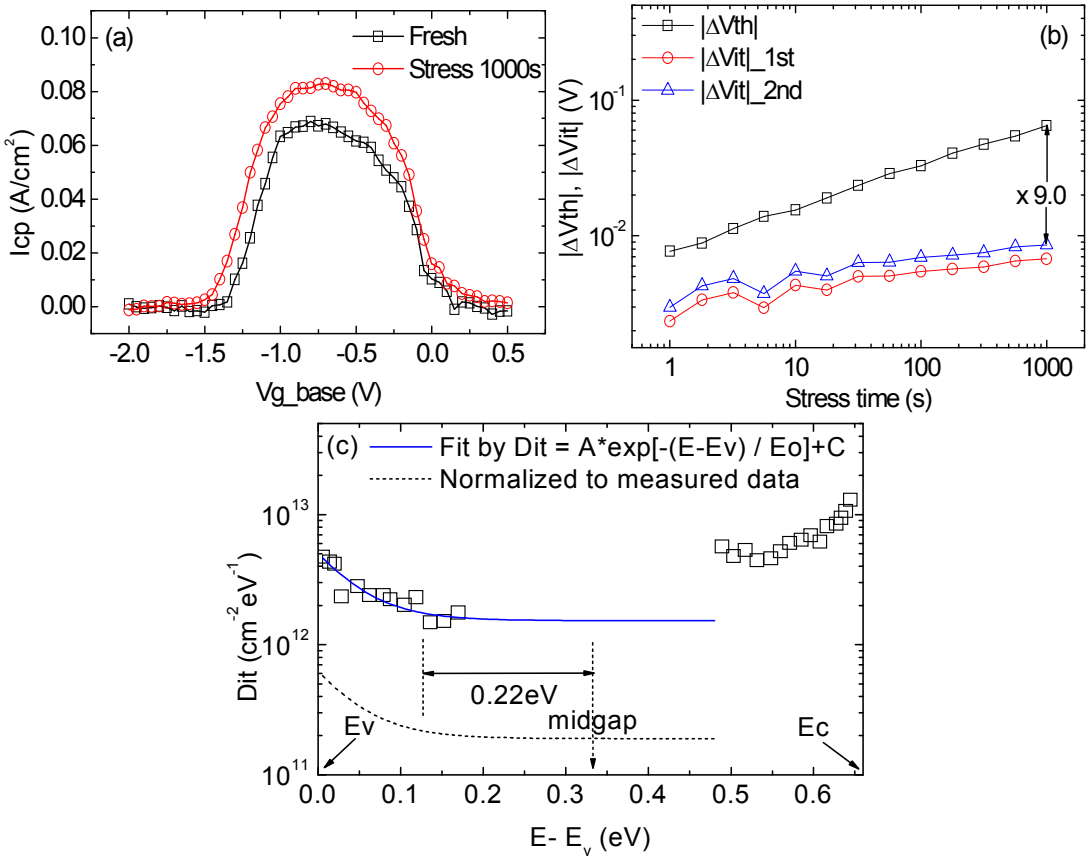

Fig. 4.11 (a) The charge pumping current, Icp, before and after a stress under Vgst = -1.2V at 20 ºC. (b) A comparison of the 1st and 2nd order estimated contribution of generated interface states to the threshold voltage shift with the measured ΔVth. (c) The energy distribution reported in ref. [174]. The dashed line is obtained by normalizing the solid line to the measured 1.88×10^{11} $cm^{-2}eV^{-1}$ in the range of 0.22 eV from midgap. The charge pumping amplitude is 1V, frequency is 1 MHz and the rise and fall time are 20 ns.

4.5.2 Confirmation by Id-Vg Measurement

To confirm that the interface states beyond the energy range probed by charge pumping are insignificant, the source current was plotted in logarithmic scale. If interface state generation were significant, the I-V shift should be non-parallel, especially in the subthreshold region. Fig. 4.12, however, shows that the shift is in parallel, supporting that the degradation is dominated by the positive charge in dielectric for Ge MOSFETs.

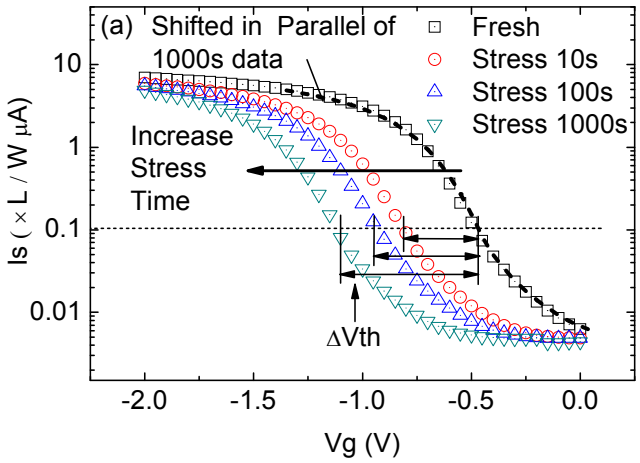

Fig. 4.12 The parallel shift in the sub-threshold region of Id-Vg curve. The black dashed curve is a parallel shift of the 1000 sec data.

4.6 Positive charges in dielectric: energy switching model

It has been shown in Section 4.3 and 4.4 that NBTI in the Ge sample behaves differently from that in Si samples. In this section, the cause for these differences will be investigated at the defect level.

4.6.1 Properties of Positive charges (PC)

For Si pMOSFETs, the positive charges (PC) in gate oxides have a complex behavior and have been explained differently by different groups [117, 125, 160, 179, 194, 196, 197].

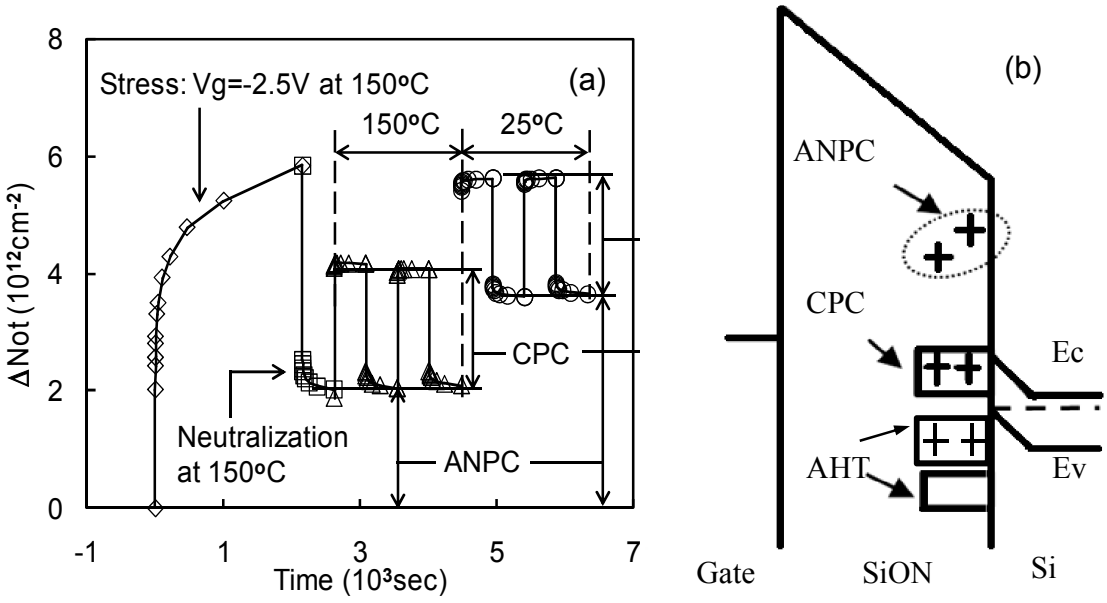

Fig. 4.13 (a) Different types of PCs in Si/SiON/HfO_2. After stress and neutralization, Eox = ± 5MV/cm were applied with alternating polarity to show the traps ~Ec and above Ec at 150 ºC and then 25 ºC [189]. Vg>0 V reduces ΔNot and Vg<0 V increases PCs. (b) illustrates the energy level differences for the three types of PCs. ΔNot was measured from the Id-Vg shift at midgap, where interface states are neutral for Si MOSFETs.

Fig. 4.13(a) and (b) summarize their typical behavior and one way of characterizing them is to separate them into three groups according to their energy ranges: As-grown hole traps (AHTs) below the Si Ev, Cyclic positive charges (CPCs) around Si Ec, and Anti-neutralization positive charges (ANPC) above Si Ec [17, 22, 94, 99, 177, 186].

After building up PCs during stress at high |Eox|, substantial neutralization occurs under Vg > 0 at a relatively low Eox = 5 MV/cm. By alternating the polarity of Eox = ± 5 MV/cm, the CPC around Si Ec can be repeatedly charged and neutralized, and the ANPC well above Ec remain charged and are not neutralized. Most AHTs below Si Ev cannot be re-charged under Eox = - 5 MV/cm. In the following, we will show that PCs in GeO_2/Al_2O_3 on Ge are different.

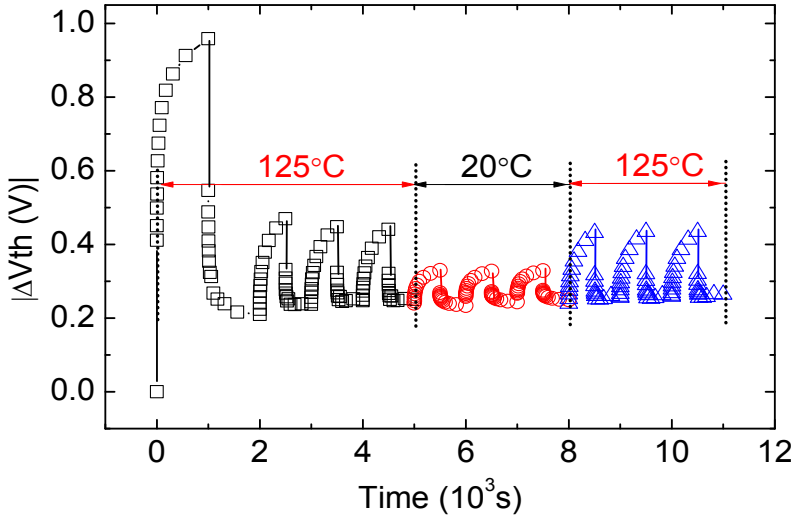

Fig. 4.14 Positive charges in $Ge/GeO_2/Al_2O_3$ device. The stress was at Vgst = -2.6 V and 125 °C. After a neutralization step at +4.2 MV/cm at 125 °C, Eox = ± 3.3 MV/cm were applied with alternating gate polarity in a temperature sequence of 125 °C, 20 °C and 125 °C. The time for switching temperature is 40mins with gate floating and this time was not included in the time axis.

Fig. 4.14 shows a typical result for GeO_2/Al_2O_3 on Ge. Although the first impression is that the PCs behave similarly to those in Si samples, a close inspection, however, reveals several important differences:

- The charge and neutralization of CPCs around Ec by alternating Vg polarity for Si samples in Fig. 4.13(a) is insensitive to measurement temperature, i.e. T, since it has an energy level accessible even at room temperature and the charge and neutralization are through carrier tunneling here that is a process insensitive to T. In contrast, Fig. 4.14 shows that the charge/neutralization cycling in Ge sample reduces for lower T.
- The density of ANPC above Ec in Si samples in Fig. 4.13(a) clearly increases at lower T. After being neutralized at a higher T, the defect energy level remains above Ec. As soon as T is reduced, electrons leave the defects, tunnel into the Si conduction band, recharge the defects, and result in the higher PCs. For the Ge sample, however, Fig. 4.14 shows that the remaining PCs hardly increase when the temperature lowers from 125 °C to 20 °C.

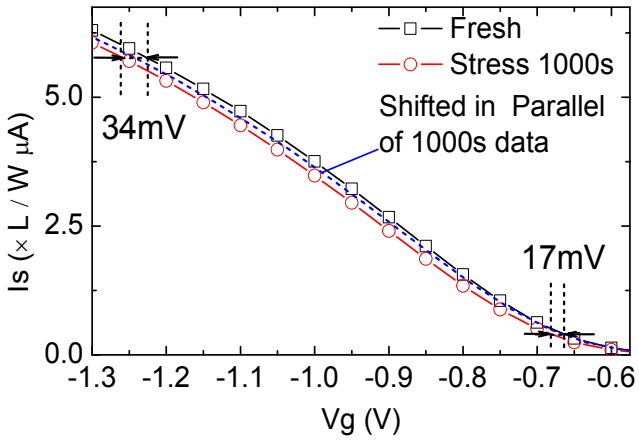

Fig. 4.15 Is - Vg before and after stress under Eox = -6.5 MV/cm for 1000 s on a Si/SiON/HfO/AlO device. The dotted line is a parallel shift of the line for 1000 sec data until it reached the fresh Is - Vg at low |Vg|. It shows the stressed Is - Vg is not in parallel with the fresh Is - Vg.

- When Vg sweeps from the stress level in the positive direction to a sensing Vg, some traps in Si samples fall below the Fermi level and are neutralized [22, 125, 160]. Fig. 4.15 shows that |ΔVth| nearly halved when Vg moves from -1.2 V to -0.6V. In contrast, Fig. 4.12 shows parallel shift of I-V curve for Ge sample, as the change of ΔVth with Vg is much smaller for Ge samples (Fig. 4.16), indicating detrapping from traps below Ev for Ge is less important than that in Si.

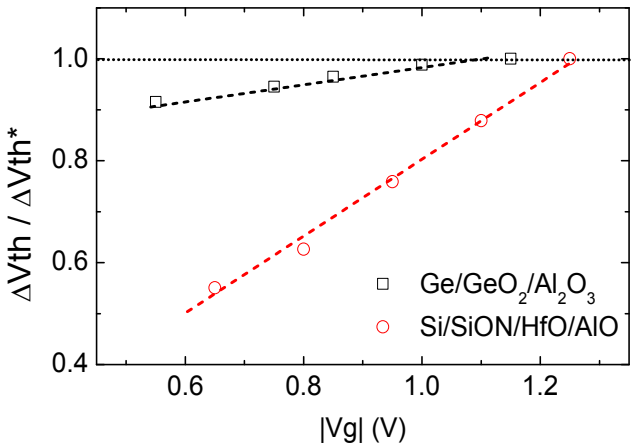

Fig. 4.16 Dependence of ΔVth on the sensing Vg. ΔVth* is the ΔVth measured at the highest sensing |Vg| for a sample. Devices were stressed under an initial Eox = -6.5 MV/cm for 1000 s at 20 °C.

4.6.2 Energy Alternating Model

The above differences indicate that the PCs in Ge samples are different from those in Si samples, so that a different model is needed. We propose an 'energy alternating model' to explain these differences. A defect in gate dielectric has different energy levels, according to its charge-status [198]. The 'energy alternating' means that the energy level of a defect switches from one value to another, when its charge-status changes. As illustrated in Fig. 4.17(a), neutral hole traps have a spread of energy levels below Ev of

Ge. Application of higher |Eox| allows charging the traps further below Ev, leading to the field activation of NBTI in Fig. 4.5(a). Application of higher temperature also charges the hole traps further below Ev, resulting in the higher ΔVth at higher temperatures in Fig. 4.6 and Fig. 4. 7.

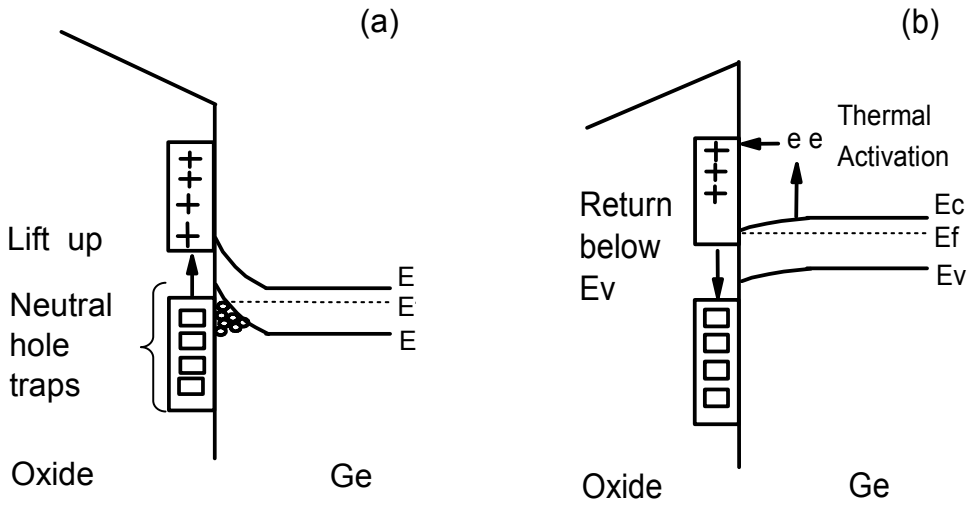

Fig. 4.17 The energy-switching model for positive charges in $Ge/GeO_2/Al_2O_3$. (a) shows charging under Vg < 0, (b) shows neutralization under Vg > 0. '□' represents neutral hole traps and '+' represents charged hole traps.

After being charged, instead of staying at the same energy level, the defects are lifted to energy levels well above Ge Ev. This allows most hole traps holding their PCs when Vg is swept from stress toward threshold levels, giving rise to the smaller reduction in Fig. 4.16, when compared with that in Si/SiON.

If the energy levels of the lifted PCs were near Ec, their neutralization should be insensitive to temperature, similar to those in Si samples in Fig. 4.13. Fig. 4.14 shows

that this is not the case for Ge samples, however. On the other hand, if the lifted PCs are above Ec, their neutralization should be thermally enhanced, as illustrated by Fig. 4.17(b), similar to the PC above Si Ec in Fig. 4.13(b) [17, 94, 99, 177]. This is confirmed below.

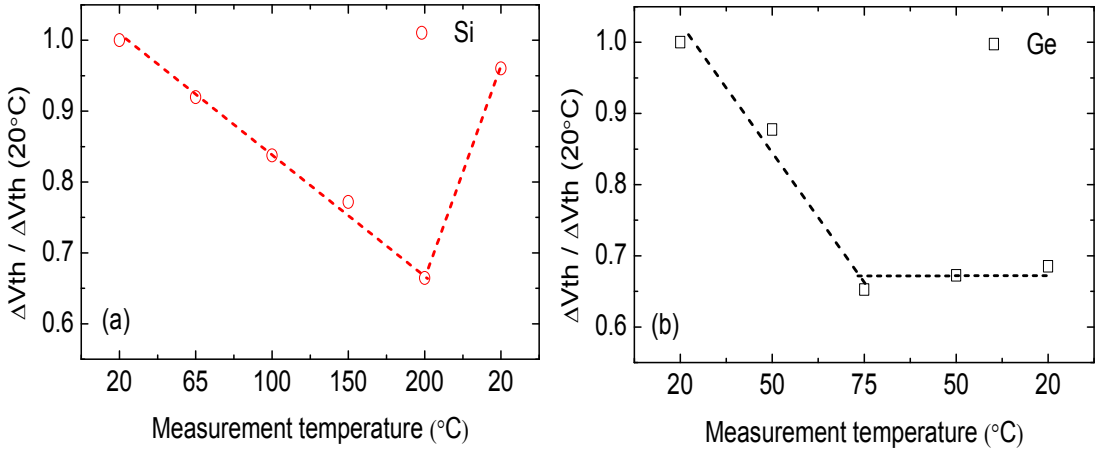

Fig. 4.18 Impact of measurement temperature on ΔVth for (a) Si/SiON and (b) Ge/GeO_2/Al_2O_3. The lines are a guide for the eye. tm = 1s.

Fig. 4.18 shows that an increase of T clearly lowers ΔVth for both Si (Fig. 4.18(a)) and Ge (Fig. 4.18(b)) samples. The thermal activation of neutralization supports the proposition that there are PCs above the Ge Ec. However, when T reduces subsequently, ΔVth rises back for Si, but remains the same for Ge samples. This supports the view that, unlike the case of Si samples, the energy level of defects drops back below Ev after neutralization at high T to prevent recharge at the subsequent low T for Ge sample without re-stress, as illustrated in Fig. 4.17(b). Because the energy level was switched back below Ev after neutralization at 125 ºC, lowering temperature to 20 ºC did not recharge them, unlike the Si sample in Fig. 4.18.

For Ge sample at a time t*, a signature of the energy-alternate after neutralization is that the number of un-neutralized PC is determined by the highest temperature a sample was exposed prior to t*, rather than the temperature at t*. In contrast, for Si sample, the lack of energy level alternating means that the number of un-neutralized PC at t* is determined by the temperature at t*. In other words, one may say that $Ge/GeO_2/Al_2O_3$ can remember its temperature history, but Si/SiON cannot. The underlying physical mechanism for the energy alternating is not known. One speculation is the field-assisted multi-phonon emission during hole trapping [117]. To better prove the existence of energy alternating defects, further experimental evidence for the energy alternating model will be given in Chapter 5 with a detailed investigation on defect energy distributions.

4.7 Summary

This chapter characterizes the NBTI for $Ge/GeO_2/Al_2O_3$ and compares it with Si samples. Similar to Si samples, NBTI is activated both electrically and thermally for $Ge/GeO_2/Al_2O_3$. There are a number of important differences from Si samples and the new findings include: (i) The time exponent is not constant for different stress biases/fields when measured with either slow DC or pulse technique, which makes the conventional Vg acceleration lifetime prediction technique of Si samples inapplicable to the $Ge/GeO_2/Al_2O_3$; (ii) ΔVth is substantially less sensitive to measurement time; (iii) The neutralization can be nearly 100% under a temperature as low as 150 °C, in contrast with the 400 °C needed by Si sample. (iv) Defect losses were not observed for

$Ge/GeO_2/Al_2O_3$. On defects, the positive charges in GeO_2/Al_2O_3 on Ge dominate the NBTI. They do not follow the same model as that for PCs in SiON/Si and an energy-alternating model has been proposed: the energy levels have a spread for neutral hole traps below Ev, lift up after charging, and return below Ev following neutralization.

5 Hole Trap Energy Distribution by Discharge-based Multi-pulse (DMP) Technique

5.1 Introduction

Promising performance has been demonstrated, with an Al_2O_3/GeO_2 gate stack [7, 8]. After achieving good initial performance, attention should be paid to its reliability. The lifetime of Si pMOSFETs is limited by negative bias temperature instability (NBTI) [17, 192, 199] and the Ge pMOSFET with Al_2O_3/GeO_2 also suffers from substantial NBTI, as presented in Chapter 4. NBTI has two sources: generated interface states and positive charges (PCs) formed in the gate dielectric by hole trapping [199-201].

The PCs in Si MOSFETs have a complex behavior and caused much confusion since 1970s [96, 178, 184, 202, 203]. Three different types of PCs: as-grown hole traps (AHT), cyclic positive charges (CPC), and anti-neutralization positive charges (ANPC) [17, 94, 99, 100] were identified, as discussed in Section 2.4.1. Efforts were made to extract the energy distribution of PCs [24, 25], but they were based on the slow quasi-DC measurement, hence did not capture the defects that discharged rapidly. Moreover, they only provide distribution within the bandgap. As a result, two types of PCs, AHT and ANPC, were not covered by these early works [24, 25]. DMP technique has been

developed recently to evaluate the different types of PCs in Si device[26], which confirmed the framework.

Attempts have also been made to characterize the interface traps [27] and border traps [28] in high mobility channel devices. AC transconductance (AC-gm) method and TSCIS (Trap Spectroscopy by Charge Injection and Sensing) technique were combined to map the energy distribution of PBTI induced electron traps in $In_{0.65}Ga_{0.35}As/Al_2O_3$ and Ge nMOSFETs. However, there is little information on the PCs induced by NBTI in $Al_2O_3/GeO_2/Ge$ pMOSFETs. To assist understanding and further minimization, it is desirable to know their energy distribution, which also provides the PC density at a given surface potential needed for simulating the NBTI impact on devices and circuits in the future.

5.2 Principle of Discharge-based-Pulse (DMP) Technique

The DMP technique can probe the energy distribution of PCs in Si device [26] and it is adapted in this section to obtain the detailed information of hole traps for Ge pMOSFETs.

5.2.1 DMP Technique for Probing Hole Traps

The principle of the DMP probing technique is illustrated in Fig. 5.1. When discharge voltage was stepped towards positive, the PCs in the shaded area dropped below Ef and discharged. By varying gate voltage over a large range, Ef can be swept from below Ev

to above Ec at the interface. They were measured from the change in threshold voltage. It should be pointed out that the quantization effect leads to a deviation of ground state energy levels from the Ec and Ev at the interface in Fig. 5.1. The 'Ec' and 'Ev' were used here to represent band bending, following common practice [28, 204], which will be discussed further in section 5.5.

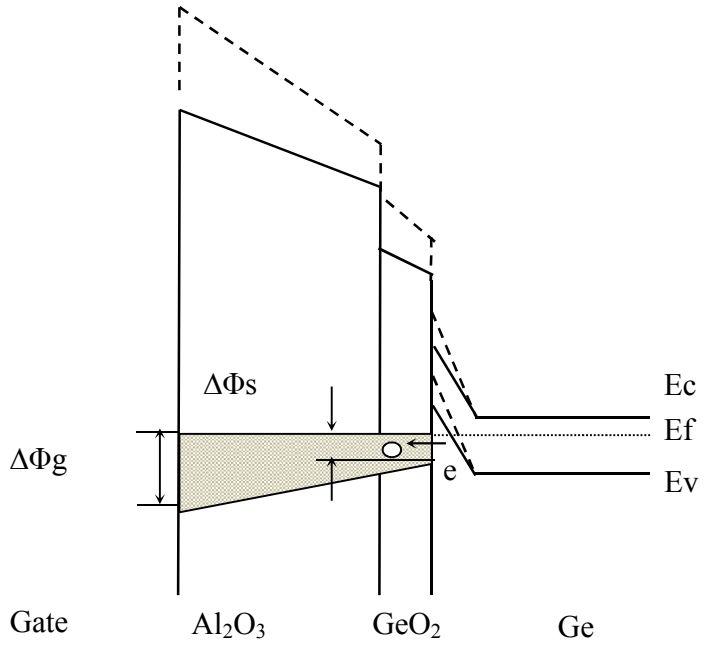

Fig. 5.1 A schematic energy diagram before (dashed lines) and after (Solid lines) Vdischarge stepping towards positive. After the stepping, the PCs in the shaped region is below Ef and will be discharged.

5.2.2 Charge Polarity of Hole Traps

The basic premise used here is that a hole trap is neutral if it is below the Ef at the interface, but positive if it is above the Ef, as illustrated by the energy band diagram in Fig. 5.2. This applies to traps both below and above Ev.

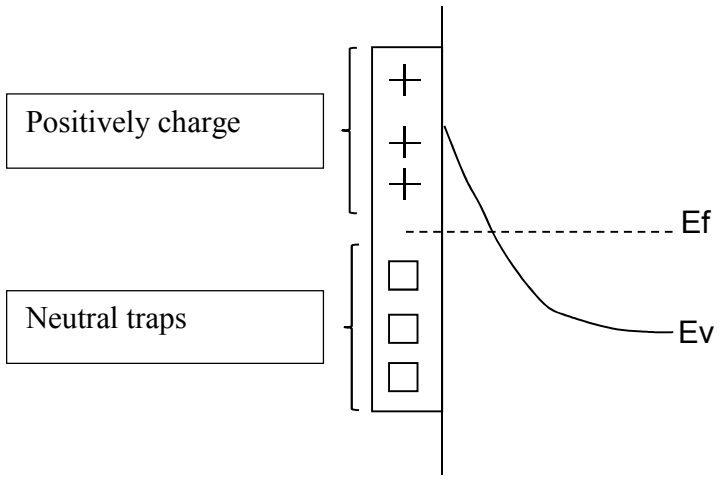

Fig. 5.2 The energy band diagram to illustrate the polarity of hole traps in the dielectric. The symbols of '□' and '+' are corresponding to the neutral and positively charged traps, respectively.

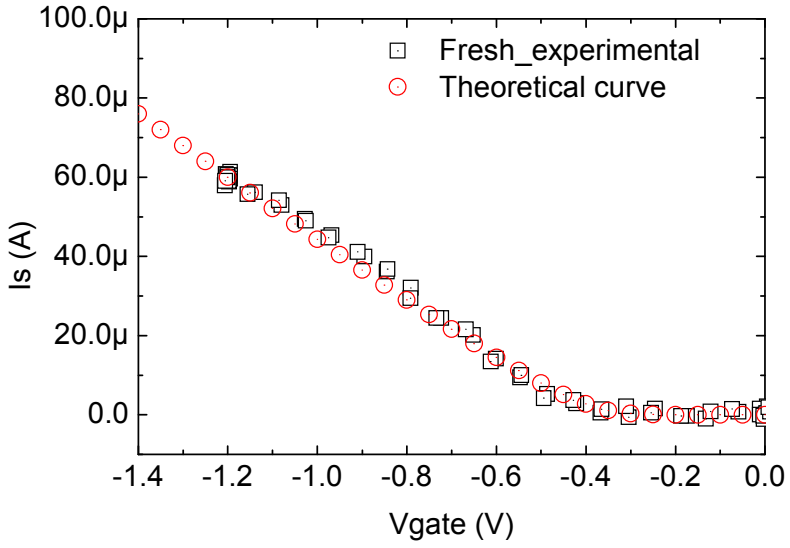

Fig. 5.3 Comparison of Pulsed Is-Vg measurement on fresh GeO_2/Ge pMOSFET and theoretical calculation by 1D simulator [175]. Good agreement indicates the traps are neutral when device is fresh.

The DMP measurement starts from the most negative Vg, i.e., the stress gate bias Vgst, under which the hole traps were charged during the stress. After stress and when Vdischarge were stepped towards positive direction, the Ef at the interface moved

upward in steps. For each step, a group of hole traps falling below Ef and were neutralized. Before electrical stress, the fresh gate dielectric is assumed to be neutral, since the measured threshold voltage agrees well with that calculated for a neutral gate dielectric, as shown in Fig. 5.3. Since the NBTI stress normally shifts the Vth in the negative direction, it can only be caused by an increase of positive charges in the oxide. During the discharge period after stress, Vth recovers through neutralization.

5.3 Measurement Time and Experimental Procedure

The device used here is the $Al_2O_3/GeO_2/Ge$, the same as that described in the chapter 4.

5.3.1 Measurement Time (tm)

The test started with recording the reference Is–Vg at Vd= -100 mV from a gate pulse edge of 5 μs [7, 125], as shown in Fig. 5.4. The reference threshold voltage, i.e. Vth0, was extracted by extrapolating from the maximum transconductance. The potential disturbance from discharging and charging during measurement is clarified below.

If the discharging occurs during the measurement itself, the measured charge will reduce for longer measurement time. Fig. 5.4 shows that this is indeed the case when the measurement time is longer than 20 μs. When the measurement time reduces from 20 μs by more than one order of magnitude, however, the ΔVth remains flat. This supports that the emission time of defects is over 20 μs under our test conditions. Discharging is

negligible during the measurement below 20 μs; therefore, a measurement time of 5 μs is used.

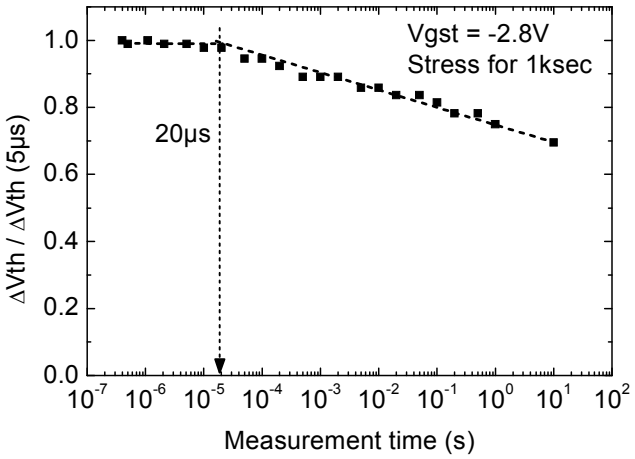

Fig. 5.4 Normalized Vth shift varies with different measurement time. Clear decrease is observed with measurement time longer than 20 μs.

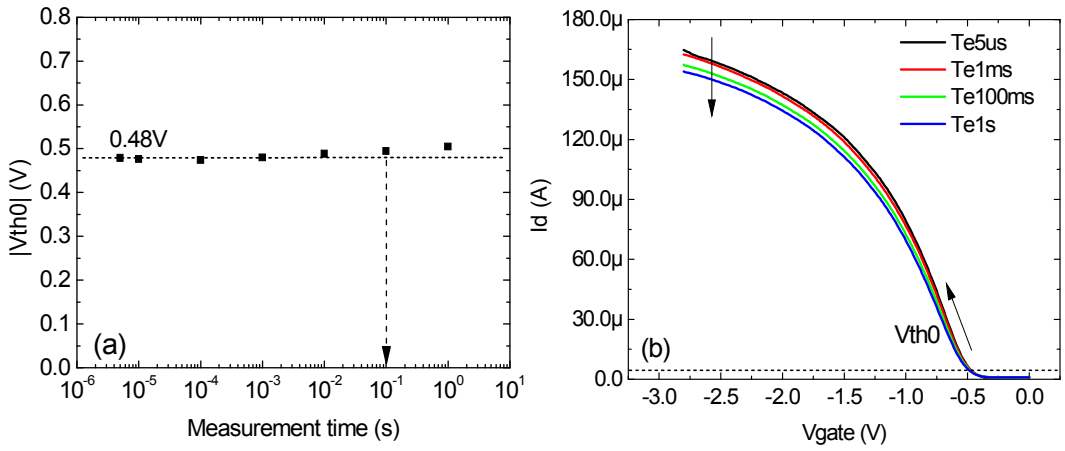

Fig. 5.5 |Vth0| is measured with different measurement time on a fresh GeO_2/Ge device (a) with corresponding Id-Vg curves (b).

Potential trapping could also happen during the measurement itself. Fig. 5.5 gives the Vth0 measured on a fresh device against the measurement time. When the measurement time is longer than 100 ms, |Vth0| clearly increases, supporting that trapping does occur

during the measurement itself. For a measurement time less than 100 ms, the measured Vth0 is flat, supporting negligible trapping. Since 5 μs was used for the measurement, the trapping during the measurement itself is also negligible.

5.3.2 Experimental Procedure

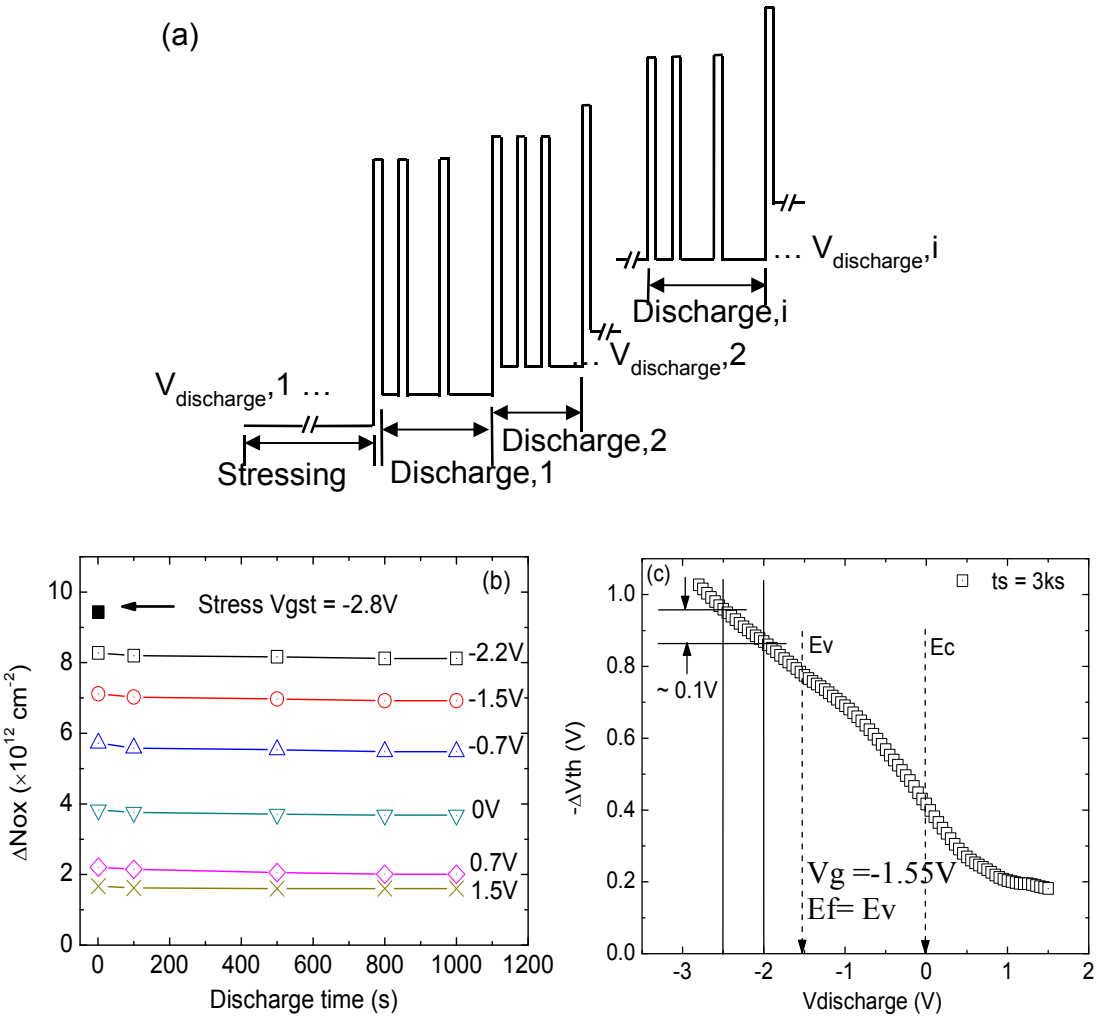

Fig. 5.6 (a) The Vg waveform; (b) The discharging against time under each Vdischarge; and (c) The ΔVth at the end of each discharge period against Vdischarge. The device was stressed at Vgst=-2.8 V, 20 °C, for 3000 sec.

After stressing for a pre-specified time, |Vg| was reduced from |Vgst| to |Vdischarge,1| by using the waveform in Fig. 5.6(a). The discharging under |Vdischarge,1| was monitored periodically by the pulses and the Vth shift, i.e. ΔVth, was measured at a constant Is = 100 × W / L nA. Once Discharge,1 completes, gate bias was stepped to |Vdischarge,2| and the same procedure was applied. It was found that a pulse edge time of 5 μs was fast enough to freeze the discharging and that charging was negligible in section 5.3.1. The effective density of positive charges, ΔNox, defined as ΔNox = Cox × ΔVth/q – ΔNit, versus discharging time is given in Fig. 5.6(b). Fig. 5.6(b) shows that the discharge mainly occurs within 1 sec, so that a discharge time of 1 sec will be used for each Vdischarge hereafter. Fig. 5.6(c) gives the ΔVth at 1 sec of discharging versus Vdischarge. The variation of ΔVth with Vdischarge is significant.

5.4 Energy distribution of Hole Traps in GeO_2/Ge Gate Stack

5.4.1 Energy distribution of Hole Traps

To obtain the energy distribution, Vdischarge should be converted to Ef - Ev at the interface. This relationship was obtained from a 1D Schrödinger-Poisson simulator [175] and the result is given in Fig. 5.7(a). It should be noted that the horizontal axis of Fig. 5.7(a) is Vg - Vth and Vth = Vth0 + ΔVth varies during discharging, where Vth0 is the threshold voltage of fresh device and ΔVth means the threshold voltage shifts.

Fig. 5.7(b) plots the effective density of PCs, i.e. ΔNox, versus Ef - Ev, evaluated from ΔNox = Cox × ΔVth / q – ΔNit, where ΔNit is the number of generated interface states charged at Is = 100 × W / L nA [26]. The ΔNit was measured by the standard charge pumping method at a frequency of 1 MHz, a rise/fall time of 20 ns, and an amplitude of 1.0 V, as detailed in Chapter 4. The effect of ΔNit on evaluating the energy distribution of PCs [26] is further discussed in section 5.4.2

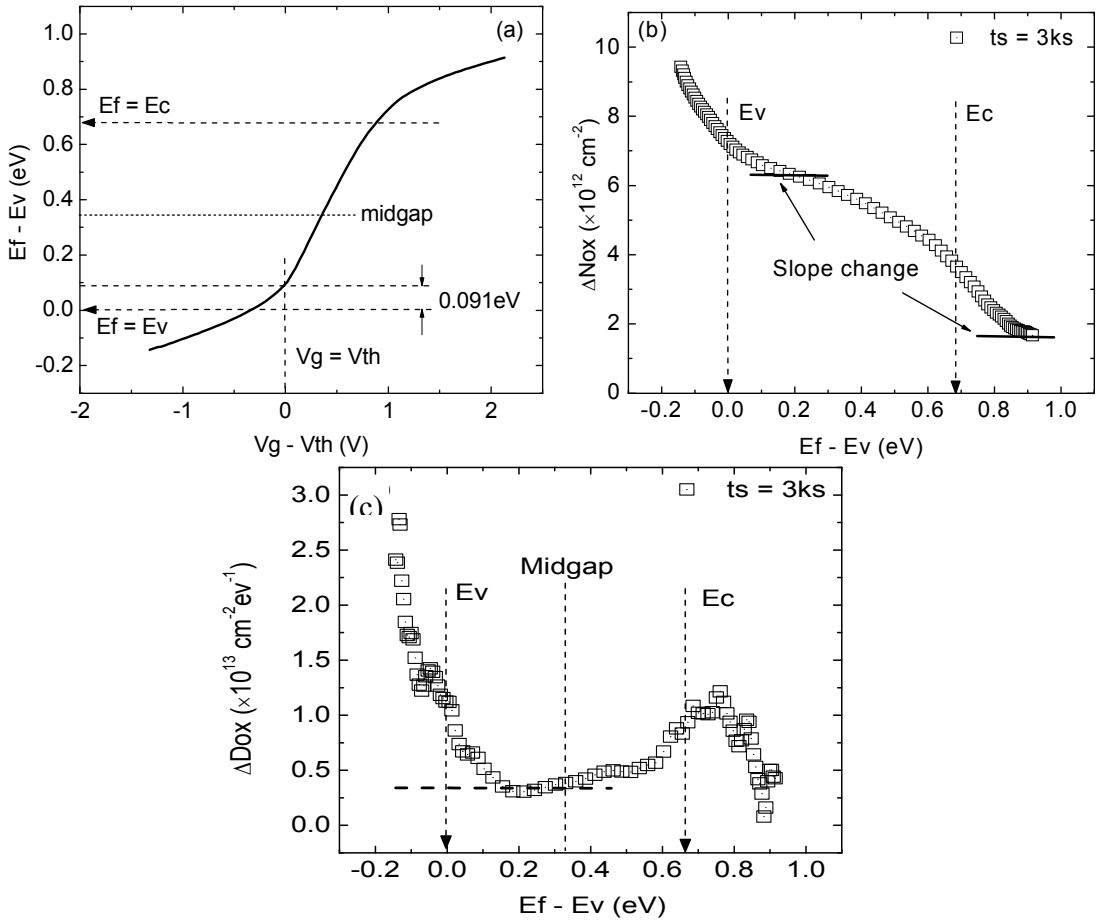

Fig. 5.7 (a) The Ef - Ev against Vg - Vth for converting each Vdischarge to an Ef - Ev. (b) The typical energy distribution of PCs per unit area, ΔNox. (c) The corresponding energy density, ΔDox. The device was stressed at Vgst = -2.8 V, 20 °C, for 3000 sec.

The energy density of PCs is evaluated from $\Delta Dox = -d(\Delta Nox) / d(Ef - Ev)$ and a typical result is given in Fig. 5.7(c). As Ef-Ev at the interface increases, Fig. 5.7(b) shows that ΔNox initially decreases rapidly, resulting in a high ΔDox in the order of 10^{13} $cm^{-2}eV^{-1}$. As Ef approaches Ev, however, the declining rate of ΔNox reduces sharply. To assess how the PCs below Ev affect device operation, Fig. 5.6(c) shows that Ef = Ev occurs at Vg = -1.55 V.

As a result, the hole traps below Ev are neutral and have no effect on devices with an operational $|Vg| < 1.55$ V. For higher operation $|Vg| > 1.55$V, however, some PCs will be positively charged, reducing the driving $|Vg-Vth|$. For example, if $|Vg|$ increases from 2 to 2.5 V, Fig. 5.6(c) shows that 0.1 V, i.e. 20% of the $|Vg|$-increase, will be used to compensate the PCs.

When Ef moves above Ev, Fig. 5.7(b) shows a slope change, leading to a low level of ΔDox between Ev and Ec. As Ef approaches Ec, however, the declining rate of ΔNox picks up again, before the second slope change above Ec. This creates a clear peak of ~ 10^{13} $cm^{-2}eV^{-1}$ in ΔDox near Ec. The PCs near Ec will be charged under an operation Vg and cause significant NBTI for $Al_2O_3/GeO_2/Ge$ pMOSFETs.

5.4.2 Contribution of Interface States

After stress, the generated interface state density, ΔDit, was measured by the charge pumping technique. It was reported that, after stress, ΔDit did not change during the measurement [192] and we also found that ΔDit changed little during our measurements.

As a result, at a given stress level, the generated interface states, ΔNit, did not change during the discharge measurement, since ΔVth was always measured at the same source current for all Vdischarge.

For a given number of generated interface states, they will give a "fixed" level of interface charges when the surface potential is "fixed" at a level corresponding to Is= 100×W/L nA, as illustrated in the energy band diagram in Fig. 5.8. Since ΔVth was always measured at this 'Is' level for all Vdischarge, the contribution from ΔDit to ΔVth is also "fixed".

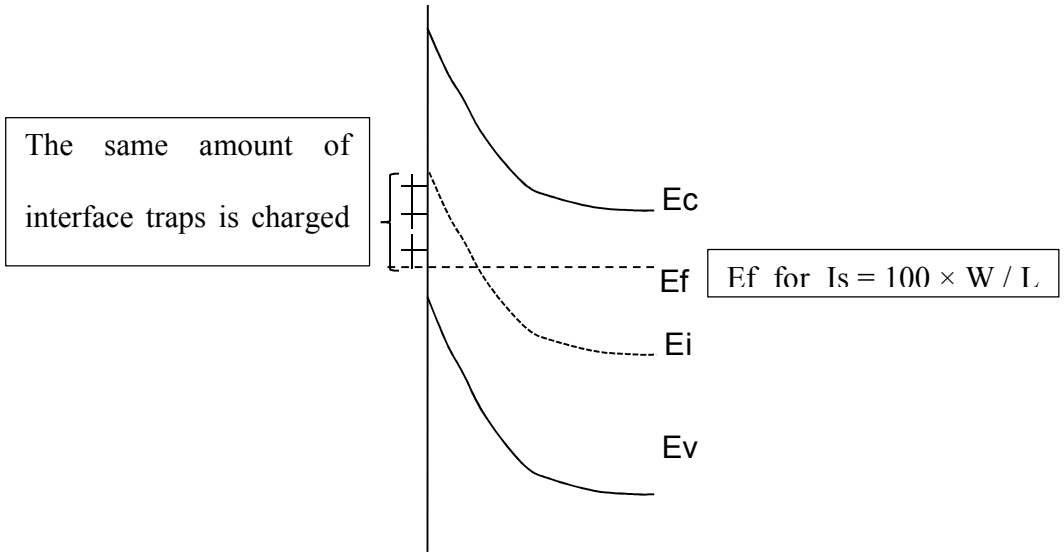

Fig. 5.8 Illustration of the amount of generated interface states corresponding to the Ef for current at threshold voltage level.

To estimate the contribution of ΔDit to ΔVth, it is desired to know the amount of generated interface states that are charged, i.e. ΔNit, at Is = 100 × W / L nA. It has been reported that the charge neutrality level for Ge is in the lower half of the bandgap, Eg [127]. As a first order estimation, however, we assumed that all interface states in the

lower half of the bandgap are positively charged, so that the number of positive charges from the ΔDit is expressed as,

$$\Delta N_{it} = \left(E_g/2\right) * \Delta D_{it} \ , \tag{5.1}$$

The total effective charge density is given by,

$$\Delta N_{th} = \Delta V_{th} * C_{ox}/q \ . \tag{5.2}$$

The effective charge density in the oxide is given by,

$$\Delta N_{ox} = \Delta N_{th} - \Delta N_{it} \ . \tag{5.3}$$

ΔNit, ΔNth, and ΔNox were compared in Fig. 5.9. It can be seen that the contribution from ΔNit to ΔNth is insignificant and this contribution is corrected by using the equations above.

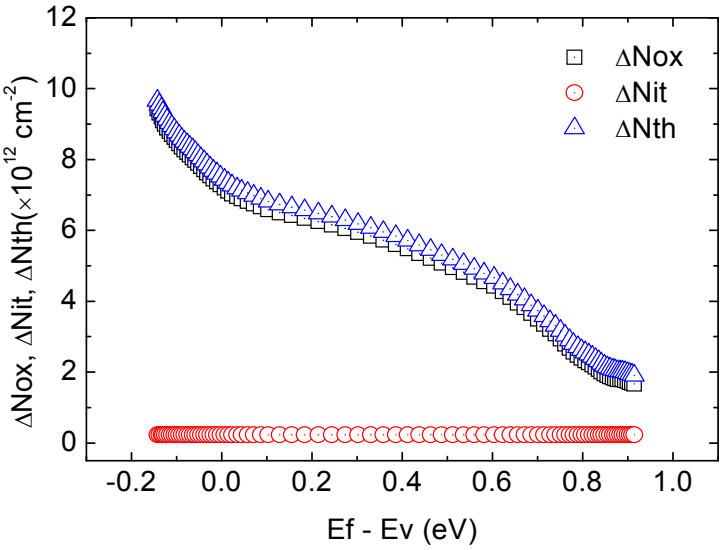

Fig. 5.9 Comparison of the interface states, oxide traps and total charged traps. The contribution of interface states is insignificant.

5.4.3 Effects of Stress Time

To explore the relation between the PCs below Ev and those above Ev, Fig. 5.10 compares their dependence on stress time. There is a substantial increase in the density with stress time. It is clear that, at short time (the symbol '●'), PCs are negligible above Ev, but substantial below Ev. As stress time increases, the PCs above Ev increase, but they do not shift up in parallel. To show that the PCs below Ev are insensitive to stress time, the top-dashed curve is used as an eye-guide for the top data-set with a stress time of 10 ksec. It is then shifted downward in parallel, showing good agreement with the data-set at 5 ms. It means that the below-Ev PCs were already fully charged after only 5 ms.

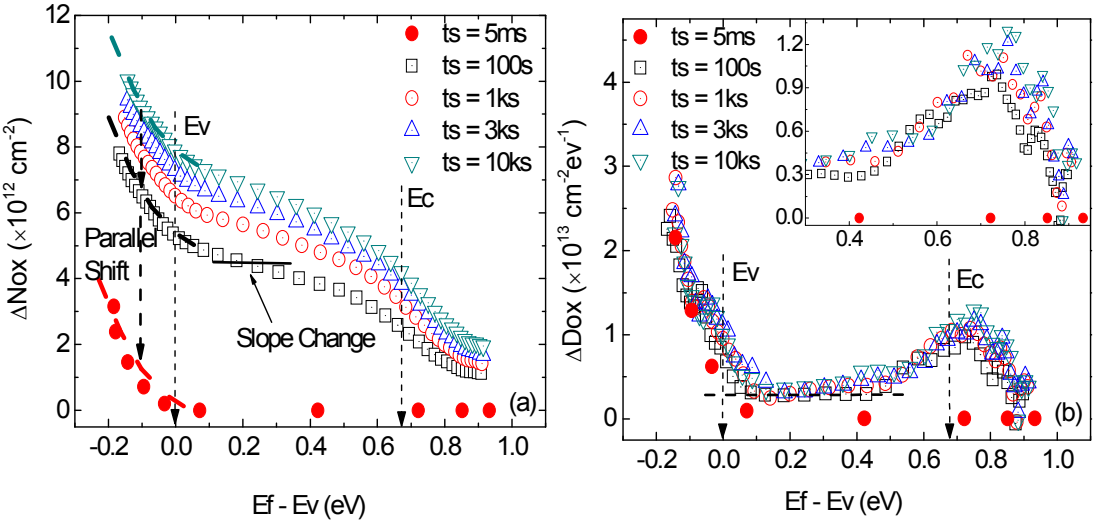

Fig. 5.10 A comparison of ΔNox(a) and ΔDox (b) after different stress time under Vgst = -2.8V at 20 ºC. The top dashed curve is an eye-guide for the top dataset at ts = 10 ks. The other two dashed curves were a parallel downward shift of the top dashed curve. The symbols '●' were obtained on a fresh device with a time for each point of 5 ms to minimize generation. The Vg was swept from positive to negative direction for this dataset.

The above energy distribution does not give a spatial distribution of positive charges and, without it, a volumetric density cannot be determined accurately. The areal density is widely used by test engineers (e.g. [20, 46, 47]), since it allows evaluating the impact of positive charges on threshold voltage and makes it easier to compare with the generated interface states.

5.5 Quantization and Fermi Level Pinning Effects

The above results showed that energy levels of hole traps are continuous and they can exist far outside the band gap. This energy distribution gives the PCs at a given surface potential needed for circuit and device simulation. In this section, we discuss the Quantization Effect and its difference from the classical understanding of the energy band. In addition, Fermi Level Pinning Effect and Discharge voltage step are further examined for the DMP Technique.

5.5.1 Quantization Effect

A particle in quantum mechanical systems is considered as 'particle in box' [205], which can only take on certain discrete value of energy. This is different from the classical particles, which can have any energy continuously. The energy spectrum of a system with discrete energy levels is named as quantized. Fig. 5.11 shows the energy levels for an electron in atoms: the lowest possible energy level, ground state and higher

energy levels, excited states. After absorbing energy, an electron may jump from the ground state to an excited state.

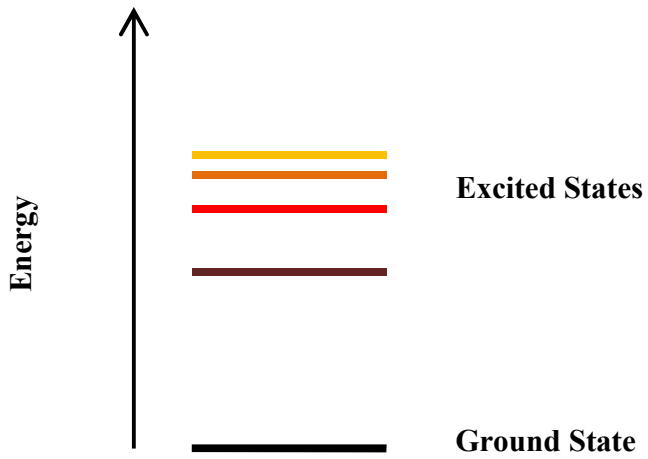

Fig. 5.11 Energy levels for an electron in an atom: ground state and excited states. After absorbing energy, an electron may jump from the ground state to a higher energy excited state.

From the view of quantum mechanics, it is difficult to move Ef beyond the bandgap by over 100 meV in Ge or Si. In the bulk of Ge or Si, the valence band edge, Ev, represents the energy level of ground states. When the band is bent upwardly under a negative gate bias, the simulation result in Fig. 5.12 shows that the energy level of ground states no longer follows the classical Ev, because of the quantization effects near the interface. As a result, although Ef is less than 100 meV below the ground state level marked as 'LH1' in the figure, it is 375 meV below the interfacial energy level corresponding to the classical Ev.

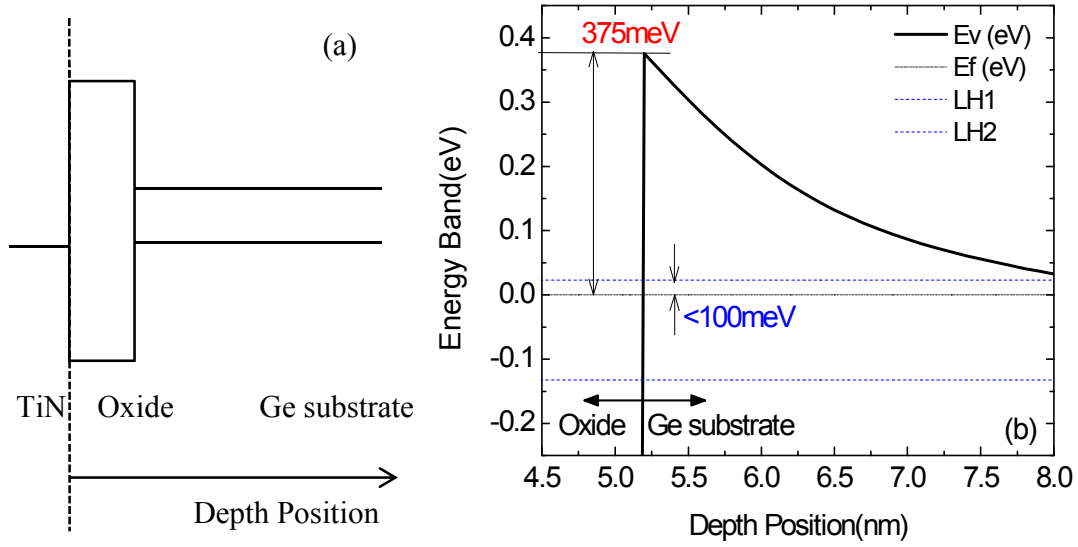

Fig. 5.12 Energy levels of ground state no longer follow classical Ev due to quantization effects near the interface.

In another word, the quantization effect causes a deviation of the ground state energy level from the classical Ev, making it possible for Ef to be several hundreds of meV below the classical Ev. Similarly, Ef can be several hundreds of meV above the classical Ec at the interface. Although the Ev and Ec at the interface no longer represent the ground state energy levels, it is a common practice to use 'Ec' and 'Ev' to represent the band bending at the interface (e.g. [27, 28, 204, 206-209]), which is followed in this thesis.

5.5.2 Fermi Level Pinning Effect

"Fermi level pinning at the band edges" was a popular phenomenon, which was noted by John Bardeen in 1947 [210]. Question would be naturally raised whether there were

high density of states at the interface of oxide/substrate, because these states are able to absorb a large number of charges, leading to a nearly fixed Fermi level as Vg changes. When the gate oxide was thick (e.g. 20 nm) and the operation voltage was 5 V, Fig. 5.13(a) shows that Ef was reasonably pinned at the classical Ec and Ev at the interface indeed, since the voltage will mainly drop over the oxide. For a 2.35 nm oxide, i.e. the equivalent thickness used in this thesis, the Ef-Ev can reach several hundreds of meV at the interface. An introduction of defects in the order of 10^{12} ~ 10^{13} cm^{-2} eV^{-1} at the interface only has a marginal effect on the Ef-Ev for both Si and Ge MOSFETs, as shown in Fig. 5.13(a) and (b).

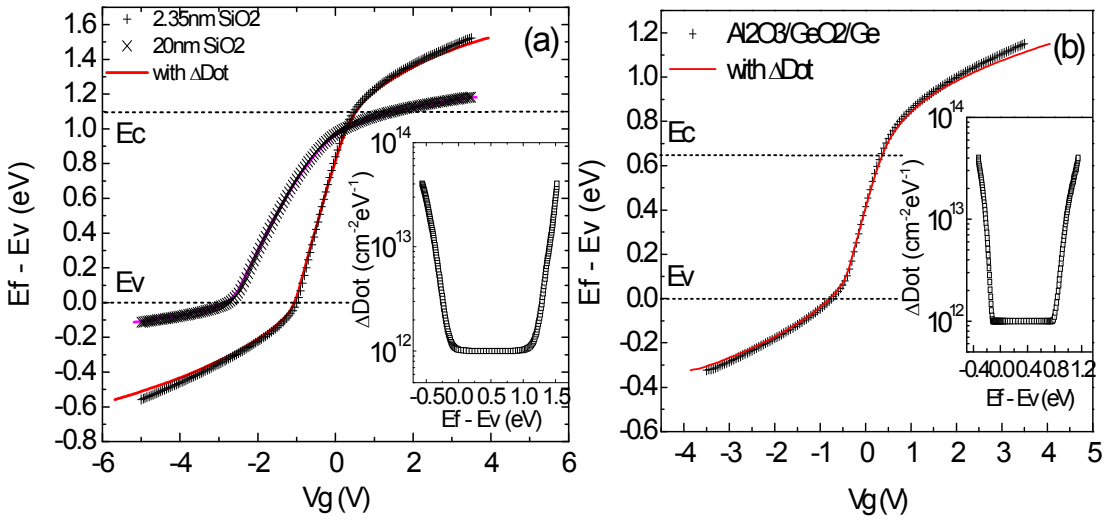

Fig. 5.13 Impact of oxide thickness and high density states on the Fermi level pinning at the band edges (a) 2.35nm & 20nm SiO_2/Si (b) 2.35nm EOT GeO_2/Ge device.

5.5.3 Discharge Voltage Step

The accuracy in the energy for the distribution measured in this chapter will be limited to around kT/q. To test if the use of a Vdischarge step as small as 0.05 V causes any

additional inaccuracy, new tests were carried out with much larger Vdischarge step. It is shown in Fig. 5.14 that the distribution is insensitive to the voltage step size.

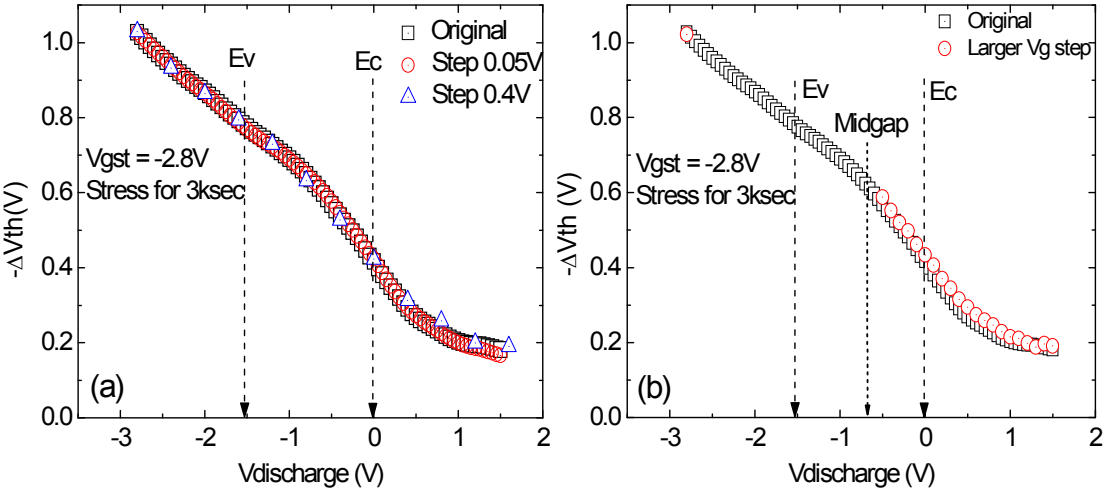

Fig. 5.14 Comparison of different Vdischarge steps (a) continuously discharging step by step (b) 'big jump' discharging step.

5.6 Understanding of Defect Differences and Energy Alternating

The different stress-time dependence of defects below Ev and around Ec shown in Section 5.4.3 indicates that they could originate from different defects, although the electrical measurements reported here do not give direct information on their microscopic structure. For SiO_2/Si, it is reported that oxygen vacancy is a hole trap [211] and some hydrogen-related defects can form different types of hole traps [201]. One may speculate that oxygen vacancy and hydrogenous defects also exist in the present Al_2O_3/GeO_2/Ge sample, which awaits further investigation [188]. In chapter 4, we

explained the differences of defects properties by a speculated energy alternating defect (EAD) model only based on the DC measurement. In this section, investigation is carried out on the defects differences in terms of the energy level by the DMP technique and the EAD model is further verified.

5.6.1 Defect Differences

1) Recovery: Fig. 5.15(a) and Fig. 5.16(a) show that the degradation in GeO_2 devices is fully recoverable, but not in Si devices, respectively;

2) 2^{nd} stress: After the recovery, 2^{nd} stress was carried out under the same stress conidition as the 1^{st} one. In GeO_2 devices, it follows the same kinetics as 1^{st} one, as shown in Fig. 5.15(b), indicating that all defects have returned to their fresh states after recovery. However, in Si devices, Fig. 5.16(b) shows that 2^{nd} stress deviates from 1^{st} one, after AHTs are refilled as indicated with the parallel shift-down of 2^{nd} stress;

3) Recharge: Following the discharge through which the energy profiles are obtained, recharge was conducted after discharge. Traps in Ge cannot be recharged until charging energy level (EL) is swept back near Ge Ev (see Fig. 5.15(c)). To compare with Ge, similar test was carried out on Si devices [26], and Fig. 5.16(c) shows different recharge behavior: it starts once the energy level is swept lower than Ec of Si;

4) Temperature (T): For Ge devices, no recharge is observed in the upper half of Ge band gap and the recharge is independent of T, either RT or 125 °C (see Fig. 5.15(d)). However, for Si, Fig. 5.16(d) shows that the recharge clearly rises near the Si Ec when lowering T from 125 °C to RT. Further explaination is given below.

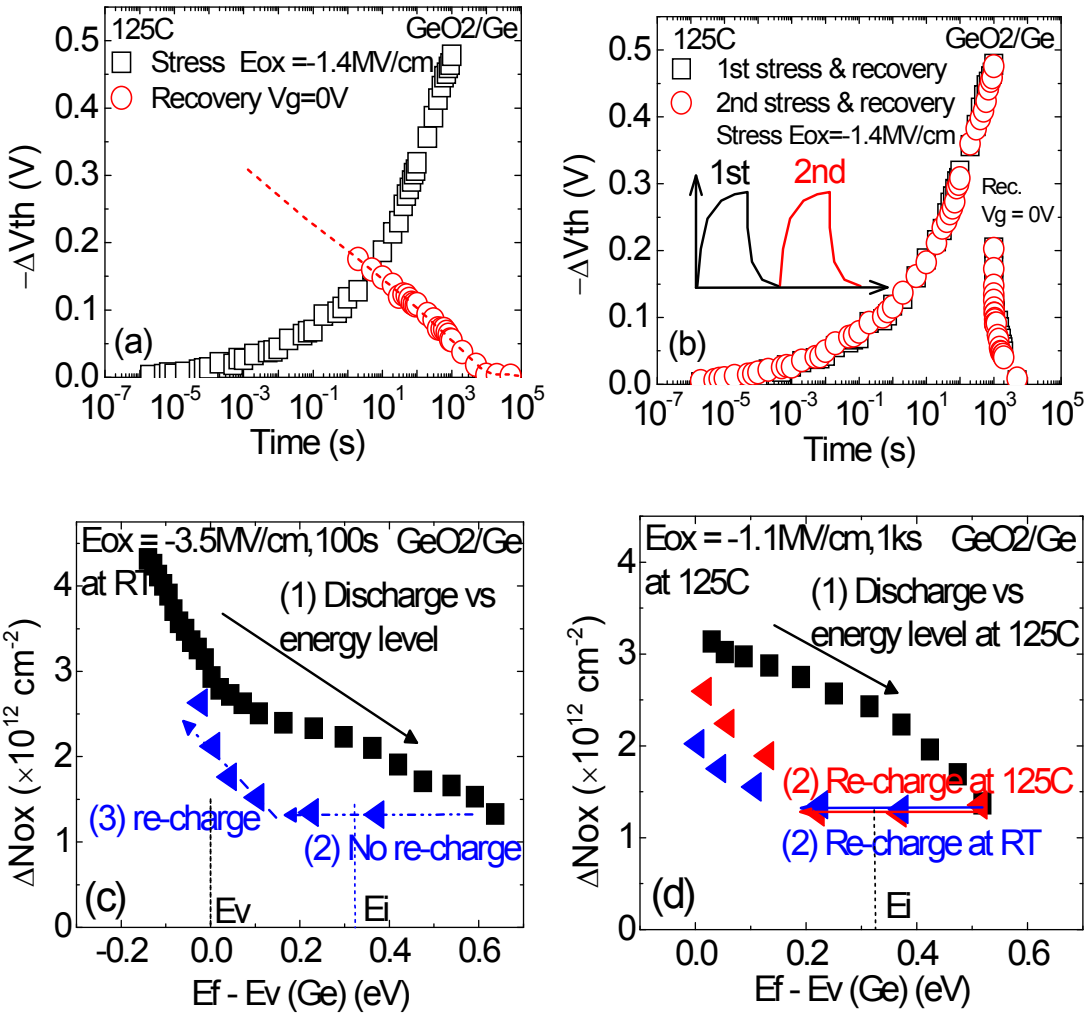

Fig. 5.15 Defects in GeO_2/Ge device: (a) Degradation is fully recoverable without a permanent component. (b) The 2nd stress after recovery follows the same kinetics as the 1st one. All defects returned to their fresh states after recovery. (c) Negligible recharge when biased in the upper half of bandgap. (d) Recharge does not increase when switching from 125 °C to room temperature (RT).

As illustrated in Fig. 5.17(a), the energy level of EAD alternates with its charge status: it shifts to energy level above Ev when it gets charged, and shifts back below Ev of Ge when neutralized. In contrast, the generated defects (GD) in Si do not alternate, with its energy level well above Ev of Si (see Fig. 5.16(b)). Since EADs in Ge devices will

return to their fresh states after neutralization, the 2nd stress in Ge has the same kinetics as 1st one as expected, as shown in Fig. 5.15(b). Recharging EAD can only take place when biased below ~Ev, the same as in a fresh device (Fig. 5.15(c)), but cannot when biased at ~Ec at either room temperature (RT) or 125 °C (Fig. 5.15 (d)).

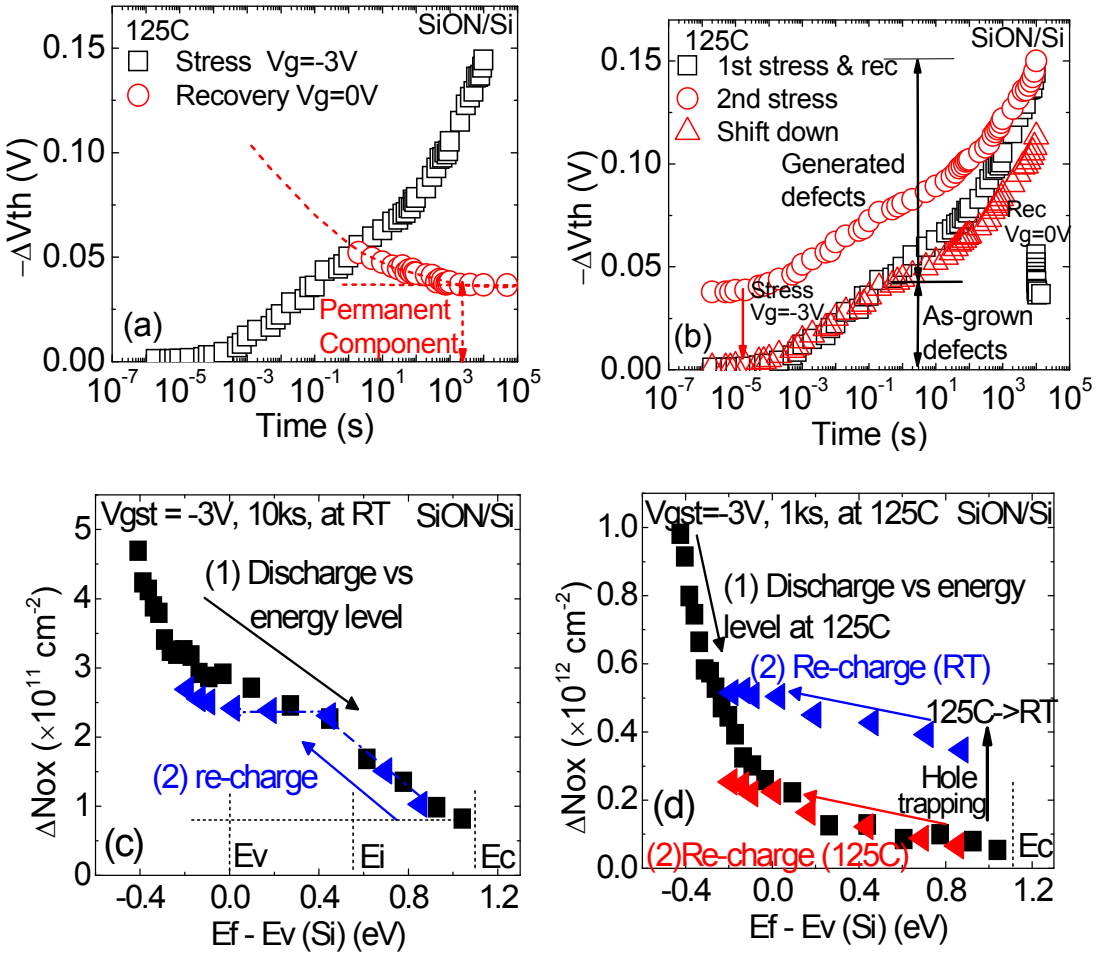

Fig. 5.16 Defects in SiO_2/Si device: (a) NBTI is not fully recovered due to permanent component. (b) 2nd stress after recovery follows the same kinetics for AHTs, but different kinetics for generated defects (GD). 'Δ' is a parallel downward shift of 'O'. (c) Recharge occurs in the upper half of band gap. (d) Recharge increases when switching from 125 °C and RT. The hole traps neutralized at 125 °C at high energy levels are recharged at RT due to lower electron energy at RT.

In contrast, since generated defects in Si keep their high energy level after being neutralized and do not return to their fresh states, its kinetics during 2nd stress is different from 1st one (Fig. 5.16(b)). The neutralized GDs at high energy level recharge once above Ef (Fig. 5.16(c)). They also recharge when switching from 125 °C to RT as there are less electrons at RT that can reach and neutralize them (Fig. 5.16(d) and Fig. 5.17(b)).

5.6.2 Energy Alternating Defects (EAD) Model

The differences shown in Section 5.6.1 can be explained by the presence of Energy Alternating Defects (EAD) in Ge, which is absent in Si devices.

As described in Chapter 2, for Si pMOSFETs, the positive charges (PC) in gate oxides can be classified into three groups according to their energy ranges: As-grown hole traps (AHTs) below the Si Ev, Cyclic positive charges (CPCs) around Si Ec, and Anti-neutralization positive charges (ANPC) above Si Ec [17, 22, 94, 99, 177]. With energy levels above Si Ec, ANPC is difficult to reach by free electrons from Si substrate [17, 94, 99, 177], making them difficult to be neutralized.

5.6.3 Confirmation of Energy Alternating Defects

As discussed above in Fig. 5.15 and Fig. 5.16, the experimental differences strongly suggest the existence of energy alternating defects (EADs) in Ge devices. To better explain the EADs in Ge devices, it is worth further emphasizing the third difference that

there is little recharge when the Ef sweeps at the upper half of the bandgap, the same energy location after the discharge, and it can only start to recharge the defects when the Ef changes its energy level to around Ev of Ge, as shown in Fig. 5.15(c). This means the energy level of this type of defects is at higher energy location after charge while at lower energy location after neutralization.

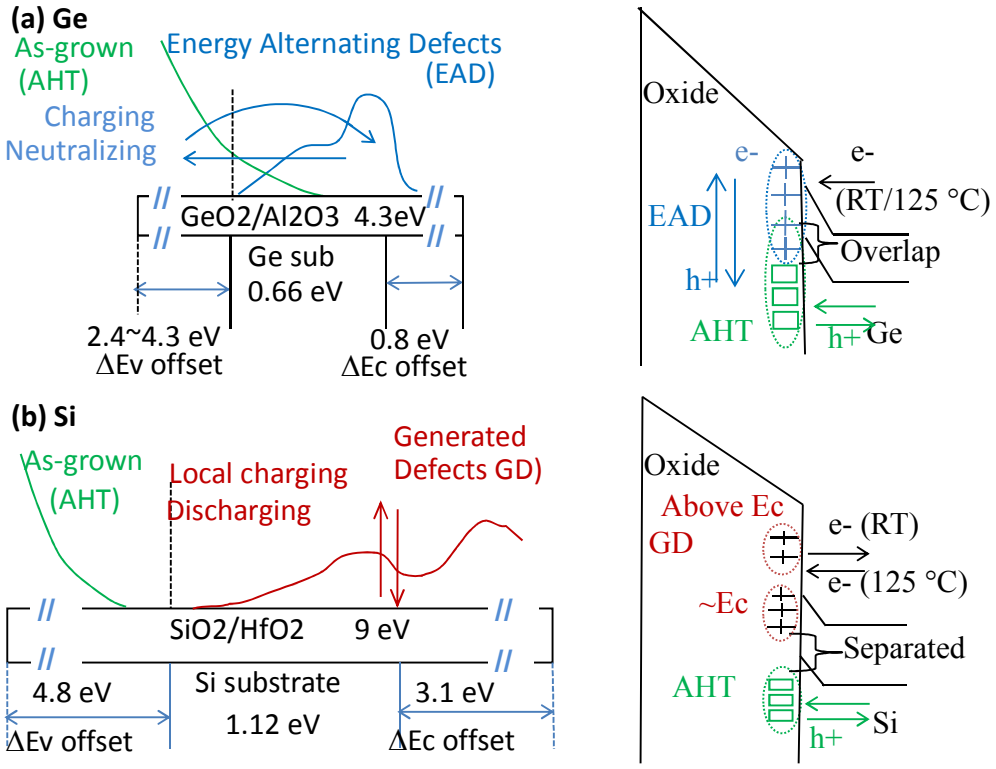

Fig. 5.17 Illustration of defect differences in Ge and Si devices. (a) GeO_2/Ge: **AHTs**, either charged or neutral, are mainly below Ev with a tail above Ev. **EADs** are below Ev when neutral, shift to above Ev once charged, return to fresh states below Ev after neutralization. (b) SiO_2/Si: **AHTs** are below Ev without the tail. **GDs** are generated and have high energy levels, either charged or neutral. **GDs** above Ec cannot be fully neutralized, leading to the permanent component. **GDs** neutralized at 125 ^oC can be recharged at RT by e-tunneling to Si conduction band. Small Ec offset at oxide/Ge allows full neutralization of **EADs**.

As comparison, shown in Fig. 5.16(c), the same experiments in Si devices shows that the recharge happened at the same energy level locally once finished the discharge period, ,which is very different from Ge, suggesting no clear experimental observation of energy changing with charge status in the Si case.

Besides, the defects were able to be fully neutralized in Ge devices, as shown in Fig. 5.15(a) and Fig. 5.15(b). They agree with what we observed during the initial characterization of anneal effects in Fig. 4.8 and Fig. 4.9. Also, the impact of measurement temperature as shown in Fig. 5.15(d) and Fig. 5.16(d) agree with the initial experimental observation as discussed in Fig. 4.18.

The absence of ‘permanent' component in Ge (see Fig. 5.15(a)) is because the charged EADs are sufficiently close to Ge Ec and fully neutralized, as the Ec offset at GeO_2/Ge interface is smaller than that at SiON/Si [188]. The anneal effects agree with the Chapter 4 [29], in which energy alternation has been speculated for possible explanation. The energy alternation with charge status is also supported by the first-principle calculations, re-plotted as shown in Fig. 5.18 [212-214], suggesting that EADs are intrinsic in Al_2O_3/GeO_2/Ge.

Results strongly support the existence of EADs in Ge devices, even when a fast measurement technique was used in this chapter, instead of conventional DC measurement utilized in Chapter 4. Therefore, the energy alternating defects (EADs)

model proposed in Chapter 4 is well confirmed in this chapter, for a better description of the mechanism and explanation of the EADs existence in Ge MOSFETs.

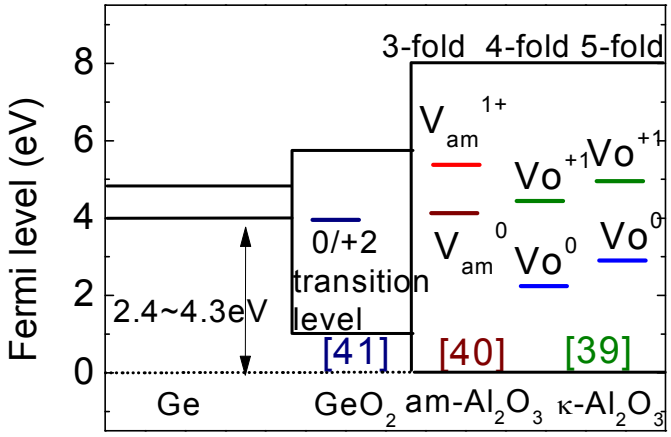

Fig. 5.18 First principle calculations show intrinsic energy alternating defects in Al_2O_3 [212, 213]. For GeO_2, the charge transition level is reported for hole traps [214].

5.6.4 Charging/Discharging via Tunneling

The charging and discharging of hole traps in the dielectric is through tunneling process. There are a significant number of holes present in the inversion layer which are ready to tunnel into the dielectric. Whether these holes can fill a trap or not, however, depends on its energy level relative to the trap. As an approximation, we assume that most holes at the interface are above Ef and there are little holes below Ef at the interface. Fig. 5.19(a) illustrates the possible process for charging a trap above Ef: either by inelastic tunneling through multiple phonons [117] or via interface states [215]. For the traps below Ef, Fig. 5.19(b) shows that tunneling holes will not fill them, since their energy is inadequate to reach them and occupation probability is low.

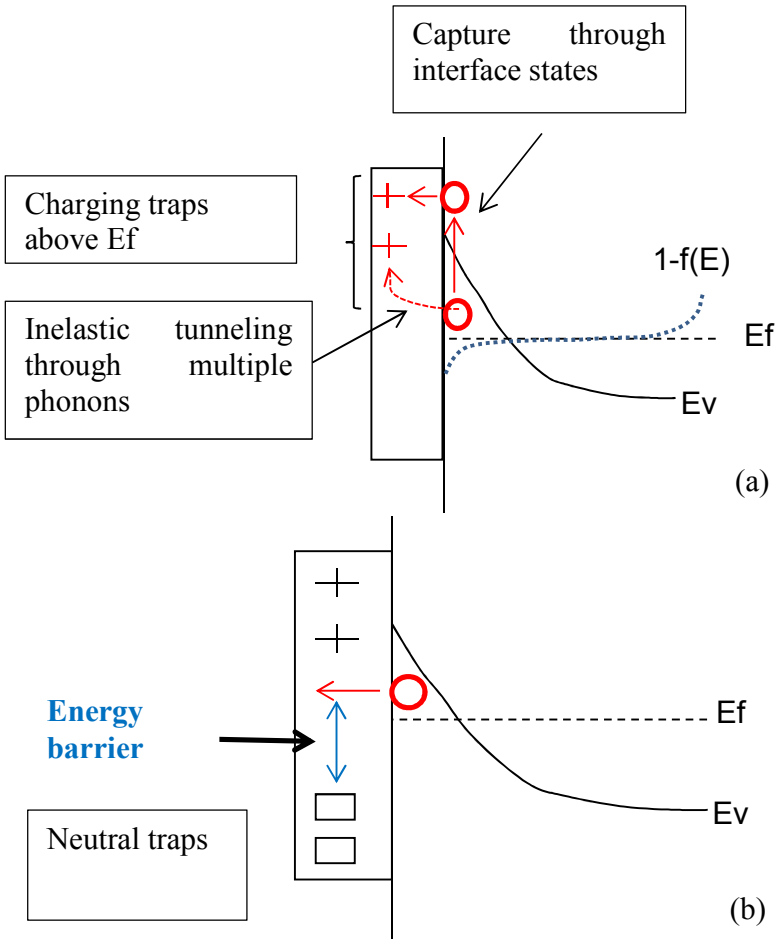

Fig. 5.19 Illustration of two possible processes for charging a trap above Ef: via interface states and inelastic tunneling through multiple phonons (a) and energy barrier for hole trap filling (b).

5.7 Summary

In this chapter, the energy distribution of PCs in the $Al_2O_3/GeO_2/Ge$ gate stack was characterized in detail and the proposed model in chapter 4 was further verified. The results show that ΔVth can vary significantly when Ef was swept from below Ev to above Ec at the Ge interface. The energy density distribution has three features: a rapid

rise when moving below Ev at the interface, relatively low between Ev and Ec, and a peak near Ec. The below- and above-Ev PCs have different dependences on stress time: the charging of below-Ev PCs is rapid and saturates, while it is slower and does not saturate for the above-Ev PCs. The density can reach 10^{13} $cm^{-2}eV^{-1}$ below Ev and 20% of |Vg|-increases will be screened by these PCs. After charging, the energy level of the defect moves upwardly after charging, when compared with that for pre-charging. The important point here is that for the $Ge/GeO_2/Al_2O_3$, this charging-induced energy level change is much larger than that for the Si sample. For the positive charges above the Si Ec, after neutralization, they are still above Si Ec and the energy level change cannot be experimentally observed. However, for the positive charges above Ge Ec, after neutralization, they fell well below Ec. This energy-alternating can explain the different behaviour of positive charges between $Ge/GeO_2/Al_2O_3$ and Si samples satisfactorily.

6 Investigation of NBTI lifetime prediction and AC kinetics in Germanium pMOSFETs

6.1 Introduction

Chapter 4 reported that the traditional lifetime prediction method with DC measurement cannot be applied to Ge with Al_2O_3/GeO_2 gate stack, due to the non-constant power exponent under different stress conditions [29]. The reason was unknown at that time. It was reported that Si-cap/Ge device has superior reliability, but NBTI degradation in Si-cap Ge devices by DC measurement also cannot be described by power law $\Delta Vth = C \cdot V_{ov}^{\gamma} \cdot t^{n}$ [30], and its lifetime, τ, cannot be predicted by power law extrapolation [30, 31]. This is also true for GeO_2/Ge devices albeit its NBTI is higher [32]. NBTI measured by fast pulse technique is further examined in this Chapter, as shown in Fig. 6.1(a) and (b). It is found that the power law is also inapplicable for both Si-cap/Ge and Al_2O_3/GeO_2/Ge, preventing reliable lifetime prediction (see Fig. 6.1(c)).

For Si devices, the latest results show that the power law can be restored for the generated defects (GD), after removing the as-grown hole trapping (AHT) [126]. This Si method works well for Si device, but does not work for Ge, as shown in Fig. 6.2.

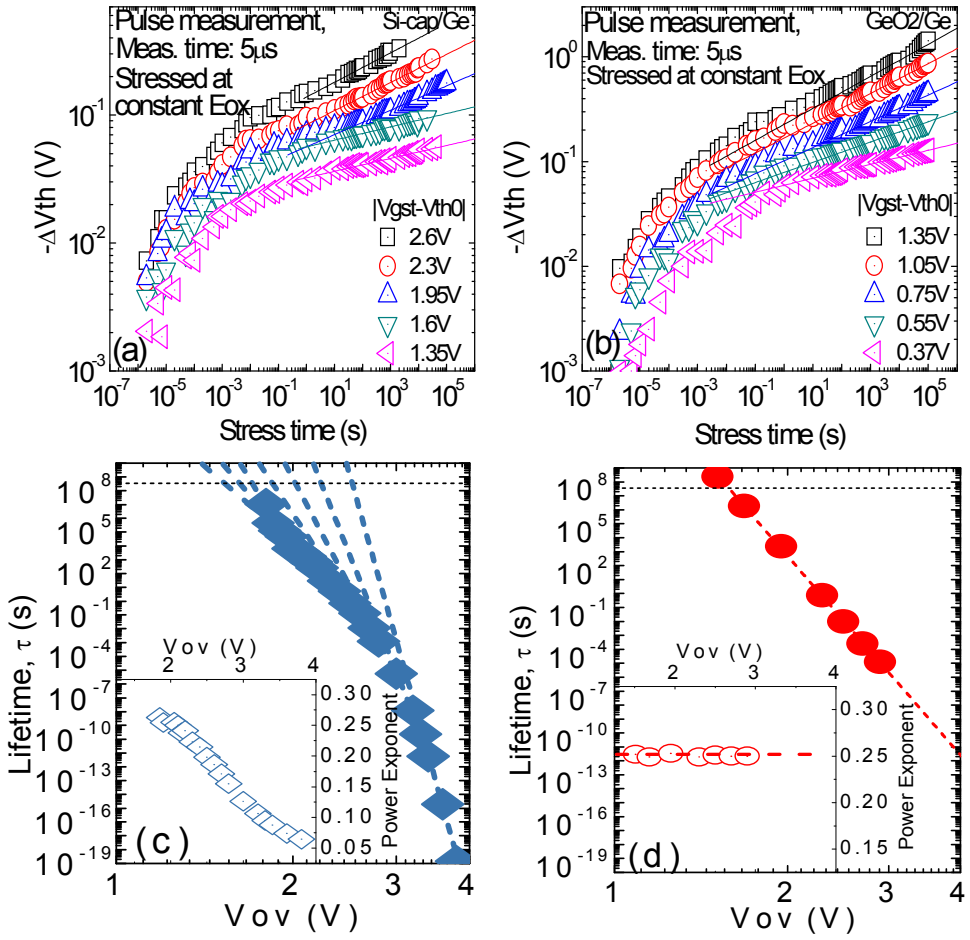

Fig. 6.1 NBTI in (a) Si-cap and (b) GeO_2/Ge devices do not follow a power law. (c) Power law extrapolation failed for Si-cap devices, as the exponent (inset) is not a constant [30]. (d) Power law is restored by the new technique developed in this work with a constant exponent (inset).

Tests [32] were carried out to characterize the energy distribution of hole traps and AHT was also observed as a parallel shift-up below Ev of Ge. Although 'AHT' are removed by this Si method after each specific stress condition [32], varying power exponent is still observable in Fig. 6.2(b). Therefore, there is a pressing need to develop a new method for Ge to restore power law, enable lifetime, τ, prediction, and assist in process development.

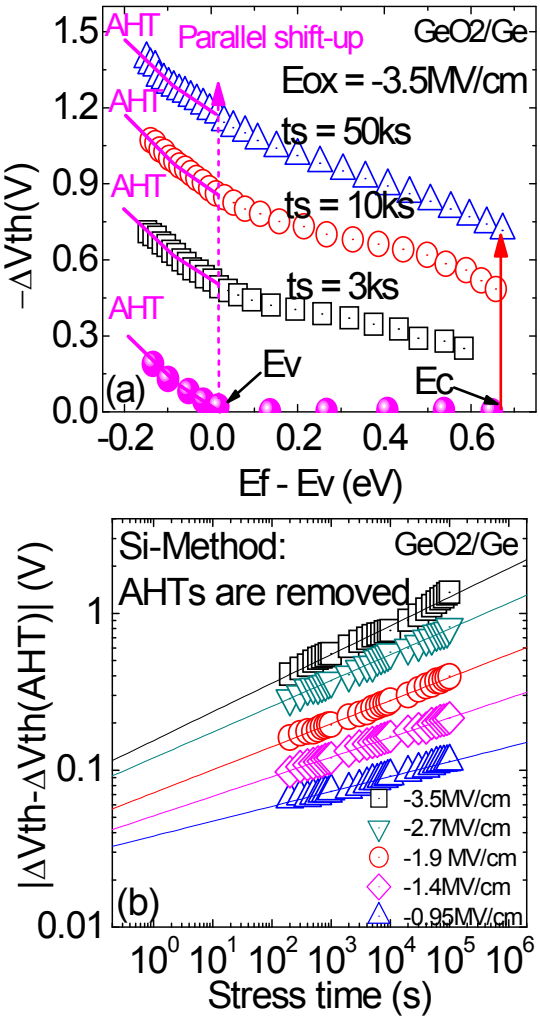

Fig. 6.2 (a) Energy profiles of defects in GeO_2/Ge are obtained by discharging defects against energy levels from low-to-high. AHTs, obtained with the Si-method by sweep-charging from high-to-low on fresh device [6], are below Ev and do not increase with stress time. (b) Removing AHT leads to a varying power exponent (slope), preventing reliable extrapolation from high stress Vg to low operation Vg.

Equipped with the knowledge gained in Chapter 4 and 5, where NBTI was initially evaluated in Chapter 4 and the proposed EAD model was verified by defect energy distribution in Chapter 5, a new technique will be developed to restore the power law for NBTI degradation in Ge pMOSFETs, enabling lifetime prediction (see Fig. 6.1(d)).

AHTs and EAD will be separated first in Section 6.4 and the degradation kinetics for EADs and lifetime prediction based on the new technique will then be investigated in Section 6.5. The applicability of this new technique in Si-cap Ge devices will be investigated in Section 6.6. NBTI under AC stress conditions in GeO_2 and Si-cap devices will be investigated in Sections 6.7 and 6.8, respectively.

6.2 Devices and experiments

The test follows the same procedures as in the chapters 4 and 5. The gate dielectric stack used for the majority of tests in this chapter is shown in Fig. 6.3(a) and (b). The GeO_2/Ge device is the same as that used in chapters 4 and 5, i.e., a 1.2 nm GeO_2 and a 4 nm Al_2O_3 [171], resulting in a SiO_2 equivalent oxide thickness of 2.35 nm for the stack.

Devices used are summarized in Table 6.1. Plasma nitrided SiON/Si structure is used for the purpose of comparison. Al_2O_3/GeO_2/Ge device process is described in chapter 4. For Si-cap/Ge device, the initial non-optimized Si-cap layer was grown at 500 °C for the Ge surface passivation, followed by an ozone oxidation forming of SiO_2. 4 nm HfO_2 is deposited using atomic layer deposition. After optimization, the deposition of Si-cap layer was under a lower temperature (350 °C), with a thinner HfO_2 (2 nm) on it.

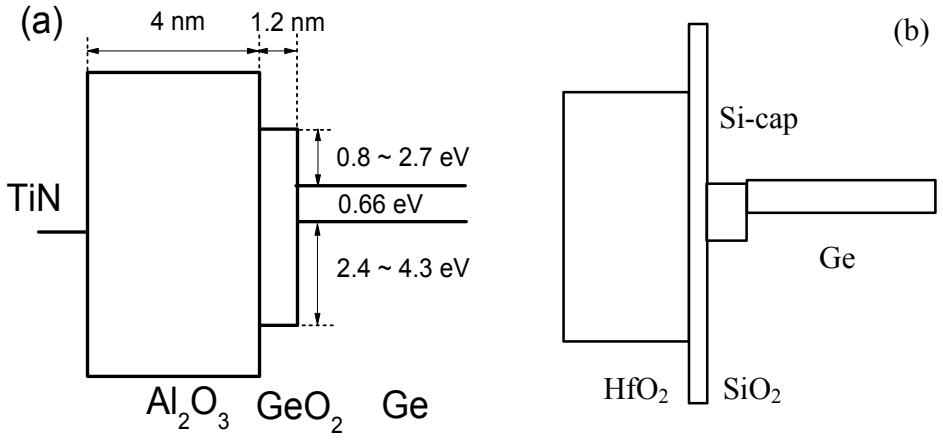

Fig. 6.3 Schematic energy band diagram and structure of (a) GeO_2/Ge (b) Si-cap/Ge devices

Table 6.1 Gate stack and exponents for Si and Ge Samples

(1) 2.3nm plasma-N **SiON/Si** (125^oC: n = 0.20, m = 16.1, γ = 3.22)
(2) 4nm Al_2O_3/1.2nm **GeO_2/Ge** (RT: n = 0.20, m = 14.4, γ = 2.88; 125^oC: n = 0.24, m = 10.9, γ = 2.62)
(3) 4nmHfO_2/~0.5nmSiO_2/**Si-cap/Ge(non- optimized)** (RT: n = 0.19, m = 25.3, γ = 2.92)
(4) 2nmHfO_2/~0.4nmSiO_2/**Si-cap/Ge(optimized)** (thick Si-cap: RT: n = 0.25, m = 46.0, γ = 11.5; 125^oC: n = 0.28, m = 34.4, γ = 9.63 thin Si-cap: 125^oC: n = 0.19, m = 34.0, γ = 6.46)

6.3 As-grown hole traps (AHT) and EAD separation

AHTs in Si devices are typically below Ev of Si and measured by sweeping energy level from high to low level [32]. When this Si method is applied to GeO_2/Ge, it appears that Ge AHTs were also below Ev, as shown with symbol '■' in Fig. 6.4(a). There are two possible explanations for the absence of AHTs above Ev. One is that AHTs do not exist above Ev. The other is that the apparent absence of AHTs above Ev is actually an artifact. There could be a substantial amount of Ge AHTs above Ev (see grey triangle in Fig. 6.4(a)) which were not detected by the Si method because of insufficient charging during sweeping when Ef is above Ev.

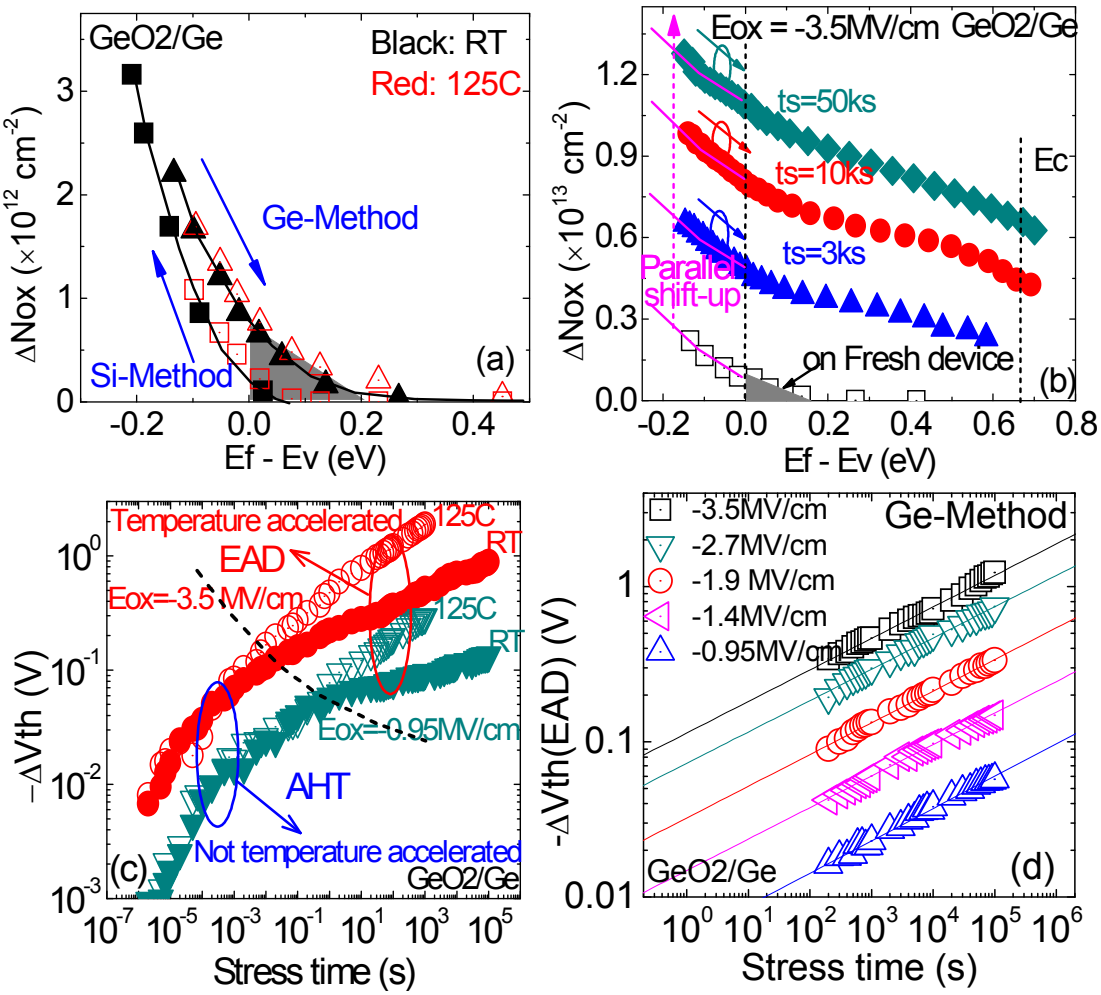

Fig. 6.4 Restoring power law extrapolation for GeO_2/Ge devices (a) A comparison of AHTs extracted using the Ge- and Si-Method. The Ge method detects a tail above Ev (Grey triangle). (b) AHTs do not increase with stress time, resulting in the marked parallel shift. (c) AHTs are filled first during stress and are temperature independent, whilst EADs are the opposite. (d) Power law is restored after removing AHT extracted with Ge-Method in (a), during which the filling time is kept short enough so that EADs are negligible.

To explore this further, a 'Ge method' is developed, which sweeps energy from low to high. The sweeping rates must satisfy two conditions: it must be slow enough to ensure AHTs are filled up and it must be fast enough to not activate the EADs. Fig. 6.4(a) shows charging near Ec is negligible, supporting that the EADs are not activated when measuring AHTs. The grey triangle confirms that AHTs exist above Ev for GeO_2/Ge, although they are absent above Si Ev. The AHTs and its 'tail' above Ev are independent of temperature (RT and 125 °C).

To support that AHTs and EADs in Ge devices are two different groups of defects, Fig. 6.4(b) shows that EADs increase with stress time, but AHTs do not, since they are 'as-grown', showing saturation marked as parallel shift-up. Temperature effect is further explored under different stress conditions (Eox = -3.5 MV/cm and -0.95 MV/cm), as shown in Fig. 6.4(c).

The initial degradation is dominated by filling AHTs, which is insensitive to temperature (from RT to 125C), supporting Fig. 6.4(a). In contrast, charging EADs is thermally accelerated and does not saturate, also shown in Fig. 6.4(b). To separate

EADs from AHTs, we obtain the saturation level of AHTs for a given stress Eox from Fig. 6.4(a) and (b). EADs are then extracted by subtracting these saturated AHTs from the total ΔVth, as shown in Fig. 6.4(d).

6.4 Restore power law and enable lifetime prediction in Ge

When EADs were extracted by evaluating AHTs with Si-method, power-law was restored (see Fig. 6.2(b)), however, the power exponent 'n' varies substantially with Eox, as shown by the symbol '▲' in Fig. 6.5(a), which prevents the reliable prediction. In contrast, when the correct amount of AHTs are determined by the Ge method and subtracted, a constant power exponent is successfully obtained for EADs, as shown by the parallel lines in Fig. 6.4(d) and the constant n in Fig. 6.5(a), demonstrating that the AHT-tail above Ev plays a crucial role. This tail does not scale with Eox and impacts more on the raw 'n' at lower Eox. After taking it into account, the variation of lifetime power exponent, m, (see Fig. 6.1(c)) disappears, which enables life time prediction, shown in Fig. 6.5(b). The method works for either RT or 125 °C. γ is extracted by the equation in the caption of Fig. 6.5. The values for all different samples are summarized in Table 6.1. A higher lifetime criterion of 350mV and 200mV are chosen for GeO_2/Ge, Si-cap/Ge (non-optimized) devices due to the high degradation level which needs further optimization, and 100mV is chosen for Si-cap/Ge (optimized) and SiON/Si devices, hereafter, for NBTI lifetime prediction.

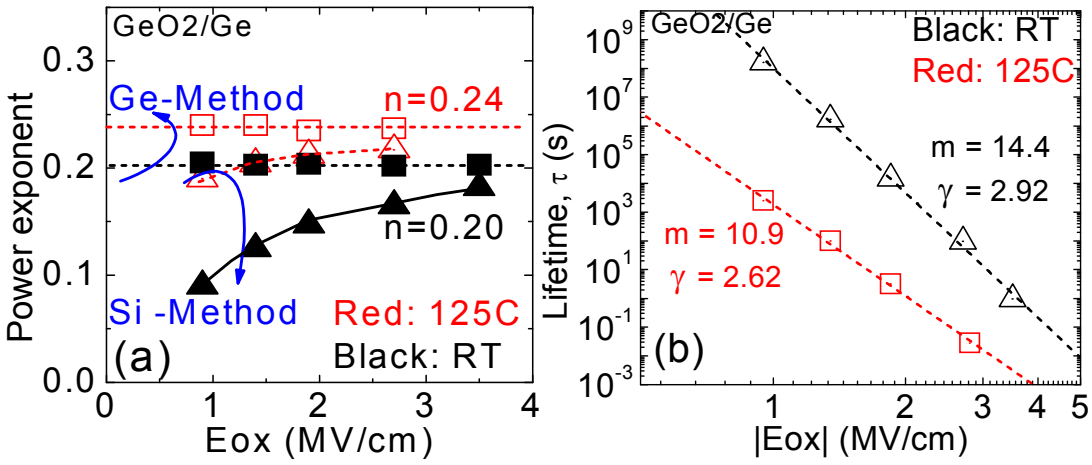

Fig. 6.5 GeO_2/Ge devices: (a) Constant time power exponents, n, are obtained at both RT and 125 °C with Ge-Method, but not with Si-Method. The impact of AHT-tail is larger at lower Eox, as it accounts for a larger percentage of total degradation. (b) Lifetime predictions are enabled at both RT and 125 °C by using the Ge-method, as a constant time-to-failure exponent, m, is restored in both cases. $m = \gamma / n$. With T increase, the reliability reduces as suggested by m & γ.

Both the generated defects (GDs) in Si devices and the EADs in Ge devices follow a power law and their similarity and differences should be explored. There are two groups of defects in both Si and Ge devices: as-grown hole traps (AHTs) and stress-changeable defects. After capturing holes, AHT change their charge status, but all other properties, such as charging time and energy levels, remain the same. For the stress-changeable defects, some other properties of the defects are also changed, in addition to the charge status. In this sense, the generated defects can be defined as the defects whose properties are changed or 'generated' during stress, in addition to charging/discharging.

For Si devices, the charging rate is changed [124] by the generation process. For Ge devices, the energy level is changed for the EADs by the generation process. Although the detailed physical processes are not known, the following speculations can be made.

In Si devices, after a precursor is converted into a GD, through bond-breaking [194] and probably followed by structure relaxation [197], the structure becomes permanently different from the precursor. After neutralization, the GD still has a different structure from the precursor, so that its recharging rate is faster than that when charged for the first time [124]. In Ge devices, activation of EADs also involves bond-breaking and is followed by structure relaxation [216], which could originate from a distribution of bond strengths [217]. The relaxed-structure, however, is repairable [218]. Following neutralization, it returns to its original precursor, so that its energy level also returns to its original one. In this sense, one may say that the Si device has the 'hard generation', while Ge device has the 'soft generation'.

6.5 Lifetime prediction in Si-cap/Ge and device optimization

6.5.1 Energy Profile of AHTs in Si-cap/Ge

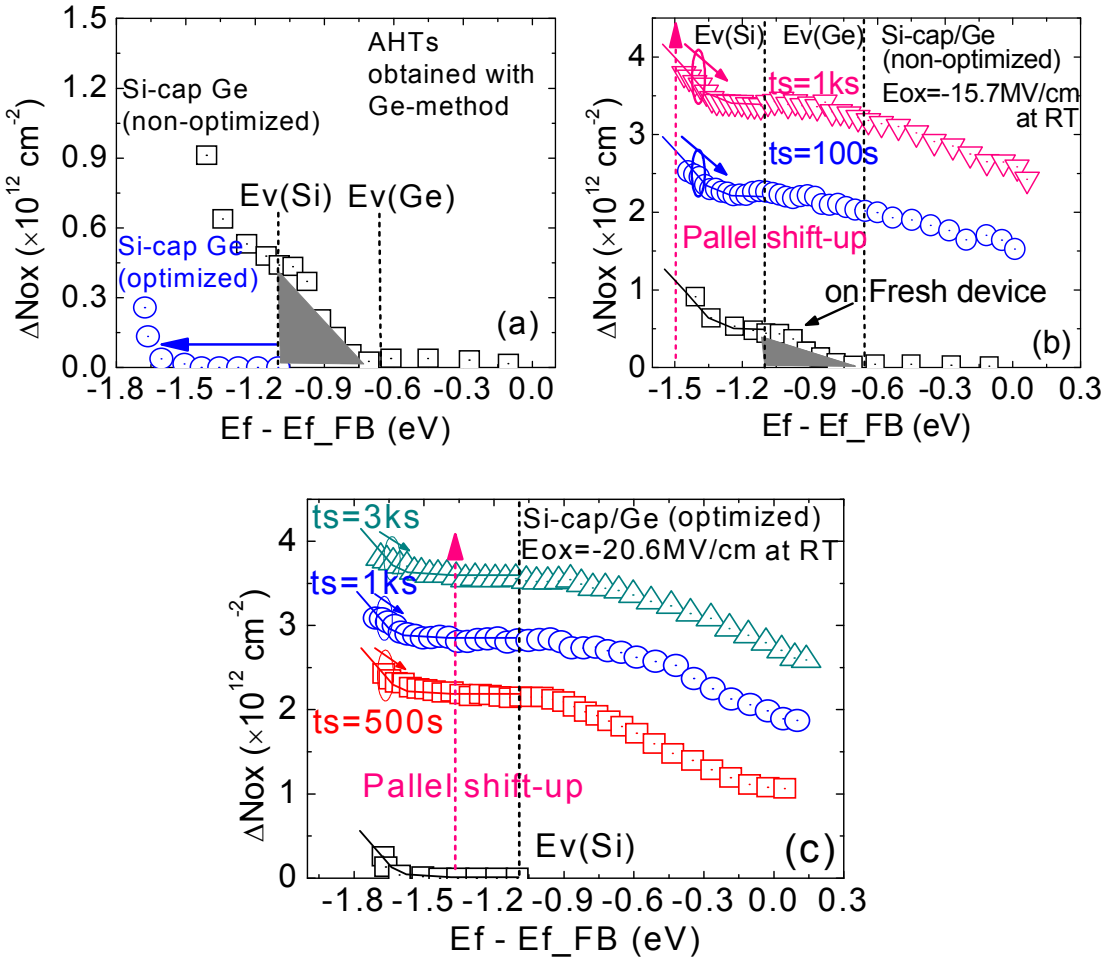

Fig. 6.6 (a) The energy profile of AHT in Si-cap/Ge (optimized) is further away (~0.4eV) from Ev than Si-cap/Ge (non-optimized). AHT tail is observable in fresh non-optimized device inside Si bandgap, but not in the optimized one. (b) Degradation of a non-optimized Si-cap/Ge device. Like GeO_2/Ge device: AHTs have a tail above Ev(Si) and do not increase with stress time. (c) Degradation of an optimized Si-cap/Ge device. Like SiON/Si device: AHTs do not have a tail above Ev and do not increase with stress time (also in the optimized thin Si-cap/Ge, not shown).

Fig. 6.6(a) compares the AHTs in optimized and non-optimized Si-cap/Ge devices obtained by Ge-method. The optimized one does not have a tail above Ev, but the non-optimized one does. The energy level of Si-cap/Ge (optimized) is further away (~0.4eV)

below Ev than that of Si-cap/Ge (non-optimized). In general, the non- and optimized Si-cap devices behave like GeO_2/Ge and Si devices, respectively. The AHTs saturate with stress time for both samples, as shown in Fig. 6.6(b) and (c).

6.5.2 Application of Ge method in Si-cap/Ge

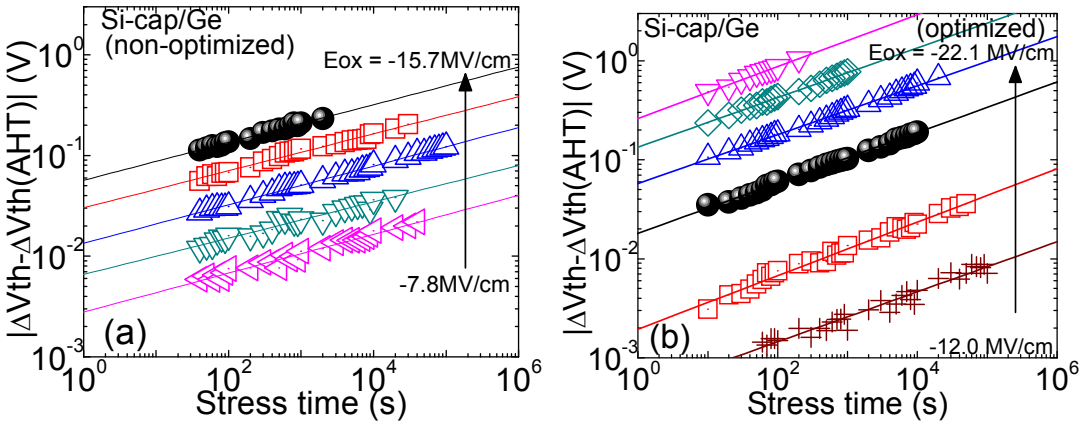

Fig. 6.7 Power law with constant time power exponent, n, is restored with Ge-Method for Si-cap/Ge (a) non-optimized and (b) optimized device. Both tests are at RT. Constant time-to-failure power exponent, m, is also restored for both cases, as shown in Fig. 6.8, enabling reliable lifetime prediction. Eox of '●' is similar for (a) and (b).

Fig. 6.7 shows that when the Ge-method is applied for the non- and optimized devices, power law was restored for both of them. The electric field is from -7.8 MV/cm to -15.7 MV/cm for non-optimized one and from -12 MV/cm to -22.1 MV/cm for optimized one. Constant time-to-failure power exponent, m, is restored for both cases, enabling reliable lifetime prediction. For the purpose of comparison, Eox of similar condition is marked out as the symbol '●', shown in Fig. 6.7 (a) and (b). Optimized one can survive much longer time than the non-optimized one, as expected.

6.5.3 Lifetime prediction of Si-cap/Ge and process optimization

The higher processing temperature (500°C) of Si-cap layer could force Ge diffusing further into/through Si-cap and the dielectrics [91], making the non-optimized one behave similarly like GeO_2/Ge. Ge–Si intermixing, caused by a Ge segregation mechanism, is strongly reduced by using different precursor at low temperatures [88, 91], for the purpose of optimization.

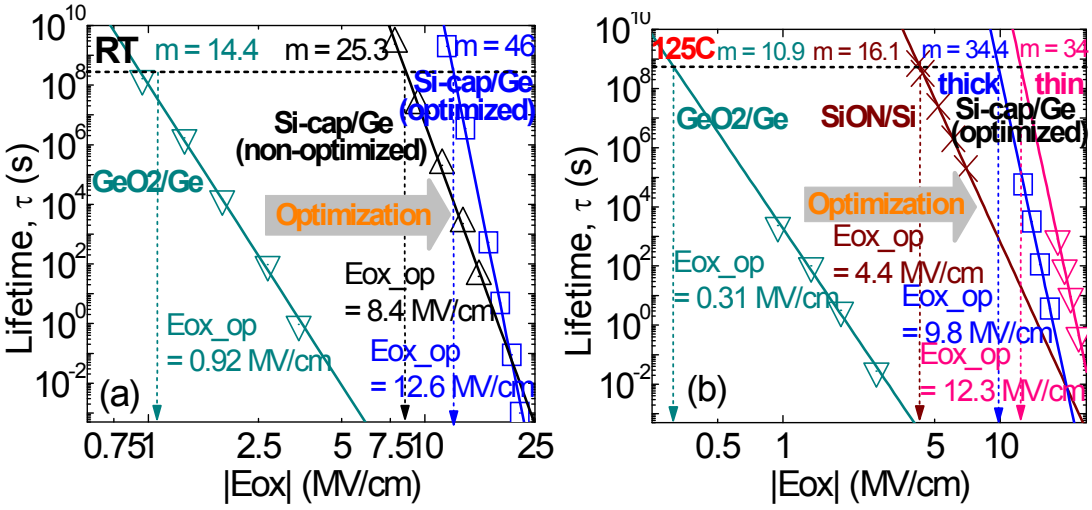

Fig. 6.8 A comparison of lifetime prediction on different CMOS processes by the new Ge-method developed in this work at (a) RT and (b) 125 °C. Si-cap/Ge MOSFETs shows superior reliability. Si-cap/Ge (optimized) shows process improvement over the non-optimized one (a). Thick and thin Si-cap (optimized) leads to a larger m & γ (Table 6. 1) and longer life time/higher maximum operational voltage than Si technology at 125 °C (b). Power law is restored in all cases, enabling process evaluation.

Fig. 6.8 compares the NBTI lifetime prediction of different devices/processes by using the new Ge-method at both RT and 125 °C. Si-cap/Ge shows superior reliability, even better than SiON/Si and the optimization is clearly needed for GeO_2/Ge, agreeing with

[10]. For the optimized thick Si-cap/Ge device, an overdrive voltage of 1.77 V (Eox = -12.6 MV/cm) can be used to keep ΔVth within 100 mV for 10 years. Both thick and thin Si-cap (optimized) lead to a larger m & γ (see Table 6.1) and longer life time/higher maximum operational voltage than Si technology at 125 °C.

Power law lifetime prediction is restored for all three technologies, enabling CMOS device/process evaluation under DC stress conditions. The applicability of this technique in GeO_2/Ge and Si-cap/Ge devices under AC stress conditions will be examined in the next two sections.

6.6 Initial investigation of characteristic time of defects in GeO_2/Ge devices and its impact on NBTI under AC stress conditions

It has been discussed in previous sections that defects behave differently in Si and Ge devices [219]. Based on the EAD model, lifetime has been successfully predicted for both GeO_2/Ge and Si-cap/Ge devices under DC stress conditions. The impact of defect differences on the AC NBTI in Ge MOSFETs has not been investigated yet, which is required for device process optimization and circuit design in future.

Extensive studies have been carried out on the NBTI relaxation and the lifetime improvement with AC NBTI in Si MOSFETs [220-222]. Existing methodologies [117, 178, 223] rely on specific physical-based models along with multiple parameters (e.g.

hole trapping/detrapping models [117] and hydrogen diffusion/reaction model [178]) and there is no agreement on the responsible physical mechanism yet [224]. The AC frequency and duty factor behavior in Si devices have been characterized by understanding the impact of different types of traps on oxides [94, 99] and a three-parameter As-grown-Generation (A-G) model has been proposed to reliably predict the AC aging and its frequency/duty factor dependence [225]. This will be reviewed in Section 6.6.1 first and preliminary investigations on its applicability in GeO_2/Ge devices will then be carried out in the remaining sub-sections.

6.6.1 Measurement procedure

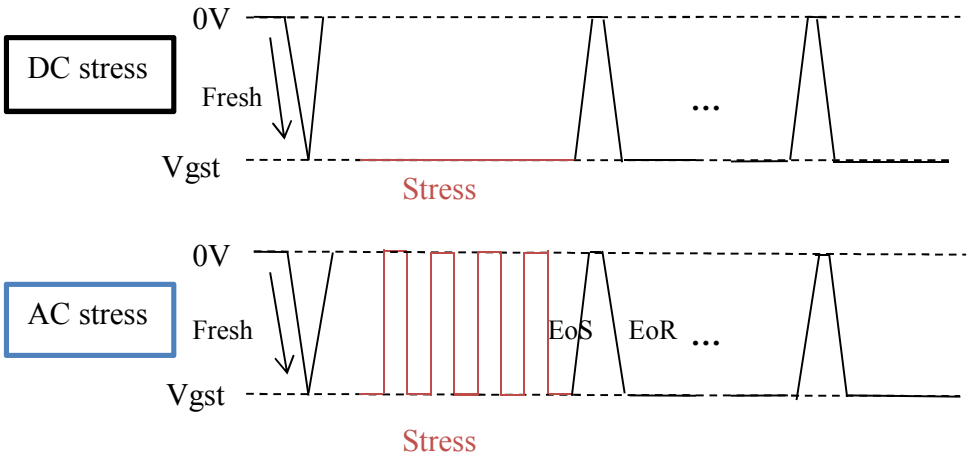

Fig. 6.9 The Vg waveform and pulse measurement procedure for DC and AC NBTI. For AC stress, the ΔVth is measured on two edges: one from zero to Vgst as "End-of-Recovery (EoR)" and the opposite one as "End-of-Stress (EoS)".

When AC NBTI was characterized by slow measurement techniques, the accuracy was affected by the fast trapping/detrapping [220, 222]. In this section, Pulse-IV measurement with 5μs was used to record the fresh reference Id-Vg and also the Id-Vg

curves measured during DC and AC NBTI stress. The measurement procedure under DC and AC stress is given in Fig. 6.9. For AC stress, the ΔVth are measured on two edges: one from zero to Vgst as "End-of-Recovery (EoR)" and the opposite one as "End-of-Stress (EoS)".

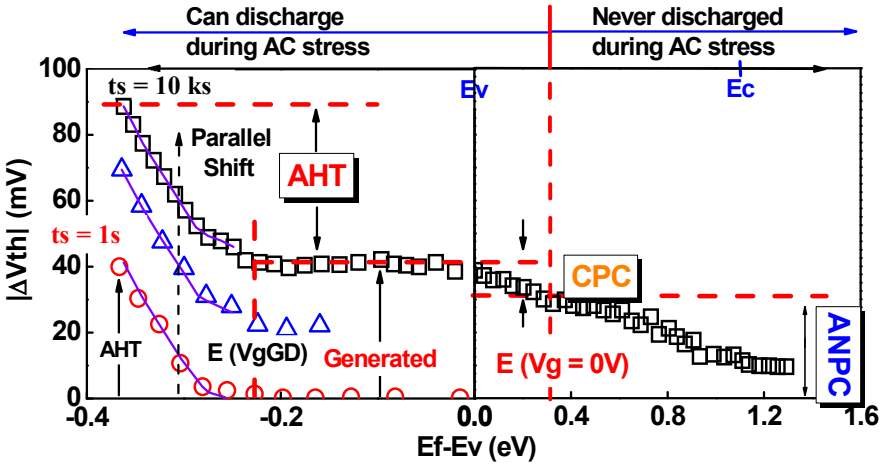

Fig. 6.10 Defects separation based on their energy location in SiON/Si device. As-grown hole traps (AHT) are below E(VgGD) and the generated defects (GD) are above E(VgGD). GD is further separated into CPC between E(VgGD) and E(Vg=0V) and ANPC above E(Vg=0). For unipolar AC, ANPC never discharges [225].

Based on their energy location, defects have been separated as As-grown hole traps (AHT) that are below E(VgGD) and the generated defects (GD) that are above E(VgGD). GD is further separated into CPC between E(VgGD) and E(Vg=0V) and ANPC above E(Vg=0). For unipolar AC, ANPC never discharges, as shown in Fig. 6.10.

6.6.2 Impact of stress bias and temperature on AC NBTI behaviors in GeO_2/Ge

The typical AC Frequency and Duty Factor dependences at RT in GeO_2/Ge devices are shown in Fig. 6.11.

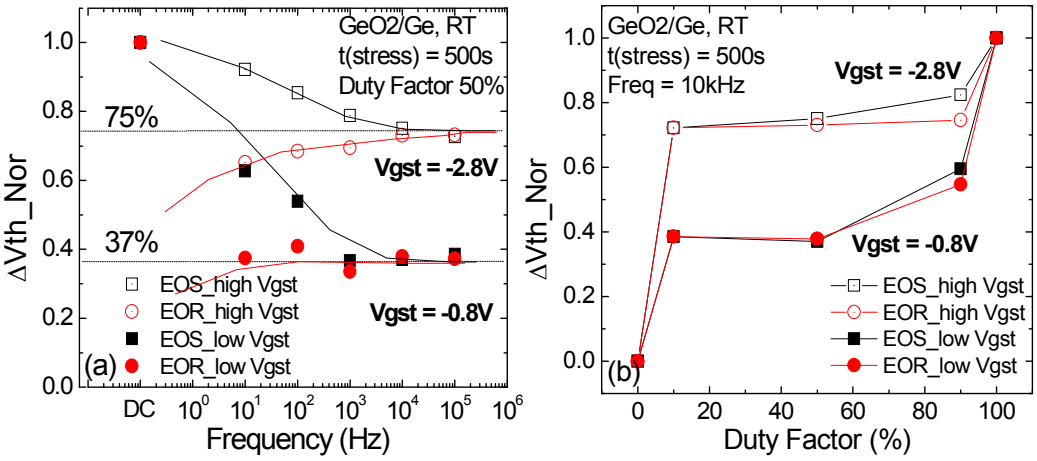

Fig. 6.11 A comparison of (a) Frequency dependence and (b) Duty Factor dependence under different Vg bias in GeO_2/Ge devices. Stress was carried out under either high Vgst = -2.8 V or low Vgst = -0.8 V for 500 sec at RT. AC stress measurement is normalized by the corresponding degradation under DC condition with same effective stress time. The black square symbol represents End of Stress (EOS) and red circle End of Recovery (EOR).

The AHTs have the lower energy and are easier to recover and are mainly responsible for the reduction of AC NBTI from its DC level. As the frequency becomes sufficiently high (>10 kHz), however, the NBTI does not reduce further for higher frequency, resulting in a plateaus in Fig. 6.11. This indicates that the contribution of AHTs is already reduced to zero at 10 kHz. The good agreement between NBTI at EoS and EoR suggests that EADs recovers little at a frequency of 10 kHz, which will be further supported later.

The NBTI(>10kHz)/NBTI(DC) is highly dependent on the stress bias, Vg. Stress was carried out under either high Vgst = -2.8 V or low Vgst = -0.8 V for 500 sec at RT. The degradation under AC stress is normalized by the corresponding degradation under DC stress condition for the same effective stress time. Clearly, after the high Vg stress, the relative percentage at high frequencies is increased dramatically to about 75%, while it is only about 37% for the low Vg stress.

Fig. 6.12 shows the impacts of temperature on (a) Frequency dependence and (b) Duty Factor dependence in GeO_2/Ge devices. In both cases, stress was carried out under high Vg_ov=|Vg-Vth0|= -2.35V for 500 sec under different temperatures, RT and 125 °C. The same percentage of traps contributes to the degradation of EOS at 10 kHz. For low frequency, more neutralization is observed from the EOR at 125 °C than at RT.

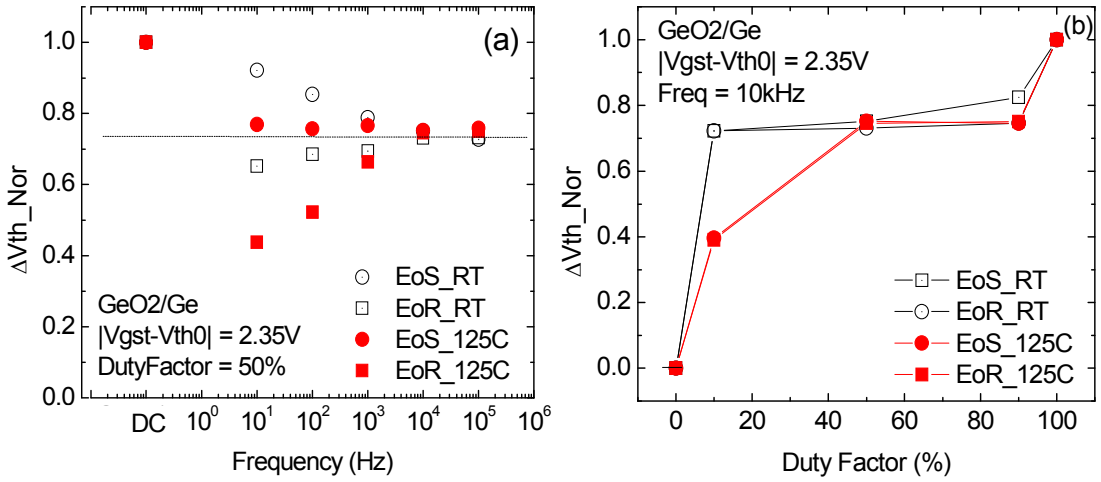

Fig. 6.12 A comparison of (a) Frequency dependence and (b) Duty Factor dependence under different Temperature in GeO_2/Ge devices. Stress was carried out under high Vg_ov=|Vg-Vth0|= 2.35V for 500sec at both RT and 125 °C. AC stress measurement is normalized by the corresponding degradation under DC condition with same effective stress time.

In order to understand the AC NBTI behavior, the responsible defects are further examined. Fig. 6.13 shows the impacts of Vg stress bias and temperature on the defect energy distribution in GeO_2/Ge. As-grown hole traps (AHT) and the Energy alternating defects (EAD) are separated and determined by the Ge-method, as described in Section 6.3.

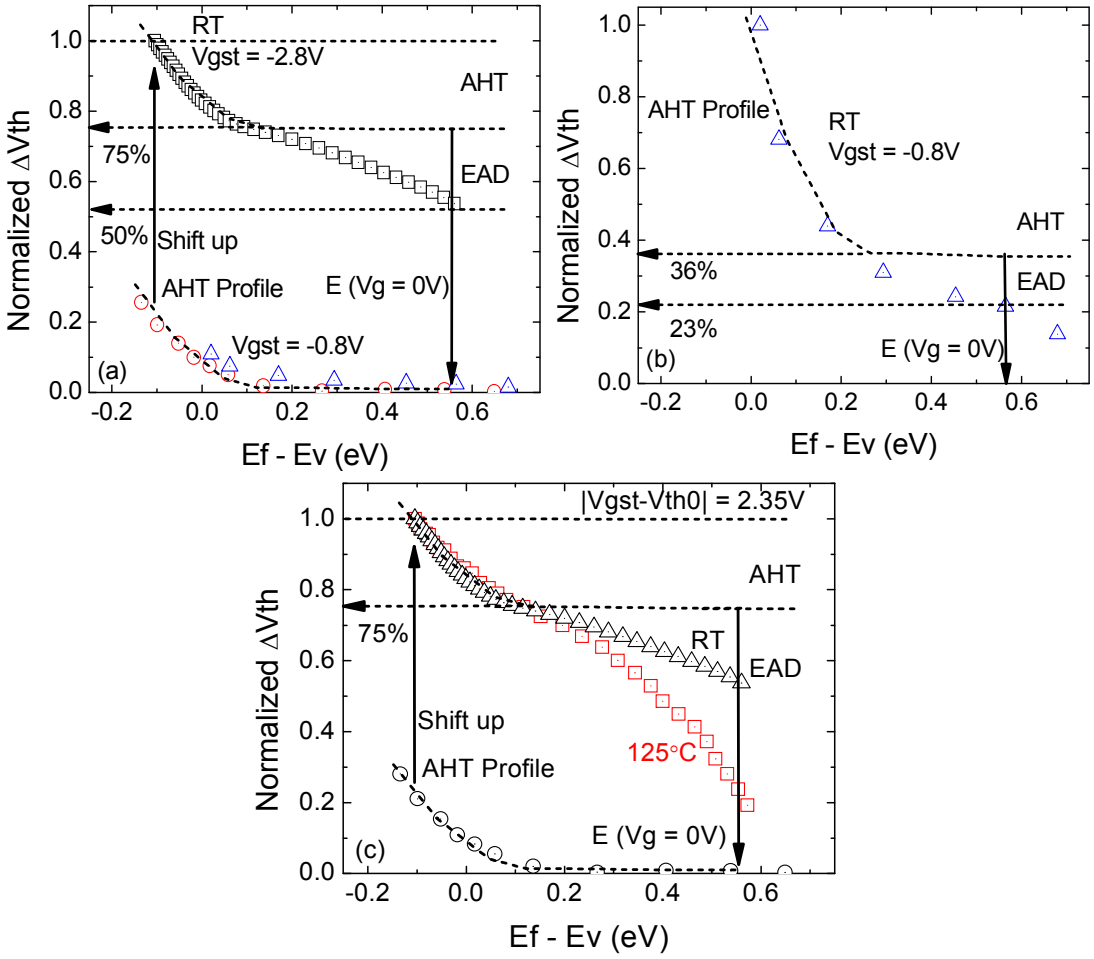

Fig. 6.13 The impact of Vg stress bias and temperature on the defects based on the energy distribution in GeO_2/Ge. As-grown hole traps (AHT) and the Energy alternating defects (EAD) are separated and determined by Ge-method. Normalized (a) defects separation (b) Vgst = -0.8V (c) comparison at RT and 125 °C. E(Vg = 0V) is marked for unipolar AC stress. EAD is rechargeable during AC stress.

As shown in Figs. 6.13(a) and (b), at RT, EAD is 75% and 35% of the total defects for high and low Vgst, respectively. This agrees well with the ratio of NBTI(10 kHz)/NBTI(DC) at both high and low Vgst in Fig. 6.11(a). It strongly supports that, at 10 kHz, AHTs contribute little and EADs are responsible for NBTI. In other words, EADs recovery is negligible at frequency > 10 kHz.

When frequency reduces from 10 kHz, Fig. 6.12(a) shows that NBTI (EoR) reduces, indicating that EADs can partially recover. To support this, the EADs level at E(Vg=0) was marked out in Fig. 6.13(c), which represents the EADs level when discharge time is long enough for the discharge to reach completion. 1s is used, during which the main discharge completed, as shown in Fig. 5.6(b). It clearly shows that EADs recovery can be substantial under Vg=0. Moreover, Fig. 6.13(c) shows that the EADs recovery is thermally accelerated, agreeing well with the thermally enhanced reduction of NBTI (EoR) for lower frequency.

6.6.3 Charging/Discharging Characteristic time of AHTs

A comparison of recovery in GeO_2/Ge after different stress conditions is shown in Fig. 6.14. After stress under the high Vgst at RT, the initial fast recovery of AHT (75% remaining) is followed by a slower recovery of EAD to 50% of the total. The overall recovery is slower than that under the low Vgst. It confirms that at higher Vgst, there are more EADs compared to that at the lower Vg condition. At 125 °C, it also shows 75% remaining after the initial AHT fast recovery, which agrees with Fig. 6.13(c). Under low

Vg at RT, 23% is left after recovery, agreeing with Fig. 6.13(b), however, the neutralization of AHT is not as obvious as the high Vg stress conditions.

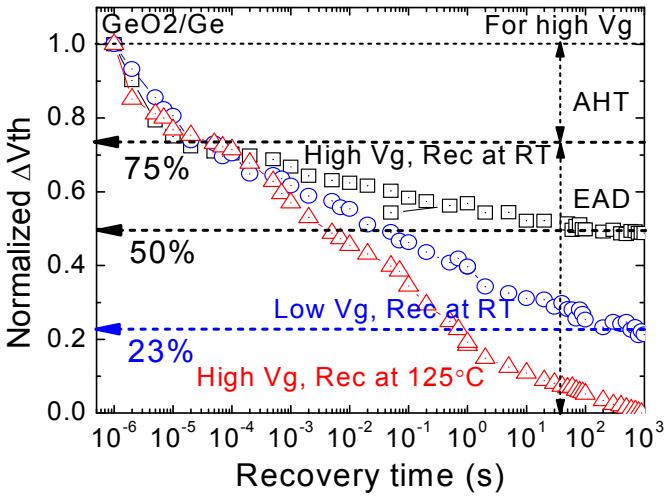

Fig. 6.14 Comparison of recovery behavior in GeO_2/Ge devices, with various conditions: high Vgst at RT, low Vgst at RT and high Vgst at 125 °C. AHT and EAD for high Vgst are marked out.

The amount of defects that remain charged under AC stress conditions depend on the ratio of charge and discharge time, t*_ch/t*_disch of each individual type of defects. When the ratio becomes higher, fewer defects are charged at the end of discharge/recovery. Characteristic times for charging (t*_ch) and discharging (t*_disch) are defined as the time reaching 63% (37%) of the maximum (minimum) value according to the RC circuit theory [226]. As an initial analysis, the charging and discharging characteristics of AHT was evaluated in Fig. 6.15. It is shown that t*_ch/t*_disch of AHT in GeO_2/Ge is around 60 and it is insensitive to temperature (RT / 125°C). Therefore, the AHT will be discharged during the AC stress measurement at high frequency, while the EADs remain charged, dominating the NBTI in GeO_2/Ge

devices, which corresponds to the GD in SiON/Si devices. Further understanding and investigation is on-going, as time constant could be more than single.

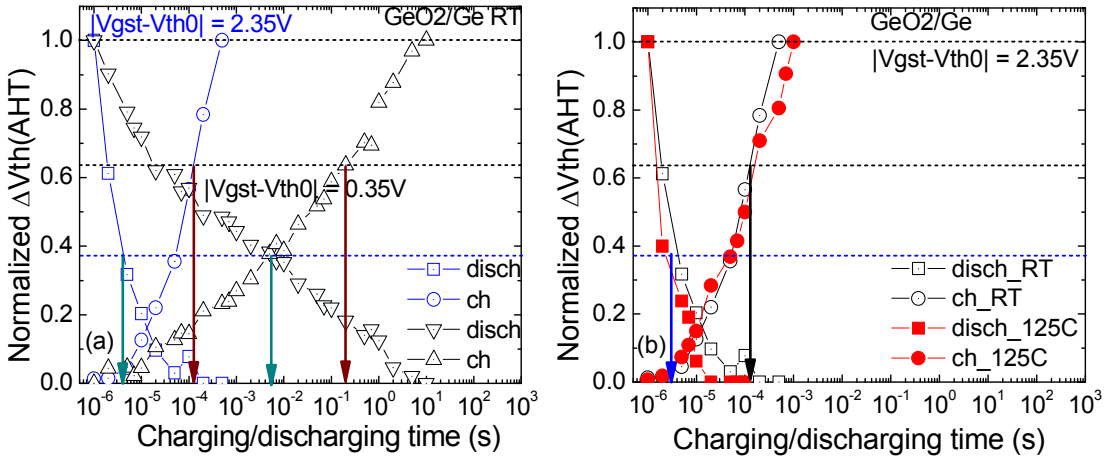

Fig. 6.15 Comparison of charging/discharging time of AHT (a) after high Vg stress and low Vg stress, and (b) at RT and 125 °C. The data gives t*_ch/t*_disch ~ 60 and the AHT is insensitive to temperature.

6.7 Defects properties and initial understanding of AC behavior in Si-cap/Ge devices

6.7.1 Frequency and Duty Factor Characteristics

The typical AC Frequency and Duty Factor dependences in Si-cap/Ge devices at 125 °C are shown in Fig. 6.16. The AC/DC ratio is similar to that in GeO_2/Ge devices shown in Section 6.6. In the following sub-sections the defects in Si-cap devices will be examined in order to provide preliminary explanations for this phenomenon.

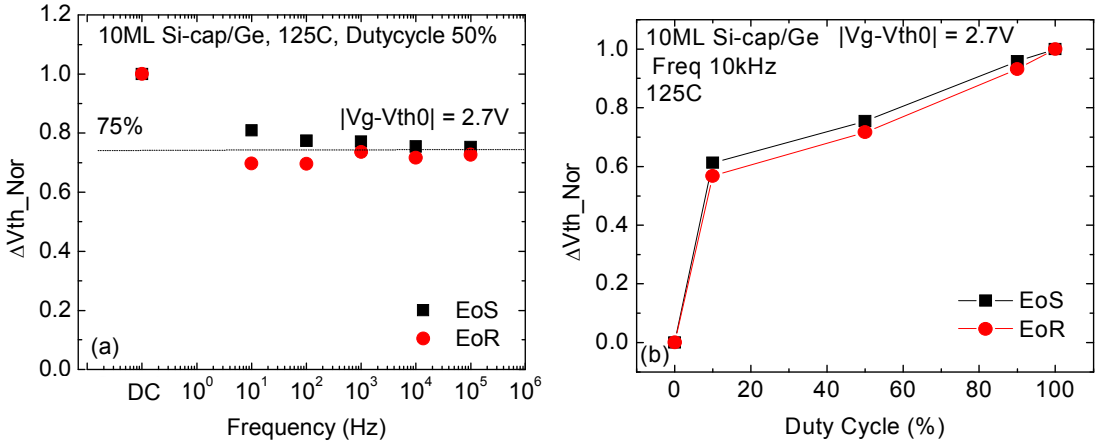

Fig. 6.16 Typical (a) Frequency and (b) Duty Factor dependence in 10ML Si-cap/Ge devices. Stress was carried out under high |Vg-Vth0| = 2.7V for 500sec at 125 °C. AC stress measurement is normalized by the corresponding stress under DC condition with same effective stress time. The black square symbol represents End of Stress (EOS) and red circle End of Recovery (EOR).

6.7.2 Defects Properties in Si-cap/Ge devices

Figs. 6.17(a) and (b) show the recovery and charging behavior after the stress under |Vg-Vth0|=2.7 V at 125 °C in Si-cap/Ge, respectively. The recovery clearly shows a fast initial recovery before 10 ms and a 2nd recovery period after around 1 sec. A 2nd stress was carried out with the same stress condition as the 1st one. The comparison of the 2nd stress with the 1st stress after shifting down the 2nd one shows that the recharge overlaps with the 1st charge within the first several milliseconds, followed by a slow recharge process starting at around a few seconds. It indicates that the AHTs were refilled initially and then other generated defects were refilled slowly as marked in Fig. 6.17(b).

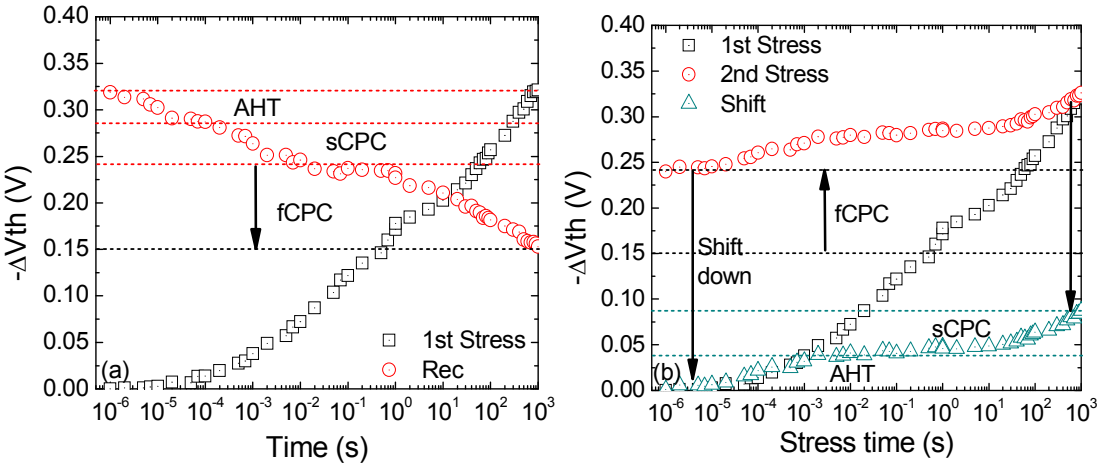

Fig. 6.17 (a) Recovery behavior after stress under |Vg-Vth0|=2.7V at 125 °C (b) 2nd stress was carried out after the 1st stress and recovery for 1ksec in 10ML Si-cap/Ge device. Triangle symbol represents the same data after parallel shift down.

A sudden jump is observed when the 2nd stress is applied for only around a few μs, which means a fast recharge of the generated defects. The slow and fast rechargeable generated defects are denoted as 'sCPC' and 'fCPC', respectively, as marked in Fig. 6.17(b).

AHTs in Si-cap/Ge devices have been determined by the Ge method as shown in Section 6.6. Fig. 6.18(a) shows that AHTs and sCPCs are discharged at Vg_rec=1V for the particular Ge samples, equivalent to the Vg_rec = 0V for Si devices. Defects that cannot be discharged until this energy level are ANPCs. During the recharge that sweeps back from high to low energy, sCPC can be recharged near Ge Ev. AHTs and fCPCs cannot be recharged until reaching the stress bias. The amount of sCPC is the same at different measurement temperatures as shown in Fig. 6.17(b).

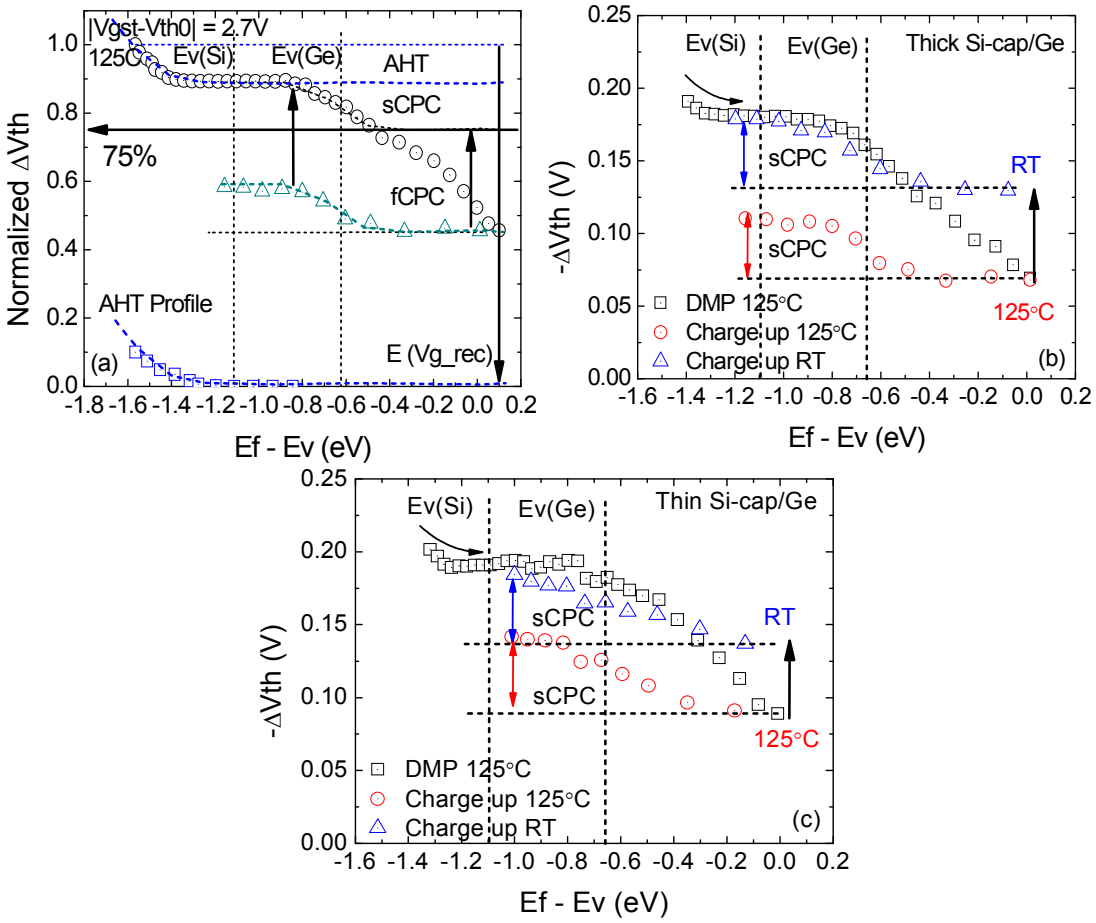

Fig. 6.18 The defects separation based on the energy distribution in 10ML Si-cap/Ge. (a) As-grown hole traps (AHT) are determined by Ge-method. GD is further separated as sCPC, 'fCPC' and ANPC. E(Vg_rec=+1 V) is marked for unipolar AC stress. sCPC is rechargeable during AC stress. (b) The same sCPC at different measurement temperature. Fast recharge after lowering the measurement temperature from 125 °C to RT. Thick Si-cap/Ge (c) thinner Si-cap/Ge.

Defects of fCPC in Si-cap/Ge show the same properties as fCPC in SiON/Si, in terms of short recharging time, as shown in Fig. 6.17(b). Fast recharge of fCPCs is also observed at Ef under flat band condition after lowering the measurement temperature from 125 °C to RT, as shown in Fig. 6.18(b). However, it cannot be recharged under low Vg bias in both thick and thin Si-cap/Ge devices, as shown in Fig. 6.18(a). In this respect, it

combines the behavior of both EAD in GeO_2/Ge and fCPC in Si-cap/Ge. Detailed investigation on these defects is on-going. The charging and discharging characteristic times of different defects will be investigated and the impacts on the AC frequency and duty factor dependence will be examined in the next sub-section.

6.7.3 Impact of Charging/Discharging Characteristic time on AC behavior

The charging and discharging characteristics of AHT in 10ML Si-cap/Ge was evaluated in Fig. 6.19. It is shown that t*_ch/t*_disch of AHT in Si-cap/Ge is around 60. Therefore, the AHT will be discharged during the AC stress measurement.

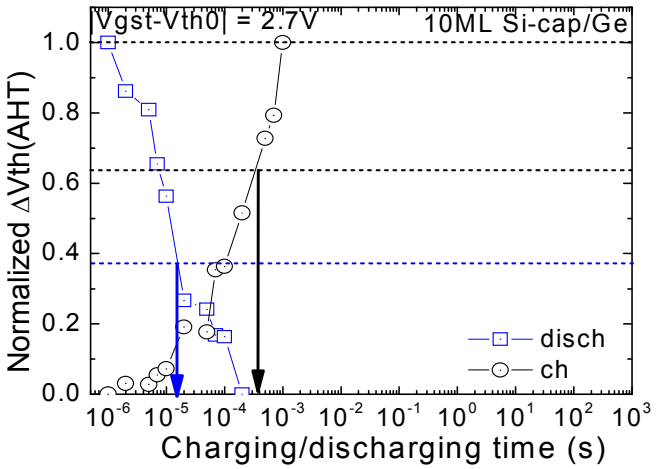

Fig. 6.19 Charging/discharging time of AHT in 10 ML Si-cap/Ge. The data gives t*_ch/t*_disch ~ 60.

As an initial analysis, Fig. 6.20 shows the charging and discharging characteristics of total CPC and sCPC in 10ML Si-cap/Ge. The t*_ch/t*_disch is around 0.001 for the total CPC and ~ 100000 for sCPC respectively. The ratio reduces significantly for the total CPC due to contribution of the large percentage of fCPC, which are charged within

a few μs and contribute to the degradation under AC stress. This is also the reason for the large AC/DC ratio observed in AC behaviors as shown in Fig. 6.16.

Therefore, the AHT and sCPC is dischargeable during the AC stress, while the 'fCPC' and ANPC-like defects contribute to the AC frequency and duty factor dependence of NBTI in Si-cap/Ge devices. As shown in Fig. 6.18(a), after the AHT and sCPC discharged, there is 75% of defects remaining charged, which agrees with the AC/DC ratio in Fig. 6.16. Further understanding and investigation is on-going, as time constant could be more than single.

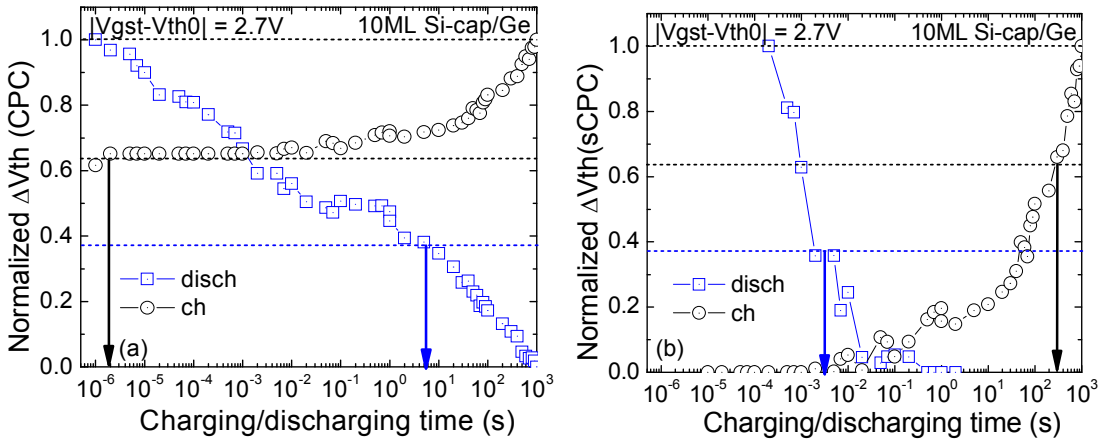

Fig. 6.20 Charging/discharging time of (a) total CPC and (b) sCPC in 10 ML Si-cap/Ge. The data gives t*_ch/t*_disch ~ 5×10^{-7} for total CPC and ~ 1×10^{5} for sCPC.

6.8 Summary

In this chapter, it is demonstrated that the defects behave differently in Ge and Si devices, in terms of recovery, 2nd stress after recovery, energy level of recharge behavior, and

temperature dependence. It is found that there are energy alternating defects (EAD) in Ge, but not in Si devices. The as-grown hole traps have a tail above Ev for Ge, but not for Si devices. EAD is separated from AHT, in order to restore power law for NBTI kinetics with a constant power exponent. The developed Ge method enables lifetime prediction for Ge devices, which is also applicable in Si-cap/Ge devices. NBTI Lifetime is predicted with power law extrapolation for three CMOS technologies, which assists in further process/device optimization. Si-cap/Ge shows superior reliability to SiON/Si, while GeO_2/Ge needs further optimization. Initial investigation is carried out on the characteristic time of defects in Ge devices and its impact on AC f requency and duty factor dependence, which is required for circuit design. Further investigation and understanding is on-going.

7 Summary and Future work

7.1 Summary

The work in this project has been focused on the performance, defects and reliability characterization of Germanium MOSFETs. Chapter 1 introduced the research concerns, rationale, and objectives of this research project. Originality and novelty of this work were pointed out. Chapter 2 reviewed the CMOS technology and challenges in the advanced Germanium MOSFETs. Surface passivation and defects responsible for them were explained for two main Ge structure devices. Reliability issues and NBTI models are also reviewed. Chapter 3 described the experimental facilities and characterization techniques used in this work. Limitations of conventional techniques and advantages of advanced pulsed techniques are discussed for Ge characterization. The main research work was divided into the following three chapters: Chapter 4 on the initial NBTI characterization and defects properties in Ge MOSFETs; Chapter 5 on the study of hole trap energy distribution by Discharge-based Multi-pulse (DMP) Technique; and Chapter 6 on the Investigation of defects behavior and lifetime prediction method for Ge MOSFETs. The summary for each chapter is given in what follows:

7.1.1 Initial NBTI characterization and defects properties in Ge MOSFETs

The NBTI in Ge devices is compared with that in Si devices. It is found out that, similar to Si samples, NBTI is activated both electrically and thermally for $Ge/GeO_2/Al_2O_3$. There are a number of important differences with Si samples and the new findings include: (i) The time exponent is not constant for different stress biases/fields when measured with either slow DC or pulse technique, which makes the conventional Vg acceleration lifetime prediction technique of Si samples inapplicable to the $Ge/GeO_2/Al_2O_3$; (ii) ΔVth is substantially less sensitive to measurement time; (iii) The neutralization can be nearly 100% under a temperature as low as 150 °C, in contrast with the 400 °C needed by Si sample; (iv) Defect losses were not observed for $Ge/GeO_2/Al_2O_3$.

On defects, early works reported that NBTI induced three types of positive charges in SiO_2 or SiON: AHT (As-grown Hole Trap), ANPC (Anti-Neutralization Positive Charge), and CPC (Cyclic Positive Charge). It is found that the positive charges in GeO_2/Al_2O_3 on Ge dominate the NBTI, but they do not follow the same model as that for PCs in SiON/Si. An energy-alternating model has been proposed: the energy levels have a spread for neutral hole traps below Ev, lift up after charging, and return below Ev following neutralization.

7.1.2 Energy Distribution of Hole Traps in Ge MOEFETs

The DMP technique can probe the energy distribution of positive charges (PCs) in Si device and it is adapted to obtain the detailed information of hole traps for Ge MOSFETs. Disturbance is negligible from the trapping/detrapping during the measurement of 5μs. Energy distribution of PCs in the $Al_2O_3/GeO_2/Ge$ gate stack was characterized. The contributions of interface states and effects of stress time were studied.

It is found that ΔVth can vary significantly when Ef was swept from below Ev to above Ec at the Ge interface. The energy density distribution has three features: a rapid rise when moving below Ev at the interface, relatively low between Ev and Ec, and a peak near Ec. The below- and above-Ev PCs have different dependences on stress time: the charging of below-Ev PCs is rapid and saturates, while it is slower and does not saturate for the above-Ev PCs. The density can reach 10^{13} $cm^{-2}eV^{-1}$ below Ev and 20% of |Vg|-increases will be screened by these PCs.

Simulation results showed quantization effect causes a deviation of the ground state energy level from the classical Ev, making it possible for DMP technique sweeping Ef by several hundreds of meV below the classical Ev. Only a marginal Fermi level pinning effect is found on the Ef-Ev for 2.35 nm EOT Si and Ge MOSFETs, after an introduction of defects in the order of $10^{12} \sim 10^{13}$ $cm^{-2}eV^{-1}$. The good accuracy was obtained with a discharge voltage step as small as 0.05 V. Although the energy distribution does not give spatial information of positive charges, the areal density is

widely used and provides the PC density at a given surface potential needed for simulating the NBTI impact on devices and circuits in the future.

It is further verified that the defects in Ge devices are different in terms of the energy level by the DMP technique. After charging, the energy level of the defect moves upwards, when compared with that for pre-charging. The important point here is that, for the $Ge/GeO_2/Al_2O_3$, this charging-induced energy level change is much larger than that for the Si sample. However, for the positive charges above Ge Ec, after neutralization, they fell well below Ec. This energy-alternating can explain the different behavior of positive charges between $Ge/GeO_2/Al_2O_3$ and Si samples satisfactorily, which further support the proposed energy-alternating model.

7.1.3 Investigation of defects behavior and enabling NBTI lifetime prediction in Ge pMOSFETs

NBTI is regarded as a severe reliability issue for scaled MOSFETs. Traditional lifetime prediction method is invalid and new pulsed technique based lifetime prediction method does not work for Ge MOSFETs. It is further clarified that the defects behave differently in Ge and Si devices from the view of trap energy location, in order to develop new lifetime prediction method for Ge MOSFETs.

It is found out that Ge MOSFETs are different from Si in several respects, including 2^{nd} stress after recovery, energy level of recharge behavior, and temperature dependence. There are energy alternating defects (EAD) in Ge, but not in Si devices. The as-grown

hole traps have a tail above Ev for Ge, but not Si devices. EAD is separated from AHT, in order to restore power law of NBTI kinetics with a constant power exponent. The developed Ge method enables lifetime prediction for Ge devices, which is applicable in Si-cap/Ge devices as well.

NBTI lifetime is predicted with power law extrapolation in three CMOS technologies, which assists in further process/device optimization. Si-cap/Ge shows superior reliability to SiON/Si, while GeO_2/Ge needs further optimization. Initial investigation is also carried out on the characteristic time of defects in Ge devices and its impact on AC NBTI.

7.2 Future work

This thesis reported the performance, defects properties, and NBTI lifetime prediction of advanced germanium MOSFETs, as compared to Si MOSFETs. Several other topics are of great interest and can be further investigated in future research, which are discussed as follows.

Duty cycle, frequency behavior, and AC stress lifetime prediction

Initial investigation shows different AC behavior of NBTI in Germanium MOSFETs, in terms of duty cycle and frequency characteristics. The impact of defects is evaluated preliminarily. Energy alternating defect model explained the key differences

successfully, based on which power law was restored and DC stress lifetime prediction was achieved. It is interesting to further understand the AC NBTI based on the defects properties and to achieve the lifetime prediction under AC stress condition in Ge MOSFETs.

Electron trapping in Ge nMOSFETs

The state-of-the-art Si-cap/Ge has superior NBTI reliability even with respect to Si pMOSFETs, although GeO_2/Ge needs further optimization. The challenges are moving toward the Ge and III-V nMOSFETs. A question is what the key factor preventing the current technology from good reliability of Ge nMOSFETs is. The DMP technology can be used to enhance the understanding by characterizing the energy distribution of electron traps in germanium device and comparison can be made with Si devices. It is desirable to know the energy location in order to optimize the future process.

The interface states beyond band gap and their impact on mobility

The energy profile of interface states estimated is generally extracted from the improved charge pumping or conductance technique for Ge, which required low temperature measurement. Therefore, it is one of the challenges to use a simpler method to extract the total interface states for germanium and other high mobility semiconductor devices. Very Low Frequency Capacitance Voltage (C-V) technique can achieve measurement at frequency as low as 0.1Hz, which is able to capture both fast and slow interface traps.

The interface states can be extracted not only within Ge bandgap, but along the whole energy range by using the experimental and theoretical C-V curves.

Future work is needed to improve the accuracy of low frequency measurement. Also, this method requires careful theoretical curve calibration with consideration of Fermi Dirac distribution by using Synopsis simulation software. The properties of interface states beyond band gap can be further explored to evaluate the impact on the mobility. Mechanism of mobility degradation on Ge can be further studied in future.

Time-dependent variability in nanometer Ge MOSFETs

As the MOSFET's downscaling continues, device variability becomes a major challenge for circuit design studies in Si nanometer devices. Time-dependent variability of driving current has been studied in Si devices, which is relevant to the operation of digital gates. As the candidates of future technology, Ge devices will have the same issue. The impact of variability in Ge devices on circuit operation should be investigated on nm-scale samples.

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List of Publications

1. **J. Ma**, W. Zhang, J. F. Zhang, B. Benbakhti, Z. Ji, J. Mitard, J. Franco, B. Kaczer, and G. Groeseneken, "NBTI of Ge pMOSFETs: understanding defects and enabling lifetime prediction," in *IEEE IEDM Tech. Dig.* (Orally presented in SFO, CA, US, December 2014)

2. **J. Ma**, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, X. F. Zheng, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. R. Chalker, "Characterization of Negative-Bias Temperature Instability of Ge MOSFETs withGeO_2/Al_2O_3 Stack," *IEEE Trans. Electron Devices,* vol.61, no. 5, pp. 1307-1315, May. 2014.

3. **J. Ma**, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. Chalker, "Energy distribution of positive charges in Al_2O_3/GeO_2/Ge pMOSFETs," *IEEE Electron Device Lett.* vol. 35, no. 2, pp. 160-162, Feb. 2014.

4. **J. Ma**, J. F. Zhang, Z. Ji, B. Benbakhti, M. Duan, W. Zhang, X. F. Zheng, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. Chalker, "Towards understanding hole traps and NBTI of $Ge/GeO_2/Al_2O_3$ structure," in Conference of "Insulating Films on Semiconductors", Krakow, Poland, 2013.

5. **J. Ma**, W. Zhang, J. F. Zhang, B. Benbakhti, Z. Ji, J. Franco, J. Mitard, L. Witters, N. Collaert and G. Groeseneken, "AC NBTI of Ge pMOSFETs: Impact of Energy Alternating Defects on Lifetime Prediction," *submitted to IEEE VLSI Technology(VLSIT), 2015.*

6. Z. Ji, S. F. W. M. Hatta, J. F. Zhang, **J. G. Ma**, W. Zhang, N. Soin, B. Kaczer, S. De Gendt and G. Groeseneken, "Negative Bias Temperature Instability Lifetime Prediction: Problems and Solutions," in *IEEE IEDM Tech. Dig.* pp. 15.6.1 - 15.6.4, Dec. 2013.

7. M. Duan, J. F. Zhang, Z. Ji, **J. G. Ma**, W. Zhang, B. Kaczer, T. Schram, R. Ritzenthaler, G. Groeseneken, and A. Asenov, "Key issues and techniques for characterizing Time-dependent Device-to-Device Variation of SRAM," in *IEEE IEDM Tech. Dig.* pp. 31.3.1- 31.3.4, Dec. 2013.