Hot carrier aging of nano-meter devices

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Abstract
As the device size downscales, hot carrier aging (HCA) scales up and remerges as a major challenge to the reliability of modern CMOS technologies. The conventional method for predicting the HCA device lifetime is based on a power law kinetics and critically depends on the accuracy of the time power exponent, n. In this work, we study how to extract the n accurately. It will be shown that the widely used forward saturation current degradation gives erroneous n, because of the channel pinch-off. To reduce the test time, it will be demonstrated that the voltage step stress technique is applicable to HCA. The accuracy of the extracted HCA model will be verified against independently measured test data.

1. Introduction

In 1980s, device sizes were scaled down, but the operation voltage was maintained at 5 V. This led to an increase of electrical field within devices. The high field accelerates electrons and makes them energetic, i.e. 'hot', near the drain junction. When these hot carriers bombard devices, they cause damage and the hot carrier aging (HCA) was the lifetime-limiting degradation mechanism [1,2].

Since 1990s, the operation voltage has been reduced for smaller devices and negative bias temperature instability (NBTI) has replaced HCA as the lifetime limiting mechanism [3-6]. As the downscaling of operation bias is approaching its limit, HCA becomes more severe than NBTI in some CMOS processes [7,8] and one example is given in Fig. 1, so that HCA remerges as a major challenge for modern CMOS technologies.

HCA requires two conditions: a high electrical field and a large number of carriers passing through this field. Conventionally, HCA is most severe when gate bias, Vg, is approximately half of the drain voltage, Vd. For modern CMOS nodes, however, Fig. 2 shows that HCA is more severe under Vg=Vd than that under Vg=Vd/2. We will focus on HCA under Vg=Vd in this work, therefore. The objective is to develop a test methodology for extracting the HCA model parameters and verifying the accuracy of the developed HCA model against experimental data.

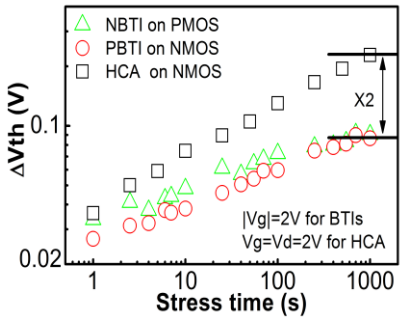

Fig. 1 For the CMOS technology used in this work, hot carrier aging (HCA) causes more damage than BTI at 125 °C.

2. Devices and experiments

The devices used in this work are nMOSFETs, fabricated by a bulk 28 nm CMOS process with a used-Vdd of 0.9 V. The devices have a metal gate and high-k stack with an equivalent oxide thickness of 1.2 nm. The channel length and width are 27 nm and 900 nm, respectively.

HCA was performed under Vg=Vd. The aging was periodically monitored by interrupting the stress and measuring the forward and reverse saturation current under Vg=Vd=0.9 V. The threshold voltage shift, ΔVth, was also measured from the Vg shift under a fixed drain current of 100 nA×W/L, which was taken from the pulsed Id-Vg under Vd=0.1 V [9-11].

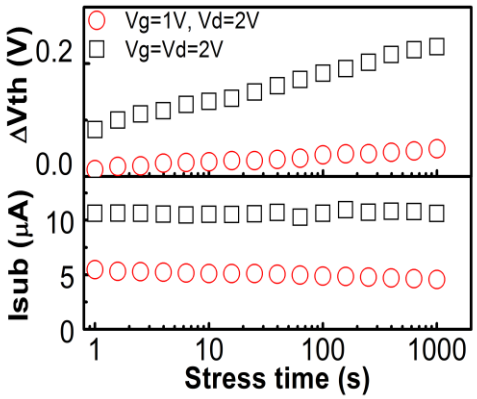

Fig. 2 For short channel devices in modern CMOS nodes, HCA under Vg=Vd is higher than that under Vg=Vd/2.

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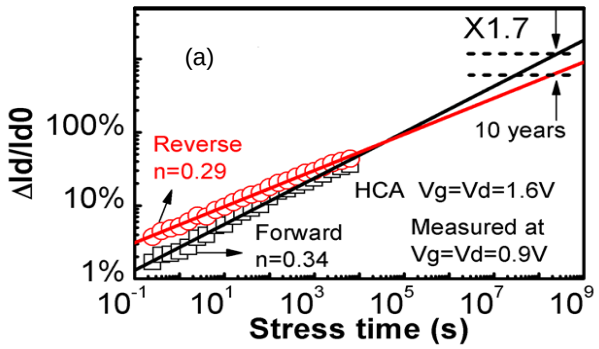
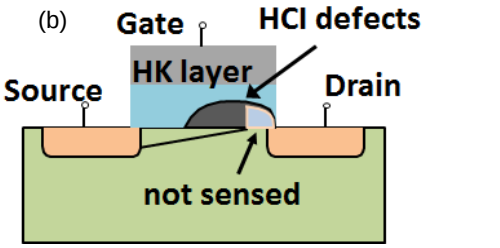
3. Extraction of time power component, n

The required device lifetime is typically 10 years, while the test time is practically limited to days. To predict device lifetime, the test data is extrapolated from days to 10 years [12-14]. The reliability of this extrapolation critically depends on the accuracy of the time power exponent, n, in eq. (1).

$$Aging = A \times Vg^m t^n. \quad (1)$$

'n' is the slope of the aging kinetics in Fig. 3a.





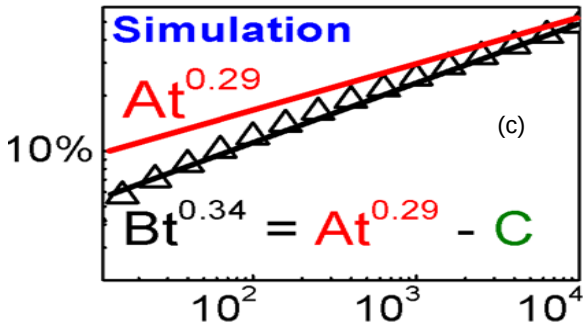


Fig. 3 (a) shows that the extracted n is 0.34 and 0.29 for ΔId/Id_F and ΔId/Id_R, respectively. This difference in n leads to the cross-over of the two lines, when extrapolating. At 10 years, ΔId/Id_F would be 1.7 times of ΔId/Id_R, which is physically incorrect. (b) shows that the damage between the pinch-off point and the drain was not sensed in the ΔId/Id_F. (c) illustrates that by subtracting a constant from a power law, it could lead to an increase of the apparent power exponent.

HCA is widely monitored from the shift of drain saturation current in the forward mode, ΔId/Id_F, namely the source and drain are the same as that used for the HCA stress. By exchanging the source and drain after HCA stress, the reverse saturation current, ΔId/Id_R, can also be used to monitor the HCA. Fig. 3a shows that the measured ΔId/Id_F is less than ΔId/Id_R. This is because the HCA is non-uniform and occurs mainly near the drain. In the forward saturation mode, the channel is pinched off and the damage between the pinch-off point and the drain contributes little to ΔId/Id_F, due to the screening effect by the space charge, as illustrated in Fig. 3b. In the reverse mode, on the other hand, all damage contributes to ΔId/Id_R, so that ΔId/Id_R is larger. When extrapolated to 10 years, however, ΔId/Id_R becomes smaller than ΔId/Id_F, which is incorrect.

To investigate the source of errors, Fig. 3c shows that by subtracting a constant from the power law of n=0.29, the apparent n can increase to 0.34. Subtracting a constant disproportionally reduces ΔId/Id_F at short time, leading to an artificially higher n. As a result, the higher n for ΔId/Id_F is caused by subtracting the damages between the pinch-off point and the drain in Fig. 3b. We conclude that the n extracted from ΔId/Id_F is erroneous.

To capture the whole damage, channel pinch-off should be avoided. Fig. 4 shows the HCA kinetics monitored from the linear threshold voltage shift measured under Vd=0.1 V. The ΔVth in the forward and reverse mode agree well and the extracted n also agrees well with that extracted from ΔId/Id_R in Fig. 3a. ΔVth will be used to extract n hereafter.

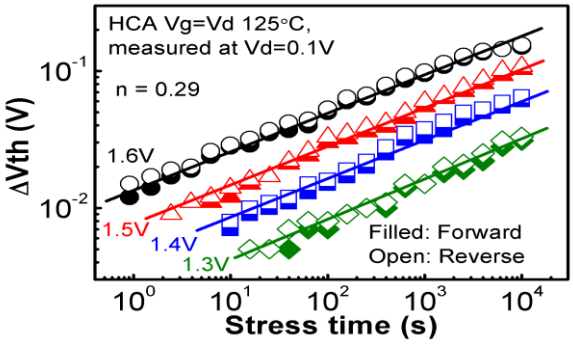


Fig. 4 Threshold voltage shift measured under Vd=0.1 V in both forward and reverse mode and they agree well. The time exponent is insensitive to the stress biases.

4. Extraction of voltage power component, m

Conventionally, the voltage exponent, m, in eq. (1) was extracted by repeating the HCA stress under several different voltages [3,13,15]. This is time consuming and it is highly desirable to extract m from a single device. To achieve this, a voltage-step-stress technique (VSS)

has been developed for NBTI [15]. We will adopt VSS for HCA here.

The stress voltage waveform used in the VSS is given in Fig. 5a. The same device was subjected to a series of voltage step and each step lasts for a fixed time. A typical result is given in Fig. 5b. As illustrated by Fig. 5c, the stress under a higher voltage V2 for a time of T is equivalent to a stress under a lower voltage V1 for a longer time of Teff through eq. (2),

$$T_{eff} = \left(\frac{V2}{V1}\right)^{m/n} \times T. \quad (2)$$

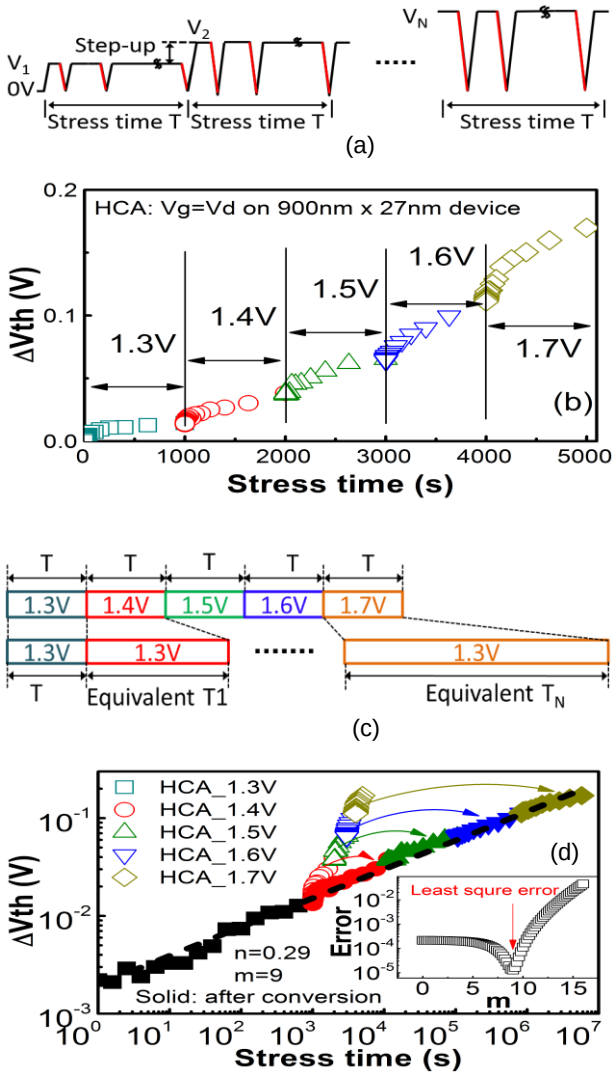


Fig. 5 The voltage-step-stress (VSS) technique. (a) shows the waveform for Vg=Vd. (b) gives a typical result. (c) illustrates the stress under a higher bias is equivalent to a stress under a lower bias for a longer time. (d) shows that the voltage exponent, m, can be extracted by fitting with eq. (2). The inset shows that m is extracted from the minimum errors.

The n in eq. (2) is extracted by fitting the data under Vg=Vd=1.3 V. The m is extracted by fitting the test data in Fig. 5b with the least error criterion, as illustrated by Fig. 5d. In this way, m can be extracted from the VSS test on a single device.

5. Verification of the model

The mission for extracting m and n is to establish a model that can be used to predict HCA under a given stress bias and time through eq. (1). To complete the mission, one must verify how accurate the extracted model can be used to predict the HCA. We now test the accuracy of the model against independently measured experimental data.

As shown in Fig. 5, the model parameters were extracted from stresses under a bias between 1.3 and 1.7 V. We now use it to predict the HCA under lower voltage in the range of 0.9 to 1.2 V. The HCA under a stress bias of 0.9 to 1.2 V were independently measured and the results are given in Fig. 6. It can be seen that the prediction agrees well with the test data. It should be pointed out that the test data in Fig. 6 themselves were not used to fit the model parameters.

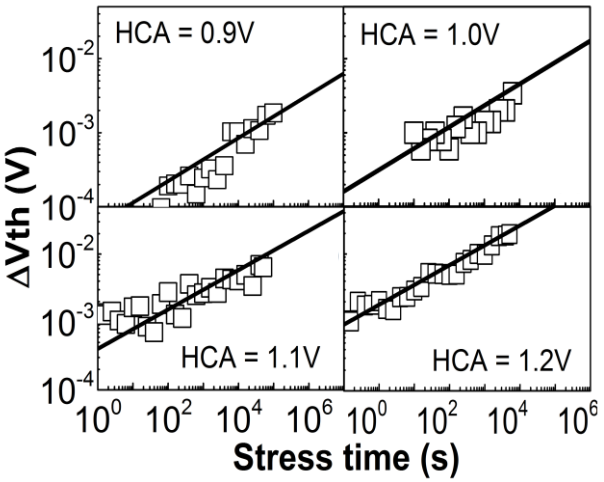


Fig. 6 A comparison of the prediction (lines) by eq. (1) with the independently measured test data under different stress biases.

The results in Fig. 6 is for the threshold voltage shift. In addition to ΔVth, it is important to know the HCA of saturation current. Fig. 7a shows that both forward and reverse saturation current agings are correlated with ΔVth. As a result, once ΔVth is predicted by eq. (1), ΔId/Id_F and ΔId/Id_R can be obtained from Fig. 7a. Fig. 7b shows that both the ΔId/Id_F and the ΔId/Id_R obtained in this way agree well with the measured data.

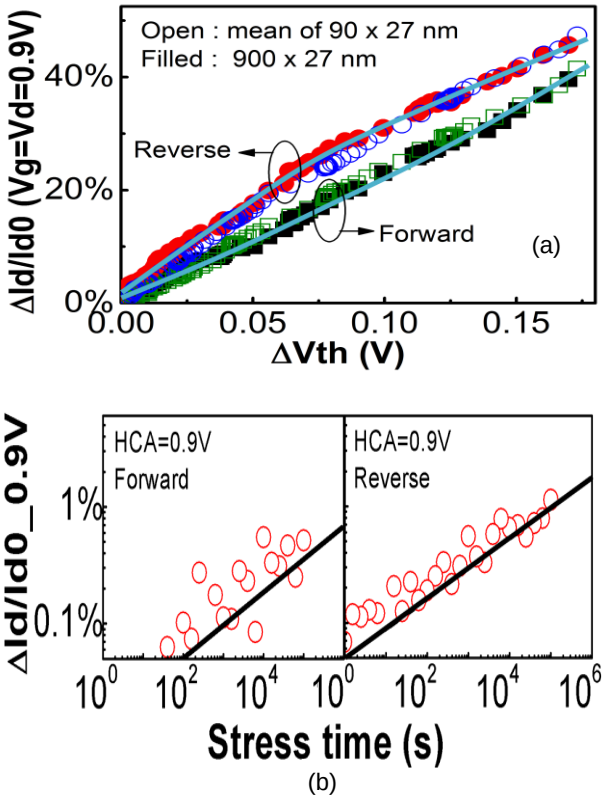


Fig. 7 (a) The correlation between the HCA-induced ΔVth and ΔId/Id. (b) A comparison between the model prediction (lines) and test data. The predicted ΔId/Id was obtained from the calculated ΔVth by using the relation in (a).

6. Summary

This work investigates the hot carrier aging for small channel devices used in modern CMOS nodes. Unlike the early CMOS technology where most severe HCA occurs under Vg=Vd/2, HCA is higher under Vg=Vd for short channel nMOSFETs. A test methodology has been proposed that allows the time and voltage exponents being extracted from a single device. It is shown that the time exponents must not be extracted from the forward saturation current degradation, since it gives erroneous value due to the screening effect for the damage between the pinch-off point and the drain. The threshold voltage shift should be used for the extraction and a voltage-step-stress technique can be used for extracting the voltage exponent. The accuracy of the model based on the extracted parameters has been verified against independently measured data.

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