Device and Circuit Performance of the Future Hybrid III-V and Ge based CMOS Technology

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***Abstract*—The device and circuit performance of a 20 nm gate length InGaAs and Ge hybrid CMOS based on an implant free quantum well (QW) device architecture is studied using a multi-scale approach combining ensemble Monte Carlo simulation, drift-diffusion simulation, compact modelling, and TCAD mixed-mode circuit simulation. We have found that the QW and doped substrate, used in the hybrid CMOS, help to reduce short channel effects by enhancing carrier confinement. The QW also reduces the destructive impact of a low density of states (DoS) in III-V materials. In addition, the calculated access resistance is found to be a much lower than in Si counterparts thanks to a heavily doped overgrowth source/drain contact. We predict an overall low gate capacitance and a large drive current when compared to Si-CMOS that leads to a significant reduction in a circuit propagation time delay (∼5.5 ps).**

***Index Terms*—III-V, Ge, CMOS, Monte Carlo, drift-diffusion, compact modeling, TCAD.**

I. Introduction

ALternative channel materials to improve CMOS performance is a rapidly growing area of research [1][2]. III-V and Ge based CMOS offers attractive possibilities for a high performance and a low power circuit implementation [3]. In addition, this device can be manufactured onto the existing Si substrate technology, allowing co-integration with conventional Si-CMOS. A high electron mobility and a low effective mass in III-V materials result in a very high injection velocity and a low back-scattering promising a high device performance and a large switching speed at a low supply voltage [4][5]. On the other hand, the investigation of Ge as an alternative channel material and a potential technology booster has experienced a revived impetus, especially for p-channel MOSFETs [6][7], where a higher carrier mobility and drive current compared to conventional Si devices have already been successfully demonstrated [8].

The high mobility and the high injection velocity of III-V and Ge materials require transistor architectures which can be readily incorporated into Si CMOS technology while simultaneously neutralizing some of detrimental effects of low density of states (DoS) [9]. The implant free quantum well (IFQW) device structure [10][11] offers such attractive technological and performance advantages. The IFQW has a better scalability, lower sensitivity to D_{it} in the tails compared to other MOSFET architectures [11], and is highly resistant to the band-to-band tunnelling (BTBT) since it is free of heavily doped source/drain (S/D) regions [12]. Combined variability simulations including random discrete dopants (RDD), line edge roughness and metal gate granularity have shown that IFQW-CMOS has a better immunity to threshold voltage (V_{th}) variability than equivalent bulk Si MOSFETs [13].

In this work, we report on the device and circuit performance of the IFQW-CMOS that is based on nIFQW III-V and pIFQW Ge device architectures using a multi-scale modelling approach by hierarchy of ensemble Monte Carlo (MC) simulation, drift-diffusion (DD) simulation, compact modelling, and TCAD mixed-mode circuit simulation techniques. The IFQW-CMOS architecture is summarised in Section II, while Sections III and IV outline the simulation methodology and device/circuit performance together with macroscopic parameters extraction. Conclusions are drawn in Section V.

II. IFQW III-V and Ge Based CMOS

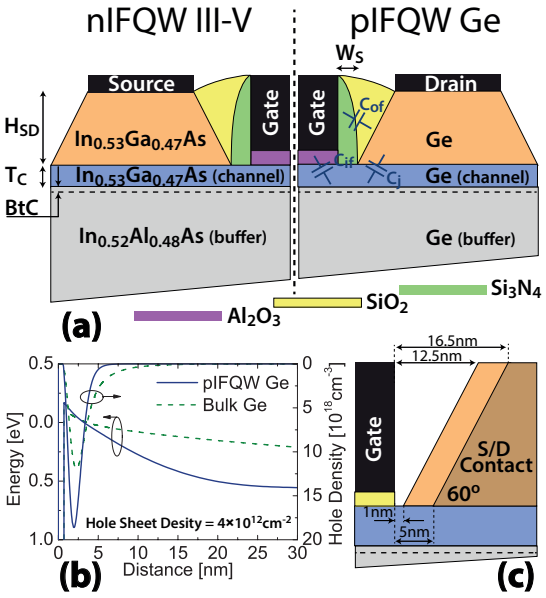

Fig. 1. (a) Cross-sections of IFQW-CMOS made of implant free quantum well device (IFQW) architectures (nIFQW III-V and pIFQW Ge). The doping concentration is low in a channel (T_C) and a buffer-to-channel (BtC) layer indicated by a dash line and is high in the rest of a buffer. (b) Valence band energy and hole density profiles across the middle of the gate for pIFQW Ge and bulk Ge MOSFETs for comparison. (c) Geometry of a tilted S/D contact that helps to reduce the effect of outer fringing capacitance (C_{of}).

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TABLE I
DIMENSIONS AND DOPING CONCENTRATIONS OF THE IFQW-CMOS.

	n**IFQW III-V**	p**IFQW Ge**
Dimensions [nm]		
Gate length (L_g)	20.0	20.0
Lateral spacer width (W_S)	1.0 or 5.0	1.0 or 5.0
S/D height (H_{SD})	20.0	20.0
S/D length	45.0	45.0
Gate dielectric	1.6	1.6
Channel thickness (T_C)	5.0	5.0
Buffer-to-Channel (BtC)	1.0	1.0
EOT	0.7	0.7
Doping Concentrations [$\times 10^{17}$cm^{-3}]		
Background	1.0 (p-type)	1.0 (n-type)
Buffer	20.0 (p-type)	20.0 (n-type)
S/D Contacts	500.0 (n-type)	500.0 (p-type)

The cross section of the IFQW-CMOS is illustrated in Fig. 1a. The nIFQW III-V part consists of $In_{0.52}Al_{0.48}As$ buffer, 5 nm thick $In_{0.53}Ga_{0.47}As$ channel, 1 or 5 nm Si_3N_4 lateral spacer width (W_S). The p-type buffer is uniformly doped to 2×10^{18}cm^{-3} to reduce leakage current. At 1 nm below the channel, the p-type buffer doping concentration is reduced to 1×10^{17}cm^{-3} (background doping) and remains low in the channel. The raised S/D contacts are uniformly n-type doped to 5×10^{19}cm^{-3}. The pIFQW Ge structure is similar to the nIFQW III-V with highly p-type doped (5×10^{19}cm^{-3}) Ge S/D contact, a 5 nm Ge channel. The QW of the pIFQW Ge is created by having a low n-type doping concentration in the channel and in the buffer till 1 nm below the channel. At the 1 nm below the channel till the rest of the buffer (see Fig. 1b), n-type doping is a much larger (2×10^{18}cm^{-3}). A common gate stack is used for the both n and pIFQWs with 1.6 nm Al_2O_3 dielectric layer giving an equivalent oxide thickness (EOT) of 0.7 nm. As a requirement for the CMOS co-integration, a dual metal work function of 4.6 eV and 4.2 eV is used for n and pIFQW, respectively [14], [15]. All devices have raised contact regions angled at 60°. Only a small degradation ($< 5\%$) in the drive current has been observed for the 60° S/D contacts in respect to the vertically raised contacts [16]. The dimensions and doping concentrations of both devices are optimised using DD simulations [17] whilst accounting for technological limitations as summarised in Table I.

III. SIMULATION METHODOLOGY

In this study, we have employed a set of device simulation techniques:

- Ensemble 2D finite-element MC device simulator in order to realistically predict supra-threshold characteristics (drive currents) of the IFQW-CMOS.
- For sub-threshold characteristics, 2D DD simulations calibrated against the MC data are used to assess device electrostatic like the subthreshold slope (SS) and the drain induced barrier lowering (DIBL). This is because MC simulations require extremely long runs due to inaccurate resolution of small currents. The DD calibration process consists on adjusting the I_D-V_G characteristics at low and high drain voltages via a physically based mobility model. The low drain voltage I_D-V_G characteristics are used to adjust a low-field mobility (accounting for phonon scattering and impurity scattering) while a high-field mobility is tuned via a saturation velocity and a critical field to the high drain voltage I_D-V_G characteristics.
- An industry standard compact model (PSP) is used to match the DD results and to extract the DC and AC macroscopic parameters such as gate capacitances, short channel effects, access resistances,...etc. The PSP calibration starts by adjusting the device electrostatics to match the SS and DIBL parameters from the DD. A two-stage compact model calibration and parameter extraction strategy have been employed [18].
- Finally, a full mixed-mode TCAD simulation is used to calculate the circuit propagation time delay in an inverter based on the IFQW-CMOS.

In this hierarchy of simulation techniques, the 2D MC device simulations, including quantum corrections and Fermi-Dirac statistics, employed for III-V and Ge IFQW transistors have well-recognised performance predictive power [12][19]-[22]. In the past, the III-V MC device simulator has been validated against measured I-V characteristics of a 120 nm gate length $In_{0.2}Ga_{0.8}As$ pseudomorphic [20], lattice matched metamorphic HEMTs [23], and a 50 nm gate length $In_{0.7}Ga_{0.3}As$/InP HEMT [24]. The details on the III-V MC simulator can be found in [4], [12], [20]. The Ge MC device simulator employs a $6-$band **k•p** full-band structure including Fermi-Dirac statistics [25]. Optical and acoustic phonon scatterings of holes are compared against the experimental velocity-field characteristics for relaxed, bulk Ge demonstrating a good agreement [22]. Moreover, these two MC simulation tools have been adapted to deal with the IFQW with a new treatment required for the raised S/D contacts to accurately model carrier injection velocity [12][21].

IV. DEVICE AND CIRCUIT PERFORMANCE

In order to get a good estimation of device and circuit performance of the IFQW-CMOS at the end of the roadmap, we have selected two different W_S in the devices (1 nm and 5 nm). Ensemble MC simulations are thus ideal to predict drive currents, while the DD technique is employed to simulate the sub-threshold currents. The latest helps to better understand the benefit of the good IFQW electrostatic integrity which can counterbalance the problem of low DoS and dark space (DS) in III-V materials.

A. I_D-V_G Characteristics

The I_D-V_G characteristics obtained from the MC and calibrated DD simulations of nIFQW III-V and pIFQW Ge are shown in Figs. 2 and 3, respectively. For the nIFQW III-V, there is an increase in the drive current from $\sim$1000 μA/μm to $\sim$3000 μA/μm when W_S is reduced from 5 nm to 1 nm. A quantum confinement modulated potential barrier in the channel below the lateral spacer at the source side increases back-scattering rate for thicker lateral spacers ($\sim$5 nm). As a result, the carrier concentration in this channel reduces which, consequently, limits the drive current [26].

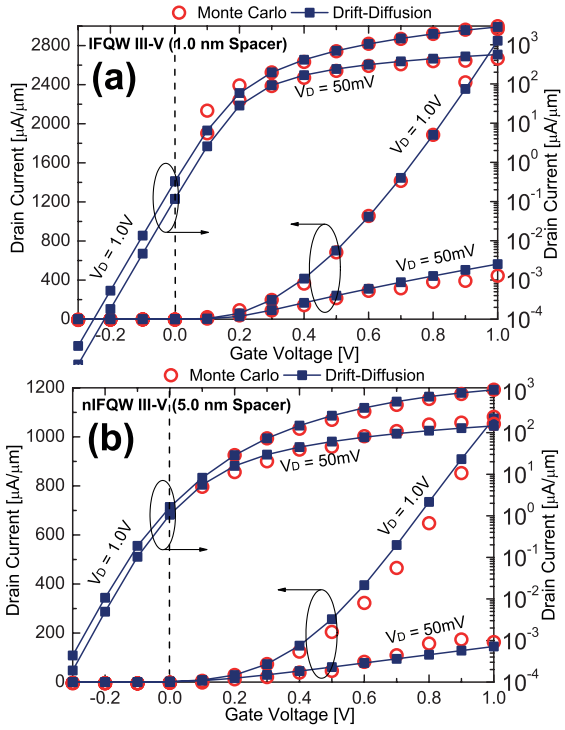

Fig. 2. I_D-V_G characteristics of the nIFQW III-V at $V_D = 50$ mV and $V_D = 1$ V. DD simulations have been calibrated against MC results. (a) Lateral spacer width W_S=1 nm (SS=71.0 mV/Dec, DIBL=35.0 mV/V, I_{OFF}=0.1 μA/μm) and (b) W_S=5 nm (SS=76.0 mV/Dec, DIBL=27.0 mV/V, I_{OFF}=1 μA/μm).

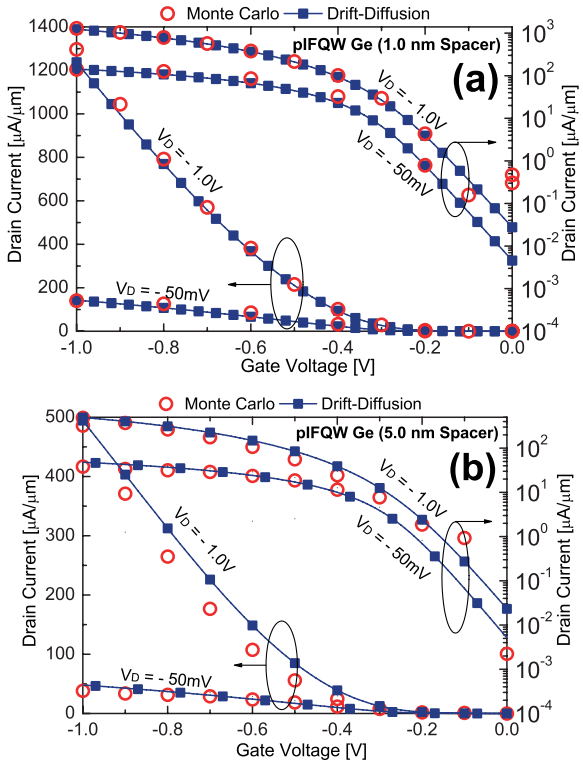

Fig. 3. I_D-V_G characteristics of the pIFQW Ge biased at $V_D = -50$ mV and $V_D = -1$ V. The DD simulations have been calibrated against MC results. (a) Lateral spacer width W_S=1 nm (SS=91.0 mV/Dec, DIBL=74.0 mV/V, I_{OFF}=4.5×10^{-3} μA/μm) and (b) W_S=5 nm (SS=95.0 mV/Dec, DIBL=65.0 mV/V, I_{OFF}=5.1×10^{-3} μA/μm).

For the pIFQW Ge, the drive current increases from ∼500 μA/μm to ∼1300 μA/μm when W_S is reduced from 5 nm to 1 nm. The calibrated DD simulations indicate that W_S has relatively a small impact on electrostatic integrity (SS and DIBL) for both nIFQW III-V and pIFQW Ge devices. I_{OFF} values of the nIFQW III-V are about two orders of magnitude higher than of the pIFQW Ge. This is the consequence of a larger leakage in III-V materials, which is related to the low DoS. The DIBL and SS are smaller than those of the 18 nm gate length Si or the 24 nm gate length FDSOI counterparts [30], [31], [32] but comparable to those of the $16 - 28$ nm gate length SOI FinFETs by the 14 nm technology [33]. The DD simulations are then used to generate continuous output I_D-V_D characteristics (not shown) needed for macroscopic parameters extraction for the IFQW-CMOS. The latest are vital information for the overall performance predictions of IFQW-CMOS at short gate lengths.

B. Gate Capacitances

The gate capacitance (C_G) and its different components (dynamic charge distributions) are central parameters in determining the circuit performance of nano-transistors. In this context, we have used an industry standard compact models (PSP) to extract the AC behaviour of the IFQW-CMOS. The PSP has attracted significant attention because of its capability for a good physical description of device characteristics, especially for advanced technology nodes [27].

In this section, we have first calibrated the PSP models against the DD simulated characteristics (I_D-V_G and I_D-V_D). Then, we have employed the split CV method [28] to distinguish the extrinsic gate capacitance (C_{GEXT}) from the intrinsic gate capacitance (C_{GINT}). C_{GEXT} includes both inner and outer fringe capacitances as shown in Fig. 1a. In contrast to the conventional MOSFETs with implanted S/D junctions, C_{GEXT} of the IFQW does not include the overlap capacitance: $C_G = C_{GINT} + C_{GEXT}$. In the first order, the gate-to-channel capacitance is proportional to the metallurgical gate length (L_g) but C_{GEXT} remains virtually constant. Varying L_g, which will not change C_{GEXT} contribution, the intrinsic gate-to-channel capacitance can be extracted. Different devices were simulated at a single frequency 1 MHz at each DC bias during a sweep of V_G performed in the AC simulation analysis. Results for gate lengths of 100 nm and 200 nm were used to cross-check accuracy of the results for the 20 nm gate length devices investigated here, although those are not shown here.

Fig. 4 compares the total, intrinsic and extrinsic capacitances versus the gate voltage (V_G) for the nIFQW III-V and pIFQW Ge (W_S=1 nm and W_S=5 nm), respectively. W_S has a relatively small impact on C_{GEXT}. This can be explained by geometrical shape of the S/D, particularly the large horizontal distance between the top of metal-gate and the S/D contact that reduces the effect of the outer fringing capacitance. Fig. 1c illustrates that at the bottom of the S/D contact, a relative difference between the 1 nm and 5 nm W_S devices is 80 % while it is just 24 % at the top. Note that shrinking W_S leads to lowering potential barrier in the channel and, consequently, to lowering of the inner fringing capacitance.

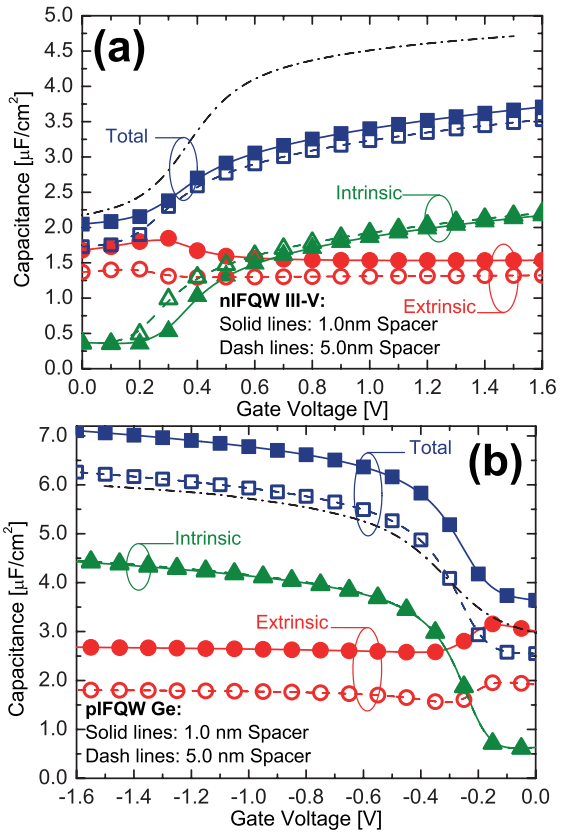

Fig. 4. Capacitance-voltage characteristics per unit area ($L_g \times W_g$) of the IFQW-CMOS: (a) nIFQW III-V and (b) pIFQW Ge. The "dash dot" lines represent the C_G of the 18 nm gate length bulk Si devices (pMOSFET and nMOSFET).

The gate capacitance of the pIFQW Ge is larger than that of the nIFQW III-V. This difference can be explained by a low inversion layer capacitance in the $In_{0.53}Ga_{0.47}As$ channel due to a combination of low DoS and a larger equivalent gate dielectric thickness in inversion (T_{INV}). Note that the quantum capacitance is proportional to the DoS of channel material [29]. The overall C_G of the nIFQW transistor is lower than that of the 18 nm gate length Si counterpart [30][31]. However, the C_G of pIFQW transistor is comparable to that of the Si devices.

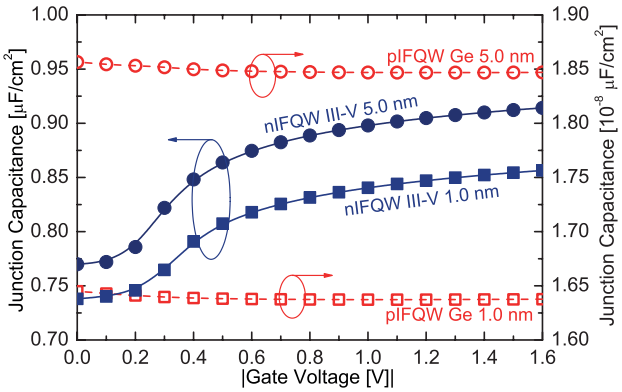

Fig. 5. Junction capacitance per unit area ($L_g \times W_g$) versus V_G of the 20 nm gate length IFQW-CMOS (nIFQW III-V and pIFQW Ge) for a lateral spacer width W_S=5 nm (circle symbols) and W_S=1 nm (square symbols).

Junction capacitances that originate from the p-n junctions formed by the S/D contacts to the channel depletion region (as illustrated in Fig. 1a) have been also extracted using the PSP model. Unlike the $In_{0.53}Ga_{0.47}As/In_{0.52}Al_{0.48}As$ nIFQW, there is no heterojunction in the pIFQW Ge between the Ge channel and the buffer, which explains a small junction capacitance in comparison to the nIFQW III-V. The junction capacitance reduces when reducing W_S. This is related to the electrostatic potential under the lateral spacer. Shrinking W_S will result in lowering of potential barrier in the channel (just under the spacer) and leads to a lower junction capacitance near the contact edges.

C. Short Channel Effects

To estimate the short channel effect (SCE), a relationship between V_{th} and L_g, a set of DD simulations was done in order to extract the behaviour of V_{th} for different gate lengths as shown in Fig. 6. For both nIFQW III-V with $W_S = 1$ nm and $W_S = 5$ nm, the ΔV_{th} is less than 100 mV. A sharp decrease of V_{th} for gate lengths ranging from 32 nm down to 10 nm is observed. This can enhance the line edge roughness induced variability for $L_g < 50$ nm. On the other hand, we have found that the pIFQW Ge suffers from larger SCEs due to a relatively weak quantum confinement in the Ge channel in comparison to the nIFQW III-V.

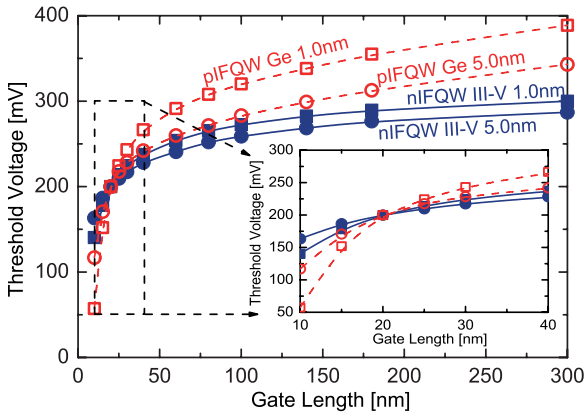

Fig. 6. Threshold voltage versus the gate length of the IFQW-CMOS for two different lateral spacer widths ($W_S = 1$ nm and 5 nm).

The confinement of carriers in the QW in a combination with the high p-type doping concentration in the nIFQW III-V (n-type doping for the pIFQW Ge) below the channel provides excellent electrostatic integrity. From the point of view of short channel control, the QW acts similarly to thin-body SOI structures preventing carriers from spilling into buffer or substrate and provides immunity to punch-trough and DIBL which occurs when the drain current starts to be partially controlled by the drain terminal [35]. The QW also helps to relax the SCEs in the nIFQW III-V. In contrast, a weak confinement in the pIFQW Ge is responsible of the SCEs enhancement in respect to the 24 nm gate length FDSOI counterparts [32] or the $16-28$ nm gate length SOI FinFETs by the 14 nm technology [33]. In general, the SCEs have a less impact on the SS and DIBL of IFQW devices when compared

to equivalent conventional 18 nm gate Si-MOSFETs [30][31] exhibiting a SS≃93 mV/Dec and a DIBL≃90 mV/V.

D. Access Resistances

We have employed the transmission line method (TLM) to calculate the access resistances. The calibrated DD simulations are used to simulate devices with different gate lengths in a linear regime. The total resistance of a device includes the S/D contact resistances (R_S+R_D) and the channel resistance (R_{CH}). The access resistance, R_S+R_D, can be extracted by extrapolating the total resistance (R_S+R_D+R_{CH}) at L_g= 0 nm as shown in Fig. 7. In the case of nIFQW III-V, increasing the W_S by a factor of 5 (from 1 nm to 5 nm) leads to an increase in the access resistance by a factor of 2 only. This demonstrates a weak dependence of the access resistance on W_S. The calculated access resistance of the pIFQW Ge for both 1 nm and 5 nm spacers are larger than those observed for the nIFQW III-V. This can be explained by a low mobility in the Ge channel below the spacer area.

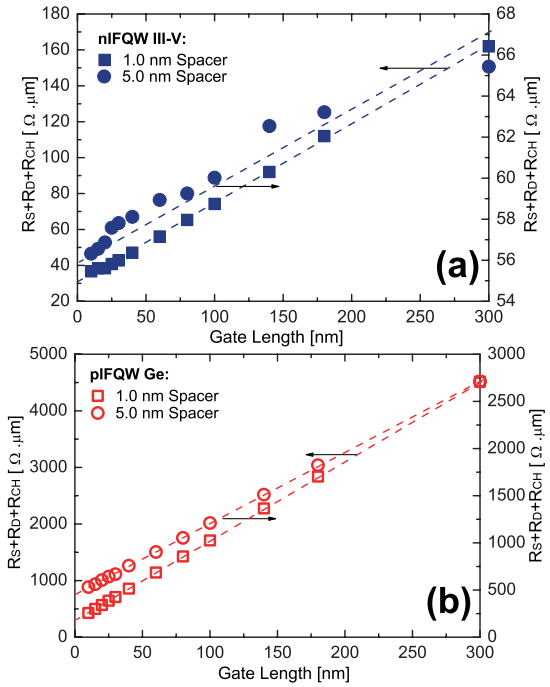

Fig. 7. Total resistances (R_S+R_D+R_{CH}) versus gate length of the IFQW-CMOS for W_S=1 nm and W_S=5 nm. (a) The nIFQW III-V and (b) the pIFQW Ge FETs.

The formation of the S/D regions using overgrowth, when dopants are incorporated and activated during the regrowth process, has technological advantages compared to implanted junctions. The drawbacks of implantation are: (i) the need for activation results in intermixing and inter-diffusion of spacers, which may result in a mobility reduction, and (ii) a relatively low S/D doping concentration that can be activated after implantation in the range of 5×10^{18}cm^{-3} to 1×10^{19}cm^{-3}, resulting in a higher access resistance. A summary of the extracted macroscopic parameters of the IFQW-CMOS is shown in Table II. There, the "effective source velocity" is a measure of the average velocity at the source end of the channel [36], a product of classical injection velocity and ballistic ratio [37].

E. Circuit Propagation Time Delay

Circuit speed is one of the most critical figures of merit in the VLSI design. The transient behaviour of a CMOS inverter, as a basic circuit element, is simulated using a mixed-mode technique involving device and circuit simulations. The IFQW-CMOS is physically simulated, subject to time-dependent bias conditions, employing the macroscopic parameters such as capacitances and access-resistances.

The IFQW-CMOS inverter has been constructed as show in the inset of Fig. 8. The drain terminals of the inverter are connected to a load capacitor, an important factor in determining a propagation delay. This load includes a wire load capacitance and input capacitances of following inverters. The edge time for an input V_{IN} (0 V → 1 V or 1 V → 0 V) is 4 ps. A propagation delay, the time difference between the 50% transition points of the input and output signals, estimated from such simulations is ∼5.5 ps. The reduced overall C_G of the IFQW-CMOS (Figs.4 and 5) in conjunction with the expected increase in the drive current (Figs. 2 and 3) significantly reduces the propagation delay. The good electrostatic control of the IFQW-CMOS with W_S = 1 nm makes its circuit performance to be a much better compared to Si or FDSOI devices [32] and to be close to SOI FinFETs by 14 nm technology [33], while the structure with W_S = 5 nm becomes largely degraded.

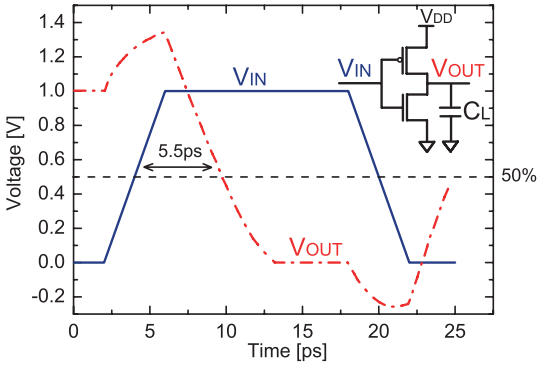

Fig. 8. Propagation time delay of an inverter based on the IFQW-CMOS (W_S=1 nm). The inset shows the schematic configuration of the inverter.

Finally, the lower DoS in III-V materials leads to a larger DS compared to Si devices, and thus to a larger T_{INV} [29]. This can impact the performance in a triple way: (i) via a decrease of the C_{OX} = κ_{OX}/T_{INV} capacitance and thus a decrease of electron density in inversion layer; (ii) via a SS relaxation and; (iii) via a DIBL relaxation [38]. The low DoS in III-V channels significantly affects the gate drivability when the gate-to-channel separation is aggressively reduced. Consequently, a part of the gate voltage overdrive that must support the inversion layer charge is consumed by the corresponding movement of Fermi level relative to a conduction band edge. A well optimised QW channel thickness can neutralize this DoS induced drawback by widening a distribution of the charge in the channel. The widely distributed charge in the channel

TABLE II
FIGURES OF MERIT FOR THE IFQW-CMOS WITH TWO DIFFERENT LATERAL SPACER WIDTHS (1 NM AND 5 NM).

	n**IFQW III-V**		p**IFQW Ge**	
	W_S=1 *nm*	W_S=5 *nm*	W_S=1 *nm*	W_S=5 *nm*
Drain Induced Barrier Lowering [mV/V]	35.0	27.0	74.0	65.0
Short Channel Effect [V]	0.1	0.087	0.16	0.20
Sub-threshold Slope [mV/Dec]	71.0	76.0	91.0	95.0
Effective Source Velocity [$\times 10^7$cm/s]	8.0	6.5	4.1	3.7
Saturation Velocity [$\times 10^7$cm/s]	0.9	0.9	0.6	0.6
Access Resistance [$\Omega.\mu$m]	15.0	28.0	100.0	375.0
Gate-to-Channel Capacitance [μF.cm^2]	1.85	1.85	4.147	4.163
Fringing Capacitance [μF.cm^2]	1.50	1.30	2.635	1.767
Junctions Capacitance [μF.cm^2]	0.90	0.82	1.63×10^{-8}	1.85×10^{-8}
Short Channel Mobility [cm^2/V.s]	472.0	276.0	125.4	71.83

will lower V_G required to move the channel potential thus quickly achieving a carrier concentration for effective channel transport.

V. CONCLUSION

Hierarchical multi-scale simulations of the InGaAs/Ge hybrid CMOS technology using MC technique, DD method, compact modelling approach, and TCAD mixed-mode circuit modelling have shown that a destructive impact of the low DoS (a large DS) in III-V materials can be partially neutralized by a design of QW channel. In addition, the QW and the buffer doped a 1 nm below the channel reduce short channel effects by enhancing carrier confinement. The simulations demonstrate a small effect of W_S on the electrostatic integrity (SS and DIBL) and access resistances in the IFQW-CMOS thanks to the device structure and the heavily doped overgrowth S/D. The calculated access resistances are lower than those in Si counterparts. W_S has also a relatively small impact on C_{GEXT} due to a geometrical shape of the S/D that reduces the effect of the outer fringing capacitance. Shrinking W_S has led to a smaller inner fringing capacitance and a larger drive current. The good electrostatic control of the IFQW-CMOS with W_S=1 nm makes its circuit performance to be a much better compared to Si or FDSOI devices, even if a DIBL degradation is observed [32], similarly to SOI FinFETs by 14 nm technology [33]. The reduced overall gate capacitance of the InGaAs/Ge hybrid IFQW-CMOS in conjunction with the large drive current have led to a significant reduction in the circuit propagation delay ($\sim$5.5 ps).

In summary, we have demonstrated that an excellent electrostatic control can be designed into a III-V/Ge hybrid CMOS by taking advantage of the channel confinement, thanks to a heterostructure transistor architecture. Such heterostructure design can be tuned for optimal performance delivering a very fast switching and a short propagation delay thus decisively reducing energy dissipation and further reducing device self-heating. This high mobility dual channel CMOS thus offers a high performance boost for the sub-16 nm technology nodes creating a competitive advantage for nano-electronics industry players.

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