A 14-bit 250 MS/s IF Sampling Pipelined ADC in 180 nm CMOS Process

Xuqiang Zheng, Zhijun Wang, Fule Li, Feng Zhao, Shigang Yue, *Member, IEEE*, Chun Zhang, and Zhihua Wang, *Senior Member, IEEE*

***Abstract*—This paper presents a 14-bit 250 MS/s ADC fabricated in a 0.18 μm CMOS process, which aims at optimizing its linearity, operating speed and power efficiency. The implemented ADC employs an improved SHA with parasitic optimized bootstrapped switches to achieve high sampling linearity over a wide input frequency range. It also explores a dedicated foreground calibration to correct capacitor mismatches and the gain error of residue amplifier, where a novel configuration scheme with little cost for analog front-end is developed. Moreover, a partial non-overlapping clock scheme associated with a high-speed reference buffer and fast comparators is proposed to maximize the residue settling time. The implemented ADC is measured under different input frequencies with a sampling rate of 250 MS/s and it consumes 300 mW from a 1.8 V supply. For 30 MHz input, the measured SFDR/SNDR of the ADC is 94.7 dB/68.5 dB, which can remain over 84.3 dB/65.4 dB up to 400 MHz. The measured DNL and INL after calibration are optimized to 0.15 LSB and 1.00 LSB, respectively, while the Walden FOM at Nyquist frequency is 0.57 pJ/step.**

***Index Terms*—Foreground calibration, low cost configuration, high linearity, high-speed comparator, parasitic optimized SHA, partial non-overlapping.**

I. Introduction

HIGH-speed, high-resolution analog-digital converters (ADCs) with IF sampling capability play key roles in recent wireless communication systems. Benefiting from the IF/RF sampling ability, the architecture of cellular based-stations evolves from multi-narrowband receivers to a single wideband multi-channel receiver, which transfers the major work of individual channel extraction to mature digital signal processing and hence significantly reduces the cost and complexity of cellular base stations [1]–[3]. Other applications such as cable modems, CCD/medical imaging, and computed tomography scanners have similar quantization requirements [2], [4], [5]. Among various ADC architectures, the pipelined ADC is considered as one of the best candidates to fulfil the above mentioned applications due to its power efficiency in realizing 12-16 bits resolution, 70-80 dB SNR, and 85-95 dB SFDR at a sampling range of 100-300 MS/s [6], [7].

The main challenge of IF-sampling ADC is the linearity distortion at high input frequency [8], [9], characterized by spurious-free dynamic range (SFDR), which is of great importance for wireless communication systems since weak signals are supposed to be detected in the presence of strong nearby interferences. Therefore, high SFDR is needed to mitigate the inter-modulation. However, the design of such ADCs is a nontrivial task, which is mainly constrained by the following factors. First, the linearity of the overall ADC is restricted by the front-end sample-hold (S/H) circuits, any nonlinearity introduced by them will be transferred to the final digital output directly. Second, the finite op-amp gain error in stages may cause the residue slope deviating from the ideal value, leading to a uniform jump in the overall ADC transfer function. Third, capacitor mismatches between the unit capacitors C_i and feedback capacitor C_f will create unique jumps in the ADC transfer function. Either uniform jump or unique jump can yield conversion errors, resulting in additional noise and distortion. Finally, insufficiently settled output induced by limited settling time may also deteriorate the SFDR. Although the capacitor mismatches can be alleviated by increasing the unit capacitor size and the inadequate settling time can be mitigated by increasing the amplifier's bandwidth, these methods cost large area occupation and increased power consumption. This is not desirable for high-density systems, since it involves severe heat dissipation problem [10], [11], colliding with the trend of low-cost and small form factor.

To address these issues, several techniques have been exploited in this work. First, a parasitic optimized S/H circuit is employed to achieve a high sampling linearity over a wide input frequency range. Second, a partial non-overlapping clock scheme is proposed to maximize the settling time. Third, a low cost foreground calibration is developed to correct the errors caused by capacitor mismatch and finite op-amp gain. These approaches are integrated in a 14-bit 250 MS/s ADC prototype that is fabricated in 0.18 μm CMOS technology.

The remainder of this paper is organized as follows. Section II describes the ADC architecture. Section III details the S/H parasitic optimization, Section IV presents the clock design schemes, and Section V discusses the foreground calibration algorithm and analog design considerations. The critical circuit implementations are illustrated in Section VI, and the complete ADC measurement results are given in Section VII. Section VIII concludes the paper.

II. The ADC Architecture

The architecture of the presented ADC is shown in Fig. 1. A dedicated sample-and-hold amplifier (SHA), in spite of increasing the power and noise of the ADC, is still utilized in this design to improve the sampling linearity at high input frequencies. This is because the SHA-less architecture has difficulties in achieving a high SFDR for IF sampling applications with fast changing input signals due to its aperture error and complicated input network. Multi-bit stage can significantly

X. Zheng, Z. Wang, F. Li, C. Zhang and Z. Wang are with the Institute of Microelectronics, Tsinghua University, Beijing 100084, China. (E-mail: lifule@mail.tsinghua.edu.cn; zhengxuqiang@mail.tsinghua.edu.cn).

X. Zheng, F. Zhao and S. Yue are with the School of Computer Science, University of Lincoln, Lincoln LN6 7TS, United Kingdom.(Email: syue@lincoln.ac.uk)

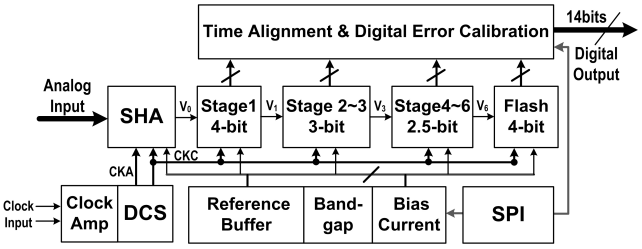


Fig. 1. Block diagram of pipelined ADC.

reduce the noise and offset requirements of succeeding stages [12]; however, the bit number is limited by the offset of comparators in flash-ADC. In this design, a 4-bit sub-ADC is integrated in the first stage, which is then followed by two 3-bit stages, three 2.5-bit stages, and a final 4-bit flash stage. A/The? developed foreground calibration is performed on the first three stages to reduce the errors resulting from capacitor mismatches and finite op-amp gain. A low jitter differential clock receiver followed by a duty cycle stabilizer (DCS) is applied to provide low jitter clock (CKA) for SHA and 50% duty cycle clock (CKC) for quantization stages. In addition, a power-efficient high-speed reference buffer is integrated to produce fast recovery references and facilitate the chip applications.

The developed low cost foreground calibration decreases the capacitor size from matching limitation to noise limitation, thus dramatically reducing the power consumption. Additionally, the proposed partial non-overlapping clock scheme associated with the improved comparator increases the residue settling time. Hence, the bandwidth requirement of residue amplifiers in this design is lessened, which also helps to save the power dissipation.

III. S/H PARASITIC OPTIMIZATION

As the analog front-end of the ADC, the S/H circuit needs to acquire a wideband input signal in high precision without introducing too much noise [8], [9]. As depicted in Fig. 2, the flip-around structure utilizing bottom plate sampling technique is preferred due to its good performance in noise and power consumption. A bootstrapped NMOS switch is used to reduce the on-resistance and its nonlinearity that is dependent on the signal amplitude, thus greatly alleviating the harmonic distortion. However, for high-speed IF sampling applications, the performance of the S/H circuit is still constrained by the following two factors [13], [14]. One is the signal dependent parasitic capacitance from input to ac ground during the track phase, represented by the variable capacitor C_{p1}. This voltage-dependant capacitor C_{p1} causes a non-linear charging current, which creates a non-linear voltage error by traveling through the ADC equivalent driving impendence R_s [15], [16] and thus degrading the tracking linearity and sampling precision. Considering the fact that this error originates as a current charging a capacitance, it becomes proportionately larger with frequency. This means the linearity corruption effect can become even more severe as the input frequency increases. The other factor is the parasitic capacitance from the input to node nb during the hold phase, represented by the capacitor

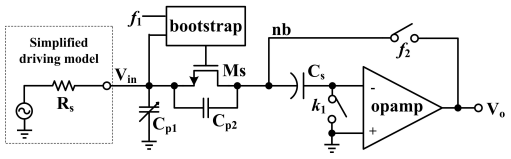


Fig. 2. Flip-around S/H circuit with bottom-plate sampling (single-ended for simplification).

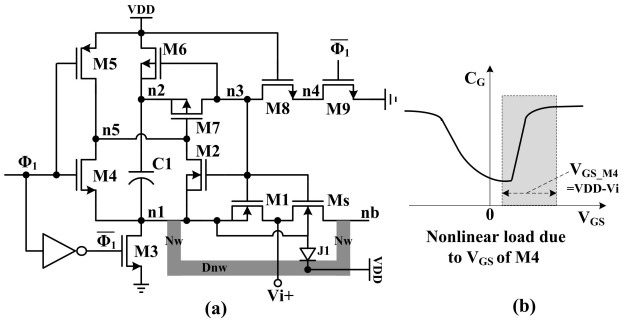


Fig. 3. Conventional bootstrapped switch.

C_{p2}, which introduces feed-forward disturbance to the settled output. These two parasitic capacitances are optimized in this section.

A. Parasitics in conventional bootstrapped switch

The circuit for a conventional bootstrapped switch in [17], [18] is shown in Fig. 3. The bulk effect of the NMOS switch devices (Ms, M1 and M2) is eliminated by connecting their bulk to the input signal through M1 during the track phase. As illustrated in Fig. 3(a), the bulk of Ms, M1 and M2 is isolated from the common p-substrate (Psub) by the isolation layer formed by surrounding nwell and buried deep-nwell (Dnw), where the n-type isolation layer is usually connected to VDD to keep parasitic diodes reversely biased. Obviously, there is a bulk-nwell diode J1, which introduces a nonlinear junction capacitance to the input during the track phase. Another important parasitic capacitance comes from the transistor of M4. When input clock Φ_1 is high, the gate of M4 is pulled up to VDD and its source and drain are connected to the input through on-transistors of M1 and M2. Fig. 3(b) gives the C-V characteristics of NMOS transistors and the V_{GS} operating range of M4 (see the shaded area, where the summation of C_{GS} and C_{GD} is approximately equal to C_G). It can be seen that M4 creates a nonlinear capacitance to the input, which will be eliminated in this work using the following technique.

B. Improved bootstrapped switch

Fig. 4 presents the details of the improved bootstrapped switch. A floating-well technique described in [3], [13] is applied to optimize the nonlinear capacitance of the diode J1. Specifically, during the hold phase, the isolation layer is reset to VDD via M10. For the following track phase, the isolation layer is left floating by switching off M10. The gate of M10 is driven by the bootstrapped clock, which makes this PMOS completely turned off during the track phase even though the isolation layer voltage is bootstrapped higher than VDD. Utilizing this technique, the presented parasitic

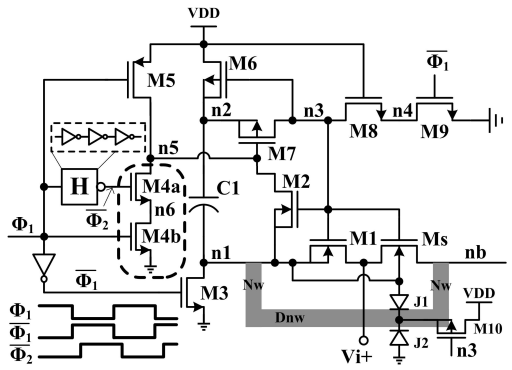


Fig. 4. Improved bootstrapped input switch.

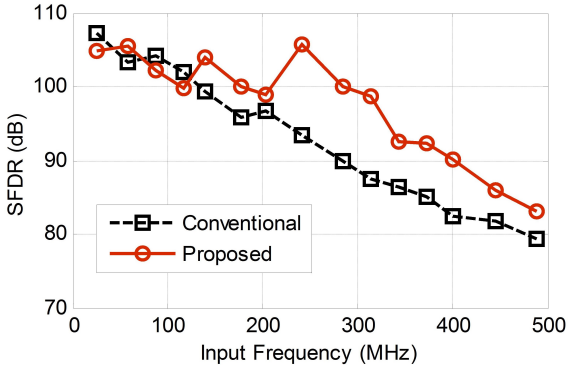


Fig. 5. Post-layout SFDR simulation via input frequency.

capacitance to the input becomes smaller and more linear for the following three reasons. First, the bulk-nwell diode J1 and nwell-psub diode J2 are connected in series, which reduces the equivalent parasitic junction capacitance. Second, the junction capacitance values of J1 and J2 vary in opposite directions with the voltage changes of the isolation layer, which improves the linearity of the equivalent capacitance. Finally, the voltage of the isolation layer is bootstrapped higher than VDD, thus the reversely biased junction capacitance can be further reduced.

To optimize the parasitic capacitance induced by M4 in Fig. 3, two transistors M4a and M4b in series shown in Fig. 4 are used to perform the function of M4. The gate of M4b is connected to Φ_1, and the gate of M4a is controlled by $\overline{\Phi_2}$ (i.e., the delayed inverted version of Φ_1). When the rising edge of Φ_1 arrives, both M4a and M4b are turned on to pull down node n5. After the bootstrapped switch is triggered, M4a is turned off by $\overline{\Phi_2}$ to isolate node n5 from the ground. Applying this approach, the signal-dependent capacitors C_{GS} and C_{GD} of M4 in Fig. 3 are optimized since the source of M4a are disconnected from input and its gate voltage is pulled down during the track phase. The simulated SFDR at different input frequencies are summarized in Fig. 5, which indicates that the proposed technique of parasitic capacitance optimization can improve the linearity at high frequencies.

C. Optimization for feed-forward coupling

During the hold phase, the large transistor Ms is turned off, but the input signal still couples to node nb through drain-source capacitor C_{DS} of Ms. The coupling effect will

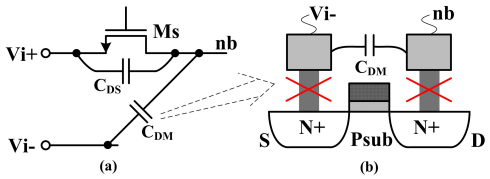


Fig. 6. Layout method for feed-forward coupling cancellation.

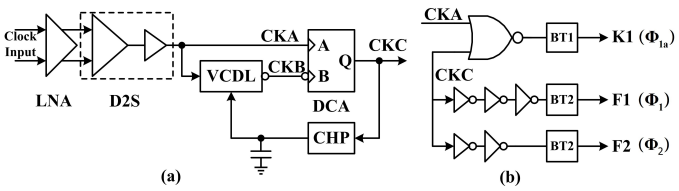


Fig. 7. Clock Schemes. (a) Input clock amplifier and duty cycle stabilizer, and (b) local clock generator for SHA.

disturb the settled output voltage, which degrades the dynamic performance at high frequencies. To neutralize this effect, the basic idea is to use a dummy capacitor, connecting the complementary input to node nb, as illustrated in Fig. 6(a). The dummy capacitor can be realized by a metal-oxide-metal (MOM) capacitor or a dummy transistor [14]. The former suffers from matching problem, while the later has the drawback of adding extra nonlinear junction parasitic. Fig. 6(b) shows the proposed physical structure of the dummy capacitor C_{DM}. It adopts a dummy transistor similar to Ms, but removes the source/drain contacts that only contribute three percent of the total parasitic capacitance. In doing so, a relatively good matching between C_{DS} and C_{DM} is achieved, which results in a 5 dB improvement on the SFDR at Nyquist frequency according to back-annotated simulations.

IV. CLOCK DESIGN SCHEMES

High-frequency and high-resolution pipelined ADCs have imposed stringent requirements on clock designs, including low jitter property for SHA, precise duty cycle for pipeline stages, and non-overlapping clocks for sampling/transferring in stages [3], [19], [20]. First, clock jitter leads to sample-to-sample variations, which can result in prominent errors for IF-sampling applications because of the high slew rate of fast changing input signals. These errors can be converted into digital output directly, which introduces substantial distortion, thus degrading the SFDR. Second, both the positive and negative clock phases are required for charge settling in adjacent stages for pipelined ADCs. Therefore, any duty-cycle deviation from 50% may reduce the allowed settling time for odd or even stages, limiting the maximum operating speed or degrading the settling accuracy. Third, non-overlapping clocks are needed to prevent switch operating noise from coupling into the sampling voltages. However, the non-overlapping time occupies a portion of the amplification phase, which decreases the settling time of the residue amplifier. To accommodate these requirements, the following two techniques are applied.

A. Duty cycle stabilizer

To provide an accurate 50% duty cycle clock for quantization stages, a clock shaping front end consisting of an input

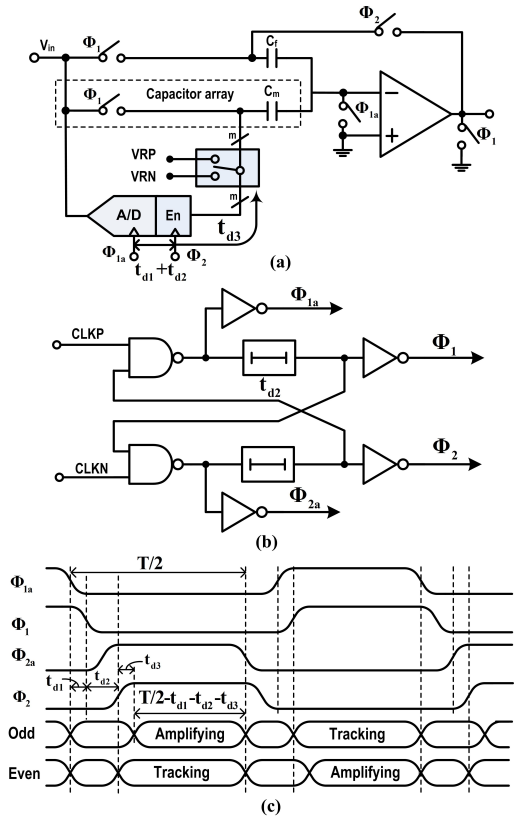


Fig. 8. Conventional non-overlapping clock scheme. (a) Simplified stage implementation, (b) a typical clock generator, and (c) timing diagram.

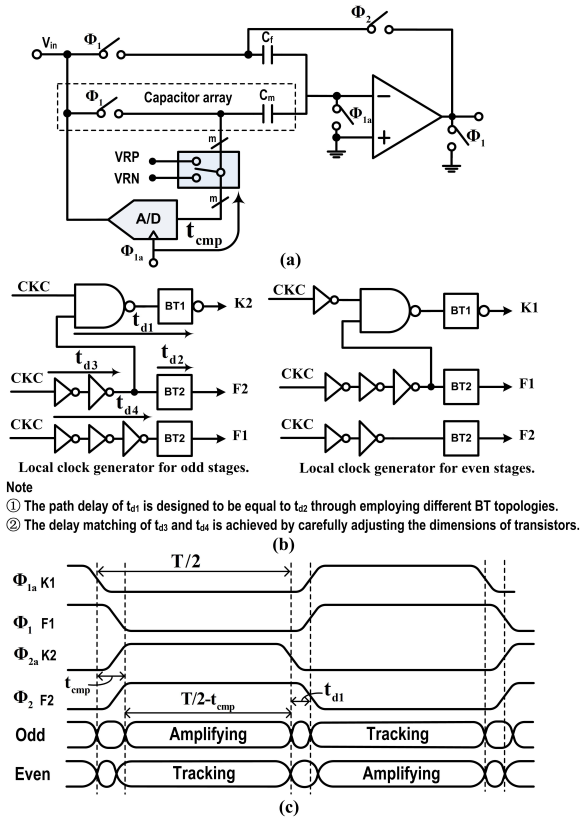


Fig. 9. Proposed partial non-overlapping clock scheme. (a) Simplified stage implementation, (b) local clock generators, and (c) timing diagram.

clock amplifier and a duty cycle stabilizer is utilized as shown in Fig. 7(a). The input clock is firstly pre-amplified by a low noise amplifier (LNA) to acquire a high swing differential signal, which is further applied to a differential to single (D2S) block to obtain the full swing clock CKA. CKA is then fed to a duty cycle adjuster (DCA) that is similar to the design in [19] to combine the rising edge of CKA and the falling edge of CKB (i.e., the half-period delayed version of CKA). As a result, a 50% duty cycle clock CKC is produced, which is distributed to pipeline stages to generate various local clocks. The precision of the duty cycle depends on the delay precision between clock CKA and CKB. To guarantee an accurate delay against PVT variations, a delay locked loop (DLL) is employed to perform automatical adjustment.

In this work, both CKA and CKC are applied to generate the sampling clock K1 as shown in Fig. 7(b). Note that the rising edge of CKA arrives earlier than that of CKC, thus the falling edge of K1 is triggered by the rising edge of CKA. Therefore, a minimum propagation path, from input to the sampling instant, is achieved. This is important for the optimization of sampling clock jitter, because it not only reduces the intrinsic noise by passing through less devices, but also decreases the deterministic jitter (proportional to the path delay) caused by power fluctuation and substrate noise.

B. Partial non-overlapping clock scheme

Fig. 8 describes a conventional non-overlapping clock scheme in pipelined ADCs [20], where input sampling, input amputating, and residue amplifying are trigged in a specific order that are controlled by Φ_{1a}, Φ_1 and Φ_2. Benefiting from the sequential operation, signal dependent injection error and potential reference charge extraction are prevented. Fig. 8(b) presents a typical non-overlapping clock generator. The clock waveforms are illustrated in Fig. 8(c), where t_{d1} is the delay from Φ_{1a} to Φ_1 and t_{d2} is non-overlapping time between Φ_1 and Φ_2. Usually, the overall non-overlapping time between Φ_{1a} and Φ_2 is designed to be long enough for the sub-ADC to resolve effective outputs. Thus, the available settling time for residue amplifier can be given by $T/2-t_{d1}-t_{d2}-t_{d3}$, where t_{d3} is the propagating delay form Φ_2 to reference selecting switches. Clearly, the non-overlapping clock scheme decreases the actual settling time of residue amplification. This effect is particularly serious for high sampling frequencies, since the settling time reduction can occupy a large portion of unit converting period.

To extend the actual settling time of residue amplification, it is worth to analyze the necessity of the non-overlapping times in Fig. 8(c). First of all, the non-overlapping time between the falling edges of Φ_{1a} and Φ_1 is indispensable, otherwise signal-dependent charge injection will be coupled to the sampled voltage. In contrast, the non-overlapping time between Φ_1 and Φ_2 is optional, depending on the bandwidth of the reference buffer. To be more specific, if the bandwidth of the reference buffer is small with a low charge recovery capability, the non-overlapping time is essential since it avoids the instantaneous connection between the reference and amplifier's output, hence preventing the charge extraction from the reference and maintaining a stable reference voltage. On the other hand, if a

high bandwidth reference buffer is adopted, charge extraction caused by instantaneously connecting the output of amplifier and the reference can be quickly recovered by the high-speed buffer. Therefore, this non-overlapping time can be eliminated to increase the settling time of the residue amplification.

Fig. 9 depicts the proposed partial non-overlapping clock scheme along with its circuit implementation and the timing diagram. Compared to the traditional design, the output enabling phase of Φ_2 in the sub-ADC is eliminated (see Fig. 9(a)), and the non-overlapping time between Φ_1 and Φ_2 is removed (see Fig. 9(c)). Thus, the maximum available settling time is possibly extended to $T/2 - t_{d1}$, as long as the the resolving time of the sub-ADC is shorter than the non-overlapping time t_{d1}. Otherwise, the actual settling time is limited by the resolving time of the sub-ADC. In this design, the non-overlapping time is designed to be $(2-3)T_{inv}$,where T_{inv} is an inverter delay. This time is usually shorter than the resolving time of sub-ADC. Therefore, the practical settling time can be considered as $T/2 - t_{cmp}$, where t_{cmp} is the resolving time from the sampling instant (i.e., the falling edge of Φ_{1a}) to the last-bit changing moment for reference selection. Simultaneously, since the output enabling clock Φ_2 is removed and the rising edges of Φ_1 and Φ_{1a} are aligned, the instantaneously connecting time between the reference and amplifier's output is decided by the resetting time of the sub-ADC, thus the sub-ADC should have a short resetting time. Fig. 9(b) describes the circuit implementation details for the partial non-overlapping clock generation. To achieve the timing relationships described in Fig. 9(c), appropriate topologies for BT1 and BT2, careful transistor size selection, and sophisticated layout routing are adopted.

In this part, we present a novel clock scheme by removing the output enabling clock Φ_2 in the sub-ADC and the non-overlapping time between Φ_1 and Φ_2. As a result, the resolving time of flash-ADC becomes the most possible limiting factor that impedes the settling time extension. Hence, a high-speed comparator with the capabilities of fast resolving and quickly resetting is desirable. To achieve a maximum residue settling time, an optimized comparator is developed in Section VI. In addition, the proposed partial non-overlapping clock scheme needs a high-speed reference buffer to provide a fast charge recovery ability. To solve this problem, a fully NMOS reference buffer is employed to guarantee a sufficient bandwidth, which will be explained in Section VI as well.

V. Digital Calibration

Digital calibration techniques are widely used to correct the nonlinearity impairments to reduce the power consumption by relieving the stringent requirements on capacitor matching accuracy and high open-loop gain of op-amp. These techniques becomes popular due to their potentials on realizing high power efficiency linear ADCs. However, the developed calibration techniques have been proven to suffer from various penalties. For example, the earliest evolving foreground calibration discussed in [21], [22] requires switching the precise analog circuitry in and out of the pipeline to connect to a special set of input signals, which adds overheads to the analog front end

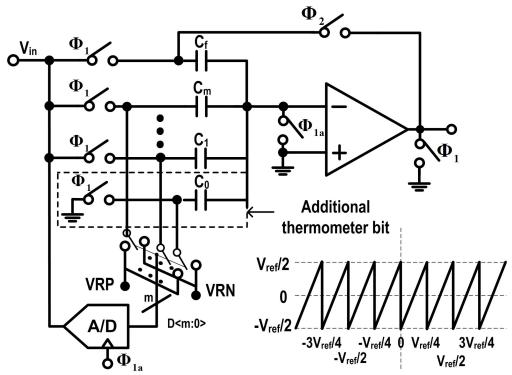


Fig. 10. Circuit implementation of the pipeline stage with 1-bit redundancy (single-ended for simplification).

in terms of introducing additional capacitances or shortening effective conversion time. The dithering-based digital calibration presented in [13], [23] suffers from a slow convergence speed and less accuracy due to limited dithering magnitude and strong interference from the input signal, which impede its spread in applications that support intermittent operation. Although the LMS-based background calibration described in [8], [24] can speed up the convergence rate, it involves an auxiliary slow but accurate ADC to statistically estimate and correct the nonlinear errors of pipelined ADCs. Moreover, these overheads associated with these digital calibrations are often translated into either higher power dissipation or reduction of conversion speed.

In this section, an improved foreground calibration, which is well suitable for intermittent applications, is developed. By adopting an 1-bit redundancy pipeline stage, the actual bit weight measurement can be performed by applying a sole zero input instead of the special set of input signals in traditional implementations [21], [22]. Meanwhile, a complete auxiliary reconfiguration scheme is proposed to keep the analog-signal path completely intact and a compact digital algorithm is employed to save hardware resources and power consumption. The proposed correction technique, which avoids impairing the critical high-speed path and introducing many auxiliary circuits, can maintain the maximum conversion speed for a specific process and thus can be utilized to improve the conversion speed and/or to reduce power consumption. In this section, the residue transfer error is firstly analyzed, then calibration configuration in the analog front end and calibration procedure in the digital part are elaborated.

A. Residue transfer errors analysis

Eq. (1) gives the residual output voltage of the 1-bit redundancy pipeline stage depicted in Fig. 10, which is utilized in the first three calibration stages.

$$V_{res} = \left(\frac{C_f + \sum_{i=1}^{m} C_i}{C_f} \cdot V_{in} - \frac{\sum_{i=0}^{m} b_i C_i}{C_f} \cdot V_{ref} \right) \cdot \left(\frac{1}{1 + 1/A\beta} \right), \quad (1)$$

where A is the DC-gain of the op-amp and β denotes the feedback factor. Undoubtedly, the finite op-amp gain could introduce a gain error $\Delta \approx 1/A\beta$. Additionally, if there is

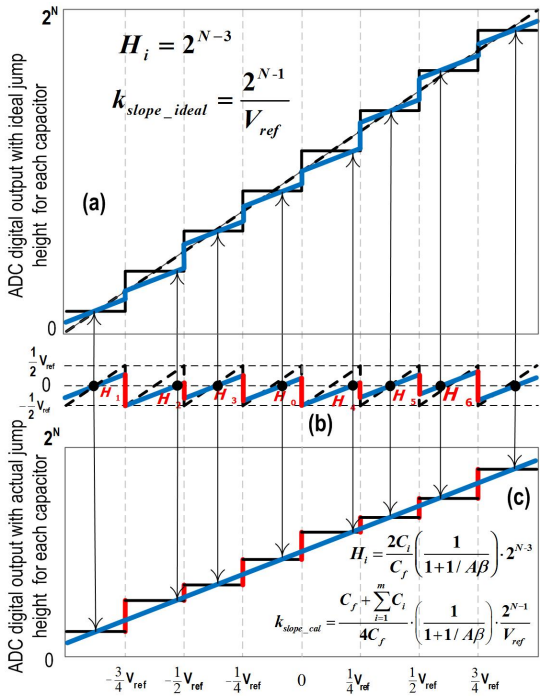


Fig. 11. Illustration of pipelined ADC nonlinearity when static gain error and capacitor mismatches are included. (a) Using ideal bit weight for digitalization, (b) residue transfer curve, and (c) using actual bit weight for digitalization.

mismatch between $\sum_{i=1}^{m} C_i$ and C_f, there will be an additional error in the desired stage gain. These stage gain errors make the transfer slope deviate from its ideal value, which results in a uniform jump when there is an output changes in the sub-ADC. Furthermore, fabrication mismatches between sampling capacitors lead to unique jumps [20]. Fig. 11(b) depicts a 3-bit residue transfer curve including static gain error and capacitor mismatches, while Fig. 11(a) illustrates these effects on the linearity of the pipelined ADC when an ideal bit weight is adopted. Clearly, these errors lead to prominent differential nonlinearity (DNL) and integral nonlinearity (INL).

Note that the residue transfer segments in different regions shown in Fig. 11(b) shares the same slope, which can be written as,

$$k_{slope} = \left(\frac{C_f + \sum_{i=1}^{m} C_i}{4C_f} \right) \cdot \left(\frac{1}{1 + 1/A\beta} \right) \cdot \frac{2^{N-1}}{V_{ref}}, \qquad (2)$$

where N is the bit number from the calibrating stage to the back-end. Then the actual bit weight can be given as,

$$H_i = \frac{2C_i}{C_f} \left(\frac{1}{1 + 1/A\beta} \right) \cdot 2^{N-3}. \qquad (3)$$

Fig. 11(c) illustrates the digital output of the overall ADC when actual bit weights are adopted. It can be seen that the discontinuous segments in Fig. 11(a) are linearly jointed with an attenuated gain k_{slope}. Consequently, the static linearity can be significantly improved by utilizing the actual bit weights.

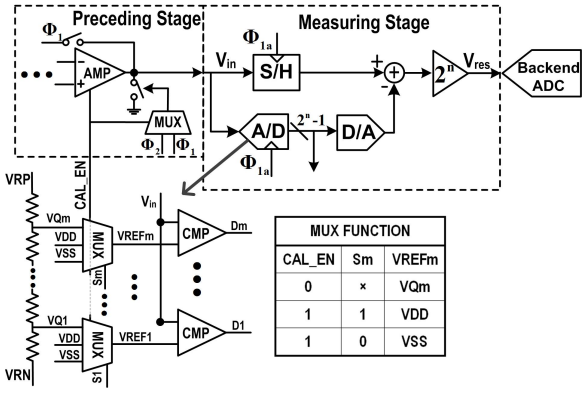


Fig. 12. Configuration of pipeline stages for bit weight measurement.

B. *Calibration configuration in pipeline stages*

Based on the analyses in Part A, the essence of the foreground calibration is measuring the actual bit weights in calibration mode and using the actual bit weights instead of the ideal ones during data conversion mode. Thus, the analog front-end needs to be able support two operating modes, bit weight measurement mode and normal data conversion mode. During the bit weight measurement period, the main task of the pipeline stage under calibrating is to generate residual voltage that represents the bit weight of the measuring capacitor, while all the following stages operate as a back-end ADC to convert the analog bit weight voltage to digitized output. The main challenge lying in such two-mode pipeline stages is how to produce precise bit-weight voltage without introducing too many supporting circuits to the critical high-speed path.

A traditional method to measure the bit weight is to quantize the residual output voltages, while fixing the input at a specific voltage to make sure that the digitalized value is corresponding to the bit weight of the measuring capacitor [22]. For the conventional 0.5-bit redundancy pipeline stage, additional driving circuitry is needed to provide the specific input voltages for the measurements of difference capacitors. However, this requirement suffers from the following problems. First, input variations caused by insufficient settling or noise may degrade the measurement accuracy. Second, the switching circuitry for input selection introduces overhead to the high speed path, which tends to deteriorate the high-frequency performance of the overall ADC. Third, the additional circuits that generate such input voltages involve substantial area occupation and power consumption. To address these issues, 1-bit redundancy pipeline stages and a complete auxiliary configuration scheme are developed to produce the precise bit weight voltages. Fig. 10 shows the 1-bit redundancy pipeline stage implementation for calibration stages, where an extra comparator with zero threshold voltage is added to to contribute a zero crossing output change in the residue transfer curve. Accordingly, the bit weight voltage can be measured by setting a zero input, while changing the output of the sub-ADC.

Fig. 12 presents the pipeline stage configuration during bit weight measurement, where the stage input and the sub-ADC output are reconfigured. The input voltage of the measuring stage is set to zero through properly configuring the preceding stage, including powering down the amplifier and switching

the output reset clock from complementary phase clock Φ_2 to in-phase clock Φ_1. Applying this method, the input is set to zero without introducing extra circuit to the critical high-speed path. To implement the output control of the sub-ADC, a threshold voltage adjustment based method (see Fig. 12) is employed to avoid introducing any delay between the sub-ADC and the sub-DAC. As shown in Fig. 12, the threshold voltages are selected through an analog MUX under the control of CAL_EN and S_m. When the calibration enable signal CAL_EN is activated, the threshold of comparator is switched to either VDD or VSS, depending on the polarity control signal S_m. If S_m is high, the threshold is connected to VDD, thus the comparator's output is forced to low. On the contrary, when S_m goes down, the threshold is changed to VSS, hence the output of the comparator is high.

To demonstrate the bit weight measurement process, the measurement of capacitor C_i in the first stage is taken for instance, where the input of stage-1 is set to zero by the aforementioned preceding stage reconfiguration. The polarity control signal S_i is driven by a half-rate clock, which is obtained by dividing the sampling clock by a factor of 2. Thus, the output of this comparator is alternatively changed between low and high. It means that the capacitor C_i under measuring is connected to $+V_{ref}$ and $-V_{ref}$, alternatively. At the same time, half of the remaining selection signals are set to high, while the other half is configured to low. Correspondingly, half of the remaining sampling capacitors are connected to $+V_{ref}$ and the other half are connected to $-V_{ref}$. According to Eq. (1) , when C_i is connected to $+V_{ref}$, the residual output voltage can be given by,

$$V_{resi}^{+} = -\frac{C_i}{C_f}\left(\frac{1}{1+1/A\beta}\right)\cdot V_{ref} + \frac{\Delta C_h}{C_f}\left(\frac{1}{1+1/A\beta}\right)\cdot V_{ref}, \quad (4)$$

where ΔC_h is the mismatch between the summation of the two halves of capacitors that are connected to $+V_{ref}$ and $-V_{ref}$, respectively. Since this mismatch is minor, the value of V_{resi}^{+} is close to $-V_{ref}/2$.

When C_i is connected to $-V_{ref}$, the residual output voltage is computed by,

$$V_{resi}^{-} = +\frac{C_i}{C_f}\left(\frac{1}{1+1/A\beta}\right)\cdot V_{ref} + \frac{\Delta C_h}{C_f}\left(\frac{1}{1+1/A\beta}\right)\cdot V_{ref}. \quad (5)$$

Thus, the digitalized value of the actual bit weight can be deduced as follows,

$$\begin{aligned} HD_i &= D(V_{resi}^{+})\times(-1) + D(V_{resi}^{-})\times(+1) \\ &= D\left(\frac{2C_i}{C_f}\left(\frac{1}{1+1/A\beta}\right)\cdot V_{ref}\right). \end{aligned} \quad (6)$$

This alternative bit weight measurement method possesses several advantages. First, the high precise zero input is easily achieved by properly configuring the preceding stage, which avoids introducing any additional circuit to the critical load-sensitive path, thus exhibiting little effect on the performance of the overall ADC. Second, the output reconfiguration of sub-ADC is implemented by adjusting the threshold voltages, which is performed at the low-speed threshold-selection side rather than the high-speed sub-ADC output side. Thus, the output reconfiguration of sub-ADC presents little effect on ADC performance as well. Third, the alternative measurement approach is essentially a realization of chopping technique (see Fig. 13) that can move the offset and low frequency noise including 1/f noise to high frequency, which are then filtered by the averaging filter in the digital part. Combining all the features mentioned above, it can be expected that the proposed alternative measurement can perform a high accurate bit weight measurement at a low cost for both circuit addition and power penalty.

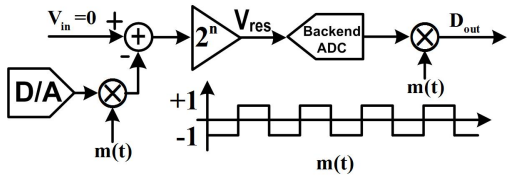


Fig. 13. Illustration of chopping implementation.

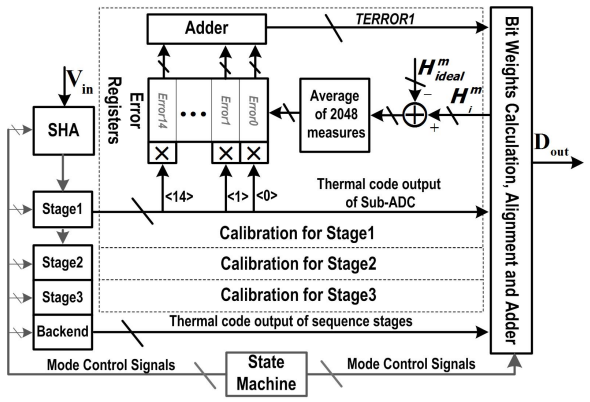


Fig. 14. Calibration block diagram.

C. Calibration process in digital part

The calibration is carried out on the first three stages and begins with the third stage, forward to the first stage. Fig. 14 presents the block diagram of the calibration, where the first stage implementation is described in details and the designs for stages 2 and 3 are similar. The calibration is divided into two working periods, namely measurement period and conversion period. During the measurement period, the analog front-end is configured in the bit weight measurement mode. The actual bit weight H_i^m for each capacitor is repeatedly measured and then subtracts the ideal bit weight H_{ideal}^m to get instant errors. These errors are fed into an averaging filter to obtain an averaged bit weight error H_{ei}^m , which is stored in the i^{th} error register $Errori$. Until all the bit weight errors are sequentially measured and stored in the error registers under the control of the digital machine, the measurement period is finished and the error registers remain unchanged. During the conversion period, an additional path is introduced to calculate the total bit weight errors, which are finally added to the normal conversion results. By storing and using bit weight error H_{ei}^m instead of actual bit weight H_i^m, the data bit-width participating in the calibration process is reduced, and the timing requirement for real-time digital calculation is relaxed, thus exhibiting a better potential for high-speed operation.

Note that each capacitor bit weight is measured under the practical noisy environment, the measurement accuracy is

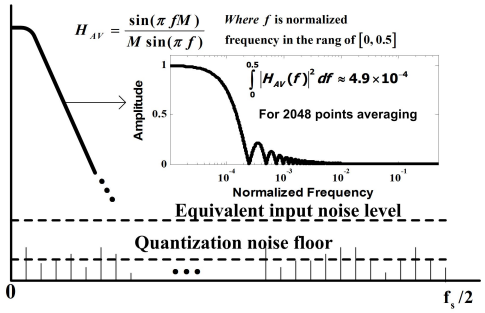


Fig. 15. Function of noise attenuation by digital averaging filter.

TABLE I
DESIGN PARAMETERS FOR THE FIRST STAGE.

Parameters	Values
Sampling capacitor (C_{total})	2 pF
Sampling rate (f_s)	250 MHz
Ideal stage gain ($1/\beta$)	8
Equivalent noise factor (η)	1.5
Back-end ADC resolution	14 bits
Average point number	2048

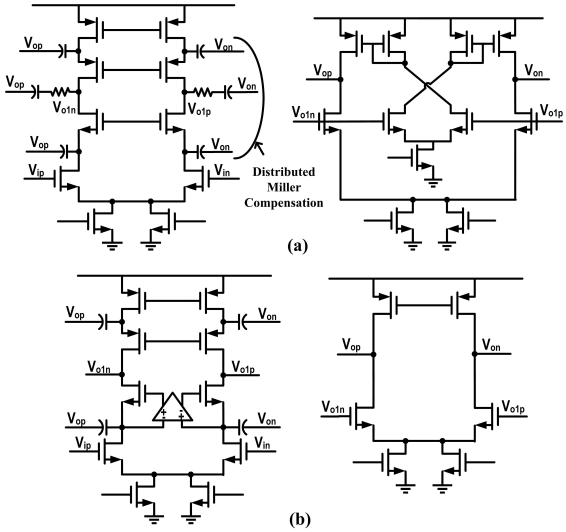


Fig. 16. Simplified schematic for (a) Op-amp in the SHA, and (b) Op-amp in pipeline stages.

highly constrained by the non-ideal factors, mainly including offset, circuit noise, and quantization error, where the circuit noise includes sampling KT/C noise, 1/f noise, and thermal noise of residue amplifier. As discussed earlier in this part, offset and 1/f noise can be chopped to high frequency, which can be suppressed by the 2048-point averaging filter. Thus, the measurement accuracy is predominantly constrained by the remaining quantization noise, sampling noise, and amplifier's thermal noise, where the equivalent input noise of the last two types can be represented by multiplying sampling noise with a factor η, where η is larger than 1. In this design, simulation results demonstrate that η should be set to 1.5. Since the stage gains are larger than the scaling factors of the capacitors between successive stages, noise in the first stage brings about a higher measurement corruption than other stages. Hence, we focus on the analysis of noise suppression in the first stage.

Here, the noise-free resolution (NFR), which is usually used to characterize the measurement accuracy of low frequency signals, is employed to estimate the measurement precision. It is defined as [25],

$$NFR = \log_2\left(\frac{Full-scale\ input\ voltage\ range}{Peak-to-peak\ input\ noise}\right), \quad (7)$$

where the peak-to-peak input noise is set to $6.6V^n_{rms}$ (V^n_{rms} is the RMS input noise) to guarantee a 99.99% confidence level.

Then, the equivalent average output noise spectrum of the first stage, i.e., the average input noise spectrum of the subsequent 14-bit back-end ADC, can be given as,

$$S_{EQA} = \frac{KT/C_{total}\cdot\eta}{f_s/2}\cdot\frac{1}{\beta^2}. \quad (8)$$

Considering the fact that the KT/C noise is much higher than the quantization noise, the average noise spectrum of the measured quantification errors of the 14-bit back-end ADC can be approximate as,

$$S_{QUA} = \frac{\Delta^2/12}{f_s/2}. \quad (9)$$

These two types of noise are further attenuated by the digital averaging filter. Therefore, the RMS noise passed to the final output, denoted as V_H^N, can be deduced by,

$$V_H^N = \sqrt{(S_{EQA}+S_{QUA})\times\frac{f_s}{2}\times\int_0^{0.5}|H_{AV}(f)|^2 df}, \quad (10)$$

where $H_{AV}(f)$, as shown in Fig. 15, is the transfer function of the averaging filter.

Finally, NFR can be calculated by,

$$NFR = \log_2\left(\frac{V_{swing}}{6.6V_H^N}\right). \quad (11)$$

Substituting the above equations with the practical parameters listed in Table I, an NFR of 14.7 bits can be obtained. It indicates that the measurement accuracy can reach 14 bits, which determines the effective number of bits that participates in the digital calibration.

VI. CRUCIAL BUILDING BLOCKS

A. Operational amplifier

Operational amplifier is one of the most important components in the whole pipelined ADC, which constraints the maximum operating speed, linearity, and power efficiency of the overall ADC. Fig. 16 describes the op-amps used in the front-end SHA and the pipeline stages. Both of them adopt a two-stage structure to achieve the requirements of high gain and high output swing, where a telescopic topology is used in the first stage to reduce the device noise and power consumption. To drive the large sampling capacitor in the first quantization stage, the op-amp in SHA employs a class AB driving stage associated with a distributed miller compensation to provide a fast settling behavior for large output swing [26]. For the op-amp exploited in the pipeline stages, a gain boosting amplifier is added to the weak NMOS path to improve the equivalent output impendence, resulting in a good balance among the requirements of high gain, high speed, and high power efficiency. Simulation results show that the op-amp in

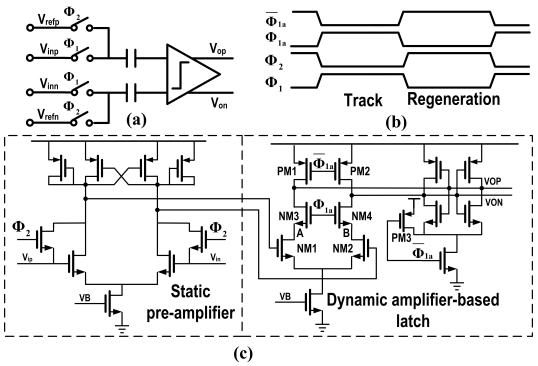


Fig. 17. (a) Switch-capacitor comparator implementation, (b) timing diagram, and (c) details of proposed comparator.

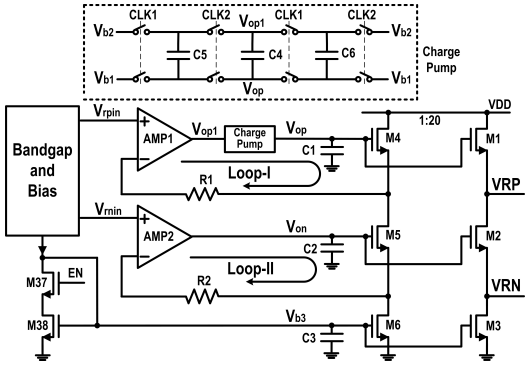


Fig. 18. A fully integrated high-speed reference buffer.

the SHA achieves a GBW of 1 GHz with a power consumption of 90 mW, while the op-amp in the first 4-bit stage consumes 72 mW to obtain a BW of 1 GHz at a gain of 18 dB.

B. Comparators

Referring to the analysis in Section IV, the effective settling time of residue amplifier is limited by the sub-ADC's resolving time t_{cmp}. Generally, this resolving time can be divided into two parts: the regeneration time introduced by decision comparators in the sub-ADC, and the propagation time induced by inevitable driving circuits and possible additional blocks for calibration configuration. As discussed in Section V, this design applies an approach based on threshold voltage adjustment to implement the reconfiguration of sub-ADC's output. Thus, the distribution time is optimized. This part will focus on the design of an improved high-speed dynamic comparator based on the design in [4], which aims to optimize the comparator's regeneration time and reset time, thus maximizing the amplifier's settling time and minimizing the instantaneously connecting time.

The proposed high-speed comparator, consisting of a static pre-amplifier and a dynamic amplifier-based latch, is depicted in Fig. 17, where the controlling timing diagram is also illustrated. During the track phase, both of the static preamplifier and the dynamic preamplifier are in amplification mode and the effective input voltage (i.e. input voltage minus the threshold voltage) is amplified onto the input nodes VOP/VON. The two stage preamplifiers dissipate 150 μA and provide a gain of about 9 dB, which not only yields a large swing to reduce the regeneration time but also effectively attenuates the offset and noise introduced by the latch. When the falling edge of Φ_{1a} arrives, the dynamic amplifier is set to high-impendence state by cutting off the transistors of PM1/PM2 and NM3/NM4. Simultaneously, the cross-coupled inverter based latch is enabled to start regenerating the output. After a non-overlapping time, Φ_2 goes up to make the input transistors of the static preamplifier connected in diode mode, and the threshold voltage associated with the offset of the static pre-amplifier is stored on the capacitor to prepare for next operating period.

The regeneration time is mainly decided by the time constant of g_m/C_p, where g_m is determined by the current flowing through the latch, and C_p is the total capacitance of the input node of the latch. To achieve high regeneration speed, the latch described in [4] employs a compact cross-coupled inverter based NMOS controlling structure to obtain a large start current, thus resulting in a high regeneration g_m (mainly contributed by the NMOS transistors). Aiming to further improve the operating speed, this design introduces a pair of cascode transistors NM3/NM4 into the dynamic amplifier (see Fig. 17(c)). During the regeneration phase, NM3/NM4 are turned off, thus a low C_{GD} can be obtained. Moreover, the size of NM3/NM4 can be designed to be much smaller than NM1/NM2 due to the full swing gate voltage, which will further reduce the parasitic capacitances. Additionally, a large size of NM1/NM2 is allowed to provide a high gain without increasing the latch load since they are isolated from the output node by NM3/NM4. Finally, the kick-back noise is also isolated by the opened transistors NM3/NM4. Simulation results show that the decision time of the modified comparator is less than 100 ps with an mV-magnitude input voltage. To obtain the desired fast resetting ability as analyzed in Section IV, a pull-up transistor PM3 that is connected to the common source of the cross-coupled latch (see Fig. 17(c)) is also added. When $\overline{\Phi}_{1a}$ goes down, PM3 provides a fast charging path to quickly pull up VON/VOP to turn off the reference selection switches, thus reducing the instantaneously connecting time between the reference and amplifier's output. Meanwhile the introduced PM3 exhibits little effect on the gain of the dynamic amplifier since the cross-coupled NMOS transistors are set in cut-off region due to the amplifier's high common mode voltage for high bandwidth considerations.

C. On chip high-speed reference buffer

As discussed in Section IV, a high-speed reference buffer is desired to provide fast charge recovery capability. However, it is rather difficult to design a negative feedback buffer with such a high bandwidth (larger than 4 times of the sampling rate). Hence, an open-loop source follower with low output impedance becomes a preferred choice [27]. Compared to PMOS transistors, NMOS transistors present a much higher efficiency of translating current into transconductance (g_m/I_D). This design exploits an NMOS source follower based buffer as shown in Fig. 18. The reference voltages VRP/VRN are generated by a separate path consisting of two stacking NMOS source followers. The gate voltages of Vop and Von are determined by Vrpin and Vrnin through the negative feedback

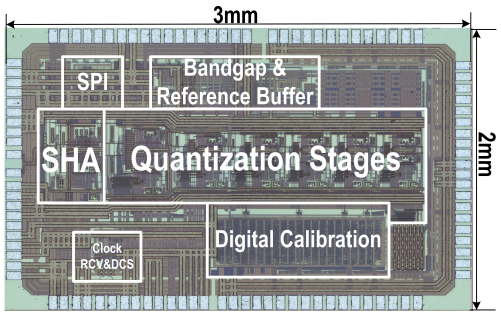


Fig. 19. Chip micrograph.

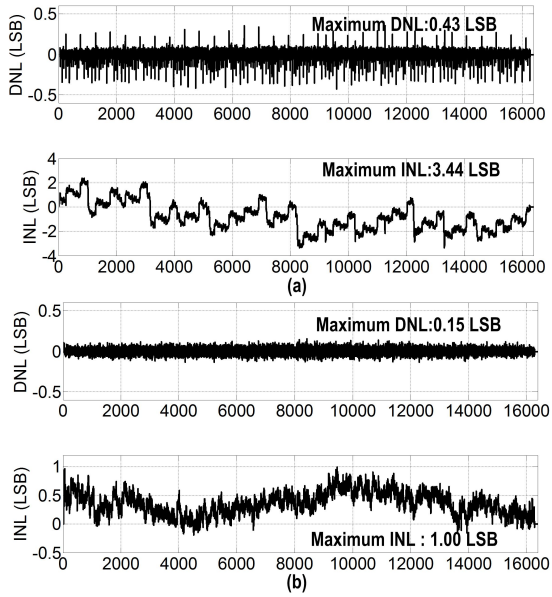


Fig. 20. Plots of DNL and INL for (a) without calibration and (b) with foreground calibration.

loops. Thus, the output impedance is mostly restricted by the transconductance of NM1 and NM2. Considering the fact that the current efficiency of NMOS is about 2-3 times higher than that of PMOS, this full NMOS implementation can achieve a high power efficiency. In addition, VDD sees high impedances to both VRN and VRP, which produces a high power supply rejection ratio (PSRR). In order to provide a large output swing, a charge pump controlled by two non-overlapping clocks is used to boot the gate voltages of M1 and M4. The input reference voltage and various biases are generated from an on-chip bandgap. To suppress the noise produced by the bandgap, low bandwidths (<1MHz) of the two loops are employed.

VII. EXPERIMENTAL RESULTS

The 14-bit pipelined ADC is fabricated in 0.18 μm 1P6M CMOS process, and it occupies an area of 6 mm^2. The die micrograph is illustrated in Fig. 19. As depicted in Fig. 20(a), the measured DNL and INL before calibration are 0.43 LSB and 3.44 LSB, respectively. After the foreground calibration, the DNL and INL are decreased to 0.15 LSB and 1.00 LSB (see Fig. 20(b)).

Fig. 21 provides the 16K-FFT plot at 250 MS/s for input frequencies of 30 MHz and 403 MHz. With a 30 MHz input

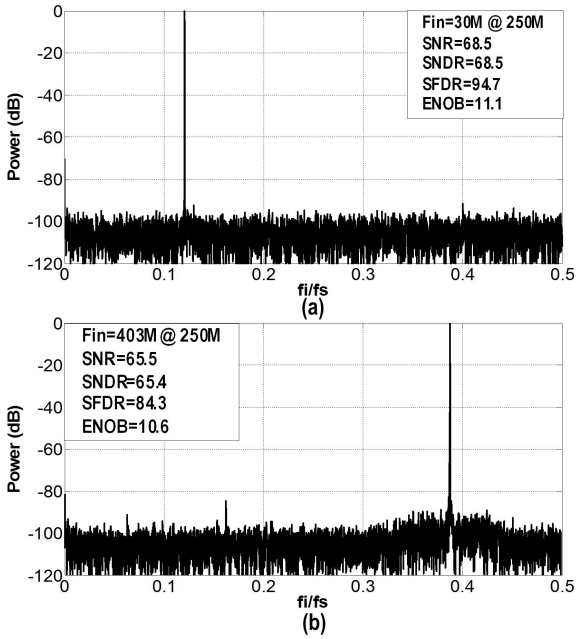


Fig. 21. FFT spectrum with 16K samples at (a) f_{in}=30 MHz and (b) f_{in}=403 MHz.

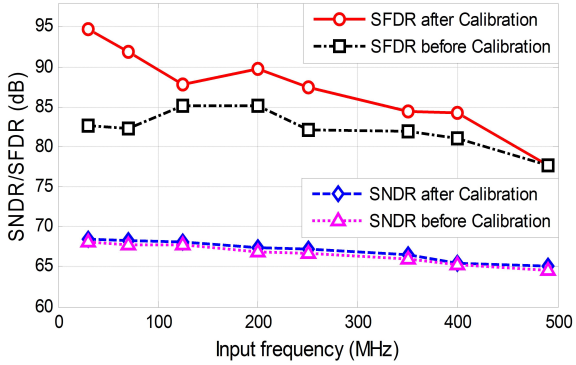


Fig. 22. Measured SFDR and SNDR versus input frequency at 250 MS/s.

signal, the ADC achieves an SFDR of 94.7 dB and an SNDR of 68.5 dB. Even the input frequency is raised to 403 MHz, the measured SFDR and SNDR can maintain 84.3 dB and 65.4 dB, respectively. The measured SFDR and SNDR before and after calibration with different input frequencies at a sampling rate of 250MS/s are depicted in Fig. 22. We can see that the proposed foreground calibration can improve the SFDR prominently up to 400 MHz. For a 490 MHz input signal, the calibration exhibits little effect on the SFDR, which implies that the input network and/or front-end SHA may become the main limitation around this frequency. Meanwhile, the SNDR at different input frequencies are slightly optimized by the digital calibration. As described in Fig. 22, when the input frequency increases form 30 MHz to 490 MHz, SFDR varies from 94.7 dB to 77.7 dB and SNDR differs from 68.5 dB to 65.1 dB for the measurements after the developed digital calibration. The pipeline ADC consume 300 mW from a 1.8 V supply at a sampling rate of 250 MS/s. Considering the fact that the latter stages are over-designed due to the minimum size capacitors, there is still potential to optimize the power dissipation through aggressive scaling of the latter stages. To evaluate the power efficiency of this ADC, the Walden figure-

TABLE II
MEASURED PERFORMANCE SUMMARY AND COMPARISON.

Reference	[3]	[8]*	[13]	[28]	[2]	[29]	[30]	This work
Technology (nm)	180	180	180	180	90	90	55	180
Supply (V)	1.8	1.8/3.0	1.8	1.8	1.2	1.2	1.1	1.8
Resolution (bit)	14	16	14	13	14	10	12	14
f_s (MHz)	100	250	100	250	100	320	200	250
DNL/INL (LSB)	0.8/2.2	0.5/3	0.18/1.1	N/A	0.9/1.3	0.96/1.75	0.28/1.89	0.15/1.0
SNDR† (dB)	69.2	76.5	65.7	65.9	69.3	51.2	63	68.2
SFDR† (dB)	87.3	94	84.1	78	78.7	66.7	76	87.9
Area (mm^2)	6.3	50	7.2	0.89	1	0.21	0.28	6.0
Power (mW)	92**	1000	220	140	250	40	30.7	300
FOM† (pJ/step)	0.39	0.73	1.40	0.35	1.05	0.42	0.13	0.57
Calibration	Background	Background	1.40	N/A	Background	Foreground	Background	Foreground
Analog Front-end	SHA-less	SHA-less	SHA	N/A	SHA-less	SHA-less	SHA-less	SHA

*Fabricated in BICMOS process; †input frequency is around Nyquist frequency; **excluding the power of reference buffers.

of-merit (FOM) [5] is calculated by,

$$FOM = \frac{Power}{2^{(SNDR-1.76)/6.02} \times f_s}, \tag{12}$$

where SNDR is the signal-to-noise-plus-distortion ratio and f_s represents the sampling rate. Table II summarizes and compares the measurement results with state-of-the-art high performance ADCs. It can be seen that the peak DNL/INL of this design outperforms the others, owing to the foreground calibration. The SFDR of the ADC in this work is comparable to the best results in [8] (fabricated in BICMOS process), which is mainly because of the integration of the improved SHA, the partial non-overlapping clock scheme associated with the proposed high speed comparator, and the costless foreground calibration.

VIII. CONCLUSION

In this paper, a 14-bit 250 MS/s pipelined ADC has been developed, which is implemented in a 180 nm CMOS process. It employs an improved SHA based on parasitic-optimized bootstrapped switches to achieve a high sampling linearity over a wide input frequency range. The foreground calibration at low cost in analog front-end helps to alleviate the errors caused by finite op-amp gain and capacitor mismatches, and also to reduce the power consumption through relaxing unit capacitor size restriction and the op-amp gain requirement. In addition, a partial non-overlapping time scheme is proposed to increase the amplifier's settling time, which is equivalent to improving the operating speed or reducing the power consumption. The DNL/INL measurements indicate that the calibration can effectively improve the static linearity of the ADC. Meanwhile, the SNDR/SFDR measurements prove that the ADC presents excellent dynamic performance at high input frequency with an efficient power consumption.

ACKNOWLEDGMENT

This work was supported by the National High Technology Research and Development Program of China (863 Program), No. 2013AA014302 and FP7-LIVECODE, No.295151.

REFERENCES

[1] J. Brunsilius *et al.*, "A 16b 80MS/s 100mW 77.6dB SNR CMOS pipeline ADC," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 2011, pp. 186–187.

[2] H. V. de Vel *et al.*, "A 1.2-V 250-mW 14-b 100-MS/s digitally calibrated pipeline ADC in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1047–1056, Apr. 2009.

[3] Z. Wang *et al.*, "A high-linearity pipelined ADC with opamp split-sharing in a combined front-end of S/H and MDAC1," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, no. 11, pp. 2834–2844, Nov. 2013.

[4] C. C. Lee *et al.*, "A SAR-assisted two-stage pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 859–869, Apr. 2011.

[5] K. H. Lee *et al.*, "A 12b 50 MS/s 21.6 mW 0.18 μm CMOS ADC maximally sharing capacitors and op-amps," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 09, pp. 2127–2136, Sep. 2011.

[6] S. Devarajan *et al.*, "A 16-bit, 125 MS/s, 385 mW, 78.7 dB SNR CMOS pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3305–3313, Dec. 2009.

[7] Y. J. Kim *et al.*, "A 12 bit 50 MS/s CMOS nyquist A/D converter with a fully differential class-AB switched op-amp," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 620–628, Mar. 2010.

[8] A. M. A. Ali *et al.*, "A 16-bit 250-MS/s IF sampling pipelined ADC with background calibration," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2602–2612, Dec. 2010.

[9] R. Sehgal *et al.*, "A 12 b 53 mW 195 MS/s pipeline ADC with 82 dB SFDR using split-ADC calibration," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1592–1603, Jul. 2015.

[10] M. Dessouky *et al.*, "Input switch configuration for rail-to-rail operation of switched opamp circuits," *Electronics Letters*, vol. 35, no. 1, pp. 8–10, Jan. 1999.

[11] S. Lee *et al.*, "A 12 b 5-to-50 MS/s 0.5-to-1 V voltage scalable zero-crossing based pipelined ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1603–1614, Jul. 2012.

[12] C. C. Lee *et al.*, "A 12b 50MS/s 3.5mW SAR assisted 2-stage pipeline ADC," in *Proc. IEEE Symp. VLSI Circ. Dig. Tech. Papers*, 2010, pp. 239–140.

[13] L. Luo *et al.*, "A digitally calibrated 14-bit linear 100-MS/s pipelined ADC with wideband sampling front end," in *Proc. IEEE European Solid-State Circuits Conf.*, Sep. 2009, pp. 472–475.

[14] C. C. Liu *et al.*, "A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 731–740, Apr. 2010.

[15] $\mathrm{MaximIntegrated}_{\mathrm{TM}}$, *Analysis of ADC System Distortion Caused by Source Resistance*, ser. Application Note 1948, Mar. 2003.

[16] A. M. A. Ali *et al.*, "A 14b 1GS/s RF sampling pipelined ADC with background calibration," in *IEEE ISSCC Dig. Tech. Papers*, 2014, pp. 482–483.

[17] L. Sumanen, M. Waltari, and K. A. I. Halonen, "A 10-bit 200-MS/s CMOS parallel pipeline A/D converter," *IEEE J. Solid-State Circuits*, vol. 36, no. 7, pp. 1048–1055, Jul. 2001.

[18] D. Mohamed and A. Kaiser, "Input switch configuration suitable for rail-to-rail operation of switched opamp circuits," *Electronics Letters*, vol. 31, no. 1, pp. 8–10, Jan. 1999.

[19] K. Agarwal *et al.*, "A duty-cycle correction circuit for high-frequency clocks," in *Proc. IEEE Symp. VLSI Circ. Dig. Tech. Papers*, 2006, pp. 106–107.

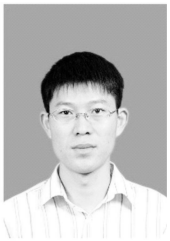
[20] I. Ahmed, *Pipelined ADC Design and Enhancement Techniques*, M. Ismail, Ed. Springer, 2010.

[21] D. Y. Chang *et al.*, "Radix-based digital calibration techniques for multi-stage recycling pipelined ADCs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 11, pp. 2133–2140, Nov. 2004.

[22] K. Iizuka *et al.*, "A 14-bit digitally self-calibrated pipelined ADC with adaptive bias optimization for arbitrary speeds up to 40 MS/s," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, pp. 883–890, Apr. 2006.
[23] Y.-S. Shu and B.-S. Song, "A 15-bit linear 20-MS/s pipelined ADC digitally calibrated with signal-dependent dithering," *IEEE J. Solid-State Circuits*, vol. 43, no. 2, pp. 342–350, Feb. 2008.
[24] Y. Chiu *et al.*, "Least mean square adaptive digital background calibration of pipelined analog-to-digital converters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 51, no. 1, pp. 38–46, Jan. 2004.
[25] Analog Device Corporation, *Data conversion handbook*, W. A. Kester, Ed. Newnes, 2005.
[26] W. J. Huang *et al.*, "A rail-to-rail class-B buffer with DC level-shifting current mirror and distributed miller compensation for LCD column drivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 8, pp. 1761–1772, Aug. 2011.
[27] C. Yang *et al.*, "An 85mw 14-bit 150MS/s pipelined ADC with 71.3dB peak SNDR in 130nm CMOS," in *Proc. A-SSCC*, 2013, pp. 85–88.
[28] M. Anthony *et al.*, "A process-scalable low-power charge-domain 13-bit pipeline ADC," in *Proc. IEEE Symp. VLSI Circ. Dig. Tech. Papers*, 2008, pp. 222–223.
[29] C. J. Tseng *et al.*, "A 10-b 320-MS/s stage-gain-error self-calibration pipeline ADC," *IEEE J. Solid-State Circuits*, vol. 47, no. 6, pp. 1334–1343, Jun. 2012.
[30] S. K. Shin *et al.*, "A 12 bit 200 MS/s zero-crossing-based pipelined ADC with early sub-ADC decision and output residue background calibration," *IEEE J. Solid-State Circuits*, vol. 49, no. 6, pp. 1366–1382, Jun. 2014.

Xuqiang Zheng received the B.S and M.S degrees from School of Physics and Electronics, Central South University, Hunan, China, in 2006 and 2009, respectively.

From 2010, he began working as a mixed signal Engineer in the Institute of Microelectronics of Tsinghua University, Beijing, China. He is currently pursuing his Ph.D. degree in University of Lincoln, Lincolnshire, United Kingdom. His research interests focus on high-performance A/D converters and high speed wire-line communication systems.



Zhijun Wang received the B.S from Xian JiaoTong University and M.S degrees from Tsinghua University, in 2004 and 2009, respectively.

From 2009, he began working as a mixed signal Engineer in the Institute of Microelectronics of Tsinghua University, Beijing, China. His research interests include analog and mixed-mode integrated circuit design.

Fule Li received the B.S. and M.S. degrees from electrical engineering, Xidian University, Xian, China, in 1996 and 1999, respectively, and the Ph.D. degree in electronic engineering from Tsinghua University, Beijing, China, in 2003.

He has been working in Tsinghua University since 2003. Now, he is an Associate Professor in the Institute of Microelectronics of Tsinghua University. His research interests include analog and mixed-mode integrated circuit design, especially high-performance data converters.

Feng Zhao received the B.Eng. degree in electronic engineering from the University of Science and Technology of China, Hefei, China, in 2000, and the M.Phil. and Ph.D. degrees in computer vision from The Chinese University of Hong Kong, Hong Kong, in 2002 and 2006, respectively.

From 2006 to 2007, he was a Post-Doctoral Fellow with the Department of Information Engineering, The Chinese University of Hong Kong. From 2007 to 2010, he was a Research Fellow with the School of Computer Engineering, Nanyang Technological University, Singapore. He was then a Post-Doctoral Research Associate with the Intelligent Systems Research Centre, University of Ulster, U.K. From 2011-2015, he was a Workshop Developer and Post-Doctoral Fellow with the Department of Computer Science, Swansea University, U.K. Since 2015, he has been with the School of Computer Science, University of Lincoln, U.K., where he is currently a Research Fellow. His research interests include image processing, biomedical image analysis, computer vision, pattern recognition, and machine learning.

Shigang Yue received the B.Eng. degree from Qingdao Technological University, Shandong, China, in 1988, and the M.Sc. and Ph.D. degrees from Beijing University of Technology (BJUT), Beijing, China, in 1993 and 1996, respectively.

He is a Professor of Computer Science in the School of Computer Science, University of Lincoln, Lincoln, U.K. He worked in BJUT as a Lecturer (1996-1998) and an Associate Professor (1998-1999). He was an Alexander von Humboldt Research Fellow (2000-2001) at University of Kaiserslautern, Germany. Before joining the University of Lincoln as a Senior Lecturer (2007) and promoted to Reader (2010) and Professor (2012), he held research positions in the University of Cambridge, Newcastle University, and the University College London (UCL), respectively. His research interests are mainly within the field of artificial intelligence, computer vision, robotics, brains and neuroscience. He is particularly interested in biological visual neural systems, evolution of neuronal subsystems and their applications, e.g., in collision detection for vehicles, interactive systems and robotics. He is the founding director of Computational Intelligence Laboratory (CIL) in Lincoln. He is the coordinator for several EU FP7 projects. Dr. Yue is a Member of IEEE, INNS, ISAL, and ISBE.

Chun Zhang received the B.S and Ph.D. degrees from the Department of Electronic Engineering, Tsinghua University, Beijing, China, in 1995 and 2000, respectively.

He has been working in Tsinghua University since 2000 till now. He worked in the Department of Electronic Engineering from 2000 to 2004. From 2005, he is an Associate Professor of the Institute of Microelectronics. His research interests include mixed signal integrated circuits and systems, embedded microprocessor design, digital signal processing, and radio frequency identification.

Zhihua Wang received the B.S., M.S., and Ph.D. degrees in electronic engineering from Tsinghua University, Beijing, China, in 1983, 1985, and 1990, respectively. In 1983, he joined the faculty at Tsinghua University, where he is a full Professor since 1997 and Deputy Director of Institute of Microelectronics since 2000. From 1992 to 1993, he was a Visiting Scholar at Carnegie Mellon University. From 1993 to 1994, he was a Visiting Researcher at KU Leuven, Belgium. His current research mainly focuses on CMOS RF IC and biomedical applications. His ongoing work includes RFID, PLL, low-power wireless transceivers, and smart clinic equipment with combination of leading edge CMOS RFIC and digital imaging processing techniques.

Prof. Wang has served as Deputy Chairman of Beijing Semiconductor Industries Association and ASIC Society of Chinese Institute of Communication, as well as Deputy Secretary General of Integrated Circuit Society in China Semiconductor Industries Association. He had been one of the chief scientists of the China Ministry of Science and Technology serves on the expert committee of the National High Technology Research and Development Program of China (863 Program) in the area of information science and technologies from 2007 to 2011. He had been an official member of China Committee for the Union Radio-Scientifique Internationale (URSI) during 2000 to 2010. He was the chairman of IEEE Solid-State Circuit Society Beijing Chapter during 1999-2009. He has been a Technologies Program Committee member of ISSCC (International Solid-State Circuit Conference) during 2005 to 2011. He is an Associate Editor for IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS and IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS¦PART II: EXPRESS BRIEFS.