Hot carrier aging of nano-scale devices: characterization method, statistical variation, and their impact on use voltage

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Abstract
Hot carrier aging (HCA) has attracted a lot of attentions recently, as it can be a lifetime limiting mechanism for both I/O and core devices. The applicability of the conventional characterization method developed for large devices to nano-scale devices is questionable, as nano-scale devices suffers from within-a-device-fluctuation (WDF). This work shows that the inclusion of WDF measured by the commercial quasi-DC SMU gives erroneous results. A method is proposed to separate the WDF from the real HCA for reliable parameter extraction of the HCA model. The lifetime and use voltage become yield dependent and the impact of statistical variations on SRAM is assessed.

1. Introduction

Hot carrier aging (HCA) used to be limiting the device lifetime in 1980s, when the device sizes were downscaled with the use voltage kept at Vdd=5 V [1,2]. Since 1990s, the reduction of Vdd has relieved HCA and the attentions have been turned to other reliability issues, such as time dependent dielectric breakdown (TDDB) [3] and negative bias temperature instability (NBTI) [4]. As Vdd becomes less than 1 V, further reduction becomes difficult, as it is limited by the silicon bandgap. Recently, HCA has been revisited [5-8], as it becomes lifetime limiting again.
When the device is large, the current under a given Vdd is stable and the device-to-device variation (DDV) is negligible. For the nano-scale devices used in the current CMOS nodes, however, DDV can be substantial [9-11]. For the same device under a given bias, the current fluctuates with time due to the random charge-discharge of traps in gate dielectric. This within-a-device-fluctuation (WDF) complicates the characterization of HCA and we propose a method for suppressing the impact of WDF on HCA. This method is then used to study the DDV of HCA and its effect on the use Vdd and SRAM.

2. Characterization method

Test samples were fabricated by an industrial 28 nm bulk CMOS process with metal gate and high-k dielectric. The channel length and width is 27 × 90 nm. HCA stresses were carried out under Vg=Vd at 125 °C [6-8].
Fig. 1a shows that HCA-induced drain current degradation, ΔId/Id, taken from two devices. There is a clear DDV. For the same device, ΔId/Id fluctuates between an upper envelope (UE) and a lower envelope (LE). The step-like change is caused by the charge-discharge of individual traps [12,13]. The simplest form of the WDF is the Random Telegraph Noise, as shown in Fig. 1b. Conventionally, HCA has been measured by the commercial source-and-measure unit (SMU), which took the average value within a period, e.g. 10 ms. The measured result is marked out as 'DC' in Fig. 1b, which is between UE and LE.

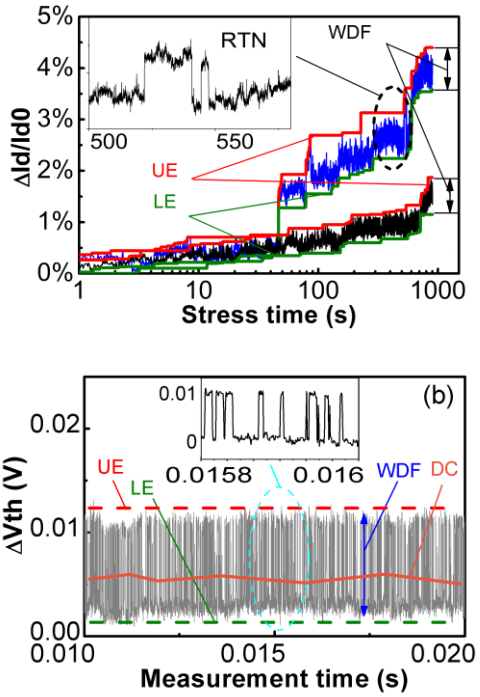

Fig. 1. (a) HCA(Vg=Vd=1.3V) of two W=90nm devices shows large DDV. WDF, UE, and LE is 'within-a-device-fluctuation', upper- and lower-envelope. (b) The simplest form of WDF: a two level RTN. The 'DC' marked out the average value within 10 ms, as used in a typical SMU [6].

It is well known that HCA follows a power law,

$$HCA=CVg^{m}t^{n}, \quad (1)$$

where 'C' is a constant. The common practice is to extract the parameters, C, m, and n, based on short time accelerated tests. The eq.(1) is then used to predict the long term HCA under use Vdd by extrapolation, as shown in Fig. 2a. The accuracy of the prediction critically depends on the accuracy of n.

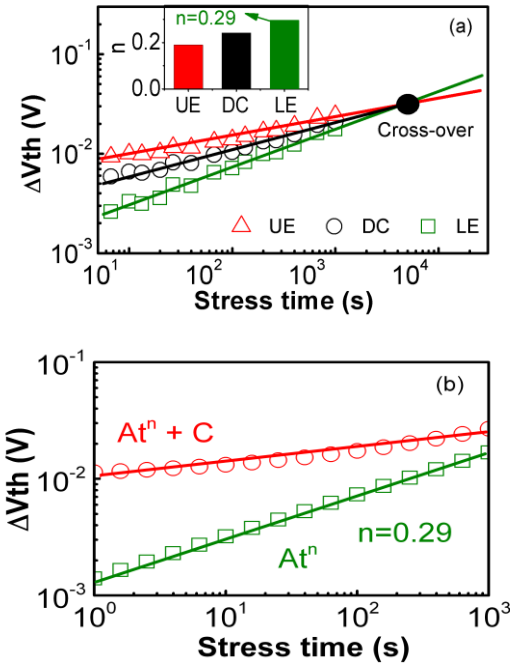

Fig. 2. (a) HCA kinetics for the mean of 40 W=90nm devices. UE, DC, and LE have different 'n' (inset). (b) Incorrect inclusion of an as-grown component, 'C', gives an apparent lower 'n' [8].

For nano-scale devices, the problem is that the ΔId/Id after a given HCA stress is not unique and fluctuates between UE and LE, as illustrated in Fig. 1a. One cannot extract the n based on the result of a single device reliably. Fig. 2 shows that the test data can be smoothed by averaging over multi-devices, but different n was obtained from UE, LE and DC data. UE gives the lowest n, while LE gives the highest. When extrapolating, they cross-over. This "cross-over" is not meaningful physically, as UE should never be smaller than LE.

Our early works on NBTI shows that aging follows an **A**s-grown-**G**eneration (AG) model, where defects were divided into two groups: As-grown traps and Generated traps [14-20]. Importantly, the charge of as-grown trap saturates once all traps were filled and only the generated defects follow a power law. The inclusion of the as-grown traps in the data will result in an apparent lower n. This is demonstrated in Fig. 2b: by adding a constant 'C' to a real power law, the data give an apparent lower n.

We believe that the lower n of UE is because the WDF contained in the UE is as-grown, i.e. WDF is not caused by HCA and does not follow the power law. To support this, Fig. 3a shows that the WDF remains the same as stress increases and Fig. 3b show the mean and standard deviation of WDF is not affected by the HCA. On the other hand, LE clearly increases with HCA, so that LE is generated by HCA. As a result, n should be extracted from LE. If the DC data measured by a typical commercial SMU is used, they are somewhere between UE and LE and contain part of WDF, as shown in Fig. 1b. As a result, the n extracted from DC data is erroneous and the quasi-DC SMU should not be used to measure the HCA of nano-scale devices. Instead, an oscilloscope should be used for the measurement to capture the WDF and separate it from LE [9].

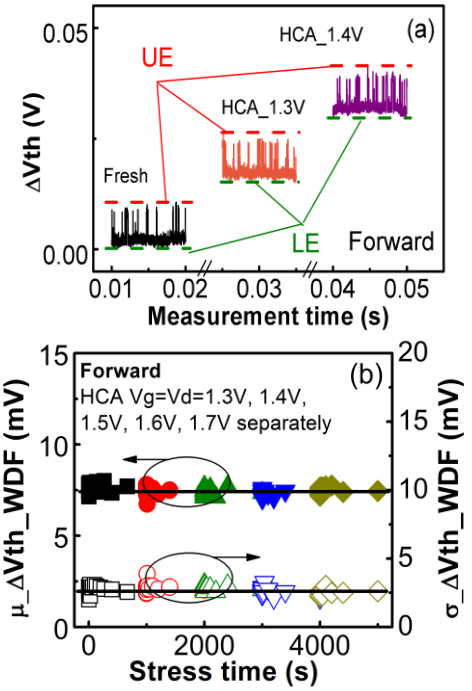

Fig. 3. (a) For L×W=27×90nm, LE increases with HCA, but WDF=UE-LE does not. (b) The μ_WDF of 40 devices and its sigma do not increase with stress time [6].

3. Statistical DDV of HCA-generated LE

Fig. 1a shows that the HCA-generated LE varies from device to device. By repeating the tests on multiple devices, the statistical properties of the DDV can be extracted. Fig. 4 gives the standard deviation, σ, against

the mean, μ. It follows a power law, as predicted by the Defect-Centric model [12].

Fig. 5 gives the statistical distributions of LE after stresses for different time (Figs. 5a&b) and under different biases (Figs. 5c&d). The spread is substantial: the maximum more than doubles the minimum in many cases.

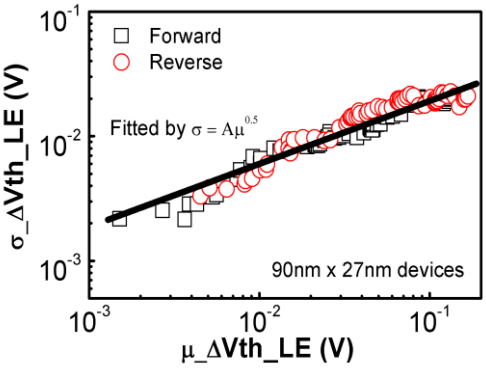

Fig. 4. Standard deviation versus the mean of HCA-induced DDV. The lines are fitted with the defect-centric distribution [8].

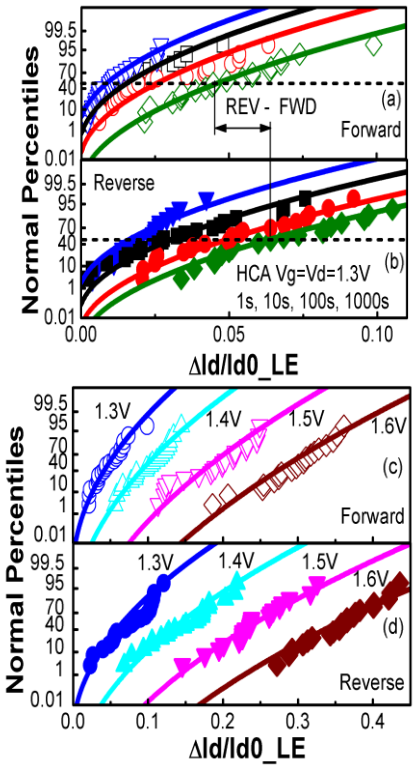

Fig. 5. The statistical distribution after different stress time (a&b) and biases (c&d). The lines are fitted with the defect-centric model [6]

The 'Forward' datasets in Fig. 5 were measured when the source and drain used for the measurement is the same as that used for stress. The 'Reverse' datasets were obtained when the source and drain for the measurement were swapped from that used for stress. It can be seen that the saturation ΔId/Id is higher for the 'Reverse'. This is because part of the generated defects are located above the space charge region between the pinch-off point and the drain under 'Forward' measurement condition and they are not sensed.

The lines in Fig. 5 are the fitted results with the Defect-Centric model. In this model, the number of defects per device have a Poisson distribution and the impact of a defect on the device has an exponential distribution [12].

4. Impact on use voltage and SRAM

A popular conventional definition for device lifetime is the time for the HCA-induced ΔId/Id reaching 10%. For large devices of little DDV, the statistical spread is zero, so that there is only one lifetime for a process. The DDV of nano-scale devices makes the lifetime definition become yield dependent.

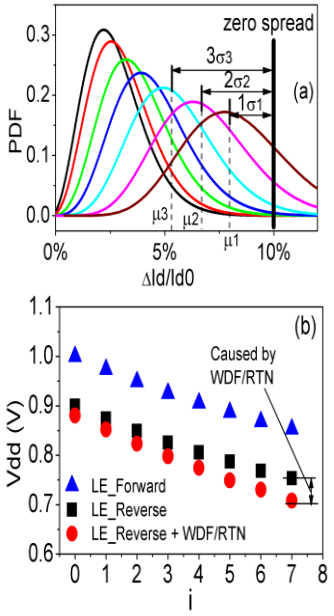

Fig. 6. Impact of DDV on use-Vdd. When Δ Id/Id reaches 10% at i × σ, the mean Δ Id/Id, μ, of defect-centric distributions reduces for higher i (a). This in turn requires a lower use-Vdd (b) [6].

For higher yield, the lifetime criterion, i.e. ΔId/Id=10%, must be met at higher i×σ, Fig. 6a shows that an increase of I shifts the distribution toward left, resulting in a smaller tolerable mean value. This in turn reduces the maximum use Vdd, as illustrated in Fig. 6b.

The impact of the HCA of the access nMOSFET in the

standard SRAM cell is simulated in Fig. 7. The HCA reduces the driving current of the access nMOSFET and weakens it. This makes the SRAM less vulnerable to read disturbance, but more resistive to writing. As a result, the static noise margin increases (Fig. 7a), but the write noise margin reduces (Fig. 7b).

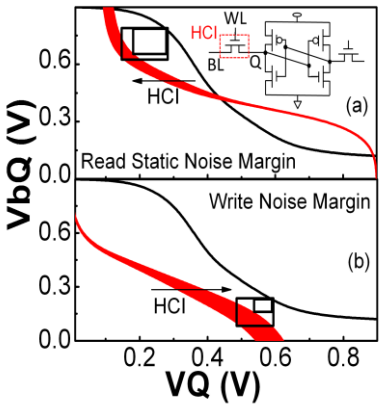

Fig. 7 Impact of HCA on static read (a) and write (b) noise margins. The spread of red curves originates from device-to-device variation of HCA [6].

5. Conclusions

A method has been proposed for characterizing the HCA of nano-scale devices. The model parameter must be extracted from the lower envelope (LE) of the within-a-device-fluctuation (WDF). To separate LE from WDF, the data should be measured by an oscilloscope, rather than the commercial quasi-DC SMU. HCA has a substantial DDV and its statistical distribution follows the Defect-Centric model well. The lifetime now is yield dependent and an increase of yield requires using lower operation bias.

Acknowledgments

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