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TDDB mechanism in a-Si/TiO$_2$ non-filamentary RRAM device

J. Ma, Z. Chai, W. Zhang, J. F. Zhang, J. Marsland, B. Govoreanu, R. Degraeve, L. Goux, G. S. Kar

Abstract—**Mechanisms of time-dependent-dielectric-breakdown (TDDB) in non-filamentary a-Si/TiO$_2$ RRAM cell (a-VMCO) have been examined in this work, including defects generation in the grain boundary, defects clustering and different defects generation rates in a-Si and TiO$_2$ layers. The unique feature of a bimodal Weibull distribution at low resistance state (LRS) and a single shallow slope distribution at high resistance state (HRS) cannot be explained by the above mechanisms. By using a combination of constant-voltage-stress (CVS), time-to-breakdown Weibull distribution and random-telegraph-noise (RTN) based defect profiling in devices of various sizes, layer thickness and processes, it is revealed that the defect profile is modulated when switching between HRS and LRS and the correlation of defect profile modulation with local defect generation rate can explain the difference in Weibull distributions at HRS and LRS. The transition from bimodal distribution at LRS to a single-steep-slope with thinner a-Si layer, and the good area scaling of Weibull distribution at HRS but not at LRS, can also be explained. The critical layers affecting the TDDB in a-VMCO are identified, providing useful guidance for device performance improvement.**

Index Terms—**Time-to-breakdown, TDDB, Si, TiO$_2$, a-VMCO, Dielectrics, RRAM, Weibull Distribution, RTN.**

I. INTRODUCTION

Resistive switching memory is a promising emerging non-volatile memory [1-8]. Good characteristics have been achieved in various binary metal-oxide based devices (RRAM), such as NiO [2], TiO$_2$ [3, 4], HfO$_2$ [5, 6], and Ta$_2$O$_5$ [7, 8]. In filamentary type RRAM, forming operation is normally needed to create a conductive filament first, and the switching between high resistance state (HRS) and low resistance state (LRS) can be considered as a progressive 'soft breakdown' and "recovery" process, controlled by oxygen vacancy modulation in the filament constriction [2-10]. Reliability issues in these devices such as retention, endurance and variability have been extensively studied [5-10]. Time-dependent-dielectric-breakdown (TDDB) has also been used to investigate the forming, switching and breakdown mechanisms [11-13]. Degradation of the critical filamentary constriction region will lead to endurance failure such as memory state stuck at either HRS or LRS or breakdown [6-13].

In contrast, resistance switching in the non-filamentary type RRAM has been attributed to the uniform defect profile modulation at the interface either with the electrode [14] and/or between two dielectric layers [15-16]. The vacancy modulated conductive oxide RRAM (a-VMCO) has demonstrated good

non-filamentary properties, such as area-dependent resistance switching, larger than ×10 resistance window, self-rectifying and self-compliance [15-16]. Its reliability issues such as retention, noise and the differences from the filamentary RRAM have been discussed in detail [17]. Further optimization was explored, for example, by using higher set/reset voltage to improve the resistive window, but this leads to degradation and causes device breakdown [18]. The breakdown mechanism in a-VMCO RRAM has not been characterized in detail yet.

The time-to-breakdown Weibull plot has been extensively used to analyze the dielectric breakdown mechanism [19-21]. In addition to the well accepted percolation model with random defect generation, further investigations have been carried out recently to explain the bimodal Weibull distribution observed in nanoscale dielectrics, for example, by the localized defect generation in grain boundaries of polycrystalline materials [22-24], defect clustering effect in SiO$_2$ or high-k oxide materials [12], or different defect generation rates in dual dielectric layers [25,26]. In this work, we will investigate the TDDB mechanism in non-filamentary a-VMCO by using the constant voltage stress (CVS) combined with Weibull plot and random telegraph noise (RTN) based defect profiling technique. In the following sections, its unique features of TDDB dependence on voltage polarity, dielectric layer thickness and cell areas will be studied to identify the breakdown mechanism.

II. DEVICES AND EXPERIMENTS

As shown in **Fig. 1a,** a-VMCO devices were fabricated with a CMOS-compatible process: The active stack consists of an 8 nm PVD amorphous silicon (a-Si) layer and on top of it, an 8nm ALD TiO$_2$ layer crystallized in anatase phase [15]. The stack is sandwiched by TiN bottom electrode (BE) and top electrode (TE). The TiO$_2$ layer serves as resistive switching layer and the a-Si acts as the barrier and oxygen-scavenging layer.

The a-VMCO features forming free, self-compliance, and analogue switching characteristics [16], as shown in the DC I-V characteristics in **Fig. 1b**. The on/off window can be enhanced by increasing the reset voltage (V$_{reset}$), but further increase will lead to degradation and cause hard breakdown [17]. In order to investigate the defects' profile and their impact, RTN measurements are carried out at incremental biases for both LRS and HRS, and the typical RTN measurement procedure and results are given in **Fig. 2a-2c**. Details of the defects and profile extraction methods and considerations can be found in refs. [18, 28]. Constant voltage stresses (CVS) are carried out to characterize the TDDB performance, which is interrupted at pre-set internals by RTN measurements to analyze the defect profiles. For each bias condition, 40-50 devices with the same size were stressed and the current was measured until reaching hard breakdown. To avoid the resistive switching during stress, CVS were applied with negative bias polarity when the cell is intrinsically at LRS, and with positive

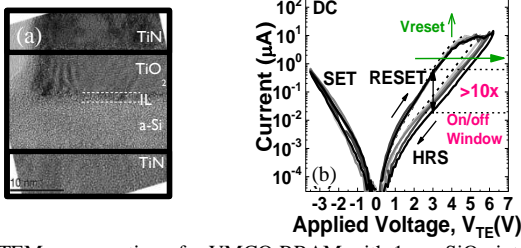polarity after it has been reset to HRS first. Table 1 summarizes the devices being used.

Fig. 1 (a) TEM cross-section of a-VMCO RRAM with 1-nm SiOx interfacial layer (IL). (b) DC switching I-V at increased Vreset. Vread=3V. Cell size 40nm.
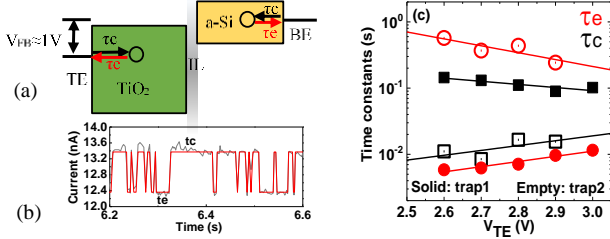

Fig. 2 (a) Illustration of the energy band diagram of a-VMCO. (b) A typical RTN signal. (c) Typical RTN time constants extracted against V_{TE} [18, 28].

Table 1: Summary of devices used in this work			
Sample	#	Layer & thickness	Process
Standard a-VMCO RRAM	W1	8nmTiO$_2$/8nm a-Si	Standard
	W2		Improved PDA
	W3		Additional pre-TiO$_2$ deposition cleaning
a-Si MSM	W4	5nm a-Si	Standard
Thin a-VMCO	W5	8nmTiO$_2$/5nm a-Si	Standard
Thin a-VMCO	W6	8nmTiO$_2$/4nm a-Si	Standard
Thin a-VMCO	W7	8nmTiO$_2$/3nm a-Si	Standard

All the above samples have sizes ranging from 40nm*40nm to 170nm* 170nm. Specific sizes used in each figure are given in the respective captions. More detailed device information can be found in refs. [15-18].

III. RESULTS AND DISCUSSIONS

A. Polarity and material dependent TDDB

TDDB of the standard a-VMCO cell with 8nm a-Si/8nm TiO$_2$ stack (W1/P1) is examined first. The time-to-failure at hard breakdown, t_{BD}, are extracted and its Weibull plot is shown in **Fig.3a&b** at opposite stress polarities, respectively [11-13].
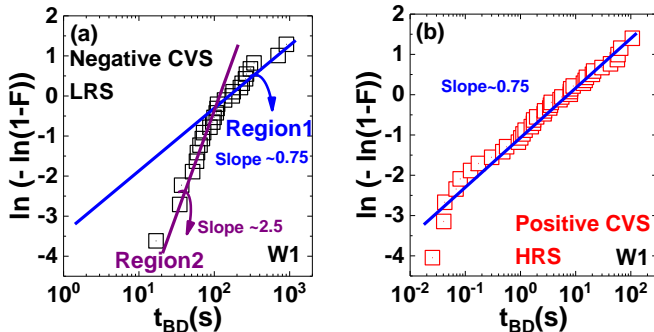

Fig. 3 Weibull distribution of time-to-failure for (a) Negative CVS of -3.5V at LRS (on-state) (b) Positive CVS of +6.6V at HRS (off-state). V$_{stress}$ is applied on a fresh device at -3.5V for LRS and at +6.6V after reset to HRS. Device structure: W1, 8 nm a-Si/8 nm TiO$_2$. Cell size: 40 nm.

For negative CVS (LRS), it exhibits the bimodal distribution behavior. For positive CVS (HRS), a single-shallow-slope Weibull distribution is observed, which is similar to the shallow one of the negative CVS. This voltage polarity dependence of breakdown and Weibull slopes have not been observed in the dielectrics in MIM capacitors or MOSFETs [11-13, 19-26].

It is generally well accepted that a percolation path will be gradually formed during the stress through random defect generation, leading to an abrupt hard breakdown and the conventional single Weibull slope with good area scaling, as observed in thicker dielectric layers [19-21]. Bimodal slopes have also been reported in nanoscale dielectrics, and several different explanations have been provided [12, 22-26]. In dielectrics with grains and grain boundaries (GB) [22-24], the steep Weibull slope at the lower percentile was attributed to breakdown at GBs leading to early device failure, and the upper percentile was mostly related to grain breakdown. Similar bimodal distribution has been observed in dual-layer structures with a transition from a steep Weibull slope at low percentiles to a shallow slope at high percentiles [25-26], and has been explained by the difference in defect generation rates in the two layers [26]. Defect clustering model has also been developed to explain the bimodal distribution in nanoscale dielectrics, by introducing the non-uniform clustering defect generation [12]. However, the co-existence of single and bimodal distributions at opposite stress polarities in a-VMCO devices in Fig. 3 has not been observed in other devices. It cannot be explained by the above mechanisms, either.
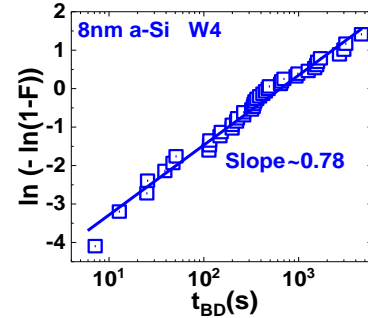

Fig.4 Weibull distribution of time-to-failure for the MSM devices with a single 8-nm amorphous-Si layer (W4), stressed at -2.0 V. Device size: 40 nm.

To further investigate the failure mechanism responsible for the bimodal distribution at negative CVS in a-VMCO (**Fig.3a**), Metal-(a-Si)-Metal (MSM) devices consisting of a single amorphous-Si layer with the same thickness as the a-Si barrier layer in a-VMCO RRAM cells [29] are stressed at negative bias. As shown in **Fig. 4,** the t_{BD} Weibull distribution for a-Si MSM has a single slope, which is the same as the shallow slope in **Fig. 3a** and in **Fig. 3b**, suggesting that the a-Si layer is responsible for the shallow slope breakdown in all these cases and the presence of TiO$_2$ reduces the early breakdown probability and causes the early steep slope at LRS. This seems agreeing well with the explanation in ref. [26] that the defect generation rate in the a-Si layer may be substantially lower than that in the TiO$_2$ layer, leading to the bimodal distribution in **Fig. 3a**. If this is the case, question remains as why it cannot be applied to TDDB at HRS (**Fig. 3b**) where a single shallow slope dominates.

B. Area and thickness dependent TDDB

Conventionally, time-to-failure follows the same Weibull distribution after area-scaling [19-20]. To further examine the Weibull slopes and the responsible failure mechanism, negative and positive CVS were performed in a-VMCO devices with different sizes and a-Si layer thickness (W2, W5-W7). The t_{BD} of large cells are scaled to the reference t_{BD} of the minimal cell by a vertical shift of $\ln(A_i/A_{Ref})$ in the Weibits plots, where A_{Ref} is minimal cell area (40*40nm) and A_i is the area of larger cells.
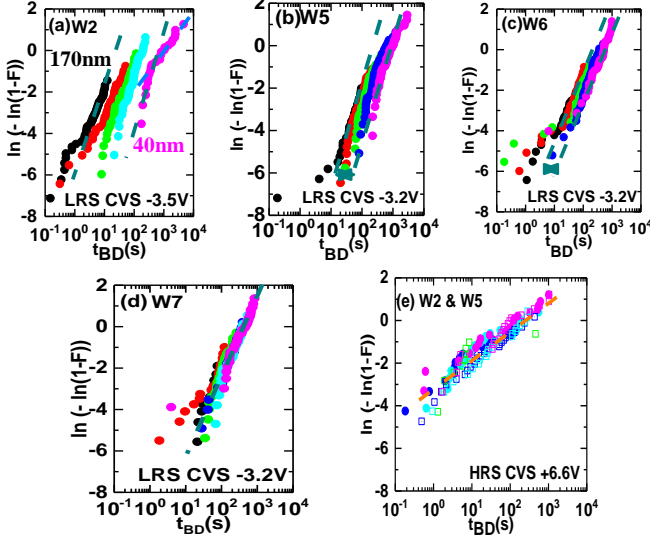

Fig. 5 (a)-(d) Area scaling results at negative CVS (LRS) with different a-Si thickness: (a) 8 nm (b) 5 nm (c) 4 nm (d) 3 nm. The TiO₂ layer thinness is 8 nm. Device sizes range between 40nm, 60nm, 90nm, 120nm and 170nm. The scaling of Weibull distribution at negative CVS improves with a-Si layer becomes thinner. Devices with thinner a-Si layers (W5-W7) are stressed under the same CVS voltage at -3.2 V. (e) Weibull distributions have good area-scaling at positive CVS showing a single shallow slope.

The area scaling results at negative CVS (LRS) with different a-Si thickness are shown in **Figs. 5a-5d**. Devices with 8nm a-Si do not scale well with area, but it improves for thinner a-Si and the distribution becomes dominated by the steeper slope. In contrast, devices stressed at positive CVS (HRS), as shown in **Figs. 5e**, scale well with area, exhibiting the shallow slope only. It is clear that the stress polarity has a significant impact on the Weibull distribution and also on how the device size and layer thickness affects the breakdown mechanism. This cannot be explained by the previously proposed mechanisms. Next we will first describe in Section III.C the defect profile difference between HRS at positive CVS and LRS at negative CVS, and also the physical process of bimodal TDDB caused by different defect generation rates. Based on their correlation, we will then investigate the TDDB polarity dependence in Section III.D.

C. Defect profile modulation and TDDB process

Defects profiles have been extracted in our precious work for both HRS and LRS using RTN signals in an unstressed a-VMCO device [18], as shown in **Fig. 6a**. Defects exist in both TiO₂ and a-Si layers. At HRS, there is defects-'less' region at TiO₂ side of TiO₂/a-Si interfacial layer (IL), which does not exist at LRS, suggesting that defect profile modulation occurs predominantly at TiO₂ side of IL. The resistance states, represented by the read out

current at $V_{TE} = 3$ V, are correlated well with the 'defects-less' region, as it becomes wider at HRS and narrower at LRS, as illustrated in **Fig. 6b**, confirming that the defect profile modulation in TiO₂ near the IL is responsible for the resistive switching. Note that this defect profile modulation is caused by the movement of pre-existing defects in un-stressed devices which have uniform spatial distribution in the lateral direction as shown in **Fig. 6b** [15-18], instead of by those defects generated by the stress. The nature of the defects responsible for resistive switching in a-VMCO device has been investigated in our previous works [15-18]. Switching in a-VMCO devices has been attributed to the distribution modulation of positively charged oxygen vacancies in the TiO₂ switching layer, through field-accelerated drift of the defects. This profile modulation of pre-existing defects provides a foundation for analyzing the TDDB mechanism in a-VMCO RRAM
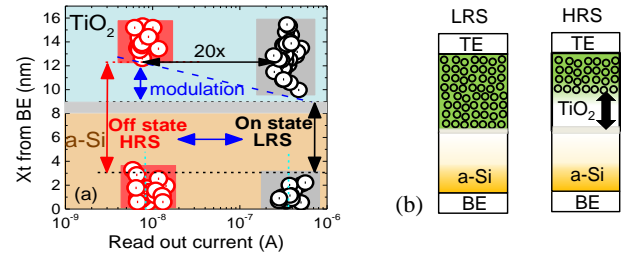

Fig. 6 Defects profile extracted based on RTN at LRS ('o') and HRS ('o'). (a) the distribution plotted vs resistance state by plotting X_T (from BE) vs. I_{read} measured at V_{TE}=3.0. Defect profile modulation predominantly occurs in a 'defect-less' region in TiO₂ near IL. (b) 'Defect-less' region becomes wider at HRS, resulting in higher resistance.

For the physical process of bimodal Weibull distribution, Raghavan et al [24, 25] reported that it could be explained and modelled by the much higher new defect generation rates (DGR) in localized grain boundaries in high-k layer. The bimodal distribution occurs only in small size devices due to the random distribution of GB where some devices may have many GBs while others may only have a few, as shown in **Figs. 7a&b**. For large size devices, the average distribution of GB across the HK film leads to a single slope, hence an overall area scaling is not valid [25]. This seems to agree well with **Fig. 5a**. Wu et al further developed the non-uniform defect clustering generation model to explain the bimodal distribution [12]. As shown in the TEM image in **Fig. 1a**, there indeed exists grains and grain boundaries in the TiO₂ layer, which may intrinsically lead to localized or clustered defect generation and higher generation rates, and contribute to the bimodal distribution.

Nigam et al [26] demonstrated that the difference in defect generation rates of the two layers can also change the Weibull distribution from bimodal to a single slope. For devices in region 1 in **Fig.3a**, the number of GBs and defects generated in the top TiO₂ layer happens to be sufficiently high so that breakdown can take place anywhere through the top layer, which acts effectively as an electrode and the breakdown is controlled by the bottom a-Si layer only, as shown in **Fig. 7a**, resulting in the shallow slope.

For devices in region 2 in **Fig.3a**, GBs and defects generated in the top TiO₂ layer is not sufficient to always warrant a conduction path when the bottom a-Si layer breaks down, as illustrated by the dashed green arrow in **Fig.7b**. The top layer

here can provide additional protection, so that the breakdown probability at low t_{BD} reduces in region 2 in **Fig.3a**, resulting in the steep slope that deviates from the shallow slope in region 1. In another word, the breakdown at low t_{BD} is controlled by both layers, as illustrated by the black arrow in **Fig.7b**.
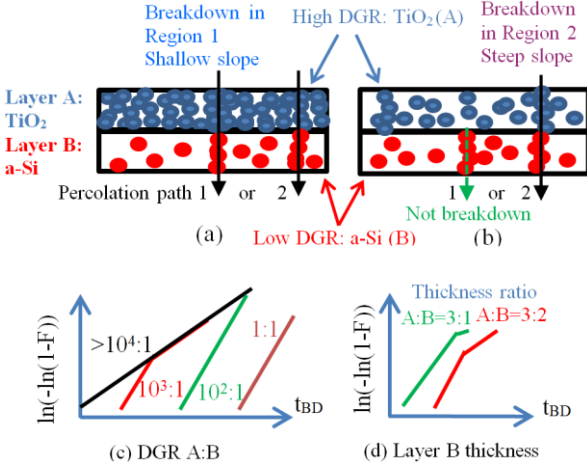

Fig. 7 Schematic illustration of the breakdown process for dual-layer dielectric stack (a) for devices in the region 1 in Fig. 2a and (b) in the region 2. The dashed green arrow indicates that the stack does not break down when the bottom layer is broken. The black arrow indicates the possible breakdown path of the stack. The impact of (c) DGR ratio in two layers and (d) a-Si layer thickness on Weibull distribution as in Ref. [26].

The results in ref. [26] can be briefly summarized in **Figs. 7c &d** as, (1) TDDB distributions are bimodal when defect generation rate is significantly different in the two layers (**Fig. 7c** A:B=10^2~10^4), where the shallow TDDB slope is limited by the more robust layer B and the Weibull slope is that of B (**Fig. 7a**); The steep slope occurs in devices that TDDB is limited by lucky events in both layers (**Fig. 7b**) and the slope is that of the entire thick stack; (2) When the difference in DGR is small (1~10^2), only steep slope can be observed (**Fig. 7c**); (3) When the difference is huge (>10^4), only shallow slope can be observed (**Fig. 7c**); (4) A thinner layer B leads to further decrease of the shallow slope, and an increase of the Weibit value where the transition occurs so that smaller sample sizes are required to observe the shallow part of the TDDB distributions due to area scaling effect (Fig. **7d**) [19-20].

In the next section, we will examine the correlation between defect profile modulation in a-VMCO and the DGR difference as proposed above, and analyze its impact on the polarity, area and thickness dependence of Weibull distribution observed in a-VMCO devices.

D. Correlation between defect profile and DGR

Since a-VMCO is at HRS when stressed at positive CVS, and is at LRS at negative CVS, the difference in pre-existing defect profile should have a significant impact on the breakdown process and mechanism, as illustrated in **Figs. 8(a-c)** by a picture of TDDB mechanism in a-VMCO RRAM. The pre-existing defect profile modulation occurs predominantly at TiO$_2$ side of IL, leading to the switching between HRS and LRS. Defect generation by CVS (●) will form a percolation path leading to the breakdown [18]. The different Weibull distributions observed in a-VMCO can be explained as follows.

As shown in **Fig. 8(a)**, at HRS ('○'), the defects-'less' region at TiO$_2$ side of TiO$_2$/a-Si interfacial layer (IL) region, which

does not exist at LRS, leads to ×10 higher overall device resistance. The good agreement between the shallow slopes in a-VMMCO in **Fig. 3b** and in the single a-Si layer MSM device shown in **Fig. 4** where the TiO$_2$ layer is absent support the TDDB is controlled by the a-Si layer. The absence of pre-existing defects in the TiO$_2$/IL region under positive CVS at HRS widens the high-resistance "defect-less" region at TiO$_2$ side of IL, as shown in **Fig. 5b**. The much higher resistance in this TiO$_2$ region leads to a very high internal electric field. Since defect generation generally follows a power law against the stress voltage and stress time, $\Delta N = A \cdot V^m \cdot t^n$, [23-26], where ΔN is the amount of degradation induced by defect generation, m and n are the power factors for stress voltage and time, respectively, and A is a constant. Higher internal electric field significantly increases the DGR, so that the breakdown is dominated by a-Si as shown in **Fig. 7a**, and hence the single slope and good area scaling under positive CVS shown in **Fig. 3b & Fig. 5e**. This also agrees well with the explanation in **Fig. 7c** when the DGR ratio is larger than 10^4.
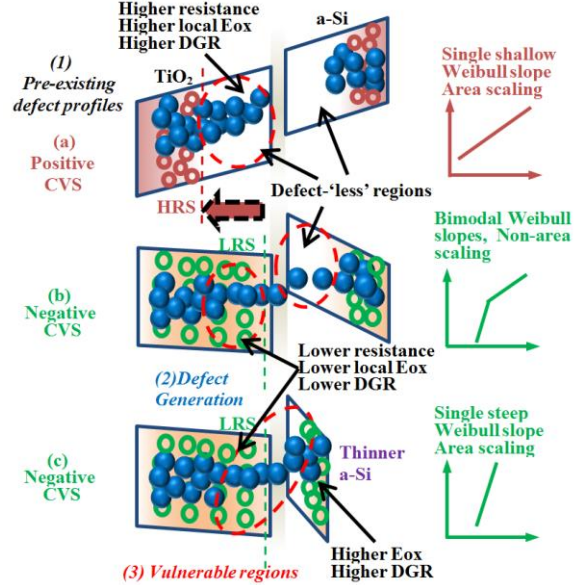

Fig. 8 The overall picture illustrating the failure mechanisms in a-VMCO RRAM (a) at positive CVS, (b) at negative CVS and (c) for thinner a-Si stack at negative CVS.

In contrast, at LRS, the pre-existing defects move back to TiO$_2$ side of TiO$_2$/a-Si IL region ('○'), as shown in **Fig. 8(b)**, similar to that occurred in a fresh device (**Fig. 6a**), leading to ×10 lower device resistance, lower internal electric field in TiO$_2$, and a relatively lower local DGR. The smaller difference in DGR between TiO$_2$ and a-Si layers results in the bimodal Weibull distribution at LRS in **Fig. 3a**, as the shallow slope of the bimodal distribution occurs in devices with higher DGRs in TiO$_2$ layer, in which the breakdown is controlled by the more robust a-Si layer, hence the shallow slope (**Fig.7a**). This is similar to what happened at positive CVS. The steep slope occurs in devices with less GBs and lower DGRs in TiO$_2$, in which the breakdown is dominated by lucky events in the entire stack. The steep slope is determined by the full thickness of the complete stack, as shown in **Fig. 7b** and also in **Fig. 7c** when the DGR ratio is between 10^2 and 10^4.

To further examine the above analysis, TDDB in devices with different process conditions that lead to different qualities in TiO$_2$ layer and at its interface are measured. As shown in **Fig. 9a & b,** W2/P2 has an improved overall processing condition with better quality in both TiO$_2$ and a-Si layer than W1/P1. The t$_{BD}$ has improved ~10 times at both CVS polarities when compared to W1. The process of W3 is improved over W2 by adding a specific cleaning treatment prior to the TiO$_2$ deposition; hence improved the quality of the TiO$_2$ only. Interestingly, as shown in Fig, 9a, further improvement of the TiO$_2$ quality alone leads to a further improvement only in the steep slope region at negative CVS, where the value of steep slope is unchanged but the Weibit at the transition point from steep slope to shallow slope becomes higher. This agrees well with refs. [25, 26] that moderately less GBs and lowered DGRs in TiO$_2$ layer will lead to longer T$_{BD}$ in the steep slope region only, as shown in **Fig. 7c**. Furthermore, the improvement of TiO$_2$ quality in W3 is not sufficient enough to reduce its DGR significantly at the high local Eox under positive CVS, so that the TDDB at positive CVS in W2 and W3 is not affected and is still dominated by the a-Si, as shown in **Fig. 9b**. This result provides strong support for the correlation between defect profiles at HRS/LRS and defect generation rates during TDDB, and hence the different Weibull distributions.
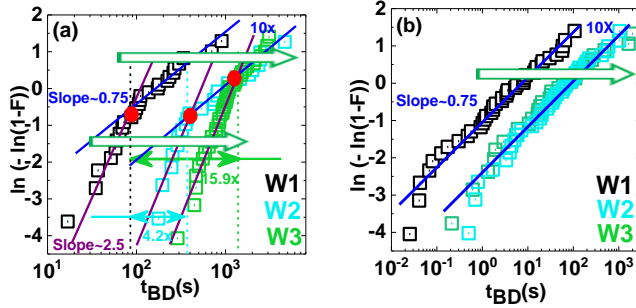

Fig. 9 Comparison of Weibull distribution of time-to-failure in processes W1, W2 and W3 for (a) Negative CVS at -3.5V, LRS (on state) (b) Positive CVS at +6.6V, HRS (off state). Cell size is 40 nm.

The above correlation can also explain the different TDDB area and thickness dependence at positive and negative stress polarities observed in **Fig. 5a-5e**. At positive CVS, the higher defect generation rate in the wide "defect-less" region in TiO$_2$ leads to a single breakdown mechanism controlled by a-Si, hence the single shallow slope and good area scaling in the Weibull distribution even when the a-Si layer is thinner, because the overall defect generation rate in a-Si is much lower than that in TiO$_2$.

At negative CVS, the difference in defect generation rate in a-Si and TiO$_2$ is smaller, but still exists, in the 8-nm TiO$_2$ / 8-nm a-Si device (W2). This leads to the bimodal distribution and prevents the good area scaling [25]. When a-Si becomes thinner **(Fig. 5b-d)** and stressed under the same voltage, the steep slope becomes dominant and the area-scaling is improved. This is because Eox in both layers increases proportionally, so that the Eox value in a-Si increases much more due to its much higher resistance than the TiO$_2$ at LRS, leading to a higher DGR in a-Si **(Fig. 8c)**, which is getting closer to that in TiO$_2$ eventually in devices with 3-nm a-Si layer and the breakdown is controlled by the entire stack. The Weibull distribution becomes

dominated by one single steep slope, and hence the better area scaling. This also agrees with **Fig. 7d** that reducing the thickness of the more robust layer in the dual layer structure leads to an increase of the Weibit value where the transition occurs and eventually a transition of Weibull distribution from bimodal slopes to a single steeper slope, as the dominating layer for TDDB shifts from the more robust layer to the entire stack [26].

To further support this analysis, Weibull distributon at negative CVS with a-Si thichness ranging from 8 nm to 3 nm, all stressed under similar electric field, are compared in **Fig. 10a**. Reducing a-Si thickness leads to the steep slope becomes slightly shallwer when all thinner devices are stressed at the same Eox =-12.6 MV/cm, apart from the occasional early failures due to lower yield. This again agrees well with **Fig. 7d**, indicating that TDDB is controlled by the entire stack. Furthermore, t$_{DB}$ under the same Eox has sinificantly improved for thinner a-Si, as confirmed in **Fig. 10b**, indicating the better overall stack quality is achieved with thinner a-Si layer.
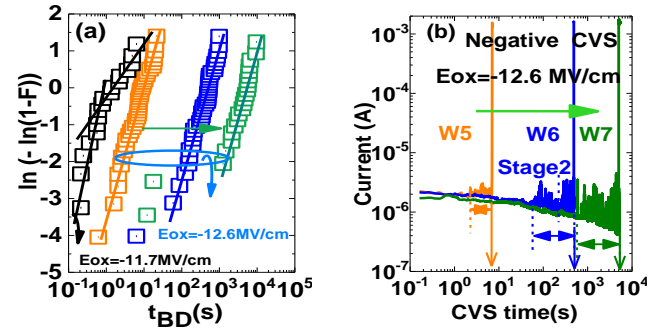

Fig. 10 (a) Time-to-failure Weibull distribution of devices with same Eox but different a-Si thickness, under negative CVS. Device size: 40 nm; TiO$_2$ thickness: 8 nm; a-Si thickness (from left to right): 8 nm (W1), 5 nm (W5), 4 nm (W6), 3 nm (W7); Thinner a-Si leads to steep slope and longer t$_{BD}$ at same Eox. (b) I-t curves comparison under the same negative electric field for thinner stacks in W5, W6 and W7.

Based on the results obtained in this work, several factors and their correlations should be considered in order to improve the TDDB in a-VMCO, including the pre-existing defect profile modulation, its impact on local electric field and DGR, the thickness of the a-Si layer, the quality of the dieletric layers and their interface. The quality of a-Si layer determines the higher percentile at negative CVS and the overall performance at positive CVS, as the defect-'less' region in a-Si is the last strong hold before the device breakdown. Using thinner a-Si layer may improve the area scaling at negative CVS, and the resultant lower yield and higher DGR may need to be mitigated, possibly by keeping the same Eox in the a-Si layer. The quality of the TiO$_2$ layer is also critical, because it, combined with the a-Si layer, determines the lower percentile of the bimodal Weibull distribution at negative CVS.

IV. CONCLUSIONS

TDDB characteristics and mechanism in non-filamentary a-VMCO RRAM are investigated in this work by using CVS and Weibull distributions combined with the defect profile modulation obtained from the RTN technique. The unique feature of a bimodal Weibull distribution at LRS and a single shallow slope distribution at HRS, including its stress polarity, device area

and a-Si layer thickness dependence, can be explained by the correlation between defect profile modulation and different defect generation rates in different layers and in grain boundaries in TiO_2. The critical layers affecting the TDDB performance are identified, which provides useful guidance for device performance improvement.

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