



LJMU Research Online

Chai, Z, Zhang, WD, Clima, S, Hatem, F, Degraeve, R, Diao, Q, Zhang, JF, Freitas, P, Marsland, J, Fantini, A, Garbin, D, Goux, L and Kar, G

Cycling induced metastable degradation in GeSe Ovonic threshold switching selector

<http://researchonline.ljmu.ac.uk/id/eprint/15425/>

Article

Citation (please note it is advisable to refer to the publisher's version if you intend to cite from this work)

Chai, Z, Zhang, WD, Clima, S, Hatem, F, Degraeve, R, Diao, Q, Zhang, JF, Freitas, P, Marsland, J, Fantini, A, Garbin, D, Goux, L and Kar, G (2021) Cycling induced metastable degradation in GeSe Ovonic threshold switching selector. IEEE Electron Device Letters. 42 (10). pp. 1148-1451.

LJMU has developed [LJMU Research Online](http://researchonline.ljmu.ac.uk/) for users to access the research output of the University more effectively. Copyright © and Moral Rights for the papers on this site are retained by the individual authors and/or other copyright owners. Users may download and/or print one copy of any article(s) in LJMU Research Online to facilitate their private study or for non-commercial research. You may not engage in further distribution of the material or use it for any profit-making activities or any commercial gain.

The version presented here may differ from the published version or from the version of the record. Please see the repository URL above for details on accessing the published version and note that access may require a subscription.

For more information please contact researchonline@ljmu.ac.uk

<http://researchonline.ljmu.ac.uk/>

Cycling induced metastable degradation in GeSe Ovonic threshold switching selector

Zheng Chai, Weidong Zhang, Sergiu Clima, Firas Hatem, Robin Degraeve, Qihui Diao, Jian Fu Zhang, Pedro Freitas, John Marsland, Andrea Fantini, Daniele Garbin, Ludovic Goux and Gouri Sankar Kar

Abstract—Ovonic threshold switching (OTS) selector is a promising candidate to suppress the sneak current paths in emerging memory arrays, but there is still a gap between its performance and the rigorous requirement from memory devices, especially its endurance improvement is hindered by insufficient understanding of the mechanism. In this work, cycling induced degradation of GeSe-based OTS selectors is studied with electrical characterization techniques. The existence of metastable state between the on- and off-state during cycling is observed and statistically analyzed alongside with the gradual off-state leakage current increase. Such metastable degradation may be attributed to the generation of unstable Ge-Ge bonds that might be induced by element segregation, which is also responsible for the higher off-state leakage current in GeSe selectors after large cycling or with higher Ge component. This work provides experimental guidance for optimizing OTS selectors.

Index Terms—selector, OTS, GeSe, endurance, reliability

I. INTRODUCTION

SELECTORS are two-terminal volatile devices used in series with the resistive-switching element, such as Spin-Transfer Torque Magnetic Random-Access Memory (STT-MRAM), Resistive Random-Access Memory (RRAM) and Phase-change memory (PCM), to suppress the sneak-path current in memory arrays [1]-[3]. GeSe Ovonic threshold switching (OTS) selectors have recently demonstrated strong performance with high on-state current, nonlinearity and endurance [4]-[8], [15]-[22]. However, detailed study of its reliability is still lacking and the understanding on the responsible mechanism is limited.

Selectors need to be turned on and off during both the writing and reading of the memory elements. Therefore, better endurance is required even than that for memory elements. The emerging memory devices have achieved excellent program records: RRAM and STT-MRAM devices have already achieved write/erase endurance records of 10^8 - 10^{12} [9]-[13]. This sets rigorous targets for selector development. For the chalcogenide OTS selectors, although endurance of 10^{10} in GeSe-based devices by using a recovery scheme [14] and 10^{12} in SiGeAsTe material without recovery scheme [15] have been achieved, it is still desirable to achieve a higher target. The effort to overcome the existing gap, via material engineering or

structure optimization, is hindered by a lack of in-depth understanding of endurance failure.

In this work, cycling induced degradation of GeSe-based OTS selectors is studied with electrical characterization techniques. The existence of metastable state between the on- and off-state during cycling is observed and statistically analyzed, alongside with the gradual off-state leakage current increase. Such metastable degradation may be attributed to the generation of unstable Ge-Ge bonds induced by the element segregation, which are also responsible for the higher off-state leakage current of GeSe selectors after large cycling or with higher Ge component. This work provides experimental guidance for further optimizing the OTS selectors.

II. DEVICE AND CHARACTERIZATION

Amorphous $\text{Ge}_x\text{Se}_{1-x}$ films were sandwiched between two TiN electrodes to form a TiN/ $\text{Ge}_x\text{Se}_{1-x}$ /TiN structure. The OTS devices were integrated in a 300 nm process flow and device size was defined by the TiN bottom electrode [5]. The $\text{Ge}_x\text{Se}_{1-x}$ chalcogenide films were achieved and passivated a low-temperature BEOL process scheme. Unless otherwise stated, the device size is 65 nm and the $\text{Ge}_x\text{Se}_{1-x}$ thickness is 10 nm. **Fig. 1a** shows the typical I-V of a triangular switching pulse. Devices with $x = 0.4$ and 0.6 are comparatively studied. The fast I-V characterization was done with a Keysight B1500A semiconductor analyzer with embedded B1530A Waveform Generator/Fast Measurement Unit (WGFMU). Before normal switching, the device is first-fired (FF) with a stronger amplitude of 6V and rise/fall time of 1 μs . Off-state leakage current is measured with DC from -1 V to 1 V [16].

III. RESULTS AND DISCUSSIONS

The off-state current of a fresh OTS device remains very low until the voltage reaches the threshold voltage (V_{th}) where the current abruptly increases by several orders to the on-state (**Fig. 1a**). The off-state leakage current is area dependent at fresh-state before FF, and area independent after FF, indicating the formation of a volatile conductive path during FF (**Fig. 1b&c**). The ab-initio calculation in our earlier work reveals that the OTS volatile switching in $\text{Ge}_x\text{Se}_{1-x}$ is based on the modulation of electronic structure of mis-coordinated amorphous Ge-Ge

This work was supported by the EPSRC of U.K. under EP/M006727/1 & EP/S000259/1. (Corresponding author: Zheng Chai, Weidong Zhang)

Zheng Chai and Qihui Diao are with the Center for Spintronics and Quantum Systems, State Key Laboratory for Mechanical Behavior of Materials, and School of Materials Science and Engineering, Xi'an Jiaotong University, Xi'an, China. (e-mail: zheng.chai@xjtu.edu.cn)

Weidong Zhang, Jian Fu Zhang, Pedro Freitas and John Marsland

are with the School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K. (e-mail: w.zhang@ljmu.ac.uk).

Sergiu Clima, Robin Degraeve, Andrea Fantini, Daniele Garbin, Ludovic Goux and Gouri Sankar Kar are with imec, 3001 Leuven, Belgium.

Firas Hatem is with the Huawei Technologies Research & Development (UK) Ltd.

bonds as tail states, and the high electric field at V_{th} and the charge injection to conductive band lead to the Ge-Ge bond over-coordinated and thus transitioned from the ground state to the excited state with a much reduced mobility gap, delocalized with large physical size and lower energy level. [14-16]. This is further supported by the excitation energy (E_a) measurement which evidences that the defects in a fresh device are localized and at above the electrode's Fermi level with a high energy barrier of 0.43 eV, leading to very low leakage via Poole-Frenkel tunneling [14]. When they are delocalized at switch-on, a filament is formed with ohmic-like conduction via defect-to-defect tunneling and with the E_a reduced to nearly 0 eV. Some of the slower defects remain delocalized after switch-off so that a much weaker filament is retained at off-state.

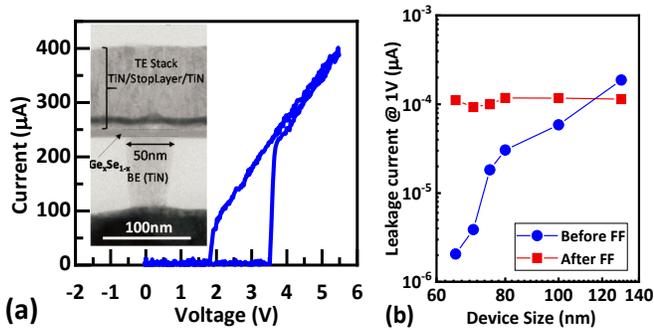


Fig.1. (a) Volatile switching of a $Ge_{0.6}Se_{0.4}$ OTS selector. Inset: TEM of the selector. (b) Off-state leakage current measured with DC is area dependent at fresh-state and area independent after FF.

As cycling number increases, the endurance degradation of OTS selectors is a gradual process as demonstrated in Fig. 2a. The $Ge_{0.6}Se_{0.4}$ device is switched for 10^6 cycles, and the off-state current increase can be clearly observed. Eventually, the volatile switching is entirely overwhelmed, as the non-linearity totally disappeared completely after 1M cycles. Such endurance performance is common for Ge_xSe_{1-x} selectors [17]-[22]. Endurance of more than 10^{10} in GeSe-based devices has been achieved in our earlier work by using a recovery scheme [14], make this device meet the requirement of selector specification. The off-state current increase with cycling is confirmed by the off-state leakage current measurement at low bias in Fig. 2b.

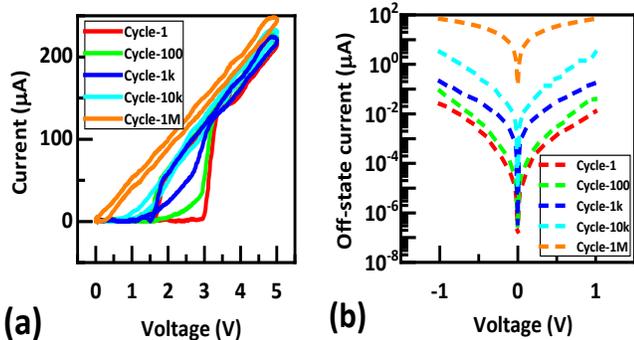


Fig.2. (a) Observation of the leakage current increasing during AC cycling. Volatile switching (VS) is entirely overwhelmed by off-state leakage current after 1M cycles. (b) Off-state leakage current increase with cycling is confirmed by DC I-V measurement at low bias.

Our previous works have reported the observation of delayed switch-on in fresh OTS devices during constant voltage stress (CVS), with the time-to-switch-on (t_{on}) following the Weibull

distribution [23]. Despite this, the device remains at the on-state until CVS ends (Fig. 3a). In the cycled devices, however, the scenario is more complex, as severe current fluctuations can be observed after the device is already switched on. The fluctuations happen between discrete levels including the on-state, the degraded off-state, and a metastable-state in the on/off window (Fig. 3b). Such fluctuation is also observed when the device is biased near the hold voltage after being firstly switched on using a triangular pulse (Fig. 3c-d). The fluctuations between the on-state and the metastable-state will further reduce the usable on/off window besides the increased off-state current, while those between the metastable-state levels and the degraded off-state will cause erroneous selector switch-offs which are not acceptable for the memory program and read operations.

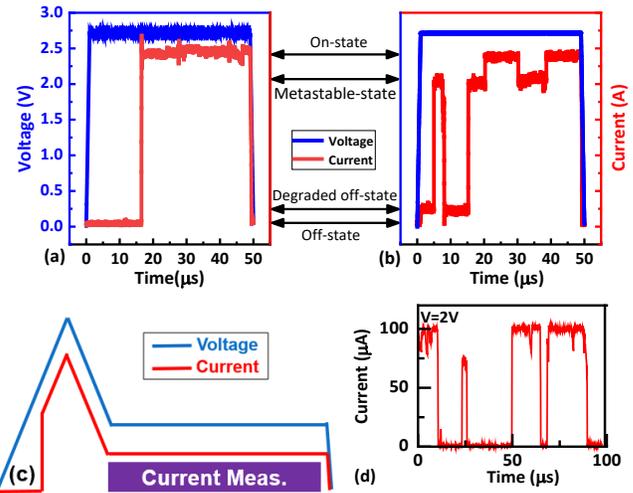


Fig.3. (a) Current response to CVS in a normal device, after t_{on} , the device remains at on-state until the CVS ends. (b) Current response in the same device after 1k cycles. After switch-on, current fluctuates between the on-state level, the degraded off-state level, and some metastable-state levels in the on/off window. (c) Waveform that firstly switch-on the device using a triangular pulse and then bias it at a constant voltage level near V_{hold} . (d) Current fluctuation can also be observed close to the hold voltage.

Such fluctuations are further analyzed statistically in multiple CVS cycles and at various voltage amplitudes. Fig. 4a demonstrates all the current responses measured during 100 CVS cycles with an amplitude of 2.7 V and a width of 50 μs . It is clear that, after switching on, the current fluctuates between three states: the on-state, the degraded off-state and a metastable state. This metastable state, along with the on- and off-states, increases linearly with the voltage amplitude in the range from 2.6 V to 2.9 V and the trend seems in parallel to the off-state curve (Fig. 4b). The static distribution and dynamic series autocorrelation between the three levels are visualized using histogram and time lag plot as shown in Fig. 4(c, d-g).

Although the three states can be found at all the 4 voltage amplitudes as plotted in Fig. 4b, their distributions are quite different: the current has a larger probability to be fluctuating between the lower two states at lower voltage, and between the higher two states at higher voltage. 2.7 V seems a balanced bias point where the metastable state has an equal probability to interact with both the on- and degraded off-state (Fig. 4c). The

direction of state interaction is shown in the time lag plot (**Fig. 4 (d-g)**). Taking $y=x$ as the line of symmetry, more points on one side of this line indicate that the current tends to fluctuate more in one direction: for example, more rise to the higher level and less return when more points are above the line. At higher voltages, the fewer points below the $y=x$ line and also fewer in its lower half indicate a smaller probability of current falling from a higher state to a lower one and more interactions between the intermediate and on states.

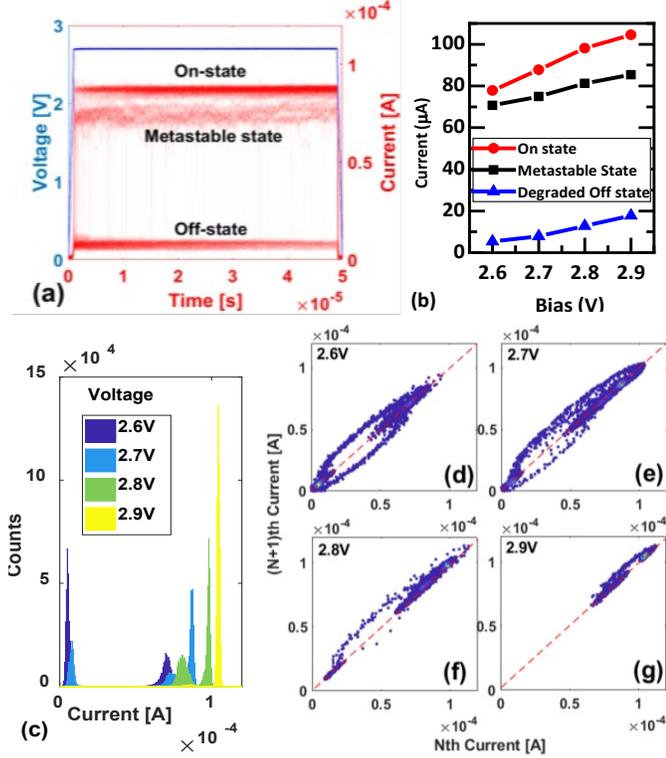


Fig.4. (a) Current response during 100 CVS cycles with an amplitude of 2.7 V and a width of 50 μ s; (b) Averaged current at on-state, metastable state and degraded off-state, at 2.6V ~ 2.9V. (c) Histogram of current at 2.6V ~ 2.9V; (d-g) Time lag plot of the current measured at 2.6V ~ 2.9V with $y=x$ as the line of symmetry.

The above observations reveal that during cycling, accompanied with the off-state current increase, a metastable state is generated, resulting in on/off reduction and device on-state instability. For comparison, a GeSe device with $x = 0.4$ is tested under the same cycling conditions. The off-state leakage current of the relative Ge-poor device is lower than the Ge-rich one before 10^4 cycles (**Fig. 5a**). With lower leakage current, such metastable state cannot be observed at earlier cycles, until after 10^4 cycles when the leakage currents reach roughly the same level (**Fig. 5b**). This could be attributed to that the two types of devices have the identical degradation mechanism: the generated Ge-Ge bonds. The larger number of Ge-Ge bonds pre-existing in $\text{Ge}_{0.6}\text{Se}_{0.4}$ make it easier to generate new Ge-Ge bonds in the earlier cycles, thus a larger number of generated conductive defects may form a cluster and facilitate the formation of an intermediate conduction path which leads to the metastable state. As reported in our earlier work, element segregation, which causes degradation in the device, may contribute to the generation of new unstable Ge-Ge bonds and the formation of such intermediate conduction paths.

These newly generated Ge-Ge bonds are weaker and less stable than the pre-existing ones so that part of them can switch either towards the off state or towards the on state, depending on the bias amplitude. In the $\text{Ge}_{0.4}\text{Se}_{0.6}$ device, however, more additional unstable Ge-Ge bonds need to be generated/activated during longer cycling for the same phenomenon to occur. This agrees with the ab initio calculation and the excitation energy measurement, which links the volatile switching of $\text{Ge}_x\text{Se}_{1-x}$ to the modulation of electronic structure of mis-coordinated amorphous Ge-Ge bonds as tail states [14] [16] [24]. Increasing the proportion of Ge component may not only modulate the switching behavior, but also change the endurance performance as it becomes easier for more unstable new Ge-Ge bonds to be generated. As demonstrated in our earlier work, the endurance performance of $\text{Ge}_{0.4}\text{Se}_{0.6}$ OTS can be improved by more than 5 orders after applying a recovery negative pulse in each 5,000 cycles [14], as the negative pulse can prevent the element segregation, which happens only after larger cycling. Since the metastable can only be observed after 10k cycles as shown in Fig. 5(b), the recovery negative pulse is also an effective method to prevent the metastable state.

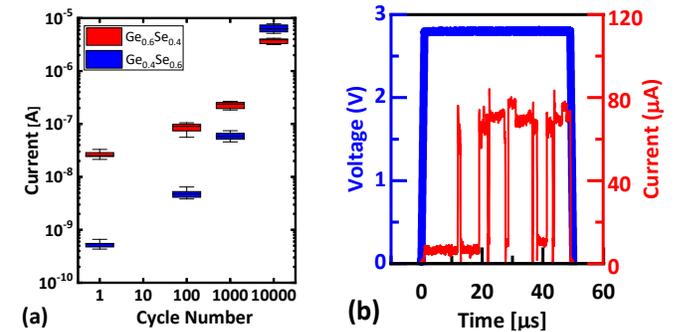


Fig.5. (a) Commonly in 5 devices, $\text{Ge}_{0.4}\text{Se}_{0.6}$ device shows lower off-state current in the early cycles (<10k cycles) than the $\text{Ge}_{0.6}\text{Se}_{0.4}$ one. (b) Metastable states in the degraded $\text{Ge}_{0.4}\text{Se}_{0.6}$ device can still be observed, after 10k cycles.

IV. CONCLUSIONS

In this work, cycling induced metastable degradation of GeSe-based OTS selectors is studied with electrical characterization techniques. The existence of metastable state between the on- and off-state during cycling is observed and statistically analyzed, alongside with the gradual leakage current increase. Such metastable degradation may be attributed to the generation of new unstable Ge-Ge bonds, which is also responsible for the higher off-state leakage current of GeSe selectors after cycling or with higher Ge component. This work provides experimental guidance for further optimizing OTS selectors.

REFERENCES

- [1] L. Zhang, B. Govoreanu, A. Redolfi, D. Crotti, H. Hody, V. Paraschiv, S. Cosemans, C. Adelman, T. Witters, S. Clima, Y.Y. Chen, P. Hendrickx, D.J. Wouters, G. Groeseneken, M. Jurczak, "High-drive current ($>1\text{MA}/\text{cm}^2$) and highly nonlinear ($>10^3$) TiN/amorphous-Silicon/TiN scalable bidirectional selector with excellent reliability and its variability impact on the 1S1R array performanc," *IEEE International*

- Electron Devices Meeting.*, San Francisco, CA, 2014, pp. 6.8.1-6.8.4. doi: 10.1109/IEDM.2014.7047000.
- [2] Q. Luo, J. Yu, X. Zhang, K.-H. Xue, J.-H. Yuan, Y. Cheng, T. Gong, H. Lv, X. Xu, P. Yuan, J. Yin, L. Tai, S. Long, Q. Liu, X. Miao, J. Li, M. Liu, "Nb_{1-x}O₂ based Universal Selector with Ultra-high Endurance (>10¹²), high speed (10ns) and Excellent V_{th} Stability," *IEEE Symposium on VLSI Technology.*, Kyoto, Japan, 2019, pp. T236-T237. doi: 10.23919/VLSIT.2019.8776546.
- [3] A. Chen, "Comprehensive methodology for the design and assessment of crossbar memory array with nonlinear and asymmetric selector devices," *IEEE International Electron Devices Meeting.*, Washington, DC, 2013, pp. 30.3.1-30.3.4. doi: 10.1109/IEDM.2013.6724723.
- [4] Myoung-Jae Lee, Dongsoo Lee, Hojung Kim, Hyun-Sik Choi, Jong-Bong Park, Hee Goo Kim, Young-Kwan Cha, U-In Chung, In-Kyeong Yoo, Kinam Kim, "Highly-scalable threshold switching select device based on chalcogenide glasses for 3D nanoscaled memory arrays," *IEEE International Electron Devices Meeting.*, San Francisco, CA, 2012, pp. 2.6.1-2.6.3. doi: 10.1109/IEDM.2012.6478966.
- [5] B. Govoreanu, G.L. Donadio, K. Opsomer, W. Devulder, V.V. Afanas'ev, T. Witters, S. Clima, N.S. Avasarala, A. Redolfi, S. Kundu, O. Richard, D. Tsvetanova, G. Pourtois, C. Detavemie, L. Goux, G. S. Kar, "Thermally stable integrated Se-based OTS selectors with >20 MA/cm² current drive, >3.10³ half-bias nonlinearity, tunable threshold voltage and excellent endurance," *IEEE Symposium on VLSI Technology.*, Kyoto, 2017, pp. T92-T93. doi: 10.23919/VLSIT.2017.7998207.
- [6] N.S. Avasarala, G. L. Donadio, T. Witters, K. Opsomer, B. Govoreanu, A. Fantini, S. Clima, H. Oh, S. Kundu, W. Devulder, M. H. van der Veen, J. Van Houdt, M. Heyns, L. Goux, G. S. Kar, "Half-threshold bias Ioffreduction down to nA range of thermally and electrically stable high-performance integrated OTS selector, obtained by Se enrichment and N-doping of thin GeSe layers," *IEEE Symposium on VLSI Technology.*, Honolulu, HI, 2018, pp. 209-210. doi: 10.1109/VLSIT.2018.8510680.
- [7] S. Yasuda, K. Ohba, T. Mizuguchi, H. Sei, M. Shimuta, K. Aratani, T. Shiimoto, T. Yamamoto, T. Sone, S. Nonoguchi, J. Okuno, A. Kouchiyama, W. Otsuka, K. Tsutsui, "A cross point Cu-ReRAM with a novel OTS selector for storage class memory applications," *IEEE Symposium on VLSI Technology.*, Kyoto, 2017, pp. T30-T31. doi: 10.23919/VLSIT.2017.7998189.
- [8] Yunmo Koo, Kyungjoon Baek, Hyunsang Hwang, "Te-based amorphous binary OTS device with excellent selector characteristics for x-point memory applications," *IEEE Symposium on VLSI Technology.*, Honolulu, HI, 2016, pp. 1-2. doi: 10.1109/VLSIT.2016.7573389.
- [9] Z. Zhang, Y. Wu, H.-S.P. Wong, and S.S. Wong, "Nanometer-Scale HfO_x RRAM," *IEEE Electron Device Letters.*, vol. 34, no. 8, pp. 1005-1007, Aug. 2013. doi: 10.1109/LED.2013.2265404.
- [10] B. Govoreanu, G.S. Kar, Y.Y. Chen, V. Paraschiv, S. Kubicek, A. Fantini, I.P. Radu, L. Goux, S. Clima, R. Degraeve, N. Jossart, O. Richard, T. Vandeweyer, K. Seo, P. Hendrickx, G. Pourtois, H. Bender, L. Altimime, D.J. Wouters, J.A. Kittl, M. Jurczak, "10×10nm² Hf/HfO_x crossbar resistive RAM with excellent performance, reliability and low-energy operation," *IEEE International Electron Devices Meeting.*, Washington, DC, 2011, pp. 31.6.1-31.6.4. doi: 10.1109/IEDM.2011.6131652.
- [11] C. Nail, G. Molas, P. Blaise, G. Piccolboni, B. Sklenard, C. Cagli, M. Bernard, A. Roule, M. Azzaz, E. Vianello, C. Carabasse, R. Berthier, D. Cooper, C. Pelissier, T. Magis, G. Ghibaudo, C. Vallée, D. Bedeau, O. Mosendz, B. De Salvo, and L. Perniola, "Understanding RRAM endurance, retention and window margin trade-off using experimental results and simulations," *IEEE International Electron Devices Meeting.*, San Francisco, CA, 2016, pp. 4.5.1-4.5.4. doi: 10.1109/IEDM.2016.7838346.
- [12] J.J. Kan, C. Park, C. Ching, J. Ahn, Y. Xie, M. Pakala, S.H. Kang, "A Study on Practically Unlimited Endurance of STT-MRAM," *IEEE Transactions on Electron Devices.*, vol. 64, no. 9, pp. 3639-3646, Sept. 2017. doi: 10.1109/TED.2017.2731959.
- [13] H. Sato, H. Honjo, T. Watanabe, M. Niwa, H. Koike, S. Miura, T. Saito, H. Inoue, T. Nasuno, T. Tanigawa, Y. Noguchi, T. Yoshiduka, M. Yasuhira, S. Ikeda, S.-Y. Kang, T. Kubo, K. Yamashita, Y. Yagi, R. Tamura, T. Endoh, "14ns write speed 128Mb density Embedded STT-MRAM with endurance>10¹⁰ and 10 yrs retention @85°C using novel low damage MTJ integration process," *IEEE International Electron Devices Meeting.*, San Francisco, CA, 2018, pp. 27.2.1-27.2.4. doi: 10.1109/IEDM.2018.8614606.
- [14] F. Hatem, Z. Chai, W. Zhang, A. Fantini, R. Degraeve, S. Clima, D. Garbin, J. Robertson, Y. Guo, J.F. Zhang, J. Marsland, P. Freitas, L. Goux, and G.S. Kar, "Endurance improvement of more than five orders in Ge_xSe_{1-x} OTS selectors by using a novel refreshing program scheme," *IEEE International Electron Devices Meeting.*, San Francisco, CA, USA, 2019, pp. 35.2.1-35.2.4. doi: 10.1109/IEDM19573.2019.8993448.
- [15] D. Garbin, M. Pakala, A. Cockburn, C. Detavernier, R. Delhougne, L. Goux, G.S. Kar, W. Devulder, R. Degraeve, G.L. Donadio, S. Clima, K. Opsomer, A. Fantini, D. Cellier, W.G. Kim, "Composition Optimization and Device Understanding of Si-Ge-As-Te Ovonic Threshold Switch Selector with Excellent Endurance," *IEEE International Electron Devices Meeting.*, San Francisco, CA, USA, 2019, pp. 35.1.1-35.1.4. doi: 10.1109/IEDM19573.2019.8993547.
- [16] Z. Chai, W. Zhang, R. Degraeve, S. Clima, F. Hatem, J. F. Zhang, P. Freitas, J. Marsland, A. Fantini, D. Garbin, L. Goux and G.S. Kar, "Evidence of filamentary switching and relaxation mechanisms in Ge_xSe_{1-x} OTS selectors," *IEEE Symposium on VLSI Technology.*, Kyoto, Japan, 2019, pp. T238-T239. doi: 10.23919/VLSIT.2019.8776566.
- [17] Bing Song, Hui Xu, Sen Liu, Haijun Liu, Qi Liu & Qingjiang Li, An ovonic threshold switching selector based on Se-rich GeSe chalcogenide, *Applied Physics A*, Vol. 125, No. 772, 2019, DOI: 10.1007/s00339-019-3073-z
- [18] Guangyu Liu, Liangcai Wu, Xin Chen, Tao Li, Yong Wang, Tianqi Guo, Zhongyuan Ma, Min Zhu, Sannian Song and Zhitang Song, The investigations of characteristics of GeSe thin films and selector devices for phase change memory, *Journal of Alloys and Compounds*, Vol. 792, July 2019, 510-518
- [19] A. Verdy, G. Navarro, V. Sousa, P. Noé, M. Bernard, F. Fillot, G. Bourgeois, J. Garrione and L. Perniola, Improved Electrical Performance Thanks to Sb and N Doping in Se-rich GeSe-Based OTS Selector Devices, 2017 IEEE International Memory Workshop (IMW) DOI: 10.1109/IMW.2017.7939088
- [20] M. Alayan, E. Vianello, G. Navarro, C. Carabasse, S. La Barbera, A. Verdy, N. Castellani, A. Levisse, G. Molas, L. Grenouillet, T. Magis, F. Aussenac, M. Bernard, B. DeSalvo, J. M. Portal, E. Nowak, In-depth investigation of programming and reading operations in RRAM cells integrated with Ovonic Threshold Switching (OTS) selectors, IEDM17-32 DOI: 10.1109/IEDM.2017.8268311
- [21] G. Navarro, A. Verdy, N. Castellani, G. Bourgeois, V. Sousa, G. Molas, M. Bernard, C. Sabbione, Innovative PCM+OTS device with high sub-threshold non-linearity for non-switching reading operations and higher endurance performance, 2017 Symposium on VLSI Technology, DOI: 10.23919/VLSIT.2017.7998208
- [22] Xiaodan Li, Zhenhui Yuan, Shilong Lv, Sannian Song, Zhitang Song, Extended endurance performance and reduced threshold voltage by doping Si in GeSe-based ovonic threshold switching selectors, *Thin Solid Films*, 2021, DOI: 10.1016/j.tsf.2021.138837
- [23] Z. Chai, W. Zhang, R. Degraeve, S. Clima, F. Hatem, J. F. Zhang, J. Marsland, P. Freitas, A. Fantini, D. Garbin, L. Goux, and G. S. Kar, "Dependence of switching probability on operation conditions in Ge_xSe_{1-x} ovonic threshold switching selectors," *IEEE Electron Device Lett.*, vol. 40, no. 8, pp. 1269-1272, Aug. 2019, doi: 10.1109/LED.2019.2924270.
- [24] S. Clima, D. Garbin, W. Devulder, J. Keukelier, K. Opsomer, L. Goux, G.S. Kar, "Material relaxation in chalcogenide OTS SELECTOR materials," *Microelectronic Engineering.*, vol.215, 2019, 110996. doi:10.1016/j.mee.2019.110996