Decoupled Modulation Techniques for a Four-level Five-Phase Open-End Winding Drive

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***Abstract*–The paper studies pulse width modulation (PWM) techniques for a five-phase multilevel open-end winding drive with two inverters supplied with unequal dc-link voltages, which are in the ratio 2:1. It is shown in the paper that application of in-phase disposition modulation (PD-PWM), often used in multiphase multilevel converters, results in overcharging of the capacitor in the dc-link of the converter intended to operate at the lower dc voltage. The voltage space vector combinations which lead to the overcharging are identified and two decoupled modulation techniques which do not activate the troublesome vector combinations are proposed. The performance of the developed modulation techniques is investigated using simulations and an experimental prototype, and the results are presented in the paper.**

I. INTRODUCTION

Open-end winding (OeW) drives offer a number of advantages over conventional multilevel drive systems. The main ones are the reduced component count (additional diodes or capacitors not required) [1] and the capability to operate under faulted conditions [2]. This paper deals with a five-phase OeW induction motor drive, supplied using two isolated five-phase two-level voltage source inverters (VSIs) with dc-link voltages fixed in the ratio 2:1. Application of unequal dc-link voltages in the ratio 2:1 enables drive operation with output voltage waveforms equivalent to those obtainable with a four-level voltage source inverter (VSI) in the single-sided supply mode [3]. The four-level multiphase topology is aimed at the high-power and traction applications where the well-known advantages of multiphase machines and multilevel converters are of particular significance. Open-end winding drives are particularly suited to EVs/HEVs [4] and electric ship propulsion [5], where use of two isolated supplies does not present a problem.

The open-end four-level topology has predominantly been investigated for three-phase drives [6-10], in conjunction with the space vector modulation (SVM) technique. The SVM algorithm developed in [6] requires large look-up tables in order to identify the sector in which the reference is positioned and the switching sequences to be applied. This makes the scheme difficult to implement. A fractal based SVM method with low computational requirements was proposed in [7]. It relies on the fact that a three-phase system produces simple triangular subsectors. Unfortunately, the algorithm is not applicable to the five-phase case since the system does not produce such uniformly distributed subsectors.

The modulation strategies discussed so far consider both inverters as a single "coupled" entity. A decoupled SVM algorithm which views the inverters as individual two-level converters is discussed in [8]. The method is based on sharing the reference between two inverters in the same ratio as the dc-link voltages with both inverters having the same switching frequency. Another strategy utilizes switching of the two inverters using switching frequencies that are proportional to their dc-link voltages.

Isolated dc power supplies are required to feed the inverters in order to deny a path for zero-sequence current flow. The dc-link of lower voltage should be supplied using a controllable supply; otherwise the higher voltage converter can overcharge the capacitor of the lower voltage converter if certain switching states are used [6]. This constraint was overcome for the three-phase case in [8]. An alternative solution is given in [9,10] where a rectifier-inverter combination is nested within the two-level inverter configuration. The dc voltage sources are formed using three diode rectifiers, supplied from a centre-tapped transformer with secondary winding ratio 1:2:1. This solution leads to a more complicated structure with an increased component count.

As mentioned previously, the majority of research has focused on the three-phase open-end winding topology. The large number of switching states and voltage vectors available in multiphase multilevel converters [11,12] makes the development of suitable control strategies difficult.

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Furthermore, some additional complexity is introduced, since more than three voltages need to be synthesised. The problem is made more difficult by the fact that the PWM scheme has to consider two planes (α-β and x-y) simultaneously in order to achieve optimum performance [13]. It is for these reasons that the carrier-based PWM is considered as a simpler technique in the case of OeW multiphase drives. The in-phase disposition (PD) PWM, widely recognised as a superior carrier based PWM technique for single-sided three-phase [14] and five-phase [1] multilevel drives, is adapted to control the four-level five-phase open-end configuration in [15, 16]. In [15] it is shown that the inverter dead-time can have a detrimental impact on the performance of the drive and a method to obviate the problem is proposed.

This paper shows that PD-PWM leads to overcharging of the capacitor in the dc-link of lower voltage in the case of the four-level converter and therefore activates the braking chopper (or requires a controllable dc-supply if energy wasting is to be avoided). A decoupled SVM algorithm is developed, which avoids the switching states that cause the overcharging. This SVM technique was originally developed in [12] for the five-phase OeW drive, supplied from two equal isolated dc voltage sources, and is here adapted to the considered topology with 2:1 dc source voltage ratio. The method is relatively straightforward to understand and implement since it is based on the previously developed SVM method for the two-level five-phase converters. General properties of the five-phase ac motor drives with sinusoidal winding distribution are at first reviewed, along with an available two-level SVM algorithm for a five-phase two-level VSI [17], which uses two large and two medium active space vectors per switching period in order to minimise low-order harmonics. Next, mathematical model of the OeW winding topology is given, along with mapping of the space vectors that are of interest into the torque-producing 2D sub-space. The performance of the open-end winding five-phase drive is investigated and verified using simulation and experimental results.

II. Two-level Five-phase Space-vector Modulation

Prior to considering the SVM schemes for the four-level open-end winding topology, it is beneficial to review the two-level SVM technique for a five-phase VSI. A five-phase machine with near-sinusoidal magneto-motive force distribution can be modelled in two 2D sub-spaces, termed α-β and x-y sub-spaces [13]. It can be shown that only current harmonic components which map into the α-β sub-space develop useful torque and torque ripple, whereas those that map into the x-y sub-space do not contribute to the torque at all. What this means is that the design of a five-phase PWM strategy must consider simultaneously both 2D sub-spaces, where the reference voltage, assuming pure sinusoidal references, is in the first plane while reference in the other plane is zero. Two-level five-phase inverters can generate up to $2^5 = 32$ voltage space vectors with corresponding components in the α-β and x-y sub-spaces, as shown in Fig. 1. Space vectors are labelled with decimal numbers, which, when converted into binary, reveal the values of the switching functions of each of the inverter legs. Active (non-zero) space vectors belong to three groups in accordance with their magnitudes - small, medium and large space vector groups. The magnitudes are identified with indices s, m, and l and are given as, respectively, $|\bar{v}_s| = 2A\cos(2\pi/5)$, $|\bar{v}_m| = AV_{dc}$ and $|\bar{v}_l| = 2A\cos(\pi/5)$, where $A = 2/5V_{dc}$. Four active space vectors are required to generate sinusoidal voltages [17]; thus, two neighbouring large and two medium space vectors are selected. For example if the reference is located in sector 1 in Fig. 1, the utilized active vectors are 16, 25, 29, 24. Hence for a given phase number n, space vector PWM has to utilise (n-1) active space vectors that neighbour the reference and the zero space vector (two zero states) in a switching sequence. It is also shown in [17] that such space vector PWM methods employ the same space vectors for the same dwell-times as one carrier-based PWM method, and thus give the same results in terms of phase and line-to-line voltages. This equivalent carrier-based PWM method is the one with offset injection (i.e. triangular zero-sequence signal injection, defined as $v_{zs} = -0.5(\max\{v_i^*\} + \min\{v_i^*\})$). The zero-sequence signal is added to the reference sinusoidal phase voltage signals. The maximum peak value of the output fundamental phase-to-neutral voltage in the linear modulation region is $v_{\max} = V_{dc}/[2\cos(\pi/10)] = 0.525V_{dc}$ (i.e., $M_{\max}$ = 1.05) [17]. The switching pattern is a symmetrical PWM with two commutations per each inverter leg.

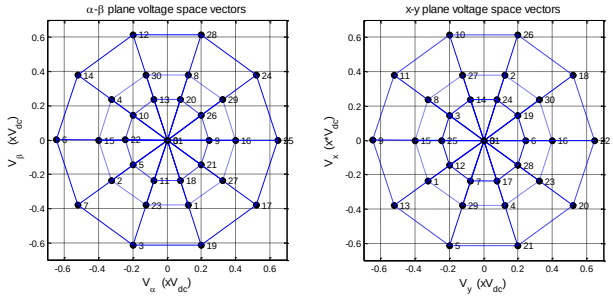

Figure 1. Two-level five-phase VSI space vectors in the α-β and x-y planes.

III. Four-Level Open-End Winding Topology

The four-level drive consists of an open-end winding five-phase induction machine, supplied via two isolated two-level voltage source inverters, as shown in Fig. 2. The inverters are supplied with unequal dc-link voltages in the ratio V_{dc2}:V_{dc1} = 2:1. This provides an overall dc-link voltage of $V_{dc} = V_{dc1} + V_{dc2}$, and the drive is equivalent to the four-level drive with single-sided supply. It is known that some switching state combinations can cause capacitor overcharging of the inverter with the lower voltage. There are four equidistant voltage levels ($-2V_{dc}/3$, $-V_{dc}/3$, $V_{dc}/3$ and 0) in the equivalent voltage, which is defined as the sum of

the phase voltage and the common-mode voltage (CMV), depicted with dotted (green) line in Fig. 2. Let us define the switching states S_{ji}, which correspond to the j^{th} inverter (VSI) and i^{th} phase in Fig. 2, where VSI_1 is supplied from V_{dc1}, and VSI_2 is supplied from V_{dc2}. The relationship between leg voltages and equivalent voltage levels is summarised in Table I and is formed as the potential difference of leg voltages of two inverters that are connected to the same phase:

$$v_i = v_{1i} - v_{2i} \tag{1}$$

Phase voltage positive direction is with reference to the upper inverter (VSI_1) in Fig. 2. Two isolated dc supplies are assumed so that the common mode voltage (CMV) v_{N1N2} is of non-zero value (the issue of CMV elimination is not addressed here). Using the notation of Fig. 2, phase voltages of the machine's stator winding can be given as:

$$\begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \\ v_{ds} \\ v_{es} \end{bmatrix} = (1/5) \begin{bmatrix} 4 & -1 & -1 & -1 & -1 \\ -1 & 4 & -1 & -1 & -1 \\ -1 & -1 & 4 & -1 & -1 \\ -1 & -1 & -1 & 4 & -1 \\ -1 & -1 & -1 & -1 & 4 \end{bmatrix} \begin{bmatrix} v_{11N1} - v_{21N2} \\ v_{12N1} - v_{22N2} \\ v_{13N1} - v_{23N2} \\ v_{14N1} - v_{24N2} \\ v_{15N1} - v_{25N2} \end{bmatrix} \tag{2}$$

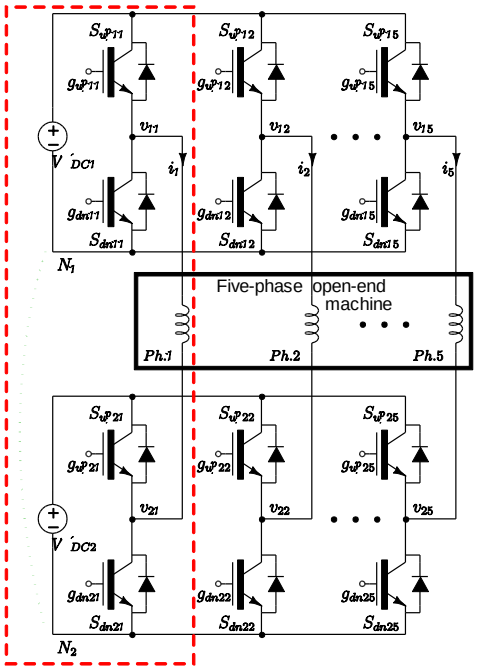

Figure 2. Open-end winding n-phase topology with dual two-level inverter supply. One load phase is boxed within the (red) dashed lines.

TABLE I. RELATIONSHIP BETWEEN SWITCHING STATES, LEG AND EQUIVALENT VOLTAGES OF FIG. 2.

S_{1i}	S_{2i}	v_{1i} [V]	v_{2i} [V]	Equivalent v_i [V]
1	0	V_{dc1}	0	$1/3V_{dc}$
1	1	V_{dc1}	V_{dc2}	$-1/3V_{dc}$
0	0	0	0	0
0	1	0	V_{dc2}	$-2/3V_{dc}$

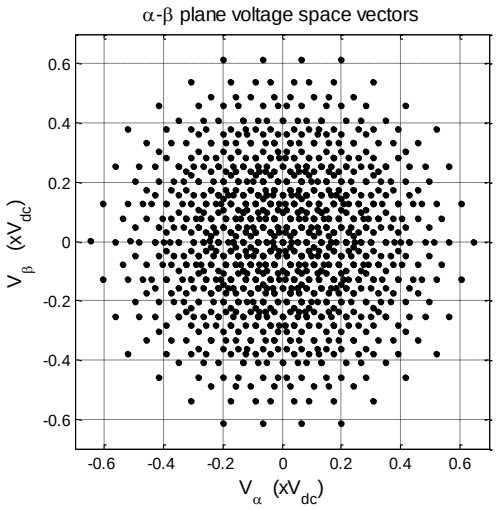

Figure 3. Four-level open-end winding space vectors in the α-β plane.

Space vectors of phase voltages in the two planes are determined with:

$$\begin{aligned} \bar{v}_{\alpha-\beta} &= (2/5)\left(v_{as} + \bar{a} v_{bs} + \bar{a}^2 v_{cs} + \bar{a}^3 v_{ds} + \bar{a}^4 v_{es} \right) \\ \bar{v}_{x-y} &= (2/5)\left(v_{as} + \bar{a}^2 v_{bs} + \bar{a}^4 v_{cs} + \bar{a}^6 v_{ds} + \bar{a}^8 v_{es} \right) \end{aligned} \tag{3}$$

where $\bar{a} = \exp(j2\pi/5)$. Using (1) and (2), one gets:

$$\begin{aligned} \bar{v}_{\alpha-\beta} &= \bar{v}_{\alpha-\beta(11,12.13,14,15)} - \bar{v}_{\alpha-\beta(21,22,23,24,25)} \\ \bar{v}_{x-y} &= \bar{v}_{x-y(11,12.13,14,15)} - \bar{v}_{x-y(21,22,23,24,25)} \end{aligned} \tag{4}$$

since $v_{N1N2}(1+\bar{a}+\bar{a}^2+\bar{a}^3+\bar{a}^4) = 0$. In (4) the two space vectors on the right-hand sides of the two equations are corresponding voltage space vectors of the two five-phase two-level VSIs, which come in six different lengths (since V_{dc1} = 0.5 V_{dc2}). Voltage space vectors, produced by the 1024 possible switching states, are illustrated in Fig. 3 for the α–β plane. There are 51 space vector magnitudes.

IV. DC-LINK CAPACITOR OVERCHARGING

The large number of voltage space vectors makes the development of an appropriate SVM algorithm difficult and is compounded by the requirement to apply appropriate voltage vectors in both planes while avoiding switching states that lead to overcharging of the dc-link capacitor of the inverter with the lower dc-link voltage. For each active vector of VSI_1 (the inverter with dc voltage of V_{dc}/3) there are 15 vectors belonging to $VS1_2$ whose activation will lead to overcharging of V_{dc1}. Assuming the reference is located in sector 1 for VSI_1, and the corresponding medium and large vectors are activated, the vectors from VSI_2 to be avoided are listed in Table II. These vectors are the ones that form an angle between 90˚ to 270˚ with the active vectors from VSI_1.

Figure 4 shows four relevant states of the five-phase open-end topology to demonstrate how the switching states

of VSI_2 can boost dc-link voltage of VSI_1 when VSI_1 holds switching state 25 [11001] (Table II). The current flow direction is assumed to be the same as for the voltage. When VSI_2 applies the switching state 11001 the complete current of the windings contributes to the increase of the dc-link voltage since it forces a current through the capacitor as if it were a load. This is the worst case scenario. When VSI_2 applies the switching states 11011 or 11101 the current forcing the rise of the dc-link voltage equals the current of the third and fourth phase, respectively. These are smaller currents than in the previous case, but they still cause an increase in the dc-link voltage. When VSI_2 applies 01111 switching state the VSI_1 capacitor is treated as a source rather than load and there can be no increase in its dc-link voltage. When one of the inverters is switched to a zero vector (0 or 31) a neutral point is created on one side of machine and the belonging capacitor floats. If both inverters apply a zero vector then both capacitors float and no current flows. The rate of the dc-link capacitor charging depends on the time constant of the load and can lead to activation of the braking chopper and wasting of energy. Alternatively a controllable dc-link could be employed; however this would lead to increased complexity and capital cost.

V. Carrier Based PD-PWM

A four-level drive requires three carrier signals for level-shifted PWM methods. These are shown in Fig. 5, together with reference that contains min-max injection. Modulation index (M) is defined as a ratio between the reference amplitude and (V_{dc}/2). Since there are two inverters and three carrier signals, gating signals cannot be obtained directly by comparison of the reference and the carriers. Some additional calculations are needed [15]. Switching states S_{ji} can be determined with simple mathematical operations applied to the logical variables A_{1i}, A_{2i} and A_{3i}:

$$A_{ki} = \begin{cases} \text{if } v_i^* > C_k & \text{then } 1 \\ \text{if } v_i^* < C_k & \text{then } 0 \end{cases} \qquad (5)$$

where v_i^* is the reference voltage for the i^{th} phase, while C_k are carrier signals shown in Fig. 5 (k = 1, 2 or 3). Relations between gating signals and logical variables A_{ki} could be written as $S_{2i} = A_{2i}$ and $S_{1i} = \text{NOT}(A_{1i}) + A_{2i}\cdot\text{NOT}(A_{3i})$. In practice, gating signals g_{upji} and g_{dnji} in Fig. 2 are determined with S_{ji} and implemented dead time.

Since two dc-link voltages are isolated and unequal, a reference offset (horizontal dashed (red) line in Fig. 5) can be used for selecting different operating modes [15]. In Fig. 5, reference offset was chosen to be 1/2, since full dc-link voltage utilisation is needed for modulation indices higher than 0.7. For low modulation index range ($0 < M < 0.35$) reference offset can be chosen as 1/6, so that two-level operation can be obtained with only one inverter operating in PWM mode. Figure 6 shows simulation results when the drive accelerates from standstill to M = 1 (50 Hz) using open-loop loop V/f mode, without brake chopper or controlled dc voltage source. It is clear that the capacitor in the VSI_1 dc-link becomes severely overcharged, resulting in higher than rated voltages being applied to the machine and

TABLE II. Switching Functions of VSI_1 and VSI_2 when the Reference of VSI_1 is in Sector 1.

VSI_1	Switching functions of VSI_2 to be avoided
0, 31	none
16	25,16,9,24,29,26,28,8,20,17,27,21,19,1,18
25	25,16,9,24,29,26,28,8,20,17,27,21,19,1,18
29	24,29,26,28,8,20,12,30,13,25,16,9,17,27,21
24	24,29,26,28,8,20,12,30,13,25,16,9,17,27,21

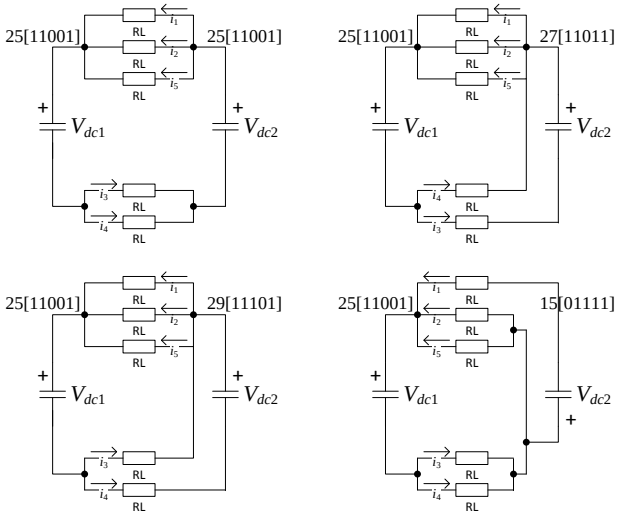

Figure 4. Load configuration for selected vector combinations.

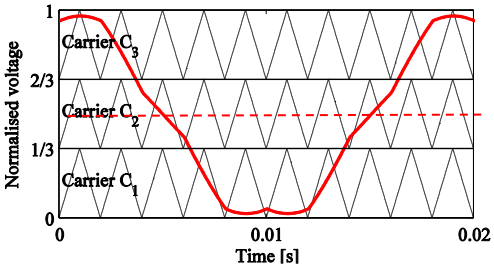

Figure 5. Reference voltage of one phase (red solid line) and triangular carrier signals for in-phase disposition (PD) PWM.

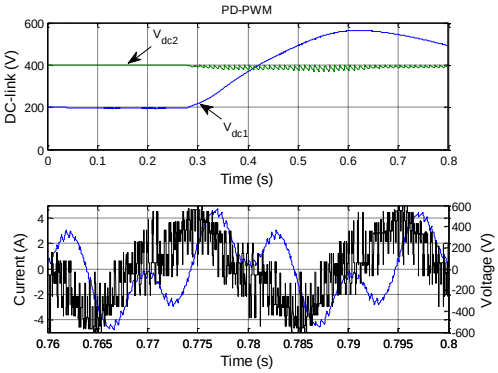

Figure 6. Dc-link voltages, stator current/voltage waveforms with PD-PWM.

highly distorted stator voltage and current waveforms. Furthermore, as discussed in [16], the PD-PWM method suffers from voltage spikes due to the dead-time effect when both inverters are commanded to switch at the same time.

VI. Unequal Reference Sharing PWM Methods

When developing a suitable SVM strategy for the dual-inverter supply and considering (4), it seems logical to adapt the two-level SVM method for five-phase VSI of [17] accordingly. The basic idea is to decompose the problem of space vector PWM of the complete system into two sub-problems of lower level complexity, by splitting the total reference into individual references of the two inverters. By doing so, it becomes possible to apply well-known SVM methods for two-level inverters [12, 17] to two individual two-level inverters at each end of the winding. The resulting SVM scheme, illustrated in Fig. 7, uses two identical two-level modulators. As mentioned earlier, the two-level multiphase SVM methods employ the same space vectors for the same dwell-times as one carrier-based PWM method. Therefore, it can be concluded that the individual two-level modulators of Fig. 7 may also use the carrier-based approach. It thus follows that the simulation and experimental results presented in this paper for the SVM are equally applicable to the carrier-based two-level modulation method with offset injection.

The voltage reference applied to the two-level modulators is apportioned according to the modulation index *M*. For clarity, it is beneficial to define $M_1 = \left|v_1^*\right| / (0.5V_{dc1})$, $M_2 = \left|v_2^*\right| / (0.5V_{dc2})$ as individual modulation indices, where $\left|v_1^*\right|$ and $\left|v_2^*\right|$ denote peak reference values for the two VSIs. Only inverter 1 is operational up to the point when M = 0.35 (M_1 = 1.05). Hence the drive operates in two-level mode, since inverter 2 is not modulated and the VSI_2 is locked in a zero switching state (11111 or 00000) forming a neutral point. When M > 0.35, inverter 1 is held at M_1 = 1.05 and inverter 2 output is modulated as well. These constraints can be expressed as:

$$\begin{aligned} 0 \le M \le 0.35 &\begin{cases} M_1 = 3M \\ M_2 = 0 \end{cases} \\ 0.35 \le M \le 1.05 &\begin{cases} M_1 = 1.05 \\ M_2 = 1.5(M - 0.35) \end{cases} \end{aligned} \tag{6}$$

Unequally apportioning the voltage reference between the two modulators leads to multi-level operation. Within the decoupled modulation technique two separate modulation methods are investigated. The first one (URS1) applies inverted modulating signals and the same carrier signals, while the other (URS2) applies inverted modulating signals and inverted carrier signals to the two inverters.

VII. Simulation Results

In order to verify the performance of the drive, a series of detailed simulations were undertaken using PLECS

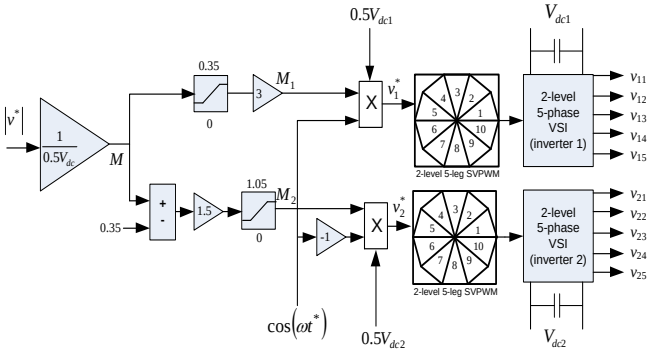

Figure 7. Unequal reference sharing scheme (URS1). $|v^*|$ stands for the total peak voltage reference.

software. Inverter dead time is set to 6 μs and the switching frequency of each inverter is fixed at 2 kHz. The phase variable model of the five-phase machine, with sinusoidal mmf distribution, is used and the drive is operated under open-loop *V/f* control. The voltage reference profile is such that the supply frequency of the machine is ramped from zero to 50 Hz in 0.5s. At the operating frequency of 52.5 Hz the maximum modulation index is reached (M = 1.05); voltage boost is not applied. The dc-link voltages of VSI_1 and VSI_2 are 200 V and 400 V, respectively. Since in a five-phase drive there are two different line-to-line voltages and dc voltages are applied from both winding sides, phase voltage is shown in what follows.

The stator phase voltage and current waveforms and their spectra are presented in Figs. 8 and 9 when M = 0.5 for URS1 and URS2, respectively. Both inverters are now modulated according to (6) and the effective dc-link voltage is now 600 V. In both cases the phase voltage levels are equidistantly spaced, i.e. the step is 40 V. The URS1 yields 21 levels while the URS2 is characterised with 23. However, it is fair to say that the drive operates with a pseudo multi-level output since the phase voltage switches to zero throughout the fundamental cycle, in contrast to a true multi-level waveform. The phase voltage and current spectra indicate a minimal low-order harmonic content with some very small third and seventh harmonics present due to the inverter dead time. The switching trajectories and the switching state of each inverter are also shown in Figs. 8 and 9 for URS1 and URS2, respectively, when the reference is positioned in sector 1 (9˚) of the α–β plane. The switching states are numbered in the same manner as in Fig. 1. When the reference is along the sector border (every 36˚) only five active vectors are used, whereas nine active vectors are used otherwise. Further simulations show that different active vectors are used as the reference moves through the sector; hence an equivalent single SVM would require a large look-up table containing the switching sequences. It can be seen that the prohibited switching functions listed in Table II are not activated.

Finally, Figs. 10 and 11 show that the dc-link voltages remain almost constant as the modulation index sweeps from 0 to 1 (0 to 50 Hz) indicating that both decoupled

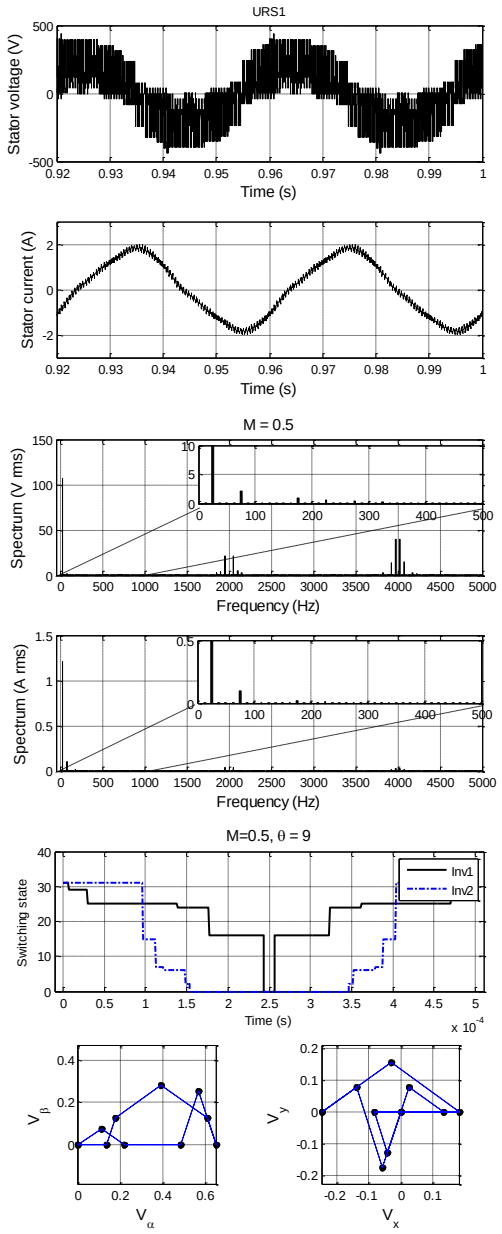

Figure 8. URS1, steady-state operation (simulation), *M*=0.5: phase voltage and current waveforms and spectra. Inverter switching states and switching trajectories (×V_{dc}).

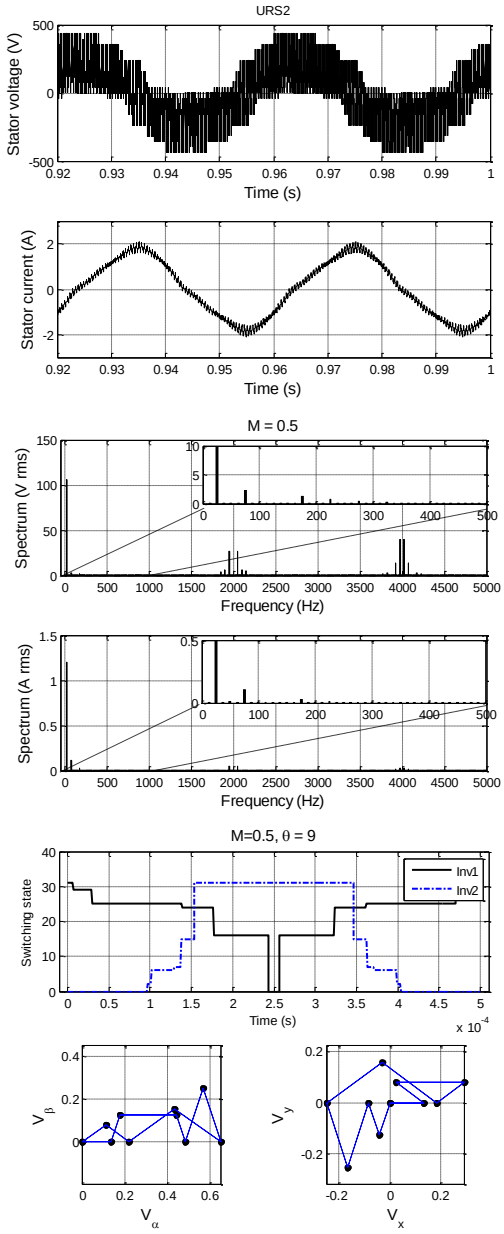

Figure 9. URS2, steady-state (simulation), *M*=0.5: phase voltage and current waveforms and spectra. Inverter switching states and switching trajectories (×V_{dc}).

PWM methods are capable of maintaining the dc-link voltages.

VIII. EXPERIMENTAL VERIFICATION

The experimental results are obtained using two custom built five-phase two-level VSIs and a 4-pole five-phase induction motor. Parameters of this motor have been used in the simulation study of Section VII and are: stator resistance = 3 Ω; rotor resistance = 3 Ω; stator leakage inductance = 45 mH; rotor leakage inductance = 15 mH; magnetising inductance = 515 mH. The inverters are controlled using a dSPACE DS1006 processor board. The dSPACE module is connected to the VSIs via a dSPACE DS5101 digital waveform unit. Both VSIs are fed via isolated three-phase supplies and autotransformers, so that the diode bridge rectifiers provide dc-link voltages of 200 V and 400V for VSI_1 and VSI_2, respectively. The braking chopper of each VSI is set to activate when the voltage of the individual VSI reaches 600 V (so that they stay in essence inactive). The motor is controlled using the same *V/f* control law with the same switching frequencies and dead time as described in the simulations. The phase and leg voltages were measured using high voltage differential probes while the phase current was measured using a high-performance Tektronix current probe.

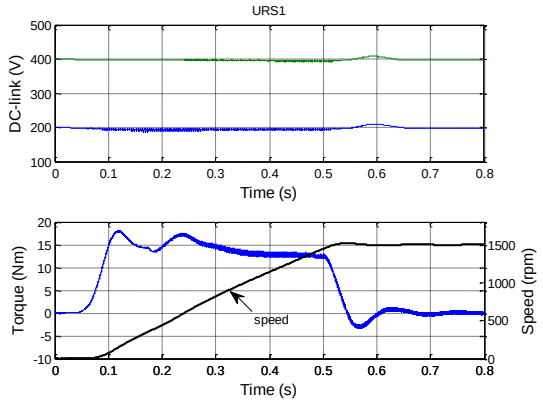

Figure 10. Simulation results (URS1), machine acceleration: inverter dc-link voltages and the torque/speed response.

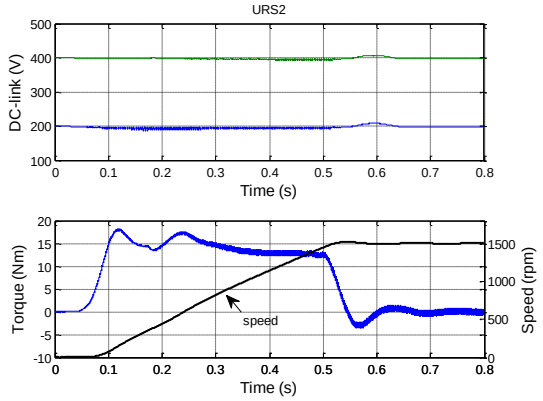

Figure 11. Simulation results (URS2), machine acceleration: inverter dc-link voltages and the torque/speed response.

Fig. 12 depicts the experimental results obtained when M = 0.2 and the drive operates in two-level mode with only the VSI_1 switching. The oscilloscope screen shot shows, from top to bottom, the VSI_1 leg voltage, VSI_2 leg voltage, machine phase voltage and the stator current. The respective leg voltages clearly show that VSI_2 is not switching and forms a single neutral point. It can be seen that the machine phase voltage is the same as for a five-phase two-level converter with an effective dc-link voltage of 200 V [17]. The phase voltage comprises nine levels and the target fundamental has been met, as indicated by the voltage spectrum.

Performance of the drive when M = 0.5 for both URS1 and URS2 is presented in Figs. 13 and 14, respectively. The drive now utilises both inverters, so the effective dc-link voltage is 600 V. The different dc-link voltages and the switching of both inverters are clearly visible. The phase voltage and current waveforms are in good agreement with those presented in Figs. 8 and 9, as are the resulting spectra. The waveforms and spectra show no evidence of capacitor overcharging and are sinusoidal, as expected. The impact of the inverter dead-time can be seen in the spectra; however, it is clear that both modulation techniques are able to achieve the target fundamental and minimal lower order harmonic content.

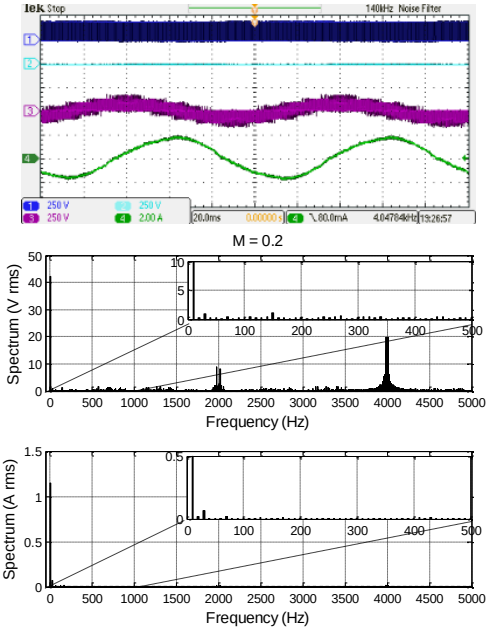

Figure 12. Experimental results, M=0.2: inverter leg voltages, phase voltage and current. Phase voltage and current spectrum.

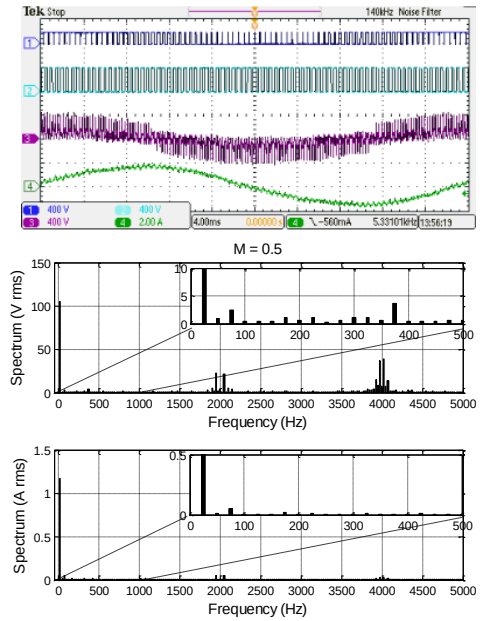

Figure 13. URS1, experimental results, M=0.5: inverter leg voltages, phase voltage and current. Phase voltage and current spectrum.

Figs. 15 and 16 depict the waveforms and spectra when M = 1. The differences between the two modulation methods can be seen from the voltage and current waveforms. The URS1 method produces lower current ripple since the switching harmonic sidebands around the switching frequency (2 kHz) are much reduced compared to those produced by the URS2 method.

Confirmation that the decoupled modulation methods do not lead to overcharging of the lower voltage dc-link

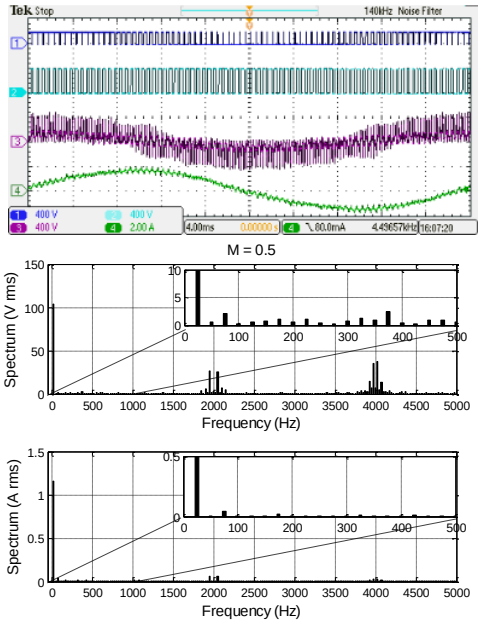

Figure 14. URS2, experimental results, *M*=0.5: inverter leg voltages, phase voltage and current. Phase voltage and current spectrum.

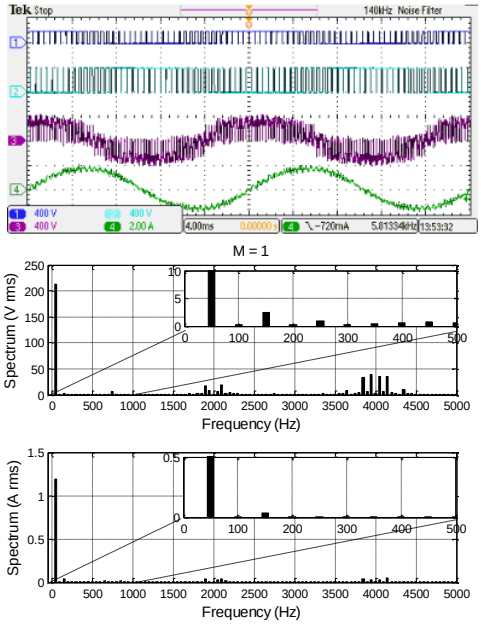

Figure 15. URS1, experimental results, *M*=1: inverter leg voltages, phase voltage and current. Phase voltage and current spectrum.

capacitor is provided in Fig. 17. The machine is slowly accelerated from standstill to 1500 rpm (M = 0 to M = 1) over 10 s. It is clear that the dc-link voltages remain at the initial values throughout the time interval, regardless of the modulation index. This is in sharp contrast to the PD-PWM method, Fig. 6.

Finally, the harmonic performance of the decoupled modulation methods is investigated using the total harmonic distortion (THD) as a figure of merit [16]. The THD is calculated for M ranging from 0.1 to 1.05 in 0.05 increments and is shown in Fig. 18. Both methods offer similar performance up to M = 0.5. Above M = 0.5 the URS1 offers superior performance since the current ripple is much lower.

IX. Conclusion

A four-level five-phase open-end winding drive is analysed in the paper. Four-level operation is realised by using two isolated dc-link voltages in the ratio 2:1. It is shown that this topology is susceptible to dc-link overcharging of the inverter with the lower dc-link voltage and therefore requires a controllable dc-link if wasting of energy in braking resistors is to be avoided. Two decoupled modulation methods, capable of eliminating the overcharging problem are developed in the paper. The unequal reference sharing methods are validated using simulations and a prototype five-phase four-level open-end

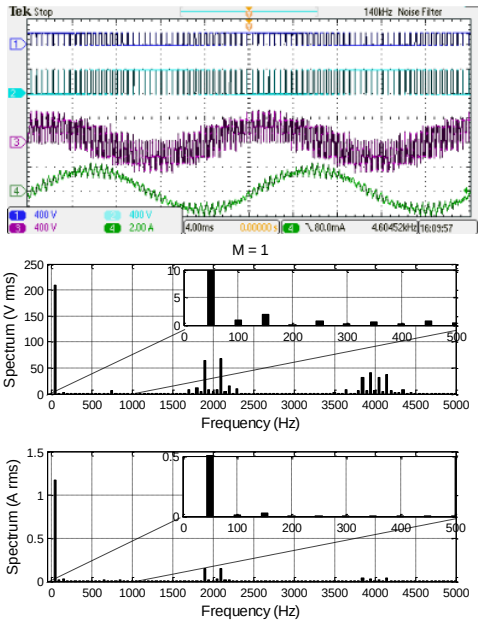

Figure 16. URS2, experimental results, *M*=1: inverter leg voltages, phase voltage and current. Phase voltage and current spectrum.

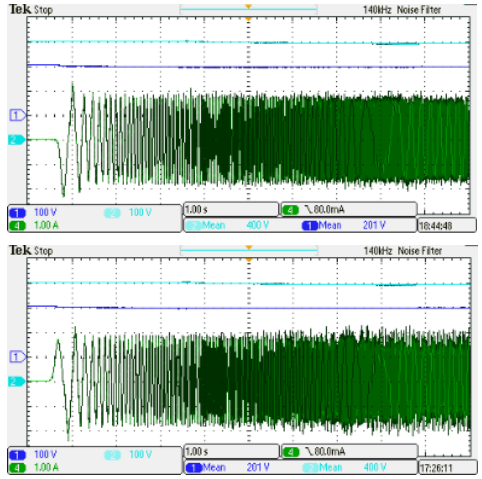

Figure 17. URS1 (upper) and URS2 (lower), acceleration 0 to 1500 rpm: dc-link voltages and phase current.

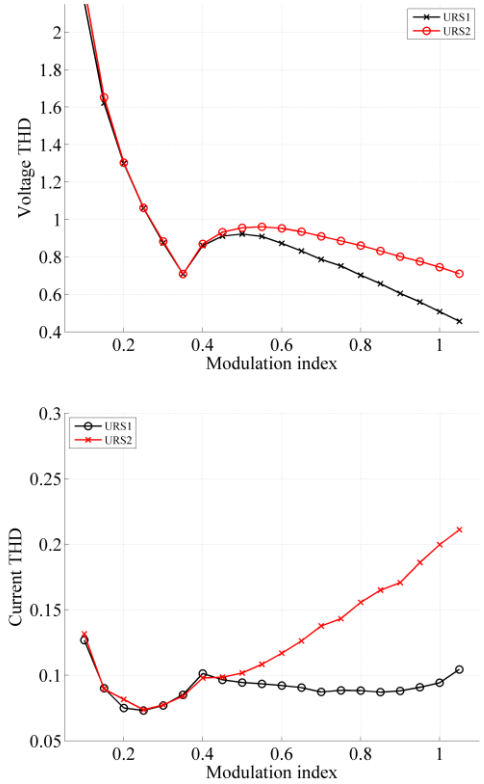

Figure 18. URS1 and URS2: THD against modulation index.

winding drive. The results indicate that URS1 offers superior performance when the drive operates with $M > 0.5$.

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