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Impact of Hot Carrier Aging on Random Telegraph Noise and Within a Device Fluctuation

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A. B. Manut, J. F. Zhang, M. Duan, Z. Ji, W. Zhang, B. Kaczer, T. Schram, N. Horiguchi, and G. Groeseneken

***Abstract*—For nanometer MOSFETs, charging and discharging a single trap induces random telegraph noise (RTN). When there are more than a few traps, RTN signal becomes complex and appears as within a device fluctuation (WDF). RTN/WDF causes jitters in switch timing and is a major challenge to low power circuits. In addition to RTN/WDF, devices also age. The interaction between RTN/WDF and aging is of importance and not fully understood. Some researchers reported aging increasing RTN/WDF, while others showed RTN/WDF being hardly affected by aging. The objective of this work is to investigate the impact of hot carrier aging (HCA) on the RTN/WDF of nMOSFETs. For devices of average RTN/WDF, it is found that the effect of HCA is generally modest. For devices of abnormally high RTN/WDF, however, for the first time, we report HCA reducing RTN/WDF substantially (>50%). This reduction originates from either a change of current distribution or defect losses.**

***Index Terms*—Random Telegraph Noise, RTN, Hot Carriers, defects, fluctuation, instability, aging, reliability.**

I. Introduction

As device area scales down, the impact of a single charge in gate dielectric scales up [1-8]. For current and future CMOS nodes, charging and discharging a single trap induces a random telegraph noise (RTN) in Id under a given Vg. When there are more than a few (e.g. 4) of traps, it becomes difficult to separate them and the complex RTN signals appear in the form of within-a-device-fluctuation (WDF) [5, 9].

RTN/WDF is observed at time-zero, i.e. in fresh devices [5, 10], becoming a major challenge for low power circuits. The low (Vg-Vth) used in low power circuits has less headroom to tolerate a given Vth shift, ΔVth, since ΔVth/(Vg-Vth) is higher and the impact of ΔVth on the driving current is relatively stronger. For instance, it has been reported that a single charge can cause a Vth shift of ~30 mV [4], while a shift of only several mV can cause errors in circuits like successive approximation analogue-to-digital converters [11].

In addition to RTN/WDF, aging also occurs through either bias temperature instabilities [4, 12-17] or hot carrier stresses [18-20]. Unlike RTN/WDF, aging causes a gradual shift of device parameters in one direction [12-20]. The interaction between RTN/WDF and aging is not fully understood and is of importance to optimize circuit performance. It has been reported that aging can either increase RTN/WDF [7] or has little contribution to it [10, 19]. The objective of this work is to investigate the relation between the amplitude of RTN/WDF and hot carrier aging (HCA) for nMOSFETs. The results show that the impact of HCA on devices of average RTN/WDF is typically modest, but can be substantial on devices of abnormally high RTN/WDF. The mechanism will be explored.

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A. B. Manut, J. F. Zhang, M. Duan, Z. Ji, and W. Zhang are with the School of Engineering, Liverpool John Moores University, Liverpool L3 3AF, U.K. (e-mail: J.F.Zhang@ljmu.ac.uk).

B. Kaczer, T. Schram, N. Horiguchi, and G. Groeseneken are with IMEC, Leuven B3001, Belgium. G. Groeseneken is also with KU Leuven.

II. Devices and Experiments

The nMOSFETs were fabricated by a 45 nm HK/MG process, having a channel length/width of 50/90 nm and an equivalent oxide thickness (EoT) of 1.45 nm. To ensure that the findings are not process specific, tests were also carried out on nMOSFETs fabricated by a 22 nm process, with a channel length/width of 90/70 nm and an EoT of 1 nm.

Tests start by measuring RTN/WDF of Id under Vg=1.0 V and Vd=0.1 V, and typical results are given in Figs. 1(a)&1(b). Fig. 2 shows the device-to-device variation of RTN/WDF amplitude for 45 nm (50 devices) and 22 nm (24 devices) processes. Two types of devices were selected: one with average and one with abnormally high RTN/WDF. After HCA under Vg=Vd=2.2 V for 1 ks, RTN/WDF were measured at the same Id as that for fresh device, so that the Si surface potential is kept approximately the same. Some devices were annealed at 400 °C in forming gas (10% H_2) for 45 min after HCA.

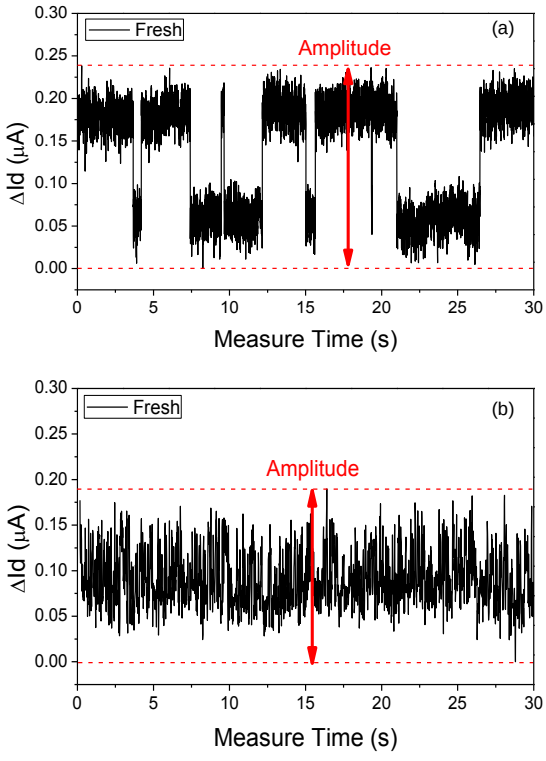

Fig. 1. Typical fresh devices with (a) and without (b) clear RTN. The ΔId= Id(measured) - Id(minimum) and Amplitude = Id(maximum) - Id(minimum).

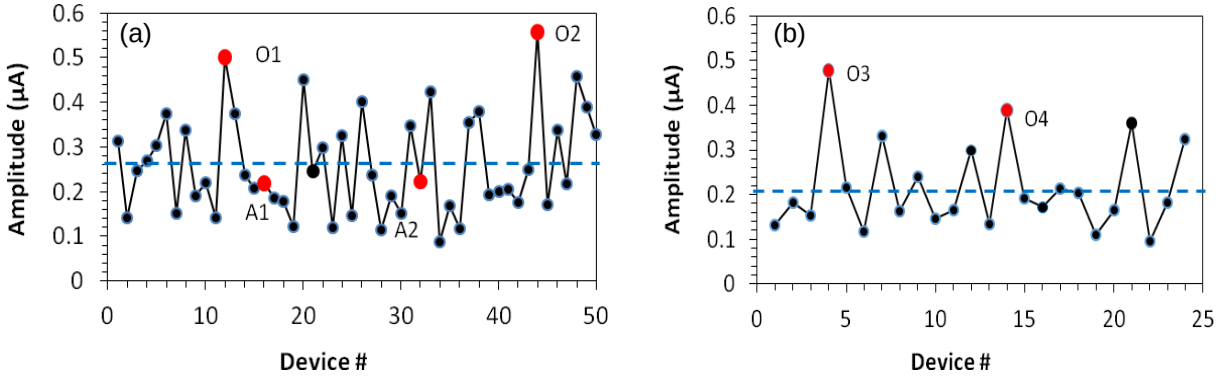

Fig. 2. The device-to-device variation of RTN/WDF amplitude. The devices were fabricated by (a) 45 nm and (b) 22 nm processes. The dashed line is the average RTN/WDF. In (a), the 'A1' and 'A2' mark two devices of RTN/WDF close to the average and 'O1' and 'O2' mark two outliers. The results for these four devices are given as representatives and their fresh RTN/WDF are marked out by the red '●'. Two outliers also were marked out as 'O3' and 'O4' in (b) for the 22 nm process.

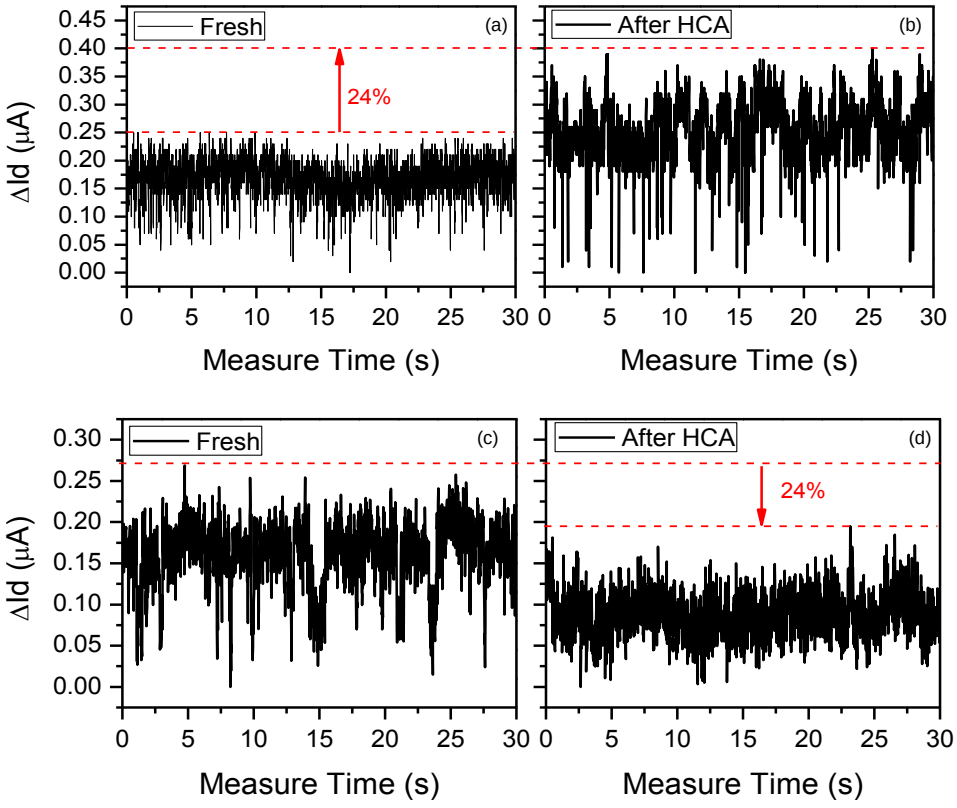

Fig. 3. Typical impact of HCA on the devices of RTN/WDF close to average, marked as 'A1' and 'A2' in Fig. 2(a). RTN/WDF can either increase by 24% (a)&(b) or decrease (c)&(d) after HCA.

III. Results and Discussion

For a device of average RTN/WDF, Figs. 3(a)-(d) show that HCA can either increase or decrease RTN/WDF modestly and the typical variation range is ±25%, which is smaller than the 6× device-to-device variation in Fig. 2(a). This agrees with the early works [10, 19] and the verdict that RTN/WDF is dominated by as-grown defects [4, 21].

The HCA-defects can affect RTN/WDF in two possible ways. On one hand, they may directly contribute to RTN/WDF by their charging/discharging. On the other hand, even if their charges do not alternate, they still can affect RTN/WDF by changing the current distribution within a device [8]. For the same as-grown defects, their effects on RTN/WDF will be different when the current density beneath it changes [4, 8]. If the HCA defects contribute directly to RTN/WDF by alternating their charging/discharging, an increase of defects by

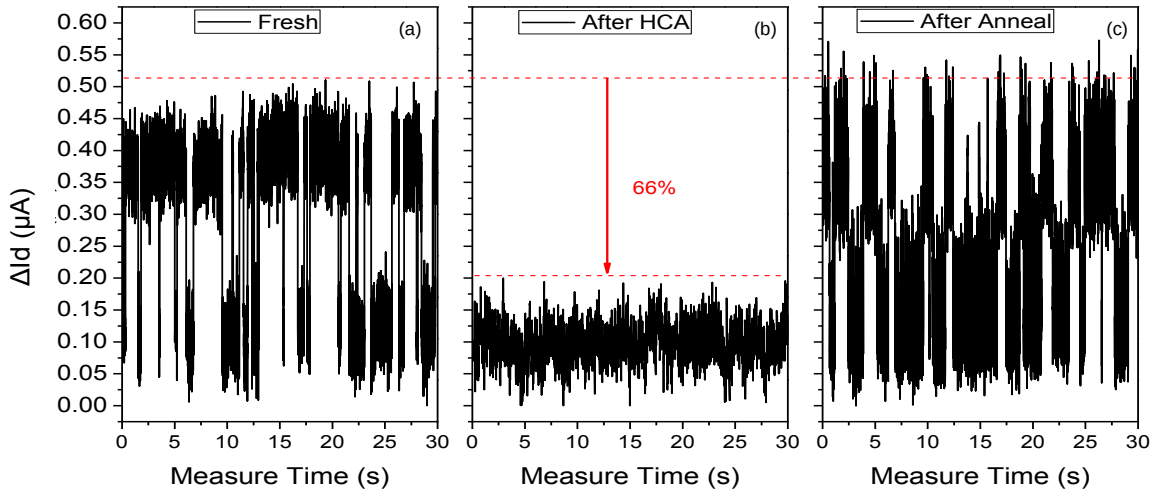

Fig. 4. Typical impact of HCA on an outlier, marked as 'O1' in Fig. 2(a). (a) is fresh and RTN/WDF reduces by 66% after HCA (b). (c) shows that RTN/WDF amplitude returns to its fresh level after an anneal at 400 °C.

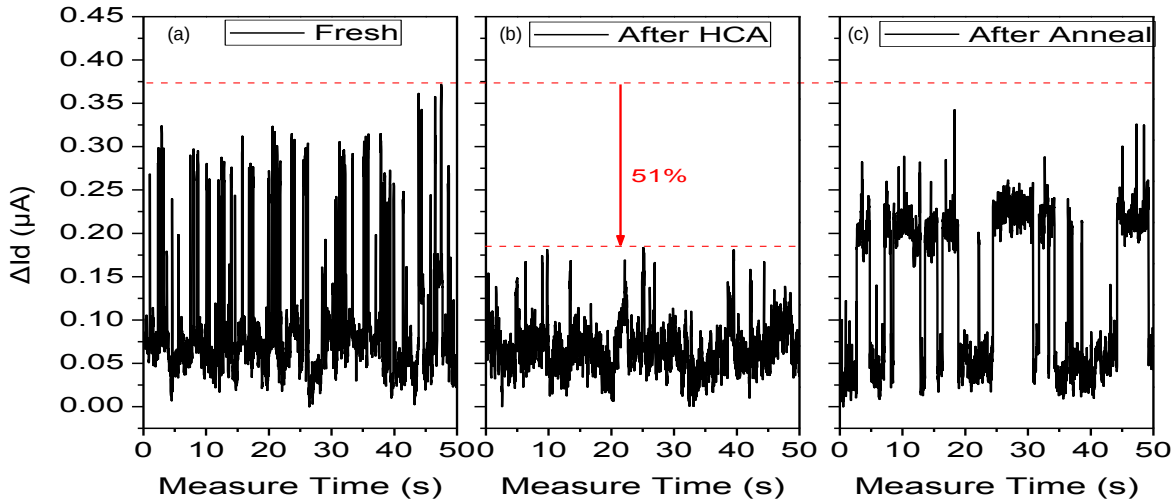

Fig. 5. The tests were similar to those in Fig. 4, but the device 'O4' was fabricated by a 22 nm processes and stressed under Vg=Vd=2 V for 1 ks.

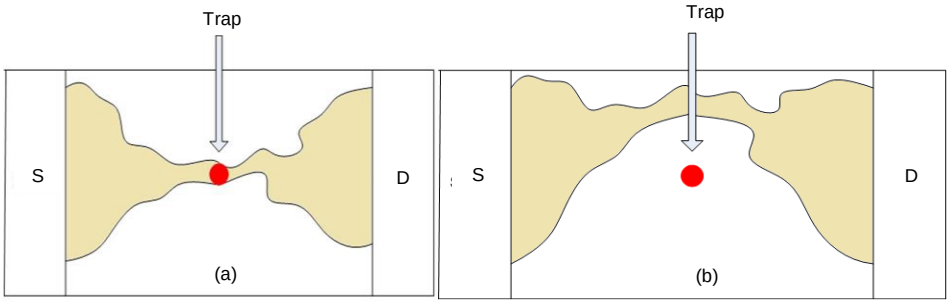

Fig. 6. A schematic illustration of HCA-induced de-sensitization of a critical trap. (a) shows that a critical trap is at the location where the current density peaks, causing abnormally high RTN/WDF before HCA. (b) shows how a change of current distribution

after HCA can reduce the current density under this trap, de-sensitizing it. This diagram is used to highlight the possible change of current distribution before and after HCA. It does not mean that current path is always strongly localized.

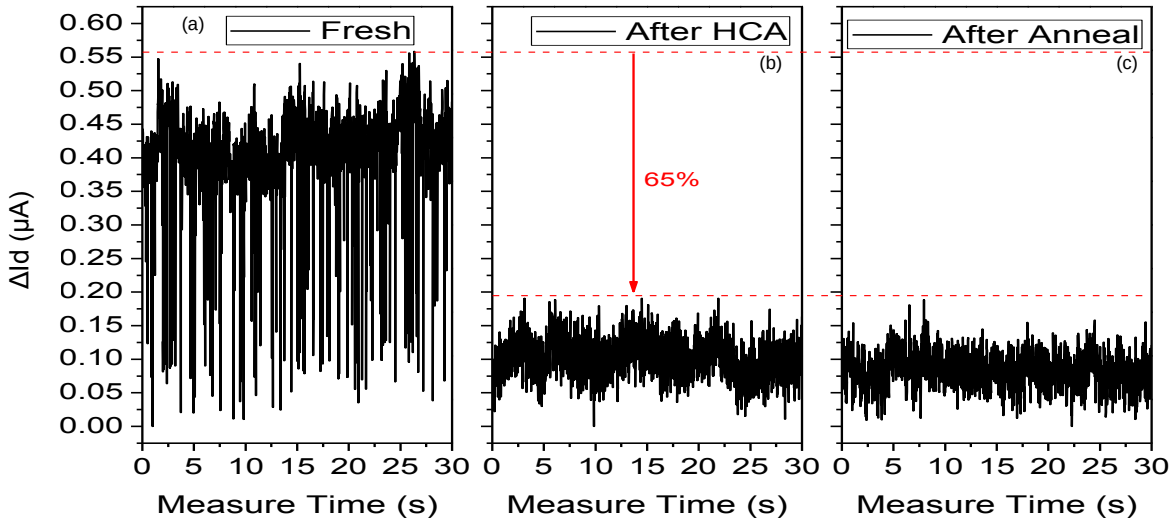

Fig. 7. The impact of HCA on a device of outlier RTN/WDF, marked as 'O2' in Fig. 2(a). (a) & (b) shows that RTN/WDF reduces by 65% after HCA. (c) shows that RTN/WDF remains low after an anneal at 400 °C, supporting defect loss.

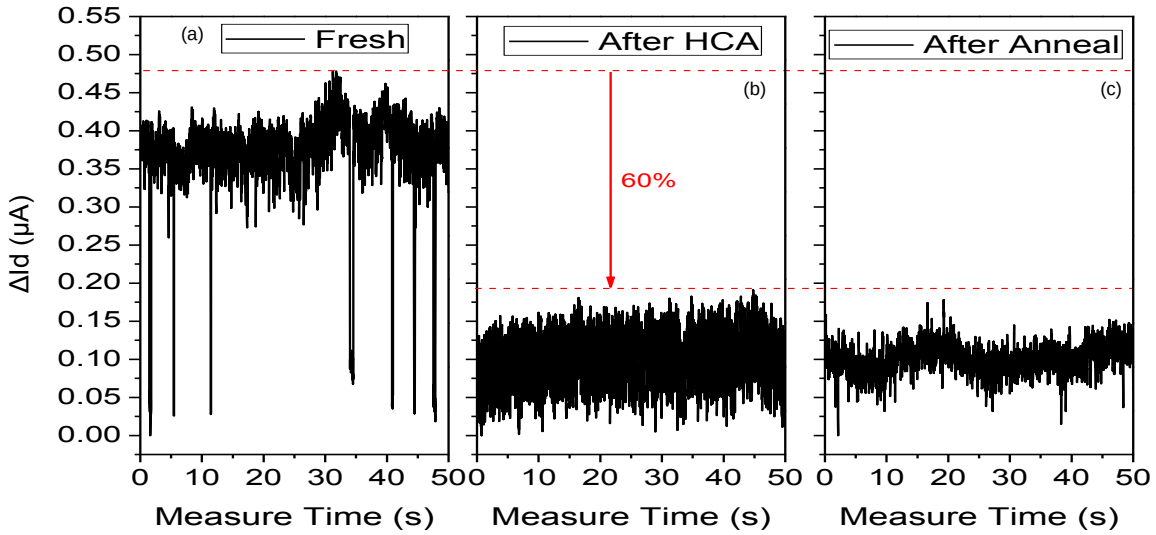

Fig. 8. The tests were similar to that in Fig. 7, but the device 'O3' was fabricated by a 22 nm processes.

HCA should lead to a higher RTN/WDF. This is, however, against the reduction in Figs. 3(c)&(d). As a result, it appears that HCA affects RTN/WDF through changing the current distribution, which will be further explored. This also agrees with early report [19] that HCA defects recover little, so that they will not contribute to RTN/WDF by not discharging.

For a device of abnormally high RTN/WDF, Figs. 4(a) & 4(b) show, for the first time, that RTN/WDF actually can be substantially (66%) reduced post HCA. After the reduction, the RTN/WDF is around the average level in Fig. 2(a).

It has been reported that RTN/WDF in pMOSFETs can be unstable during measurements and some defects can disappear and then reappear [2]. The reduction in Fig. 4(b), however, is a different phenomenon, since the RTN/WDF in nMOSFETs observed here is stable and does not disappear both before and after HCA during measurements.

To confirm that this reduction is not process-specific, Figs. 5(a) & (b) show a substantial reduction again for a device fabricated by a 22 nm process.

There are two possible explanations for the HCA-induced RTN/WDF reduction: a loss of defects [22, 23] or a change of current distribution [8].

The impact of a charged defect on the current will depend on its relative position against the current flow. On one hand, if there is a strong current flow direct beneath a charged defect, the impact of this defect on the current will be large. On the other hand, if there is little current flowing below a charged defect, its impact on the current will be weak.

The abnormally high RTN/WDF can originate from the presence of a critical trap: the current density peaks just beneath it, so that its charging/discharging has an abnormally large impact on Id, as illustrated in Fig. 6(a) [8]. Fig. 6(b) shows that HCA can modify the current distribution, reducing the density beneath this trap and de-sensitizing Id to it.

For a device of average RTN/WDF, the current distribution can be less localized and there is no critical trap where the current density peaks. Since the impact of each trap in these devices is close to average, current density beneath it changes typically modestly. On one hand, if the density increases, RTN/WDF will rise. On the other hand, if the density reduces, RTN/WDF will decrease. As a result, the HCA has a relatively modest impact on the RTN/WDF in both directions.

To further investigate the origin of the HCA-induced reduction, the devices were annealed at 400 ^{o}C for 45 min, which removed the HCA-generated defects and restored Id to its fresh level [22, 23]. When measured again post-anneal, Figs. 4(c) and 5(c) show that the amplitude of RTN/WDF nearly returns to its pre-stress abnormally high level for most devices (~75%). The anneal restores the original current distribution and, in turn, the abnormal RTN/WDF. This supports a HCA-induced change of current distribution as the origin of abnormal RTN/WDF reduction.

It is noted that the RTN/WDF after the stress-then-anneal behaves differently from that in fresh devices, although their magnitudes before and after the anneal are similar in Figs. 4 and 5. It is not known what causes these differences at present. One may speculate that the as-grown traps in the fresh devices also were affected by the stress and the subsequent anneal, leading to the changes in their RTN/WDF behavior. Since most of the devices tested in this work have a complex WDF, rather than a clear RTN, it is difficult to extract the capture and emission time reliably. As a result, we focus on the magnitude of RTN/WDF here. The main objective of this work is to report the test results and a detailed understanding of the mechanism awaits further investigation.

There are some cases, however, where RTN/WDF did not return to its pre-stress high level after anneal and an example is given in Fig. 7. This agrees with the defect loss reported in early works [22, 23]. If the critical trap is lost after anneal, the RTN/WDF cannot return to its fresh abnormally high level, even though the original current distribution is restored.

Fig. 8 confirms that similar loss also occurs for a device fabricated by the 22 nm process.

IV. Conclusion

In this work, the impact of HCA on the magnitude of RTN/WDF of nMOSFETs is investigated. For the devices of average RTN/WDF, HCA typically can either increase or reduce it modestly (±25%). For the devices of abnormally high RTN/WDF, however, the HCA generally can reduce it substantially. After an anneal at 400 ^{o}C, RTN/WDF returns to the abnormal level for most devices, supporting a HCA-induced change of current distribution as the origin of the reduction. There are cases, however, where RTN/WDF does not return to its pre-stress level after anneal, suggesting defect losses.

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Azrif Manut received B.Eng and M.Sc degrees from National University of Malaysia (UKM), Malaysia, in 2001 and 2007, respectively. He is currently pursuing the Ph.D degree at Liverpool John Moores University, Liverpool, U.K.

Jian Fu Zhang received the B.Eng. degree from Xi'an Jiaotong University, Xi'an, China, in 1982,

and the Ph.D. degree from the University of Liverpool, Liverpool, U.K., in 1987. He has been a Professor of Microelectronics with Liverpool John Moores University, Liverpool, since 2001. He has published 180 papers, including 21 invited ones. He has served or is serving at various functions at the IEDM, SISC, CSTIC, and IPFA conferences. His current research interests include the aging, variability, characterization, and modeling of nanometer-size devices.

Meng Duan received the B.Eng. and M.Eng. degrees from Xidian University, Xi'an, China, in 2000 and 2003, respectively, and the Ph.D. degree from Liverpool John Moores University, Liverpool, U.K., in 2013.He is currently with Liverpool John Moores University as a Post-Doctoral Researcher in the field of aging-induced time-dependent device variability.

Before he joined Liverpool John Moores University, he also worked in Infineon/Qimonda technologies Xi'an for mixed signal circuit design of DRAM product. His current research focuses on aging induced time dependent variability on nanometer device, and circuit level reliability evaluation.

Zhigang Ji received his Ph.D. degree from Liverpool John Moores University (LJMU), Liverpool, U.K., in 2010. He is currently a Senior Lecturer at LJMU. His current research interests include characterisation and modelling on future logic and memory devices.

Wei Dong Zhang received the B.Eng degree from Beijing Institute of Technology, China, in 1989, the M.Sc degree from Xidian University, Xi'an, China, in 1992, and the Ph.D. degree from Liverpool John Moores University (LJMU), UK, in 2003. He is currently a Professor of Nanoelectronics at LJMU. His research interests include the characterization and assessment of nanometer-scaled memory and MOS devices.

Ben Kaczer is a Principal Scientist at imec, Belgium. He received the M.S. degree in Physical Electronics from Charles University, Prague, in 1992 and the M.S. and Ph.D. degrees in Physics from The Ohio State University, in 1996 and 1998, respectively. In 1998 he joined the reliability group of imec. He has co-authored more than 350 journal and conference papers and 2 patents, presented a number of invited papers and tutorials, and received 5 IEEE IRPS Best and Outstanding Paper Awards, 2 IEEE IPFA Best Paper Awards, and the 2011 IEEE EDS Paul Rappaport Award. He has served or is serving at various functions at the IEDM, IRPS, SISC, INFOS, and WoDiM conferences. He is currently serving on the IEEE T. Electron Dev. Editorial Board.

T. Schram: Not available.

N. Horiguchi: Not available.

Guido Groeseneken (F'05) received the Ph.D. degree in applied sciences from KU Leuven, Leuven, Belgium, in 1986.

He has been with Interuniversity Micro-Electronics Center, Leuven, Belgium, since 1987.