RELIABILITY CHARACTERISATION OF III-NITRIDES BASED DEVICES FOR TECHNOLOGY DEVELOPMENT

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ABSTRACT

III-nitrides based devices are considered as outstanding options for a range of extremely relevant applications. These devices can significantly improve the efficiency of high-power switching appliations. They are predicted to dominate applications in the low carbon economy. In recent years, these devices have been steadily improved and each year new record performances have been reported.

Regardless of the superior performance of III-nitrides based devices, and particularly AlGaN/GaN high electron mobility transistors (HEMTs), achieving reliability at the same time as the high performance that the device boasts is a factor that is holding back widespread commercial and industrial development. Recoverable degradation (e.g. current collapse and on-resistance) and unrecoverable degradation (e.g. access resistance of contacts, and gate leakage current) persist to be limiting reliability factors.

The mechanisms contributing towards performance and reliability degradation of AlGaN/GaN HEMTs, namely self-heating, charge trapping and strain, are required to be minimised; an important step before large-scale deployment can be attained. The strong coupling of these degradation mechanisms, under normal device operation, makes the quantitative contribution of each mechanism indistinct due to the lack of standard characterisation techniques.

In this Thesis, the impact of the source/drain (S/D) and gate terminals of an AlGaN/GaN HEMT on its thermal management was investigated. Using Infrascope measurements, a substantial increase in temperature and resistance at the inner ends of the S/D contacts was observed. High-resolution X-ray diffraction technique combined with drift-diffusion (DD) simulations showed that strain reduction at the vicinity of S/D contacts is the origin of temperature rise. The strain reduction was also observed below the metal gate. Through electro-thermal simulations, the electrical stress on Ohmic contacts was shown to reduce the strain; leading to the inverse/converse piezoelectric effect.

A new parametric technique was developed to decouple the mechanisms constituting device degradation in AlGaN/GaN HEMTs under normal device

operation, namely self-heating and charge trapping. Both source (I_S) and drain (I_D) transient currents were used under various biasing conditions to analyse charge trapping behaviour. Two types of charge trapping mechanisms have been identified: (i) bulk trapping occurring on a time scale of < 1 ms, followed by (ii) surface trapping and redistribution > 1 ms. Through monitoring the difference between I_S and I_D, bulk trapping time constant is shown to be independent of V_{DS} and V_{GS}. Also, V_{GS} is found to have no effect on the bulk trap density. Surface trapping is found to have a much greater impact on slow degradation when compared to self-heating and bulk trapping. At a short time scale (< 1 ms), the RF performance is restricted by both bulk trapping and self-heating effects. At a longer time scale (> 1 ms), the dynamic ON resistance degradation is limited mainly by surface trapping accumulation and redistribution.

Using the understanding of the degradation mechanism behaviour and origins, optimisations to the Ohmic and Schottky contacts as well as a new AlGaN/GaN HEMT architecture were proposed. In an attempt to improve the thermal management of S/D contacts, an Ohmic contact recess process is proposed to reduce the access resistance and enhance DC/RF performance of AlGaN/GaN HEMTs with a high Al concentration. A contact resistance (R_C) of ~0.3 Ω.mm was achieved via optimal recess conditions. Small R_C was found to lead to a higher current density at the inner edges of the contact, which resulted in a large increase of channel temperature beneath the S/D contacts. A highly n-doped AlGaN overgrowth layer was proposed to reduce the current density, and thus channel temperature at the Ohmic contacts. Titanium Nitride (TiN) Schottky processing was implemented to minimise the observed strain reduction beneath the gate metal. The optimal Schottky contact is obtained for TiN thicknesses of < 10 nm, which preserves the strain within the AlGaN barrier layer. As a result, Schottky barrier of 1.06 eV, a leakage current of 6 nA and improved linearity of 1.6 was achieved. In addition, C – V and I – V characterisations revealed very low trapping density within the optimised device. Lastly, a new device architecture was proposed to increase the 2-dimentional electron gas (2DEG) density and mobility, without compromising the enhancements of our proposed S/D and gate optimisations. This structure consists of (i) step-graded AlGaN barrier layer to increase strain and (ii) AlN spacer layer.

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ABBREVIATIONS

µ-RTD	Micro-resistance thermal detector
2D	Two-dimensional
2DEG	Two-dimensional electron gas
ADC	Analog-to-digital converter
Al	Aluminium
Al_2O_3	Sapphire
AlGaAs	Aluminium gallium arsenide
AlN	Aluminium nitride
Ar	Argon
Au	Gold
B	Magnetic field
BE	Binding energy
BHFFOM	Baliga's high-frequency figure of merit
BL	Blue luminescence
CCD	Charge-coupled device
Cu	Copper
DC	Direct current
DD	Drift-diffusion
DEG1	Fast degradation period
DEG2	Slow degradation period
DLTS	Deep-level transient spectroscopy
DUT	Device under test
E	Electric field
EDS	Energy dispersive spectroscopy
ET	Electro-thermal
FE	Field emission
FIB	Focus ion beam
FOM	Figure of merit
FWHM	Full width at half maximum
Ga	Gallium

GaAs	Gallium arsenide
GaN	Gallium nitride
G-TLM	Gate transmission line model
H_2O	Water
HEMT	High electron mobility transistor
HF	High frequency
HNO_2	Nitrous acid
HP	High purity
HRTEM	High-resolution transmission electron microscopy
HR-XRD	High-resolution x-ray diffraction
HVPE	Hydride vapour phase epitaxy
IC	Integrated circuit
III-N	Group III-nitrides
I-limit	Current limit
InN	Indium nitride
IR	Infrared
JFOM	Johnson's figure of merit
KFOM	Keyes' figure of merit
LED	Light emitting diode
MBE	Molecular beam epitaxy
MESFET	Metal-semiconductor field-effect transistor
MIS	Metal/interface layer/semiconductor
MMIC	Monolithic microwave integrated circuit
Mo	Molybdenum
MOCVD	Metal organic chemical vapour deposition
MODFET	Modulation-doped field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MOVPE	Metal-organic vapour-phase epitaxy
MS	Metal/semiconductor
N	Nitrogen
NH_3	Ammonia
Ni	Nickel
O_2	Oxygen

PA CNTRL	Preamp control
PL	Photoluminescence
PMU	Pulse measure unit
Pt	Platinum
RF	Radio frequency
RL	Red luminescence
RPM	Remote pulse measure unit
RTA	Rapid thermal annealing
S/D	Source/drain
SAR	Successive approximation register
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon carbide
SiN	Silicon nitride
SiO_2	Silicon dioxide
SMU	Source measure unit
SRH	Schottky-read-hall
TCAD	Technology computer-aided design
TE	Thermionic emission
TFE	Thermionic field emission
Ti	Titanium
TLM	Transmission line model
TLTLM	Tri-layer transmission line model
UV	Ultra-violet
V-limit	Voltage limit
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
YL	Yellow luminescence

PHYSICAL CONSTANTS

c	Speed of light	$(3 \times 10^{8}\ \text{m s}^{-1})$
h	Planck's constant	$(6.626 \times 10^{-34}\ \text{m}^2\text{kg s}^{-1})$
k_B	Boltzmann constant	$(1.381 \times 10^{-23}\ \text{m}^2\text{kg s}^{-2}\text{K}^{-1})$
q	Charge of electron	$(1.602 \times 10^{-19}\ \text{C})$

SYMBOLS

a	Basal plane edge length
a_{bf}	in-plane lattice constant of the buffer
a_{sub}	in-plane lattice constant of the substrate
A^*	Effective richardson constant
A_n	Model parameter specific to semiconductor material used
b	Bowing parameter
c_0	Ideal unit height of crystal cell
C_{13}, C_{33}	Elastic constant
C_H	Heat capacitance per unit volume
C_{TH}	Thermal capacitance
d	Distance between devices
E_{00}	Characteristic energy related to the transmission probability of the carrier through a Schottky barrier
E_C	Conduction band energy
E_{BD}	Breakdown electric field
E_{crit}	Critical electric field
E_F	Fermi level
E_{FM}	Metal Fermi level
E_g	Bandgap
E_T	Trap energy
E_{TC}	Carbon trap energy
E_{TI}	Iron trap energy
E_V	Valence band energy
f	Current division factor
f_{max}	Maximum oscillating frequency
f_T	Gain cut-off frequency
G	Conductance
G_c	Carrier generation rate
G_m	Extrinsic transconductance
H	Heat generation
I	Current

i_1	Lateral current distribution at the alloy/AlGaN interface
i_2	Lateral current distribution at the metal/alloy interface
i_3	Current collected by the metal layer of the contact
I_{DS}	Drain-source current
$I_{leakage}$	Gate leakage current
I_{OFF}	OFF-state current
I_{ON}	ON-state current
I_{RTD}	Current through μ-resistance thermal detector
j_n	Current density of electrons
j_p	Current density of holes
L	Distance between ohmic contacts
L_G	Gate contact length
L_{GD}	Gate-to-drain distance
L_{SD}	Source-to-drain distance
L_{SG}	Source-to-gate distance
L_T	Transfer length
m_e^*	Electron effective mass
n	Electron concentration
N_{crit}	Doping concentration when the mobility reaches the average value of μ_{max} and μ_{min}
N_B	Impurity density concentration
N_D	Donor concentration
n_s	Electron sheet density
p	Hole concentration
P	Power density
P_{DISS}	Dissipated Power
p_g	Arbitrary band-gap energy parameter
P_n	Thermoelectric power of electron
P_p	Thermoelectric power of hole
P_{PE}	Piezoelectric polarisation
P_{SP}	Spontaneous polarisation
r	Strain relaxation
R	Bulk recombination rate of carriers

$R_{\square}$	Sheet resistance
R_C	Ohmic contact resistance
R_f	Resistance of the alloy sidewall of the Ohmic contact
R_{OFF}	OFF-state resistance
R_{ON}	ON-state resistance
R_{sa}	Sheet resistance of the metal/alloy interface
R_{SH}	Sheet resistance outside of the Ohmic contact area
R_{SK}	Sheet resistance beneath the metal of the Ohmic contact
R_{su}	Sheet resistance of the alloy/semiconductor interface
R_T	Total resistance
R_{TH}	Thermal resistance
S	Metal contact area
t	Time
t_{br}	Thickness of step-graded barrier layer
t_{bf}	Thickness of buffer layer
t_E	Pulse edge time
t_t	Wafer thickness
t_D	Alloy depth
t_{sp}	Thickness of spacer layer
t_W	Pulse width
T	Temperature
T_{CH}	Channel temperature
T_L	Local lattice temperature
V_{BD}	Breakdown voltage
V_D	Drain voltage
V_{DF}	OFF-state drain voltage
V_{DM}	ON-state drain voltage
V_{DS}	Drain-source voltage
V_{GF}	OFF-state gate voltage
V_{GM}	ON-state gate voltage
V_H	Hall voltage
V_m	Metal voltage
V_S	Source voltage

v_{sat}	Saturation velocity
V_{SC}	Semiconductor voltage
V_{TH}	Threshold voltage
W	Metal contact width
WF	Metal work function
x	Aluminium concentration percentage
x_{AlGaN}	Electron affinity of AlGaN
α	Lattice constant of semiconductor material
α_g, β_g	Empirical constant for GaN
$\alpha_\lambda, \beta_\lambda$	Fitting coefficient
β, γ, δ	Temperature dependent coefficient
ΔT	Temperature rise
ε	Strain within semiconductor material
$\varepsilon_{13}, \varepsilon_{33}$	Piezoelectric coefficient
ε_r	Semiconductor dielectric constant
η	Ideality factor of Schottky contact
λ	Thermal conductivity
μ	Electron mobility
ρ	Resistivity of semiconductor material
ρ_c	Specific contact resistivity
ρ_{ca}	Specific contact resistance of the metal/alloy interface
ρ_{cu}	Specific contact resistance of the alloy/semiconductor interface
σV_g	Schottky gate voltage
τ_i	Thermal time constant
Φ_{bn}	Schottky barrier height
Φ_{MG}	Metal work-function
Φ_n	Quasi-fermi level of electron
Φ_p	Quasi-fermi level of hole

CHAPTER 1

INTRODUCTION

Since the fabrication of the first silicon (Si) device in 1958 by Gibbons' Stanford laboratory [1], Si-based devices have been, by far, the most widely used technology in the semiconductor industry. The Si metal-oxide-semiconductor field effect transistor (MOSFET) has been the primary driver for the growth of the industry. However, Si MOSFETs have reached their limit in terms of power density, mobility and efficiency [2]–[8]. Also, scaling of these devices will reach its theoretical limit in the coming years as a result of the intrinsic material properties such as: (i) low breakdown voltage, (ii) low saturation velocity, (iii) low inversion layer mobility, and (iv) high device resistance [9]. To account for these limitations, several new semiconductor materials have been developed to accommodate the increasing need for devices that can provide higher output power at higher operating voltages and higher operating frequencies. In particular, III-nitride semiconductors such as gallium nitride (GaN) have gained significant attention in accommodating this need due to their superior material properties.

1.1. Background

To begin our investigation into III-N-based devices, we firstly advanced our knowledge in the development of GaN technology since its discovery; this includes the use of GaN technology applications and market. The importance of GaN in these applications has been shown through a comparison with other competing semiconductor materials using a range of Figures of Merit (FOMs).

1.1.1. History of GaN Technology

Since the discovery of Gallium (Ga) in 1897, the use cases of the newly found material were minimal. The introduction to the most widely used Ga compound in application today was not developed until 1930, where the first synthesis of GaN was produced [10]. Interest in the new compound did not reach any significance until 1938, where a technique was to powder GaN, producing small needles and platelets in order to investigate its crystal structure and lattice constant [11]. Successful and notable research into the development of GaN from this point did not arise until 1969, when the first deposition of GaN was produced using Hydride Vapour Phase Epitaxy (HVPE) [12]. Soon after, in 1971, the first GaN light emitting diode (LED) was fabricated [13]. This is the beginning of a large growth in the GaN market in industrial applications. The reason this development was so crucial to the market is that GaN is one of

few semiconductor materials that is capable of emitting blue light. This development is important as the optical applications of GaN are the driving force of the GaN market, even today.

The idea of a high-electron mobility transistor (HEMT) was introduced in 1980 with the aluminium gallium arsenide-on-gallium arsenide (AlGaAs/GaAs) HEMT [14]. The novelty of this structure is that two materials of different bandgaps are incorporated into the device structure to form a channel as opposed to the structure of an inversion layer device. This new structure introduced the idea of dopant injection prevention in the semiconductor material that would cause device damage, thereby reducing device mobility and reliability. It was only in 1991 that GaN technology caught up with this newly discovered structure. Here, the rapid progression in the development of GaN began when the first normally-ON AlGaN/GaN HEMT was produced via metal organic chemical vapour deposition (MOCVD) [15]. A crucial property to GaN's success today was also discovered in 1991 from this structure as a result of the technological improvements towards wafer production under high temperature. A high electron density channel at the AlGaN/GaN interface, known as the two-dimensional electron gas (2DEG) was also discovered in 1991. From this point on, rapid progression and interest was gained by academic research and industry in the development of GaN. A notable milestone was achieved in the GaN industry in 2000, when AlGaN/GaN HEMT technology was successfully grown on Si substrates via MOCVD [16]. The first normally-OFF GaN based modulation-doped field-effect transistor (MODFET) was fabricated in 1995 [17], although, the first patent involving normally-OFF GaN-based devices was not submitted until 2001 [18].

More recent developments came in 2007, when Toshiba developed a new GaN HEMT that operates at Ku-band (12 GHz to 18 GHz) that achieved 65.4 W at 14.5 GHz [19]. This technology was to add an n-GaN cap layer to an AlGaN/GaN HEMT grown on silicon carbide (SiC). Transphorm established the first qualified 600 V GaN-on-SiC device in 2009 and 600 V GaN-on-Si in 2010 [20]. Also in 2010, the first commercially available GaN power device was introduced by International Rectifier. At this point, a highly sophisticated, ultra fast monolithic microwave integrated circuit (MMIC), matched to a multi-switch monolithic GaN-based power device, was produced, doubling the switching speed of state-of-the-art silicon-based integrated power stage devices [21]. This was the highest operating voltage observed for GaN HEMTs at

the time. From then, adoption of GaN-based technology exponentially increased as GaN became a viable solution for more applications. Soon after, in 2012, a merge in operations between Fujitsu Semiconductor and Transphorm occurred. From then on, many new applications were introduced into the market with the new 600 V GaN device platform such as the world's first photovoltaic power conditioner, ultra-small AC adapters, highly efficient motion control, high-density power supplies for personal computers, servers and telecoms equipment, and many more [22].

1.1.2. Why GaN Technology?

GaN is a material that is used in the production of many semiconductor applications that are later described. The technology has demonstrated that it is significantly more capable than the commonly used Si devices for a range of applications. The limitation of Moore's Law for Si devices prevents the increase of power capabilities of Si [23]. Therefore, GaN is the new emerging technology that can overcome the power and frequency limitations of Si. With its ability to conduct a much higher density of electrons at higher velocity, all at a low production cost, GaN-based devices are increasing its value in the semiconductor industry [24], [25]. The following presents a current list of exceptional properties that are responsible for the success of GaN technology:

- A large breakdown field is achieved from the large bandgap of GaN, which is particularly useful for high power applications. The relationship between the critical field, E_{crit}, and bandgap, E_g, is given by [26]:

$$E_{crit} = 1.02 \times 10^7 \sqrt{\frac{q}{\varepsilon_r}} {N_B}^{1/8} {E_g}^{3/4} \qquad (1.1)$$

  Where q is the charge of an electron, ε_r is the permittivity of GaN, N_B is the impurity density concentration.

- The high electron saturation velocity of GaN, $v_{sat} \approx 1.7 \times 10^7$ cm s^{-1} at 300 K, is a particularly desired parameter for high frequency applications. This is a temperature dependent parameter that is enhanced considerably in AlGaN/GaN HEMTs, to be explained in Section 2.1.2. However, for bulk semiconductor materials, v_{sat} is calculated by:

$$v_{sat}(T_L) = \frac{v_{sat,300K}}{(1 - A_n) + A_n \cdot \left(\frac{T_L}{300}\right)} \quad (1.2)$$

where $v_{sat,300K}$ is the electron saturation velocity at 300 K, A_n is a model parameter specific to the semiconductor material used, and T_L is the lattice temperature.

- GaN has the ability to operate under extreme temperatures (up to 700 ºC) [27], [28] when formed into a HEMT structure. Along with their high-frequency and high-power capabilities, this is significantly beneficial for harsh environments.
- High quality GaN-based devices can be grown onto large diameter Si substrates. As a result, GaN production costs are considerably low and can be integrated onto many Si applications.
- GaN is a direct band gap material where no additional energy is required to recombine into excitons. This is particularly useful for oscillator, amplifier and photovoltaic applications. The bandgap of GaN (3.4 eV) allows for photons of around 450 nm wavelength (blue light) to be emitted upon recombination of electrons and holes [29], which allows GaN to be used as a blue LED. The bandgap is conveniently in the ultra-violet (UV) region which means that electrons in the GaN bulk excite to the conduction

Table 1.1: A comparison of the material properties of GaN and other competitors in the semiconductor industry.

Property	GaN (AlGaN/GaN)	Si	4H-SiC	GaAs
Bandgap, E_g (eV)	**3.4**	1.1	3.3	1.4
Breakdown electric field, E_{BD} (MV cm^{-1})	**2.0 (5.6)**	0.3	3.0	0.4
Electron mobility, μ (cm^2 V^{-1}.s^{-1})	**900 (2000)**	1400	700	8500
Electron saturation velocity, v_{sat} ($\times 10^7$ cm s^{-1})	**1.5 (2.5)**	1.0	2.0	2.0
Thermal conductivity, λ (W cm^{-1}.K^{-1})	**1.5**	1.5	5.0	0.5
Dielectric constant, ε_r	**8.9**	11.7	10.0	12.9

band when exposed to UV light with >364 nm wavelength. This makes them exceptionally good as UV detectors.

In addition, a comparison of the fundamental material properties of Si, GaN, 4H hexagonal polytype Silicon Carbide (SiC), and GaAs is shown in [30], [31]. Although GaAs needs doping to operate as a device, the mobility provided is for undoped GaAs and, hence, is significantly larger than if it were doped. These properties allow GaN-based devices to operate under high temperature and high pressure environments where Si devices are incapable of functioning. To note, AlGaN/GaN-based devices have enhanced properties whereby μ is increased to 2000 cm^2 $V^{-1}s^{-1}$ and v_{sat} is increased to 2.5×10^7 cm s^{-1}.

1.1.3. GaN Applications and Market

GaN-based devices have been implemented into a range of applications, shown by the III-nitrides device applications roadmap given in Figure 1.1, such as high-frequency, high-power-RF, renewable energy, automotive, UV/IR-sensors, low-cost surveillance, street-lighting, weather-systems, environmental-friendly, solar-blind, radars, 4G/WiMAS base-stations, ultra-wide-band communication, low-noise, ultra-scaled high-temperature, military, sensors for harsh environmnents, biological research,…etc [32]–[51]. The inset of Figure 1.1 shows the significant advantages of III-nitride materials over conventional semiconductors in several device parameters. As a result, many UK and international companies, such as GaN-Systems, Cree, Infineon & Panasonic, Toshiba, Fujitsu & Transphorm, Texas Instruments, Navitas, NXP-semiconductor, Dynex, Oxford-Plasmatech, IXYS, Thales, OMMIC etc., are substantially increasing their investments toward GaN research and gaining scale to reach a high-level of mass production [52]. For example, NXP-semiconductor has spent over £2.5M in 2014 on the process technology of GaN blue LEDs [51], [54]. In addition, the UK government and EU-Commission are supporting academia to boost research into the development of the GaN technology by providing more funding grants and encouraging for closer collaborations between academia and industry [45], [52], [54]. An example of such actions is the ‘UK PowerGaN’ consortium that includes 7 UK universities and 12 UK companies [55]. The market value of these devices stands to exponentially increase to an estimated $600m by 2024 and $1.7bn by 2027 [56].

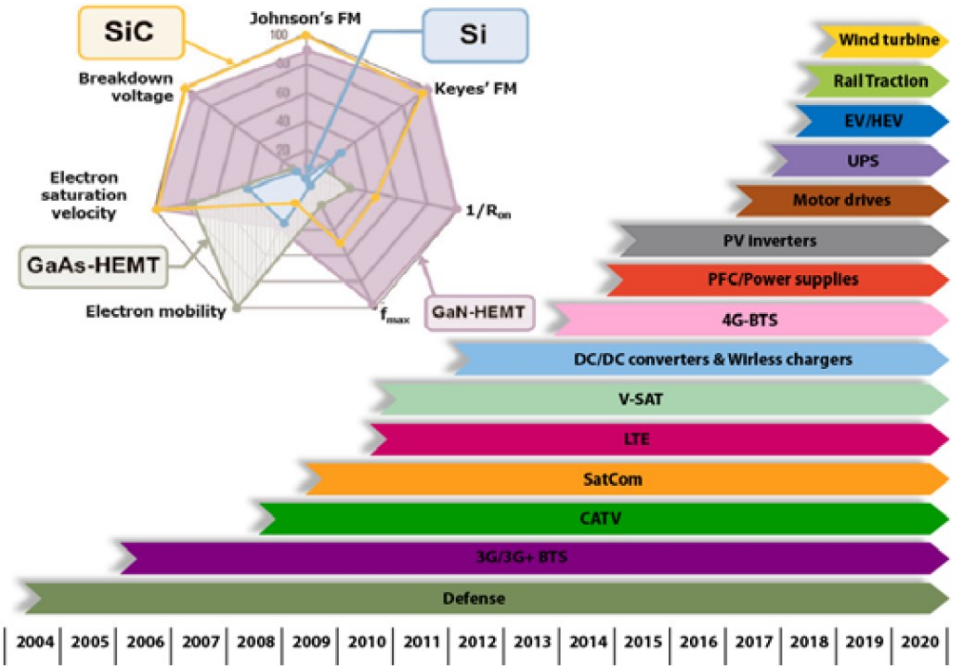

Figure 1.1: III-Nitrides device applications roadmap (short, mid and long-term growth driver). The inset shows a comparison of GaN, 4H-SiC, Si and GaAs high-power RF transistors [57].

1.1.4. Figures of Merit

In addition to the superior material properties of GaN, several widely used FOMs show the value of GaN in a range of applications. Each FOM is used for benchmarking semiconductors with respect to different application types. These FOMs take into account several relevant material properties that contribute towards the particular application type that the FOM is aimed towards. The higher the FOM value the higher performance that the semiconductor has in the relevant application type.

To begin, Johnson's Figure of Merit (JFOM) provides a quantitative estimate for the performance of a semiconductor material in high power applications operating at high frequencies. The relevant material properties are accounted for in the JFOM calculation [26]:

$$JFOM = \frac{E_{BD} v_{sat}}{2\pi} \qquad (1.3)$$

where E_{BD} is the breakdown electric field, and v_{sat} is the electron saturation velocity.

Secondly, Baliga's High-Frequency Figure of Merit (BHFFOM) focuses on the performance of field-effect transistors at high frequency power switching applications, where switching

losses are dominant, showing that significant power loss reduction can be achieved with high BHFFOM [58]:

$$BHFFOM = \mu E_{BD}^2 \left(\frac{V_G}{4V_B^3}\right)^{1/2} \quad (1.4)$$

where μ is the charge carrier mobility, V_G is the gate drive voltage, and V_{BD} is the breakdown voltage.

Finally, Keyes' Figure of Merit (KFOM) is used to estimate the thermal limitation to the switching behaviour of transistors when used in integrated circuits (ICs) [59]:

$$KFOM = \lambda \left(\frac{c v_{sat}}{4\pi \varepsilon_r}\right)^{1/2} \quad (1.5)$$

where λ is the thermal conductivity, c is the velocity of light (3×10^{-8} m s^{-1}), and ε_r is the dielectric constant.

Table 1.2 quantitatively depicts the suitability of GaN and other competing semiconductor materials in a range of application types with respect to various FOMs. A JFOM of 270 – 480 and 324 – 400 for GaN and 4H polymorphism of SiC, respectively, shows that both materials dominate in suitability for high-power and high-frequency applications [31]. GaN, however, is superior to 4H-SiC and all other competitors when compared with BHFFOM, boasting 17 to 34 times the suitability as Si, 1.5 to 2.5 times that of GaAs and 3 times that of SiC. The only FOM that has been used for comparison where GaN is not superior is KFOM. This is due to the large thermal conductivity of 4H-SiC compared to GaN. However, GaN is still 1.4 times

Table 1.2: A comparison of the various Figures of Merit (FOM) for GaN and other semiconductor competitors [26].

Property	GaN	Si	4H-SiC	GaAs
Johnson's Figure of Merit, *(JFOM)*	**760**	1.0	180	7.1
Baliga's High-Frequency Figure of Merit, *(BHFFOM)*	**77.8**	1.0	22.9	10.8
Keyes' Figure of Merit *(KFOM)*	**1.6**	1.0	4.61	0.45

larger than Si and 3.5 times that of GaAs but 4H-SiC is much larger than GaN for this FOM.

Regardless, for high-power and high-frequency applications, III-N semiconductors, GaN in particular, are far superior to that of Si.

1.2. Rationale

Regardless of the superior performance of III-N-based devices, and particularly AlGaN/GaN HEMTs, achieving reliability at the same time as the high performance that the device boasts is a factor that is holding back widespread commercial and industrial development [60], [61]. Recoverable degradation, e.g. current collapse and on-resistance, along with unrecoverable degradation, e.g. access resistance of contacts, and gate leakage current persist to be limiting reliability factors [60]–[62]. In addition, the access resistance of AlGaN/GaN HEMTs is required to be reduced in order to obtain optimal performance.

Despite the increasing efforts that have been devoted to improving reliability in III-N devices, a well-defined understanding of the underlying physics and mechanisms of defects and limitation effects is still largely unknown and currently impedes the device reliability progress [60], [61]. The mechanisms contributing towards degradation of AlGaN/GaN HEMTs, namely self-heating, charge trapping and strain, are required to be analysed in order to develop this understanding. To identify the primary mechanism contributing towards the device degradation, these degradation mechanisms need to be decoupled using a newly developed electrical parametric technique.

1.3. Research Aim and Objectives

In this Thesis, we evaluate the degradation and failure mechanisms of AlGaN/GaN-based devices, namely (i) self-heating, (ii) charge-trapping, and (iii) strain, with the aim to analyse strain-induced self-heating effects on access resistance and to decouple self-heating from charge trapping. These degradation mechanisms contribute towards current collapse and degradation of both power and radio-frequency (RF) performance. Through the knowledge gained from understanding the degradation mechanisms, we propose new device architectures to improve device reliability. In order to achieve this, the following objectives are realised:

1. Investigate the self-heating and strain mechanisms in AlGaN/GaN HEMTs using

Infrared (IR) Camera and High-Resolution X-Ray Diffraction (HR-XRD) technology under various biasing conditions.

2. To identify the relationship between device geometry and polarisation within AlGaN/GaN-based devices.
3. For the first time, develop a new electrical characterisation technique to decouple charge trapping mechanisms, namely bulk trapping and surface trapping, from self-heating under normal device operation.
4. Identify the primary cause of device dynamic degradation from the newly developed electrical characterisation technique.
5. Optimise the Ohmic contacts of AlGaN/GaN HEMTs by developing new process technology to reduce the contact resistance and improve device performance.
6. Improve the Schottky contacts through the optimisation of the TiN metallisation scheme to reduce gate leakage and enhance the high frequency capabilities of the device.
7. Propose new device architectures with the replacement of several layers of a conventional HEMT to enhance the 2DEG density and electron mobility within the device.

1.4. Organisation

Chapter 1 describes a background to GaN technology, including its history, why it is used in industrial applications, what those applications are, and its FoMs that determine its applicability in various application types (e.g. high power or RF). The rationale behind the research carried out through this Thesis is then given, briefly describing the issues with III-N-based devices, the importance of understanding these issues, and need for a new reliability characterisation technique to be developed. This leads to the research aim and objectives that are accomplished throughout this Thesis in order to challenge the device limitations. Finally, the original contribution towards the III-N-based device reliability field that the work in this Thesis presents is discussed.

Chapter 2 of this Thesis introduces a background to the physical properties of III-N materials. The typical Wurtzite crystal structure, the material properties of GaN and its polarisation effects are discussed. From then, an in-depth description of AlGaN/GaN based devices is given to provide fundamental understanding of the device used throughout the research given in this

Thesis. Included in this section is an explanation of (i) the physics behind the formation of a 2DEG channel at the AlGaN/GaN interface, (ii) the operation of an AlGaN/GaN HEMT, (iii) the choice of substrate and contact metallisation, (iv) its state of the art, and (v) comparison versus other competing semiconductors. In addition, a discussion is made for non-invasive and employed characterisation techniques used for measuring the operating temperature distribution (Infrared, Micro-Raman, Micro-Resistance thermal detector), charge trapping (Photoluminescence), strain (High-resolution X-ray diffraction), 2DEG sheet density, electron mobility (Hall-effect) and I – V characteristics (DC and Pulse measurements). Finally, the current development challenges for GaN technology are discussed to provide rationale for the research that follows this chapter.

Chapter 3 involves strain-induced self-heating effects on source/drain access resistance of AlGaN/GaN-based devices and interplay of self-heating and polarisation. There is not a well defined understanding of the origins of access resistance degradation during normal device operation within AlGaN/GaN-based devices. Therefore, we investigate the temperature and strain profiles within small and large AlGaN/GaN Transmission Line Models (TLMs) as well as AlGaN/GaN HEMTs using an IR camera and HR-XRD. Additionally, AlGaN/GaN TLMs are simulated to understand the interplay between device geometry with self-heating and polarisation. Calibrated technology computer aided design (TCAD) simulations are used to show that hot spots of temperature at the edge of the drain contact is induced by high electric field. Also, inverse piezoelectric effect is shown to decrease with decreased device length due to stress on Ohmic contacts.

Chapter 4 focuses on the development of a new electrical parametric technique to characterise drain and gate induced charge trapping. This is accomplished with the exclusion of self-heating and under normal device operation. The range of misconceptions of current research, investigating the cause of degradation of transient current, lead us to examine this degradation using our newly developed technique. The source and drain transient currents are measured under normal operating conditions in order to analyse the charge trapping contribution to transient current degradation with the exclusion of self-heating, for the first time. The dependency on biasing conditions for both bulk and surface trapping are then found through analysis of the current transient measurements. Finally, the primary contribution towards

transient current degradation is identified to lead us towards the primary focus for optimisation of device architecture.

Chapter 5 proposes several optimisations to the Ohmic and Schottky contacts as well as device architecture in order to minimise degradation and improve the reliability of AlGaN/GaN-based devices. The output of this research is the result of collaborations with University of Lille, Swansea University and University of Malaya. The reduction of access resistance, identified as an issue in Chapter 3, is accomplished through (i) recessing Ohmic contacts into the AlGaN barrier layer and (ii) overgrowing the AlGaN at an angle to reduce self-heating effects. A proposition for optimising the Schottky contact through implementation of a TiN metallisation is then investigated to understand how it reduces gate leakage and enhances operating frequency. The results gained from these two propositions are experimental measurements. Finally, to enhance the 2DEG electron mobility, a new simulated AlGaN/GaN HEMT architecture is proposed. This is achieved through the implementation of a (i) step-graded AlGaN barrier, (ii) AlN spacer, and (iii) InGaN channel layer, which contributes towards the applicability of AlGaN/GaN HEMTs in applications of high-power and high-frequency requirements.

Chapter 6 concludes the work provided by each chapter throughout this Thesis. In addition, a discussion of the future works for this project is given.

1.5. Original Contribution to Research Field

A variety of tasks have been accomplished in the research constituting this Thesis. The original contributions to the research field are as follows:

1. Successfully investigated the temperature rise at Ohmic contacts in AlGaN/GaN-based devices. Using Infrared temperature mapping system measurements, a large increase in temperature at the S/D contacts of a long AlGaN/GaN gateless device was observed. These temperature peaks are shown to be coupled in smaller devices, owing to the large increase in temperature at the centre of the device. For gated devices, the thermal coupling is revealed to enhance the temperature peak at the drain-side edge of the gate. Additionally, HR-XRD measurements and Drift-Diffusion (DD) simulations show a reduction in strain at the S/D Ohmic contacts. This is found to be the reason behind the

temperature rise within AlGaN/GaN-based devices.

2. Effects of device geometry on self-heating effects in AlGaN/GaN-based devices is analysed using DD transport model simulations. In shorter devices, the limitation of current in I – V characteristics was found to occur sooner than in long structures as a result of increased lattice temperature. In addition, the total polarisation within the device is found to reduce in larger devices due to the inverse piezoelectric effect, which has a direct impact on the degradation of 2DEG density within the channel.
3. A new source and drain transient currents characterisation technique has been developed for decoupling charge trapping from self-heating in AlGaN/GaN HEMTs under normal device operation. Using this technique, charge trapping behaviours under various bias conditions have been analysed with the exclusion of self-heating. Charge carriers that are trapped within the GaN bulk layer (bulk trapping) has been identified to be equal to the difference between the source current (I_S) and drain current (I_D). The bulk trapping magnitude is found to change as a result of drain bias, but not gate bias. Additionally, surface trapping is shown to be the dominant mechanism in slow degradation over a slow self-heating mechanism and its magnitude and its time to temperature saturation (temperature time constant) are dependent on both drain and gate bias.
4. Source and drain Ohmic contacts are etched into the AlGaN barrier layer of the AlGaN/GaN HEMT in order to reduce its contact resistance, thereby increasing current density through the device. An AlGaN overgrowth layer for Ohmic contacts is also proposed to reduce self-heating effects near the contacts.
5. A TiN metalisation scheme is developed, to generate quasi-p type doping in the AlGaN barrier layer, which enhances Schottky arrier height and reduces gate leakage.
6. Several optimisations to the architecture of a conventional AlGaN/GaN HEMT are applied (i.e. step-graded barrier, exclusion layer, and InGaN channel layer) to improve 2DEG density and mobility.

CHAPTER 2

AlGaN/GaN-BASED DEVICE FUNDAMENTALS & CHARACTERISATION TECHNIQUES

An insight into the AlGaN/GaN-based device fundamentals and its characterisation techniques are discussed in this chapter. Firstly, the physical properties of III-N semiconductor materials are described, including crystal structure, the material properties of GaN and polarisation effects present in III-N based materials. A description is provided for the physical functionality of the quantum well at the heterojunction, also known as a 2-dimensional electron gas (2DEG), of AlGaN/GaN HEMTs. The structure, operation and growth of AlGaN/GaN HEMTs as well as the typical substrate choices are reviewed. In addition, various performance enhancing layers for AlGaN/GaN-based devices are revised. From then, the metallisation schemes of the Ohmic and Schottky contacts are described, showing their role in enhancing device performance. To show the current performance capabilities of AlGaN/GaN HEMTs, their state-of-the-art is provided. Additionally, the advantages and disadvantages of AlGaN/GaN heterojunction in comparison to bulk GaN based technologies are given. Degradation mechanisms, (i) self-heating, (ii) bulk-trapping, and (iii) surface trapping, are then discussed. Furthermore, a description of non-invasive characterisation techniques that are used throughout this Thesis is summarised. Finally, the challenges that are preventing widespread commercial and industrial development of AlGaN/GaN HEMTs are discussed, providing a basis to the rationale of this research.

2.1. Physical Properties of III-N Materials

This section describes two commonly used crystal structures (Wurtzite and Zinc-blende). In addition, the several material properties of GaN (the III-N material of focus for this Thesis) are discussed, including bandgap, electron drift velocity, electron mobility, electron effective mass and energy, and thermal conductivity. Finally, a major beneficial factor known as polarisation, namely spontaneous and piezoelectric polarisation, of III-N materials is explained.

2.1.1. Crystal Structure

The crystal structure of group III-N based semiconductor materials (i.e. GaN, AlGaN, AlN, InN) is either (i) Wurtzite (α-phase) or (ii) Zinc-blende (β-phase).

The GaN Wurtzite crystal, illustrated in Figure 2.1, is a stable and hexagonal structure that is non-centrosymmetric; it lacks inversion symmetry. In this structure, there are strong bonds of Ga and N, owing to the large bandgap of 3.4 eV in comparison to Zinc-blende structure of 3.2

eV. GaN is most commonly used in its Wurtzite crystal form with [0001] orientation when used in HEMTs. This crystal structure is also thermodynamically stable, which allows for its good thermal resistance. This is important to avoid disrupting the alignment of GaN atoms when subjected to intense heat of over 600 ºC given by annealing of Ohmic contacts during device fabrication. The Zinc-blende crystal structure is a meta-stable, face-centred cubic crystal structure. This structure is more common in conventional III-V semiconductors (e.g. GaAs, InP, and InSb) [63], [64]. In this Thesis, we focus on GaN in its Wurtzite form as it is the optimal crystal structure for our purposes [65], [66].

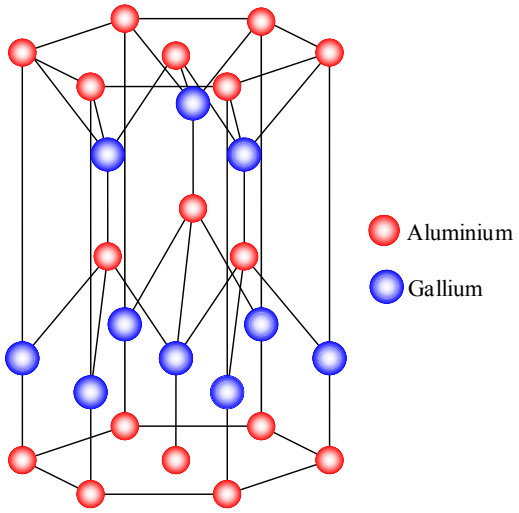

Figure 2.1: Crystal structure of GaN in Wurtzite form [67].

2.1.2. Material Properties

III-N semiconductor materials own exceedingly more beneficial material properties that dominate other conventional semiconductors. These include wide bandgap, high electron drift velocity, high electron mobility, good thermal stability, and relatively high thermal conductivity. Knowledge of the properties of III-N materials is essential for understanding device physics of AlGaN/GaN HEMTs.

2.1.2.1. Bandgap

The band gap (E_g) of a material is defined as the minimum energy required for an electron to move from the valence band (E_v) to the conduction band (E_c). This can be described as the difference in energy between the top of the valence band and the bottom of the conduction band of a material:

$$E_g = E_c - E_v \tag{2.1}$$

Materials with large band gap (> 9 eV) are considered to be insulators, zero bandgap for conductors, and in between for semiconductors. The wide band gap of GaN in Wurtzite crystal structure is 3.4 eV. This allows for its application in various high power applications. Additionally, direct band gap of GaN is the reason for its success in the blue LED market.

The bandgap of GaN is considered to be thermally stable, as modelled by the following equation:

$$E_g = E_{g,0K} - \frac{\alpha_g T_L^2}{\beta_g + T_L} \tag{2.2}$$

where $E_{g,0K}$ = 3.47 eV is the band gap at 0 K, α_g = 0.8 meV K^{-1} and β_g = 800 K are empirical constants for GaN, and T_L is the lattice temperature. These empirical constants for GaN are gathered from the research into modelling the band gap [68].

2.1.2.2. Electron Drift Velocity

The electron drift velocity is the average velocity that electrons attain within a material due to an applied electric field. It is essential for this property to be enhanced in order for devices to perform at high frequency. Using our in-house Monte Carlo simulators, the relationship between electron drift velocity and electric field at different lattice temperatures, ranging from 300 K to 700 K, is calculated, as shown in Figure 2.2. The linearity of drift velocity with electric field decreases at ~20 kV cm^{-1}, as a result of polar optical phonon emission [69]. Although, this phenomenon vanishes at high lattice temperatures. The peak drift velocity at 300 K and 700 K of 3 × 10^7 cm s^{-1} and 2.3 × 10^7 cm s^{-1} is reached at 150 kV cm^{-1} and 210 kV cm^{-1}, respectively. This can be explained by the fact that electrons gain enough energy for a transfer into the satellite valleys by intervalley phonon scattering. The increased relaxation of electron energy and momentum results in a higher critical electric field for heating electrons, which increases the probability of electron scattering into the satellite valleys. Thus, if we assume the constant separation energy for satellite valleys (we neglect a band gap renormalisation due to the change in temperature), the critical electric field increases with temperature, while the peak drift velocity decreases. However, the saturation velocity shows a reduction of 20 % in the temperature range of 300 K to 700 K, as shown in Figure 2.3. To note, a very good agreement

is obtained when our results are compared to [70].

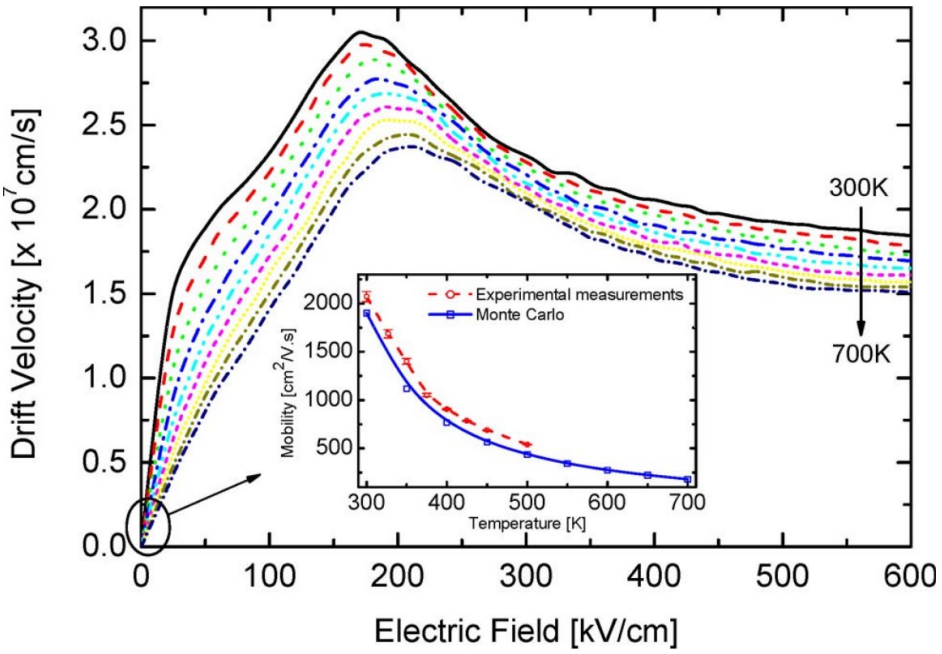

Figure 2.2: Electron drift velocity versus electric field in GaN for different lattice temperatures (from 300 to 700 K by a step of 50 K). The inset compares measured (dashed line) low field electron mobility of GaN as a function of the lattice temperature with Monte Carlo simulations (solid line).

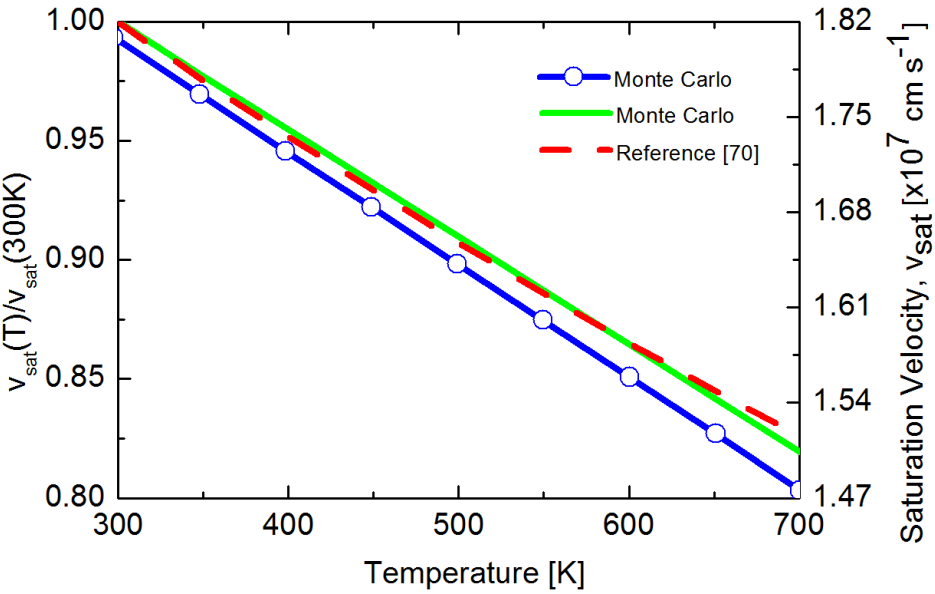

Figure 2.3: Saturation velocity of GaN versus lattice temperature. Comparison between the results of [70] (dash line) and the Monte Carlo data (solid line).

2.1.2.3. Electron Mobility

Similar to all semiconductor materials, the drift velocity per unit of electric field (electron mobility) of GaN is temperature dependent. Figure 2.4 shows measured and Monte Carlo calculated low field mobility at N_D = 10^{15} cm^{-3} and N_D = 10^{17} cm^{-3}. The electron mobility saturation is observed at very high lattice temperature, primarily limited by longitudinal optical phonon scattering. The measurements of low field mobility have been carried out in the temperature range of 300 to 500 K, due to the limitation of the Hall effect measurement. We observed a large drop of the electron mobility between N_D = 10^{15} cm^{-3} and N_D = 10^{17} cm^{-3}. The Monte Carlo data is compared to experimental results [71] showing very good agreement.

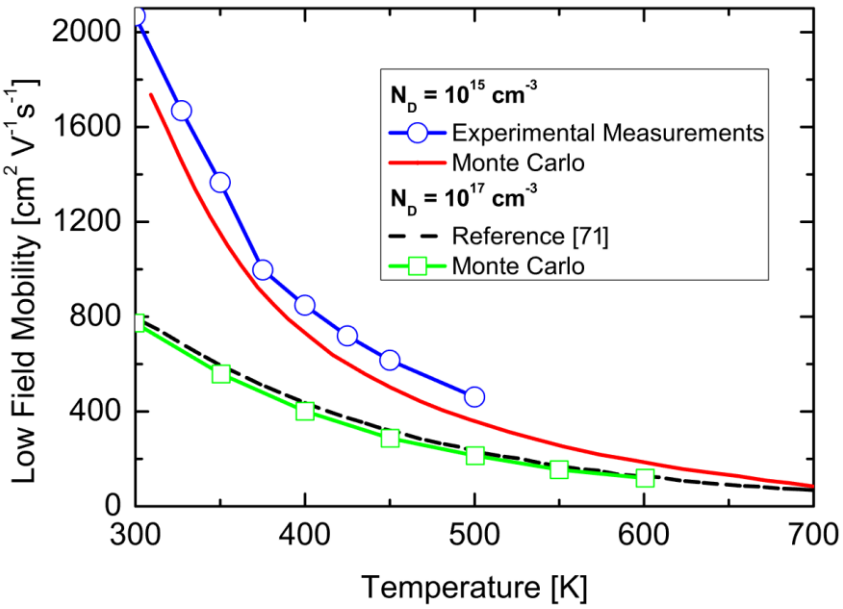

Figure 2.4: Low field mobility of GaN versus lattice temperature. Measured (circles) and Monte Carlo data at N_D = 10^{15} cm^{-3} (solid line) and N_D = 10^{17} cm^{-3} (dashed line).

2.1.2.4. Electron Effective Mass and Energy

Taking into account the electron scattering terms and degeneracy, our Monte Carlo simulations show that the electron effective masses and energy relaxation times are nearly identical for all considered lattice temperatures (Figure 2.5 and Figure 2.6) [72]–[75].

At low applied electric field, low electron energy, charge carrier scattering is dominated by (i) acoustic deformation potential scattering, (ii) piezoelectric phonon scattering and (iii) impurity scattering. At this point, electron temperature is less than the polar optical phonon temperature. Therefore, polar optical phonon emissions rarely occur and free carriers with low effective

mass are a majority. At the critical electron energy of ~2.2 eV and beyond, electrons are excited to higher energy valleys in the conduction band, whereby their effective mass is increased. With higher effective mass, greater collisions occur that increases the charge carrier scattering and reduces steady-state velocity.

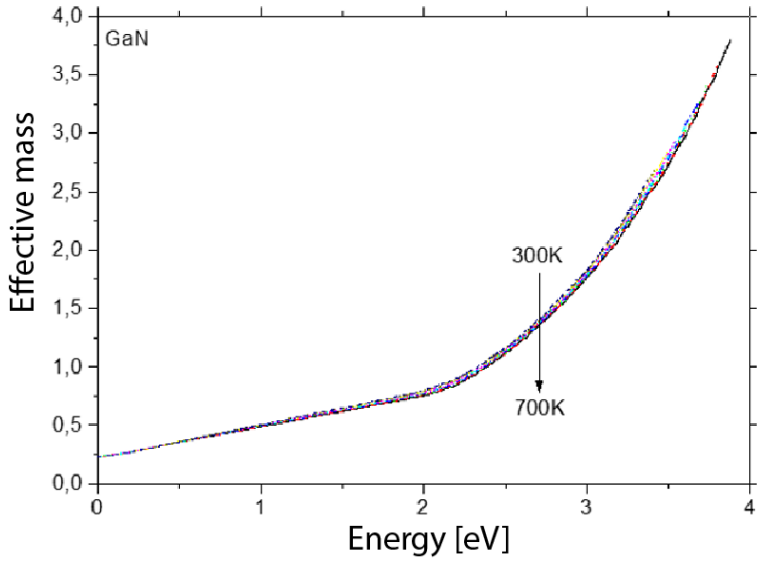

Figure 2.5: Effective mass as a function of electron energy at different lattice temperatures (from 300 K to 700 K by step of 50 K).

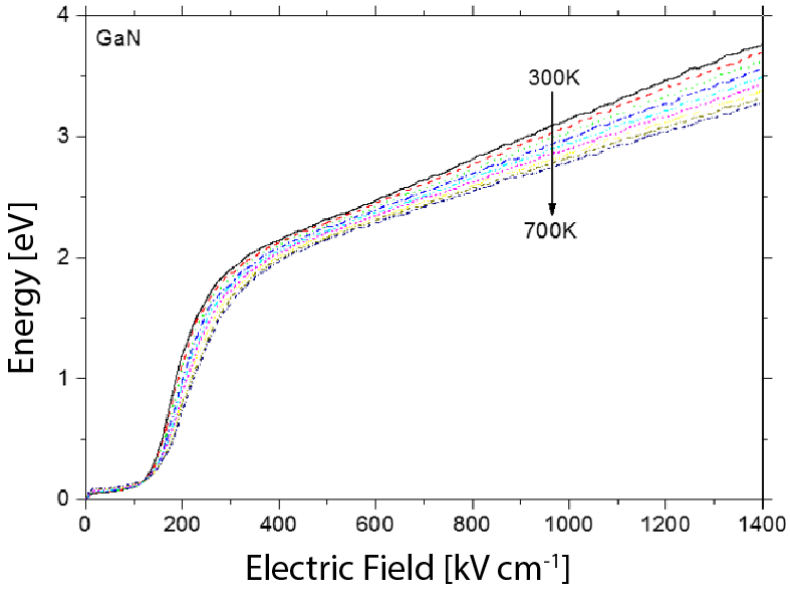

Figure 2.6: Energy – electric field characteristics at different lattice temperatures (from 300 K to 700 K by step of 50 K).

The increase of average electron energy with electric field is shown in Figure 2.6. Initially, the electron energy remains low and close to the thermal energy given by $3/2\, k_B T_L$; where k_B is Boltzmann's constant. This is due to the energy gained by electrons through the applied electric field being lost via polar optical phonon scattering. From the critical electric field (~180 kV cm^{-1}) to ~320 kV cm^{-1}, both polar optical phonon and intervalley scattering remain at relatively low rates. Hence, a large increase of energy occurs. The energy gain begins to saturate towards 320 kV cm^{-1} as intervalley scattering begins whereby an energy balance is re-established. To note, elastic scattering mechanisms such as acoustic deformation potential scattering, piezoelectric scattering, and impurity scattering do not impact the energy of the charge carriers.

2.1.2.5. Thermal Conductivity

The thermal conductivity, λ, is the property that characterises heat dissipation throughout a material. High power applications are particularly favoured devices that use high thermal conductivity materials for their ability to reduce self-heating and effective thermal management. The thermal conductivity dependency on temperature can be defined as [76]:

$$\lambda = \lambda_{300} \times \left(\frac{T_L}{300}\right)^{\alpha} \qquad (2.3)$$

Where λ_{300} is the thermal conductivity at 300 K and α is a fitting parameter. Using Equation (2.3) and parameters summarised in Table 2.1 for each substrate, the behaviour of thermal conductivity of several commonly used substrates (i.e. GaN, Si, SiC and Al_2O_3) with respect to lattice temperature is shown in Figure 2.7.

SiC is shown to be a good candidate in terms of thermal conductivity for low lattice temperatures. However, it degrades significantly when reaching higher temperatures. In addition, from a GaN-based device point of view, the influence of phonon scattering from the large thermal mismatch between the GaN buffer layer and SiC substrate induces greater thermal resistance at the GaN/SiC interface. Ideally, for high temperatures, GaN would be the optimal substrate, although, it is very costly for growing wafers with a GaN substrate. Therefore, SiC is the optimal substrate to use in terms of thermal conductivity. To note, Si would not be the most optimal in terms of thermal dissipation but will be the most beneficial substrate to use for co-integration of GaN-based devices into existing applications. Despite its low thermal conductivity, Al_2O_3 is still considered as a good candidate for optical applications.

Table 2.1: Thermal conductivity at 300 K and fitting parameters for each substrate used to measure thermal conductivity behaviour.

Material	λ_{300} [W m^{-1}K^{-1}]	α
GaN	125	-0.43
Si	148	-1.33
SiC	330	-1.61
Al_2O_3	23.1	-1

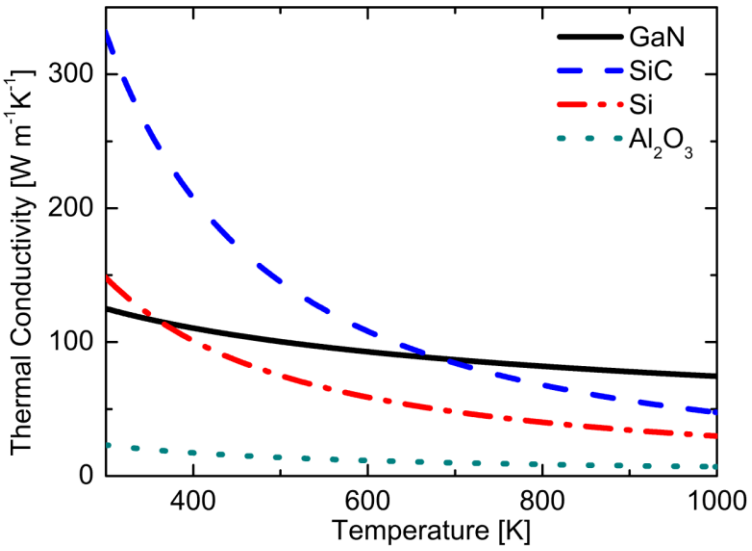

Figure 2.7: Model of thermal conductivity – temperature characteristics of various substrates (GaN, Si, SiC, Al_2O_3) using model of Equation (2.3) and thermal conductivities at 300 K and fitting parameters from Table 2.1.

2.1.3. Polarisation

The spontaneous and piezoelectric polarisations are a primary feature of AlGaN/GaN HEMTs that is enhanced by its Wurtzite structure. This is a vital characteristic necessary for providing high electron mobility and allowing high power capabilities when forming the AlGaN/GaN heterostructure. The lattice (a, a_0, c_0), piezoelectric (ε_{13}, ε_{33}) and elastic parameters (C_{13}, C_{33}) for GaN and AlN, shown in Table 2.2, are used in the calculation of both spontaneous and piezoelectric polarisations that are later discussed.

Table 2.2: Structural parameters for AlN and GaN

Material	a	a_0	c_0	ε_{13}	ε_{33}	C_{13}	C_{33}
GaN	3.197	5.210	5.185	-0.37	0.67	68	354
AlN	3.108	4.983	4.982	-0.62	1.50	94	377

2.1.3.1. Spontaneous Polarisation

The lack of inversion symmetry in the Wurtzite structure along its pyroelectric axis (c-axis) and the difference in electronegativity of Ga (1.81) and N (3.04) are the origins of spontaneous polarisation (P_{SP}). Spontaneous polarisation is induced by opposite sheet charges that occur at the faces of the Wurtzite crystal; positive sheet charge at one face and negative sheet charge at the other relative to the direction of the crystal, hence the use of [0001] crystal direction.

This opposite sheet charge is a result of a difference in electronegativity (the tendency for an atom to attract electrons) in the Ga-atoms and N-atoms that causes the Ga-N bond to exhibit mixed ionic-covalent bonds. Hence, the GaN compound is subjected to an electric dipole moment, a measure of polarity in a compound. As the arrangement of bonds in a GaN Wurtzite crystal is not perfectly symmetrical, the ideal unit cell height (c_0) and the lattice constant (a), are not equal. Therefore, there are opposite charges at the Ga-face of the crystal compared with the N-face.

For spontaneous polarisation to occur, there needs to be a difference in the ideal c_0 to a ratio of 1.633. Given the c_0/a ratio of AlN (1.6030) and GaN (1.6218) provided in Table 2.3 [77], it is clear that the ratio is not ideal. Greater difference in c_0/a occurs for AlN than GaN and, therefore, greater spontaneous polarisation occurs in AlN than GaN.

Table 2.3: Spontaneous polarisation parameters for AlN and GaN

Parameter	AlN	GaN
c_0/a	1.6030	1.6218
P_{SP} [C/m^2]	-0.090	-0.034

For different materials, the spontaneous polarisation can be seen in Figure 2.8. This shows the linear Vegard-like interpolation and the second order approximation of spontaneous polarisation in disordered ternary nitride alloys. This approximation is calculated using the parabolic model and bowing parameters [78]. It can be seen that the higher the lattice mismatch constants between each ternary, the higher the spontaneous polarisation.

$$p(A_xB_{1-x}N) = xp(AN) + (1-x)p(BN) + b_{ABN}x(1-x) \qquad (2.4)$$

where p is the arbitrary band-gap energy parameter, b is the bowing parameter (AlGaN = -0.8 eV, AlInN = -3.4 eV, and InGaN = -1.4 eV.

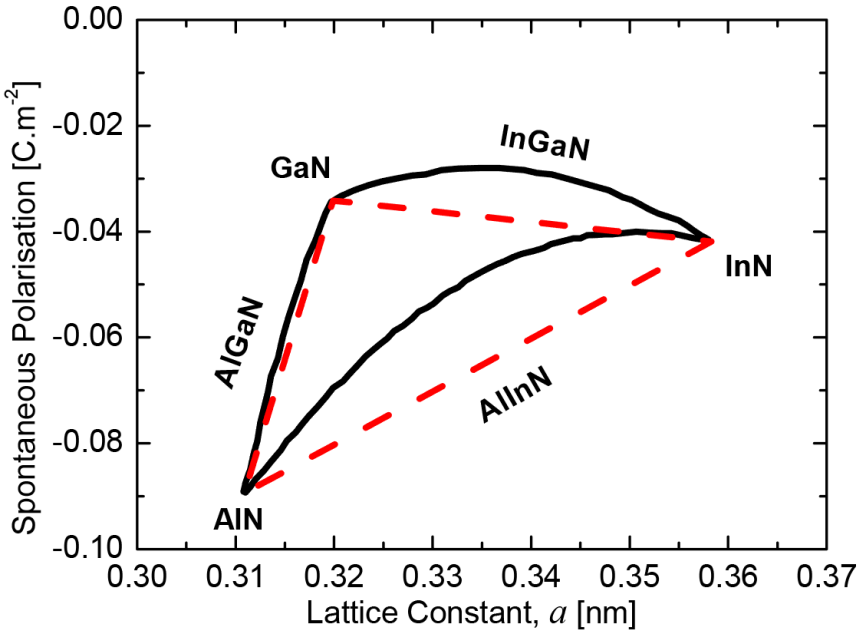

Figure 2.8: Spontaneous polarisation with respect to lattice constant of multiple compounds. The dashed red lines show linear Vegard-like interpolation, solid black lines show the approximation to second order in disordered ternary nitride alloys.

2.1.3.2. Piezoelectric Polarisation

Piezoelectric polarisation (P_{PE}) is induced when a material is subjected to mechanical stress. Mechanical stress originates from the elastic behaviour of the material governed by its elastic stiffness constant, a measure of how "hard" the material is. As a result, a charge develops in the crystal structure of a material when piezoelectric polarisation is induced. The piezoelectric polarisation is positive for when the AlGaN layer is compressively strained and negative for tensile strain.

The piezoelectric polarisation is calculated by:

$$P_{PE} = 2 \cdot \frac{a - a_0}{a_0}\left(\varepsilon_{13} - \varepsilon_{33} \cdot \frac{C_{13}}{C_{33}}\right) \qquad (2.5)$$

where ε_{13} and ε_{33} are the piezoelectric coefficients, and C_{13} and C_{33} are the elastic constants.

Polarisation effects that stem from a strained material. Electrical polarisation effects in a material is given by the summation or difference between spontaneous and piezoelectric polarisation:

$$P = P_{SP} \pm P_{PE} \quad (2.6)$$

2.2. AlGaN/GaN-Based Device Structure

This section provides fundamental information on the structure, operation and growth of AlGaN/GaN-based devices. To begin, how a high density 2DEG is formed through the AlGaN/GaN heterostructure is explained. From then, the primary device used throughout this Thesis, an AlGaN/GaN HEMT, is described in terms of its structure, operation and growth techniques. The benefits of various substrates that these devices are grown on is compared. Ohmic and Schottky contacts used for control over the operation of AlGaN/GaN HEMTs are then described. The state-of-the-art AlGaN/GaN HEMTs that are produced by various international companies are shown. Lastly, the advantages that AlGaN/GaN HEMTs have over other materials and their disadvantages, in terms of degradation mechanisms that impact device reliability, are discussed.

2.2.1. 2-Dimentional Electron Gas (2DEG) Formation

The formation of a 2DEG channel is a vital property of AlGaN/GaN-based devices. Through inducing strain, by the growth of a heterojunction, piezoelectric polarisation within the strained material is induced. This piezoelectric polarisation greatly contributes towards the formation of a high density 2DEG channel, to be described in the following sections.

2.2.1.1. Strain

The interface between two semiconductor layers of different lattice constants, and therefore different bandgaps, is known as a heterojunction, e.g. AlGaN/GaN. As there is a mismatch in lattice constants between AlGaN and GaN, simply growing a thin AlGaN layer on top of GaN will cause mechanical strain within the AlGaN layer, as illustrated in Figure 2.9. Mechanical stress originates from the elastic behaviour of the material governed by its elastic stiffness constant, a measure of how "hard" the material is. The AlGaN layer experiences strain in both x and y direction (biaxial strain) due to deformation of the material to align with GaN. The tensile strain (ε_s) in AlGaN increases its lattice constant and aligns its atoms with those of GaN to create a heterojunction. The lattice mismatch and the amount of strain applied to the AlGaN layer can be calculated by [79], [80]:

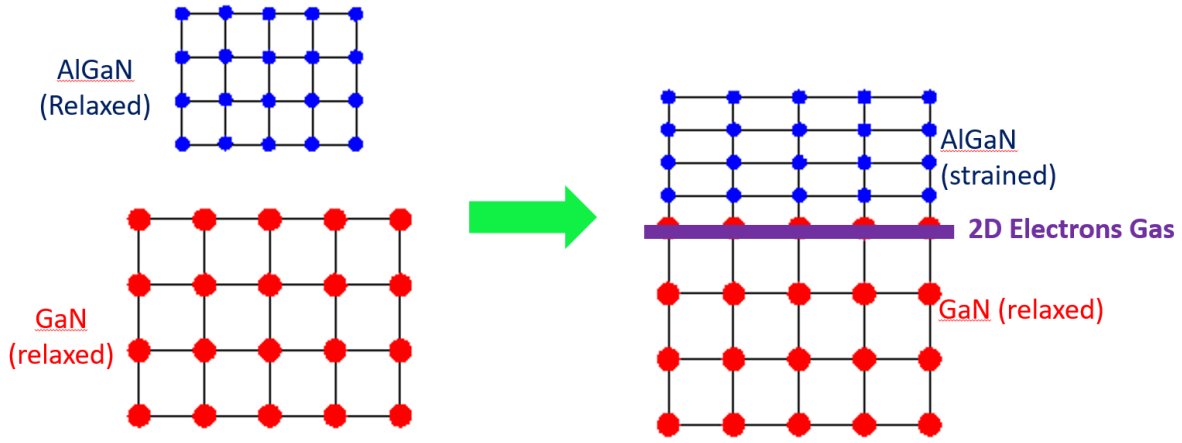

Figure 2.9: Illustration of how AlGaN is strained upon growth on GaN to form 2DEG.

$$\Delta \equiv \frac{|a_{AlGaN} - a_{GaN}|}{a_{AlGaN}} \tag{2.7}$$

$$\varepsilon_s = \Delta \cdot (1 - r) \tag{2.8}$$

where r is the amount of strain relaxation.

2.2.1.2. Polarisation

Piezoelectric polarisation is induced as a result of tensile strain in the thin AlGaN barrier layer [81]. The P_{PE} and P_{SP} in a typical AlGaN/GaN HEMT are illustrated in Figure 2.10. P_{PE} is negative, same as the P_{SP}, for tensile strain when the AlGaN layer is grown on top of GaN. P_{SP} is inherent in both AlGaN and GaN. The P_{PE} is, however, induced in the strained AlGaN barrier

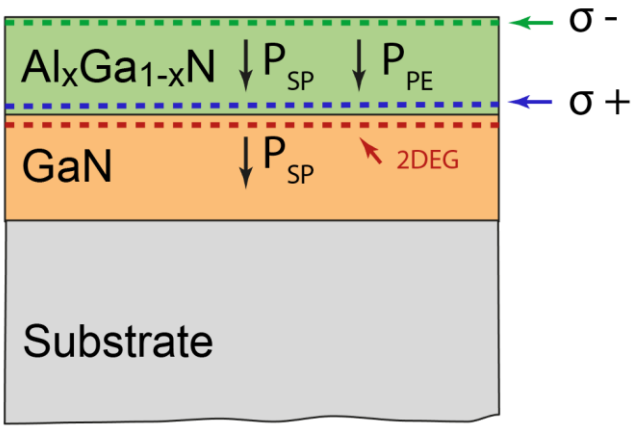

Figure 2.10: Spontaneous and piezoelectric polarisation as well as charge that produces a 2DEG in a typical AlGaN/GaN HEMT.

layer, but not in the relaxed GaN buffer layer. This produces negative charge at the top of the AlGaN layer and positive charge at the bottom. To note, P_{PE} can be positive for when the AlGaN layer is compressively strained. This strain forms defects in AlGaN, the effects of which are discussed in Section 3.2.

2.2.1.3. 2-Dimensional Electron Gas (2DEG)

The discontinuity of the polarisation (P_{PE} and P_{SP}) at the interface of AlGaN/GaN is the origin of quantum well creation, also known as 2DEG formation. The importance of P_{PE} and P_{SP} on energy band in AlGaN/GaN HEMTs is shown in Figure 2.11, illustrating the band bending influence that each polarisation has on the quantum well formation.

For up to 35 % Al concentration, the piezoelectric polarisation has the greatest influence on the band bending and, therefore, 2DEG density.

The energy band diagram of the heterostructure of a basic AlGaN/GaN HEMT is given in Figure 2.12. There is a large conduction band offset (ΔE_C) of 0.68 eV for $Al_{0.27}Ga_{0.73}N$ and GaN that is created due to the difference in affinity between $Al_{0.27}Ga_{0.73}N$ and GaN of 3.14 eV and 3.5 eV, respectively [83]. The 2DEG density (n_s) can be increased with (i) greater

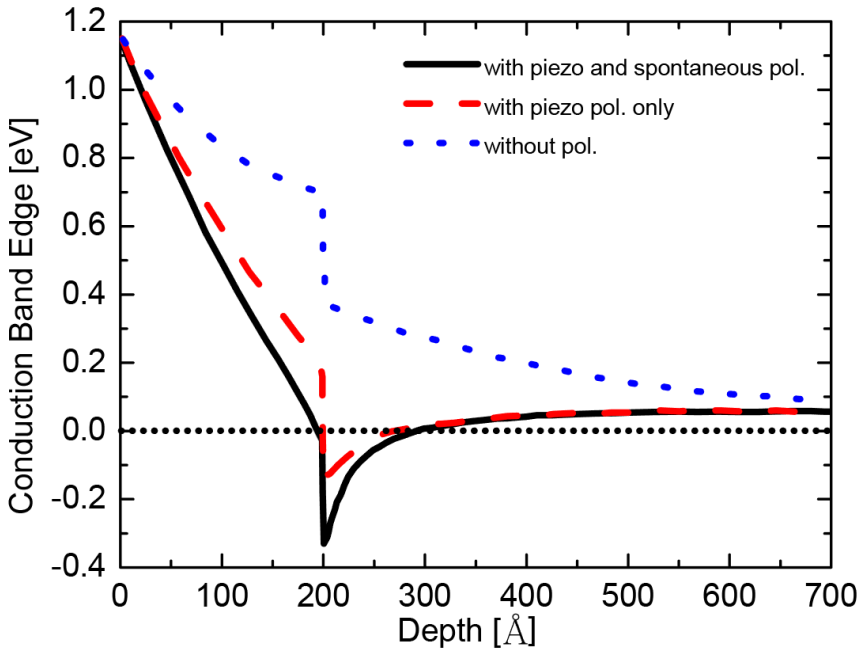

Figure 2.11: AlGaN/GaN energy band diagram demonstrating effects of P_{SP} and P_{PE} on conduction energy band [82].

concentration of Al in AlGaN, and (ii) increased AlGaN barrier thickness, shown in Figure 2.13 given by the Schrodinger-Poisson 1D model [84]. However, increasing these parameters beyond its optimal value will cause the strain in the AlGaN barrier to relax. Hence, typically used parameters are around 30 to 40 % Al concentration and 20 nm barrier thickness. Although n_s is shown to be greater with increased Al concentration beyond 40 %, it is not used in practicality as access resistance increases as a result. We propose an optimisation of Ohmic contacts in order to reduce the access resistance, which may allow for greater Al concentrations, and/or an AlN exclusion layer to be feasible.

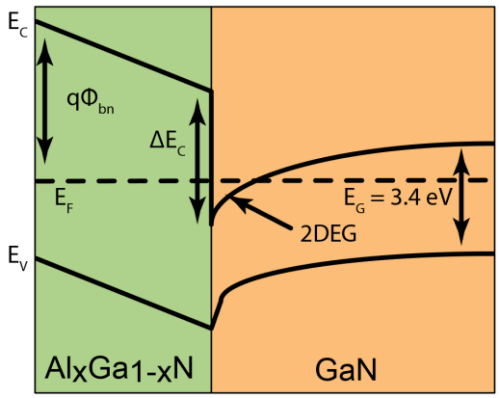

Figure 2.12: Band structure of $Al_xGa_{1-x}N$/GaN heterostructure showing 2DEG formation at the $Al_xGa_{1-x}N$/GaN heterojunction as a result of quantum well formation.

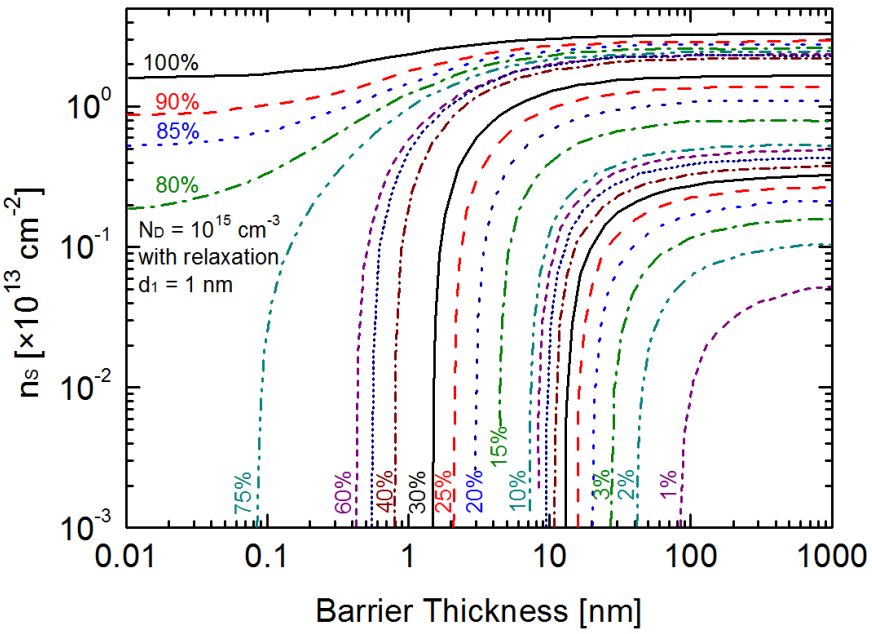

Figure 2.13: 2DEG sheet density relationship with AlGaN mole fraction.

2.2.2. High Electron Mobility Transistor (HEMT)

2.2.2.1. Device Structure

A practical example of the structure of an AlGaN/GaN HEMT is described in this section. In this device, a thick layer of GaN (around 2 to 3 µm to ensure strain relaxation in buffer) is grown onto a substrate (i.e. Si, SiC, and Al_2O_3) by either (i) molecular beam epitaxy (MBE) or (ii) metal organic chemical vapor deposition (MOCVD). Using the same epitaxy material growth technique as chosen for the buffer, a thin layer of $Al_xGa_{1-x}N$ (around 20 nm) is grown on top of the GaN layer. Typically, the concentration percentage (x) of aluminium (Al) in $Al_xGa_{1-x}N$ is up to 0.40. Higher concentrations of Al in this basic structure will result in relaxation of the AlGaN layer, reducing the strain of the material and, therefore, the 2DEG sheet density. Additional layers have been implemented into this structure in order to enhance the performance of the device. The following states the layers' (from bottom to top) typical properties and purposes that are used in more recently developed AlGaN/GaN based HEMTs.

- **Substrate** – The AlGaN/GaN HEMT is typically grown on a non-native substrate (i.e. Si, SiC, and Al_2O_3). The selection of the substrate is governed by four factors (i) resistivity, (ii) thermal conductivity, (iii) capable wafer size, and (iv) cost.
- **Nucleation layers** – A thin set of AlN, AlGaN and/or GaN layers (10 to 20 nm each) is grown on the substrate. These layers reduce the lattice mismatch between the buffer layer and the substrate. Hence, interface roughness is reduced, which reduces the thermal resistance between the buffer and substrate, allowing greater heat dissipation from the 2DEG to the substrate. Additionally, these layers increase the vertical breakdown voltage by reducing the vertical electric field between the drain side and the substrate. The choice of nucleation layers is dependent on the epitaxial growth technique and substrate that is used.
- **Back-Barrier Layer** – A thick and low Al concentration ($x < 0.15$) $Al_xGa_{1-x}N$ layer (1 to 2 µm) can be used to reduce leakage current in the buffer layer. As a result, greater energy is required by electrons to overcome the energy back-barrier and leak into the buffer layer.
- **Buffer Layer** – A thin GaN layer (>15 nm) is used as the buffer layer when grown upon a back-barrier layer. This forms a quantum well and enhances the 2DEG confinement.

If there is no back-barrier layer then a thick buffer layer of GaN (2 to 3 µm) is employed to ensure strain relaxation.

- **Exclusion Layer –** A very thin aluminium nitride (AlN) layer (1 nm) is an option for reducing alloy scattering beneath the Ohmic contacts and improving carrier concentration in the 2DEG. However, this layer prevents optimal Ohmic contact formation, which degrades the source/drain access resistance. This degradation is discussed in Section 5.2.
- **Barrier Layer –** A thin layer of $Al_xGa_{1-x}N$ (~20 nm), where $x < 0.40$, is grown above the exclusion layer or GaN buffer layer. This is to induce piezoelectric polarisation and, therefore, 2DEG formation.
- **Cap Layer –** To prevent oxidation and defect formation at the surface of the barrier layer, the implementation of a very thin GaN layer (1 to 2 nm) is common.
- **Passivation Layer –** A thin silicon nitride (Si_3N_4) or silicon dioxide (SiO_2) layer (~200 nm) grown after device fabrication to minimise defect formation at the surface of the device.

2.2.2.2. Device Operation

The AlGaN/GaN HEMT consists of 3-terminals (source, gate, and drain) and is a modification of a metal-semiconductor field-effect transistor (MESFET). The three metal terminals are given of which the source and drain terminals are made up of Ohmic contacts and the gate terminal is made of a Schottky contact. The gate terminal is placed more towards the source side (asymmetrical gate) to reduce the high electric fields between the drain and the gate that occur under high drain voltages. This increases the HEMTs lateral breakdown voltage and reduces self-heating within the device.

An AlGaN/GaN HEMT cross-section with an illustration of its operation under ON-state and OFF-state conditions is shown in Figure 2.14(a) and (b), respectively. The devices used throughout this Thesis are normally-ON, the 2DEG is formed without applying a voltage on the gate terminal (V_{GS}). The switching from ON-state ($V_{GS} > V_{TH}$) to OFF-state ($V_{GS} < V_{TH}$) is controlled by applying V_{GS}, which controls the 2DEG sheet density in the channel. In OFF-state conditions, $V_{GS} < V_{TH}$, the 2DEG will deplete, thereby preventing current flow through the device.

The applied V_{GS} controls the 2DEG sheet density in the channel. The drain-to-source voltage (V_{DS}), however, governs the conductance in the channel. Figure 2.15 shows the vertical conduction band edge profile, at the middle gate of an AlGaN/GaN HEMT, in (a) ON-state and (b) OFF-state. The relative distance between the conductuion band edge and the Fermi level (E_F) is influenced by V_{GS}. This lowers the conduction band energy, in respect to E_F, when positive, providing a larger 2DEG. Closing the channel involves raising the conduction band energy above E_F, by applying $V_{GS} < V_{TH}$.

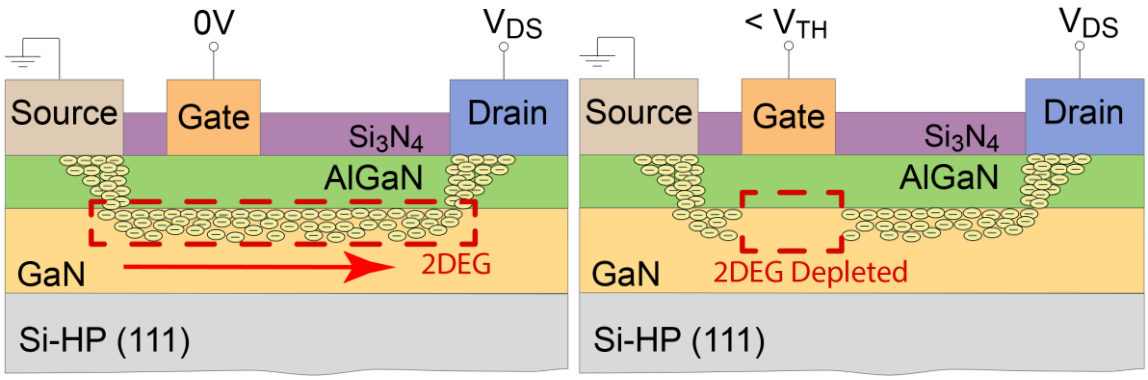

Figure 2.14: Illustration of GaN-based HEMT with AlGaN/GaN heterostructure and Si_3N_4 passivation when the device is in (a) ON-state, and (b) OFF-state.

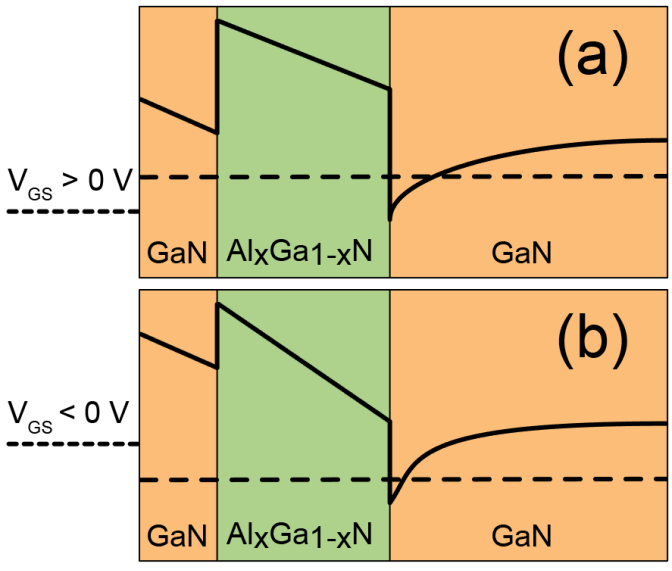

Figure 2.15: Influence of the gate voltage on the energy band structure: a) $V_{GS} > V_{TH}$ and b) $V_{GS} < V_{TH}$.

2.2.2.3. Semiconductor Growth Technique

Two main growth techniques, molecular beam epitaxy (MBE) and metal-organic chemical vapour deposition (MOCVD), are used to grow AlGaN/GaN heterostructures on a range of substrates. Generally, MBE is used for research purposes and MOCVD is used for mass production.

A. Molecular Beam Epitaxy (MBE)

MBE grows the GaN material using elemental sources and heating a substrate in an ultra-high vacuum environment, 10^{-5}~10^{-11} Torr pressure that conserves the purity of the material by vacuuming out contaminant molecules that may be trapped inside the material causing defects. The instruments used to perform this are illustrated in Figure 2.16. It is particularly used for its ability to produce an atomically sharp interface [85]. To begin to grow the GaN crystals using this technique, the substrate is heated and then GaN molecules are fired at the heated substrate from separate beams as relatively precise beams known as effusion cells. Control over these effusion cells stems from shutters that cover the beams when an unequal amount of two molecules or more are required, e.g. $Al_{0.3}GaN_{0.7}$; here, molecules that hit the substrate then condense. The condensed molecules impinge on the surface of the substrate, at a flux rate determined by the effusion cells, which then migrate towards other condensed molecules forming islands. This eventually forms an ultra-thin crystalline layer of GaN, as shown in Figure 2.17. Typically the Frank-van der Merwe (layer-by-layer) growth mode is adopted for buffer layer growth on HEMT devices when using MBE.

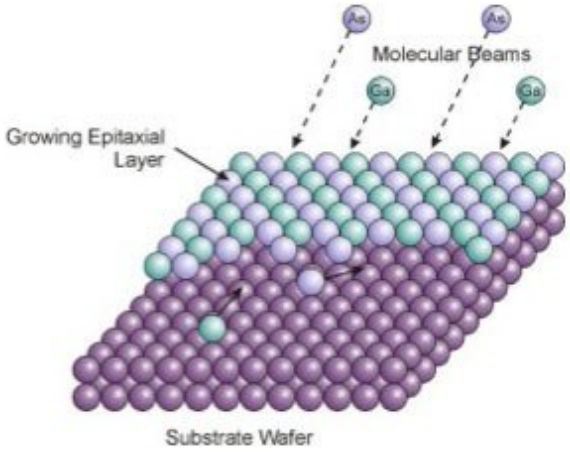

Figure 2.16: Molecular Beam Epitaxy layer-by-layer growth on substrate process.

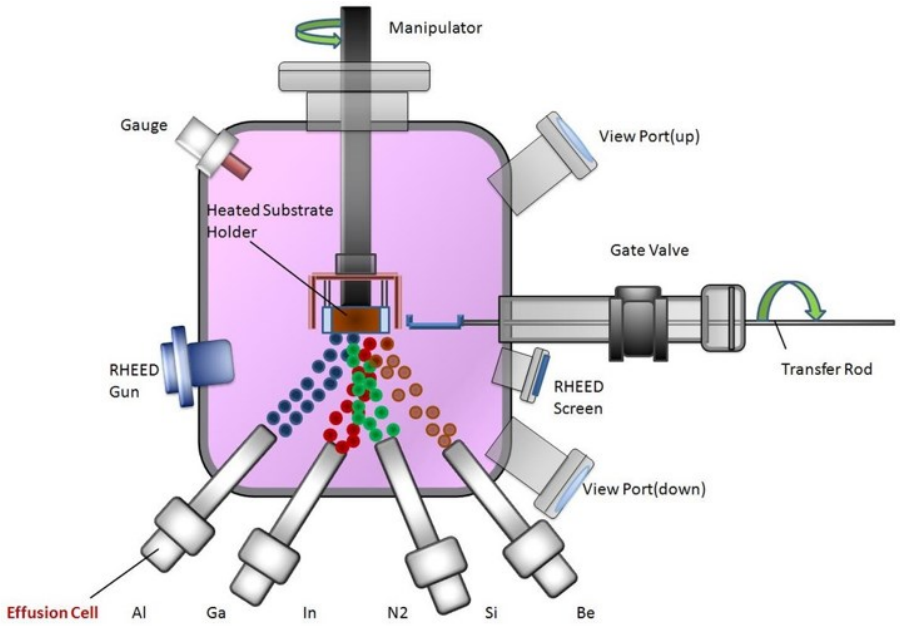

Figure 2.17: Molecular Beam Epitaxy (MBE) instruments used for growing AlGaN/GaN-based devices.

There are several processes that the GaN molecules may adopt during this growth process. The molecules may become adsorbed onto the substrate or GaN surface through weak, physical bonds via Van Der Waals forces (physisorbed), molecules become chemically bonded to the surface through an electron exchange process (chemisorbed), or molecules will diffuse about the surface from energy provided by the substrate which provides growth [86]. Continuing the process, a second crystalline layer is built upon this and the process repeats until eventually a thick GaN layer is formed. Unfortunately, temperatures lower as the GaN becomes thicker as the substrate is the source of heat. This results in interface roughness at the final layers of GaN as the source temperature (speed of molecular arrival and flux rate) does not provide enough energy for the GaN molecules to migrate towards the GaN islands hence the necessity for such substrate that requires high temperatures to provide sufficient flux.

B. Metal-Organic Chemical Vapour Deposition (MOCVD)

MOCVD, or Metal-organic vapour-phase epitaxy (MOVPE) is the growth of thin layers of compound semiconducting materials via co-pyrolysis of organometallic compound and hydride combinations. This is the primary technique of growth for virtually all III-N compounds using chemical reaction, as opposed to physical deposition that MBE harnesses. In comparison,

MOCVD is a much faster process, films grown at ~1 µm min^{-1}, when compared to MBE and a much cheaper alternative [87]. This is the thermochemical decomposition of materials by reaction with vapour-phase precursors, e.g. the gaseous state of ammonia (NH_3) used to chemically react with GaN, when under high temperatures, between 1000 to 1100 ºC for GaN and above 1100 ºC for AlGaN , due to the high chemical bond strength of GaN and typically under low pressure, between 15 to 750 Torr. Growth of GaN on substrate results in Ga-face polarity unlike the N-face polarity of MBE.

The system used to achieve growth of semiconductor materials using MOCVD is illustrated in Figure 2.18. This process involves forming oriented β-Ga_2O_3 nanoclusters at the surface of the substrate after exposure to Ga. From then, strong N_2 reactivity from a nitridation process under high plasma power and substrate temperature for a long time, whereby GaN nucleation occurs. With greater nucleation, coalescence of GaN occurs due to the decreasing distance between GaN nucleators. This process iterates to produce columnar growth of GaN which then leads to lateral growth to complete the MOCVD process. This process is illustrated in Figure 2.19.

Although, several issues occur with this method of growth. Due to the high temperatures required for deposition there is reduced control on the growth of GaN, one main concern is surface roughness. Although, the implementation of an AlN buffer layer deposited on the sapphire substrate improves the electrical and crystal qualities of grown GaN. High volatility of N results in a large concentration of NH_3 present in the gas.

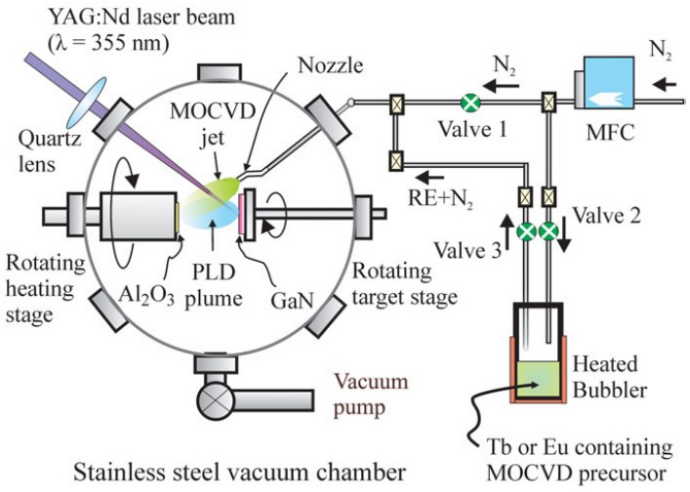

Figure 2.18: Schematic diagram of the MOCVD deposition system [26].

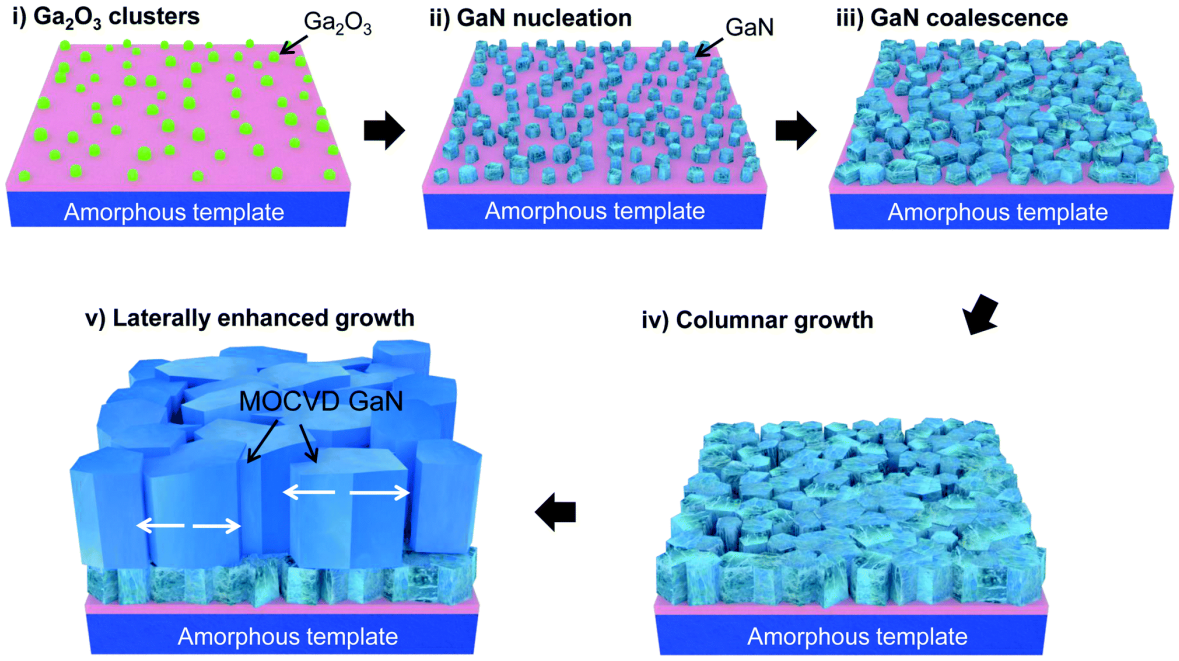

Figure 2.19: MOCVD illustration showing how reactants are deposited onto the substrate to form layers of semiconductor compounds [88].

2.2.3. Substrate Choice

An appropriate choice of substrate can provide significant advantages to the performance of the device that is grown on top of it. Some factors that determine the viability of the chosen substrate are: (i) the resistivity (ii) thermal conductivity; (iii) lattice mismatch at the buffer/substrate interface; (iv) density of dislocations; (v) cost per unit area; and (vi) size of the wafer. In addition, the lattice mismatch at the buffer/substrate interface, given by Equation (2.9), needs to be carefully considered when designing the device architecture.

$$Lattice\ Mismatch\ (\%) = 100 \times \left(\frac{a_{bf} - a_{sub}}{a_{bf}}\right) \tag{2.9}$$

where a_{bf} and a_{sub} is the in-plane lattice constant of the buffer and substrate layer, respectively.

Lattice mismatch is a source of buffer/substrate interface roughness, dislocations in the buffer, and defect generation, reduction of AlGaN/GaN HEMT RF performance. It is also responsible for thermal resistance increase at this interface, reducing the dispersion of the heat out of the device and into the substrate.

A summary of the material properties that are valuable for viability as a substrate in AlGaN/GaN based devices is given in Table 2.4.

Table 2.4: A comparison of the relevant material properties of substrates typically used in AlGaN/GaN based devices.

Property	GaN	Si(100)	Si(111)	4H-SiC	6H-SiC	Al_2O_3
Lattice Constant, *a* (Å)	**3.189**	5.431	3.366	3.073	3.073	4.758
Lattice Mismatch, (%)	**0**	41.3	5.3	3.4	3.4	34
Thermal Conductivity, λ (W $cm^{-1}.K^{-1}$)	**1.3**	1.5	2.5	3.7	4.9	0.5

2.2.3.1. Silicon (Si)

Si is by far the most widespread semiconductor material used in the semiconductor industry. Therefore, it has very high commercial availability as a substrate for various wafer diameters (from 2 to 12-inch) and has low cost to manufacture, due to the well-established fabrication techniques. The thermal conductivity of Si (100) is not exceptionally high, with a value of 1.5 W $cm^{-1}K^{-1}$ [89]. Also, the lattice constant of Si (100) is high (5.431 Å) in comparison to GaN (3.189 Å) [90], [91]. Hence, the use of Si (111) is a preferred option due to its lower lattice constant (3.366 Å), higher thermal conductivity (2.5 W $cm^{-1}K^{-1}$) and higher resistivity (6.0 Ω.cm) [92]–[94]. The vast majority of silicon substrates, Si (111) in particular, are high purity (1 part dopant per million).

2.2.3.2. Silicon Carbide (SiC)

4H-SiC and 6H-SiC, although not as abundant as Si, is widely available in the semiconductor industry, but for relatively small wafers (up to 4-inch). These substrates are expensive to manufacture in comparison to other materials. Regardless, SiC is the most commonly used substrate for commercialised AlGaN/GaN HEMTs. This is due to their high thermal conductivity, ranging from 3.7 to 4.9 W $cm^{-1}K^{-1}$, and their low lattice mismatch with GaN (<3.4%) [93], [95]. This is particularly useful for AlGaN/GaN HEMTs in high-power applications as these substrates dissipate the heat more effectively than other conventinal substrates.

2.2.3.3. Sapphire (Al_2O_3)

Al_2O_3 is a readily available substrate with wafers of up to 8-inches in diameter and is also cost effective. The thermal conductivity, however, is very low at 0.5 W $cm^{-1}K^{-1}$ [96]. In addition, with a lattice constant of 4.758 Å, the lattice mismatch is higher than other substrates (34%) [97]. Here, a large defect density will be present from the large lattice mismatch and, under normal operation, AlGaN/GaN HEMTs would experience higher temperatures compared to other materials. For this reason, this material is a good option for optical applications.

2.2.3.4. Gallium Nitride (GaN)

GaN substrates are not abundantly available but can reach diameters up to 6 inches. AlGaN/GaN HEMT grown on a GaN substrate is lattice mismatch free (0 %); this is known as homoepitaxial growth. As a result, there is greater power performance at higher frequency. For AlGaN/GaN-on-GaN device applications, particularly blue LEDs, there is a much greater device lifetime when comparing with other substrates. Although the thermal conductivity of GaN (1.3 W $cm^{-1}K^{-1}$) is less than SiC, the interface thermal resistance does not occur [98]. This is significantly beneficial for heat dissipation via the substrate. Therefore, GaN substrates are considered as a viable option for high-frequency and RF applications but better alternatives are available for high-power operation (SiC).

2.2.4. AlGaN/GaN HEMTs State of the Art

As described in Chapter 1, AlGaN/GaN HEMTs have considerably high power (up to 40 W mm^{-1}) and high frequency (up to 100 GHz) properties. A visual representation of the state-of-the-art AlGaN/GaN HEMTs from numerous manufacturers and universities is provided in Figure 2.21 by comparing the maximum output power with the maximum operating frequency [99]–[116]. It can be seen that AlGaN/GaN HEMTs grown on SiC substrates provide higher maximum power than Si. This is due to the high thermal conductivity of SiC in comparison to other substrates. Although, the growth of GaN on SiC results in interface roughness between GaN/SiC. This interface roughness causes the GaN/SiC interface to act as a thermal resistor which keeps heat within the device. The interface roughness issue also occurs with GaN/Si. Regardless, AlGaN/GaN on SiC is clearly a better but ~10 times expensive option than using Si substrates, provided by the Institute of Electronics, Microelectronics and Nanotechnology (IEMN) in the University of Lille. For the purposes of this research, devices on Si substrate

will be used as they are less expensive and (ii) it allows for the co-integration with existing and previous Si(111) technologies.

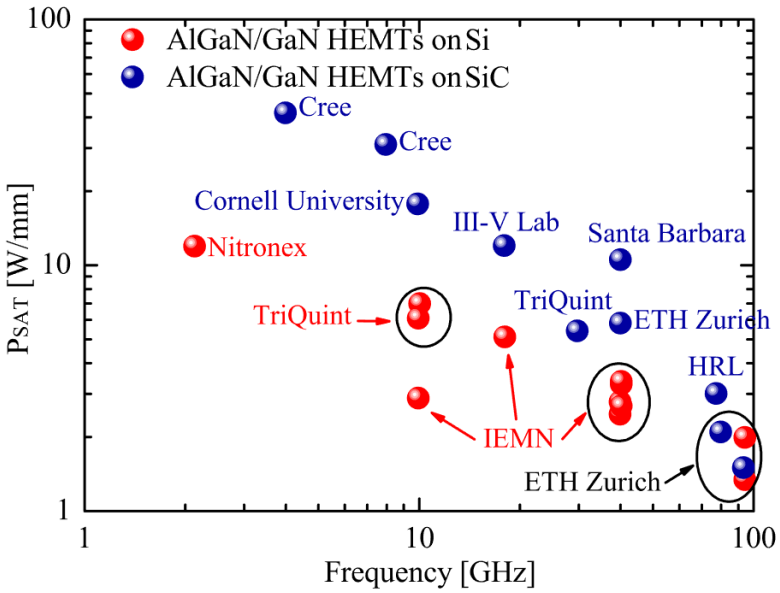

Figure 2.20: Benchmarking of state-of-the-art AlGaN/GaN HEMTs on Si and SiC, using power saturation vs. frequency, showing the superiority of AlGaN/GaN HEMTs on SiC.

2.2.5. Metallisation of Device Contacts

Optimal metallisation of contacts is a necessity to contributing towards the high performance characteristics and reliability of any semiconductor device. Their contribution towards AlGaN/GaN HEMTs in particular is even greater than other devices due to the high power that these devices operate.

Metal contacts are used to provide charge carrier transport mechanisms to/from the semiconductor. The mechanisms of charge carrier transport throughout metal/semiconductor junction are:

1. Thermionic emission (TE) – Charge carriers move over the top of the contact barrier and into/out of the metal contact.
2. Field emission (FE) – Charge carriers tunnel through the contact barrier and into/out of the metal.
3. Thermionic field emission (TFE) – Charge carriers become ‘hot’ and tunnel through the top of the contact barrier into/out of the terminal.
4. Emission by ‘hopping’ of charge carriers, particularly through deep traps.

These mechanisms are illustrated in Figure 2.21, whereby the dominant mechanism of transport in AlGaN/GaN HEMTs is FE for Ohmic contacts and both TE and TFE for Schottky contacts [117], [118].

There are two types of metal contacts present in AlGaN/GaN HEMTs that have different metallisations and transport mechanisms: (i) Ohmic contact that is used as the source/drain electrode, and (ii) Schottky contact used as the gate electrode.

2.2.5.1. Ohmic Contact

The Ohmic contact (source/drain terminals) controls the flow of current through an AlGaN/GaN HEMT. Ohmic contacts of low-resistance, high thermal stability and smooth

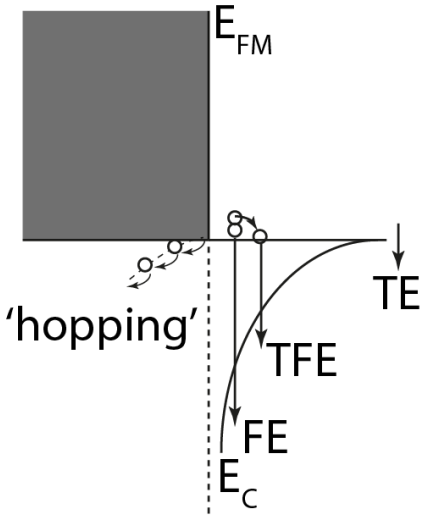

Figure 2.21: Illustration of charge carrier transport mechanisms for (i) TE, (ii) FE, (iii) TFE, and (iv) emission by 'hopping'; where E_{FM} is the metal Fermi level.

morphology are required for optimal performance of AlGaN/GaN HEMTs. These characteristics will provide: (i) low device ON-state resistance, (ii) low power dissipation in the Ohmic contacts, (iii) maximum drain current, and (iv) high extrinsic transconductance (G_m), that enhances current gain cut-off frequency (f_T), and maximum oscillating frequency (f_{MAX}).

Ohmic contacts are formed through rapid thermal annealing (RTA) at high-temperature and tend to have several metal stacks that each play their own role in optimising the Ohmic behaviour of the contacts. Typical metal schemes used for the Ohmic contact stacks, from bottom-to-top, and their roles are given:

- **Titanium (Ti)** – Ti bonds with the nitrogen (N) in the AlGaN barrier layer to form a

TiN alloy when RTA is applied to the contacts. High temperature allows the bonds to form, the short time of annealing prevents the reaction of Ti with the GaN buffer layer to provide a smooth metal/semiconductor interface. The bonds appear at threading dislocations at the metal/semiconductor interface either through rapid diffusion of atoms or from nucleation at low energy sites of TiN. This alloy has a lower work function, aiding in contact formation and facilitating charge carrier tunneling. N vacancies are also created as a result of the alloy formation. This causes the AlGaN barrier beneath the contact to become highly n-doped. As there is a thin potential barrier which separates the 2DEG and contact, electrons are able to easily tunnel to/from the 2DEG to the contact.

- **Aluminium (Al)** – Al bonds with Ti to form an Al_3Ti alloy. This alloy minimises oxidation of the Ti layer and, hence, contributes to the conductivity of the contact. Also, Al bonds with the N in the AlGaN barrier layer to form an AlN alloy. This results in N vacancies which yields a heavily doped interface beneath the contact. Electrons can easily tunnel to/from the 2DEG as a result.
- **Nickel (Ni), Molybdenum (Mo), Platinum (Pt), or Titanium (Ti) –** The electron affinity of this layer is to be lower than that of the semiconductor layer in order to provide low sheet resistance at the metal/AlGaN interface. This layer has a low work function to achieve this. Additionally, this layer minimises the out-diffusion of Al, the in-diffusion of gold (Au), and the intermixing of the Al and Au layers to form Al_2Au bonds. Al_2Au is a highly resistive alloy that is detrimental to the operation of the Ohmic contact.
- **Gold (Au) –** Au is a highly conductive material which is why it is used in the metallisation of the Ohmic contact. In addition to this, Au minimises the oxidation of the Ti and Al layers of the contact when annealed at high temperatures which enhances the contact conductivity further.

When Ohmic contacts are formed with RTA at high temperatures, voids are produced beneath the TiN alloy. The voids are enhanced by higher annealing temperatures and contribute to the contact resistance, reducing the current flow through the HEMT. Voids generation beneath the Ohmic contacts are a major reliability issue. Voids increase the contact resistance and as a result they inherently affect the high frequency operation of the device [119]. This issue is addressed

in Section 5.2. As a result of the bonding of metal stacks, high n-doping concentration is in the semiconductor, narrowing the depletion layer. This allows charge carriers to tunnel through the barrier layer from the 2DEG to the metal contact, or vice versa, but does not lower the conduction band to allow for thermionic emission. Hence, field emission is the primary transport mechanism in Ohmic contacts.

2.2.5.2. Schottky Contact

Schottky contacts are used as the gate terminal for AlGaN/GaN based devices. This contact controls the 2DEG density within AlGaN/GaN HEMTs. Upon applying a bias to the gate, the 2DEG carrier density is modulated at the AlGaN/GaN interface. The defining feature that allows this to occur is known as the Schottky barrier height (ϕ_{bn}). In theory the Schottky barrier height is calculated by the following equation:

$$\phi_{bn} = WF - x_{AlGaN} \tag{2.10}$$

where WF is the metal work function, and x_{AlGaN} is the electron affinity of AlGaN. However, this simple relationship between ϕ_{bn} and WF has been proven to be incorrect for GaN-based devices; see Section 5.3.

The materials used for the Schottky contacts tend to have high work functions in order to prevent leakage current through the gate electrode to/from the 2DEG and barrier layer defects. Notable materials with high work functions that are noted for use in Schottky contacts are (i) Ni, (ii) Au, and Pt. These materials have a work function of 5.15 eV, 5.10 eV, and 5.65 eV, respectively. Here, Pt has the highest work function. Although, it is not used as often in AlGaN/GaN based devices due to adhesion problems when deposited on GaN. A solution would be to deposit gold between these layers. Although, research has shown that high gate leakage current occurs with this metallisation [97]. Therefore, Ni would be the most suitable solution to deposit on the AlGaN barrier layer. To enhance this contact, a layer of Au is deposited on Ni in order to prevent oxidation of Ni. Hence, the most suitable and widely used metallisation for the Schottky contact is Ni/Au.

The high work function of the deposited Schottky contact metallisation prevents field emission from occurring as only the barrier height is modulated. Thermionic emission is therefore the primary transport mechanism in Schottky contacts.

2.2.6. Advantages & Disadvantages of AlGaN/GaN HEMTs

The mechanisms of a typically used AlGaN/GaN device, known as the AlGaN/GaN HEMT, has been covered. The (i) wide-bandgap (E_g) of 3.4 eV; (ii) high breakdown electric field (E_{BD}) of 3.5 MV cm^{-1}; (iii) high electron mobility (μ) of 900 cm^2 V^{-1}s^{-1}; (iv) high electron saturation velocity (v_{sat}) of 15×10^6 cm s^{-1}; and (v) low dielectric constant (ε_r) of 8.9 of III-N materials provide distinctive advantages over the conventionally used Si and even other competing semiconductor materials. These properties lead to superior high-power and high-frequency device performance [15], [120]. In order to show the advantages of AlGaN/GaN HEMTs, first the advantages of bulk GaN against other competing semiconductor materials is given. Then, the advantages and disadvantages of AlGaN/GaN HEMTs against bulk GaN is provided.

The benefit of the wide-bandgap in III-N materials is that it allows for high electric breakdown field which contributes towards high-voltage (600 V) and high-temperature (600 ^{o}C) applications. Also, large current density can be achieved, as a result of the high 2DEG electron mobility. The high saturation velocity available in III-N materials is another attribute required for high-frequency applications. Due to the superiority of the physical properties of GaN over its competitors, its ability to integrate itself into applications for high-temperature and high-frequency switching has proven valuable for the wide-bandgap semiconductor market [30], [121].

2.2.6.1. Comparison of Material Properties

One of the primary reasons for GaN to be such a valuable pioneer in the semiconductor market is its ability to form a heterojunction with other III-N materials grown on top of it; namely, AlGaN. As a result, a channel of extremely high 2DEG sheet density, $\geq 10^{13}$ cm^{-2}, is available at the AlGaN/GaN heterojunction, owing to the success of AlGaN/GaN-based devices. The performance enhancement that polarisation has in AlGaN/GaN-based devices also prevents the need to perform elemental doping to the device. There are a number of advantages to not doping the device: (i) increase in electron mobility as a result of reduced ionised impurity scattering, (ii) device reliability is not degraded further, and (iii) a costly and time consuming process is not needed.

2.2.6.2. Comparison of AlGaN/GaN against GaN Bulk Technology

A comparison is made between the AlGaN/GaN heterostructure architecture and the classical

doped GaN bulk technology to observe its advantages and disadvantages. Advantages include:

- In terms of electron mobility, the AlGaN/GaN heterostructure dominates the doped GaN bulk architecture with a significantly high value of mobility exceeding 2000 $cm^2 V^{-1}s^{-1}$ compared to the ~440 $cm^2 V^{-1}s^{-1}$ capable of the doped GaN bulk [122], [123]. Upon doping the GaN bulk, dopant atoms bombard the GaN material, which damages its crystalline structure, reducing the carrier mobility in the device.
- Another benefit of AlGaN/GaN is its high 2DEG sheet density (> 10^{13} cm^{-2}). Such density is too difficult to reach using doping implantation in bulk GaN.

Although, some disadvantages include:

- When passivating the device (e.g. Si_3N_4 on top of AlGaN) then great care is needed. Depositing the passivation layer can permanently modify strain in the AlGaN barrier layer, affecting the 2DEG density.
- The gate and source/drain contacts process technologies require particularly accurate annealing techniques. Firstly, the source/drain contacts are processed using RTA at high temperature and then the gate must be placed afterwards using low temperature in order to form a proper Schottky contact.
- Upon depositing the source/drain contacts onto the device, a reduction in strain occurs at the inner ends of the contacts that produce a significant rise in self-heating at these spatial locations; as discussed in Section 3.2.

For applications that require high power, frequency and efficiency, the advantages of AlGaN/GaN HEMTs over bulk GaN outweigh the disadvantages. The significance of these disadvantages have the potential to be reduced as development of AlGaN/GaN HEMTs progresses.

2.2.6.3. Degradation Mechanisms

The primary issue of AlGaN/GaN HEMTs that is inhibiting it from reaching mass production in the semiconductor market is their reliability. Recoverable degradation such as transient reduction in drain current (current collapse), total measured resistance between source and drain when the device is in ON-state (on-resistance), and ratio of output power and input power (efficiency) contribute towards the degradation of reliability [60]–[62]. Additionally,

unrecoverable degradation (i.e. access resistance of contacts, leakage current) also contributes towards reliability degradation. The focus of this Thesis is on identifying the kinetics of three degradation mechanisms: (i) self-heating, (ii) bulk trapping, and (iii) surface trapping. A description of each is given in the following sections.

A. Self-Heating

During normal device operation of AlGaN/GaN HEMTs, electrons gain significant energy and high velocity due to the large electric field that is induced at the drain-side gate edge. With such energy, the electron temperature is high, which causes electrons to bombard the crystal lattice. Therefore, the electrons scatter away from the 2DEG and transfer their energy to the crystal lattice, increasing the lattice temperature. Hence, the transport properties in AlGaN/GaN HEMT are degraded, reducing the device performance. Particularly in these devices, a significant amount of self-heating occurs within a very short time. As an example,

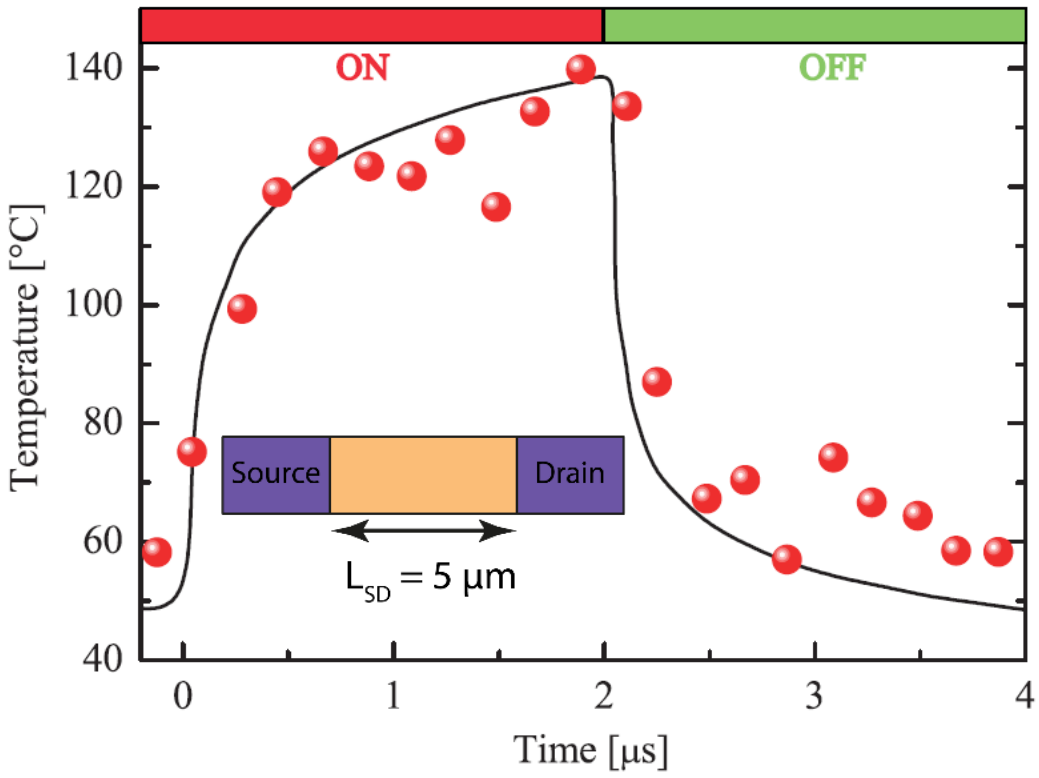

Figure 2.22: Self-heating/cooling-down characteristics for (i) experimental measurements using a W = 150 µm, L_{SD} = 5 µm AlGaN/GaN TLM, and (ii) simulation data for equivalent device [124]; V_{DS} = 20 V. Self-heating/cooling-down characteristics are shown to be near-symmetrical.

characterisation of self-heating at the centre of an AlGaN/GaN TLM with 150 µm contact width (W) and 5 µm source-to-drain distance (L_{SD}) is given via Micro-Raman (µ-Raman) in Figure 2.22. The temperature at the centre of the device heats up dramatically, reaching at least 70 % of its peak temperature within 2 µs. The cooling down process begins at 2 µs, whereby V_{DS} is set to 0 V. The heating up and cooling down processes are nearly symmetrical.

An example of the self-heating effect on the output characteristics of an AlGaN/GaN TLM is shown in Figure 2.23. The I_{DS} – V_{DS} characteristics of two AlGaN/GaN HEMTs of 2 µm and 16 µm L_{SD} are measured under DC and pulse conditions. For pulse measurements, several pulse widths were used ranging from 450 ns down to 5 ns. It can be seen that a significant enhancement in output characteristics is observed when using pulse measurements compared to DC measurement. As the pulse measurement is relatively short, little self-heating occurs when compared with DC conditions.

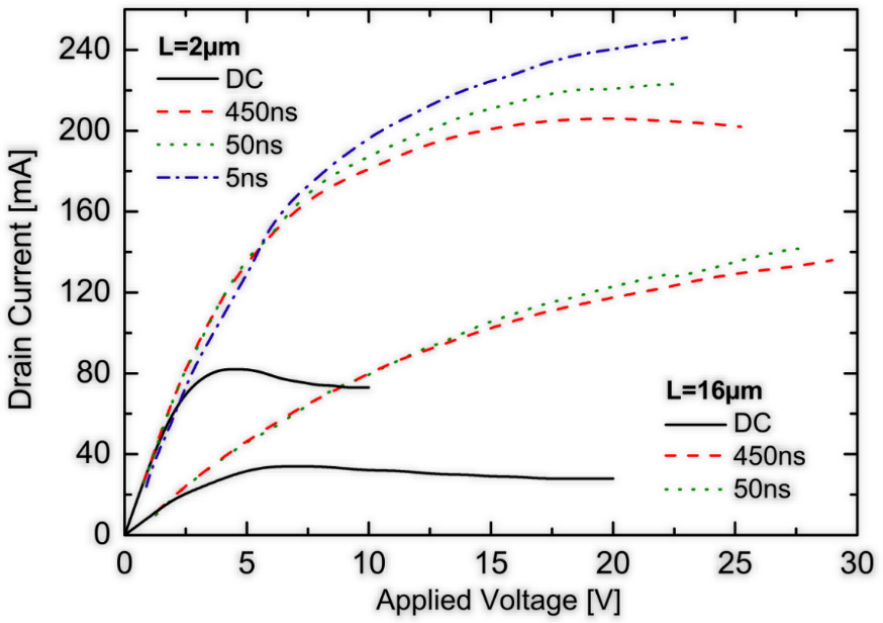

Figure 2.23: I_{DS} – V_{DS} characteristics for devices of various length measured under DC and pulse measurements with varying pulse widths.

B. Bulk Trapping

Defects form in the device (i.e. threading dislocations, dangling bonds) as a result of either material issues or imperfections in device fabrication process. As charge carriers gain sufficient energy from the applied electric field within the device, they can be trapped, as illustrated in Figure 2.24. These trapped electrons induce potential change that, in turn, reduces the 2DEG

sheet density, and therefore the source-drain current. This phenomenon is more likely to occur at the drain-gate side of the device as opposed to the source-gate side. The mechanisms of bulk trapping is more complicated than what is stated here as it is temperature dependent. We investigate this mechanism in more detail in Section 4.5.

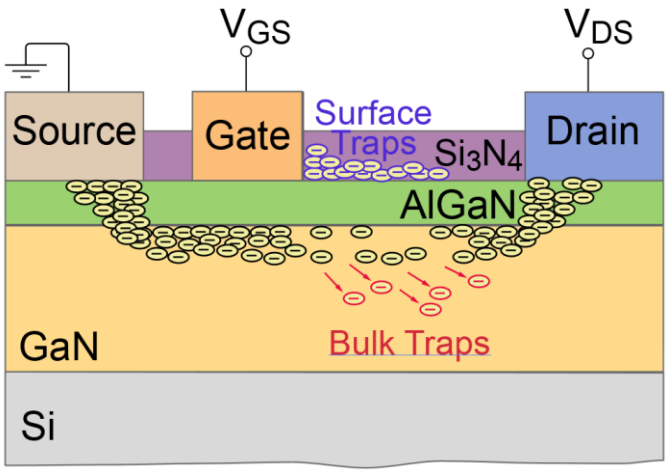

Figure 2.24: Illustration showing a typical AlGaN/GaN HEMT and the charge trapping mechanisms that occur within the device (i.e. bulk trapping and surface trapping).

C. *Surface Trapping*

Similarly to the bulk trapping, electrons can get trapped at the surface of the AlGaN barrier layer. During normal device operation (large V_{DS} and negative V_{GS}), the trapped electrons near the gate are distributed to form what we call a 'virtual-gate', shown in Figure 2.24. Although the trapped electrons are away from the 2DEG channel, they can still modify the potential and, therefore, channel resistance. This phenomenon is coupled with self-heating. In Section 4.6, we investigate both of these mechanisms to identify their impact on device degradation.

2.3. Non-Invasive Characterisation Techniques

In order to begin developing a new characterisation technique for decoupling degradation mechanisms, particularly self-heating and charge carrier trapping, current characterisation techniques used for measuring degradation mechanisms are investigated. Some of these techniques will be used for validation purposes. In this chapter, characterisation methods for measuring temperature distribution (Infrared, μ-Raman and Micro-Resistance Thermal Detector), charge-trapping (Photoluminescence) strain (X-Ray Diffraction), 2DEG sheet density and electron mobility (Hall-Effect), and electrical characteristics (DC and Pulse

measurements) are studied.

2.3.1. Infrared (IR)

Infrared (IR) is a characterisation technique used for measuring temperature distribution along the surface of a device. The technique, which was used for temperature measurements in Chapter 3 allows for surface temperature measurements at a spatial resolution of 2.2 µm and a temporal resolution of 10 µs. An IR camera measures the radiance pattern that is given off from the material. As the temperature of the material increases the greater the infrared radiance energy emitted. This radiation is captured by a sensor array within the camera of which each pixel in the array reacts to the infrared energy by producing an electrical signal. The camera is then calibrated with a signal transfer function to convert the electrical signal produced from the emitted material radiance into the appropriate temperature value. As an example, Figure 2.25 illustrates a top-down view of 2 × AlGaN/GaN HEMTs on Si that are provided by IEMN along with the corresponding 2D temperature distribution in the active region of an AlGaN/GaN HEMT.

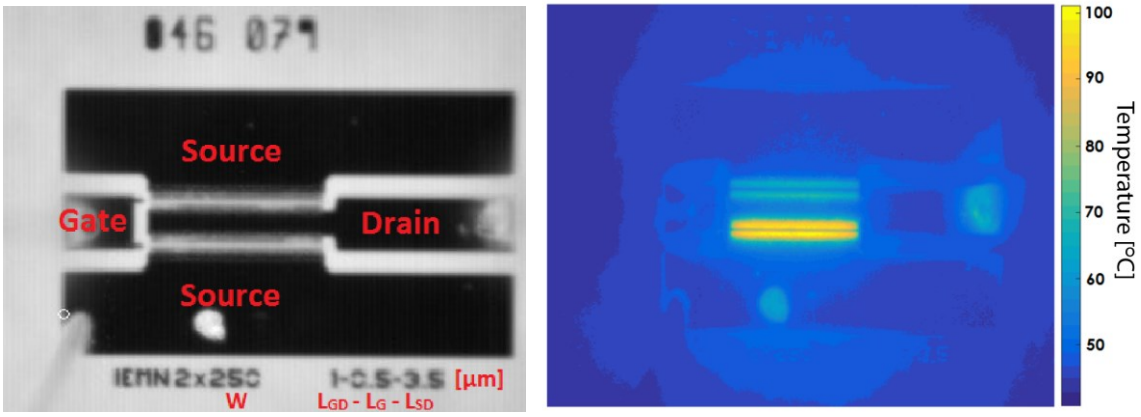

Figure 2.25: (Left) Top-down view of 2 × AlGaN/GaN HEMT on Si, provided by IEMN, with dimensions: W = 250 µm, L_{GD} = 1 µm, L_{GS} = 0.5 µm. (right) 2D IR-Camera temperature distribution through active region of the device at V_{GS} = 0V; V_{DS} = 5V.

2.3.2. Micro-Raman (µ-Raman)

µ-Raman spectroscopy is also used for measuring temperature distribution along the surface of a device. Although this technique is capable of measuring temperature at a higher resolution of ~0.7 µm, it has long integration times that provide measurement inaccuracies in the order of 10 °C. In this technique, determination of lattice temperature is based on the temperature

dependency of the phonon frequency (oscillations of atoms in the crystal lattice). Usually, one of the strongest modes available in the Raman spectrum is used for the determination of temperature. Figure 2.26 shows an example of (i) Raman shift measurements across the surface of an AlGaN/GaN device on a sapphire substrate, and (ii) corresponding Raman measurements, using a spectrometer XY Dilor® and a 100× objective, giving a 0.71 µm diameter spot on the sample surface, provide lattice temperature rise vs. applied power density. The power of the selected excitation is about 10 mW. Optical excitation is performed with the 488 nm line (2.54 eV) of an argon-ion laser. Raman spectra are recorded in the backscattering geometry with incident and scattered lights (not polarised) propagating parallel to the c-axis. The technique is based on the analysis of phonon energies (i.e. the energy of lattice vibrations depending on temperature). Measuring the evolution in phonon energy induced by the current flowing through the device helps deduce the rise in the temperature in the active area focused by the laser beam.

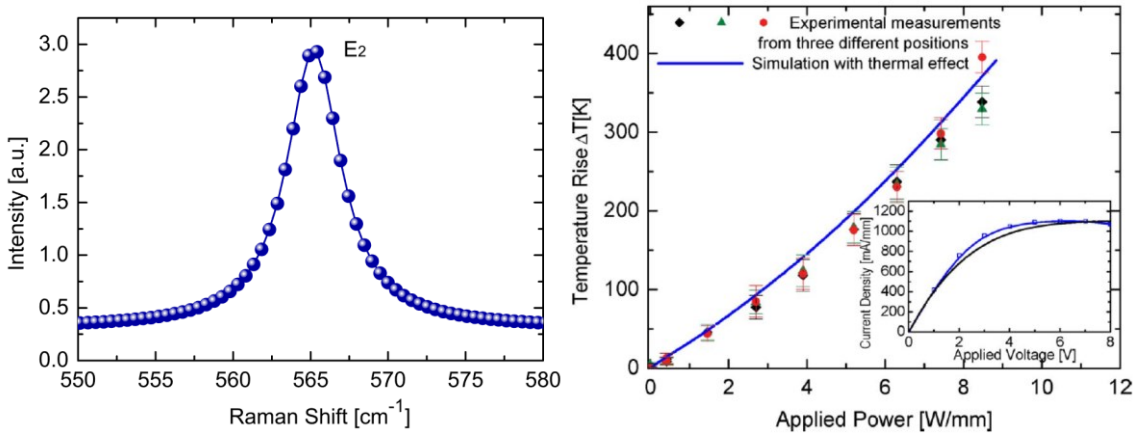

Figure 2.26: (left) Raman shift across surface of AlGaN/GaN device on sapphire substrate. (right) Corresponding lattice temperature rise versus applied power density. The inset shows $I_{DS} - V_{DS}$ characteristics.

2.3.3. µ-Resistance Thermal Detector (µ-RTD)

The electro-thermal characterisation technique, Micro-Resistance Thermal Detector (µ-RTD), accurately measures the channel temperature (T_{CH}) of AlGaN/GaN HEMTs with an error margin of 4.4 °C under a range of bias conditions [125]. It makes use of placing an additional terminal, the µ-RTD terminal, on top of the devices SiO_2 passivation layer, Figure 2.27. Firstly, $I_{DS} - V_{DS}$ measurements are taken under various gate voltages whilst the µ-RTD terminal is in open circuit. Then $I_{DS} - V_{DS}$ measurements are taken but with a small current through the µ-

resistance thermal detector (I_{RTD} = 0.3 mA) passing through the µ-RTD terminal; enough to show variation without causing additional self-heating and no electrical perturbation in the device. This provides the calibration of the µ-RTD terminal by providing similar I – V characteristics and proves functionality of the µ-RTD terminal. A second measurement is taken under various base-plate temperatures whereby the resistance of the µ-RTD is found and then compared with a µ-RTD reference temperature [125]. Lastly, I_{DS} – V_{DS} sweeps are taken at different gate voltages whilst simultaneously measuring µ-RTD resistance to get T_{CH} to finally provide an I_{DS} – V_{DS} – T_{CH} characteristic. The device under test (DUT) and testing platform used for this entire process is illustrated in Figure 2.27. These measurements may be validated by applying the IR and µ-Raman techniques to a similar device without the µ-RTD contact.

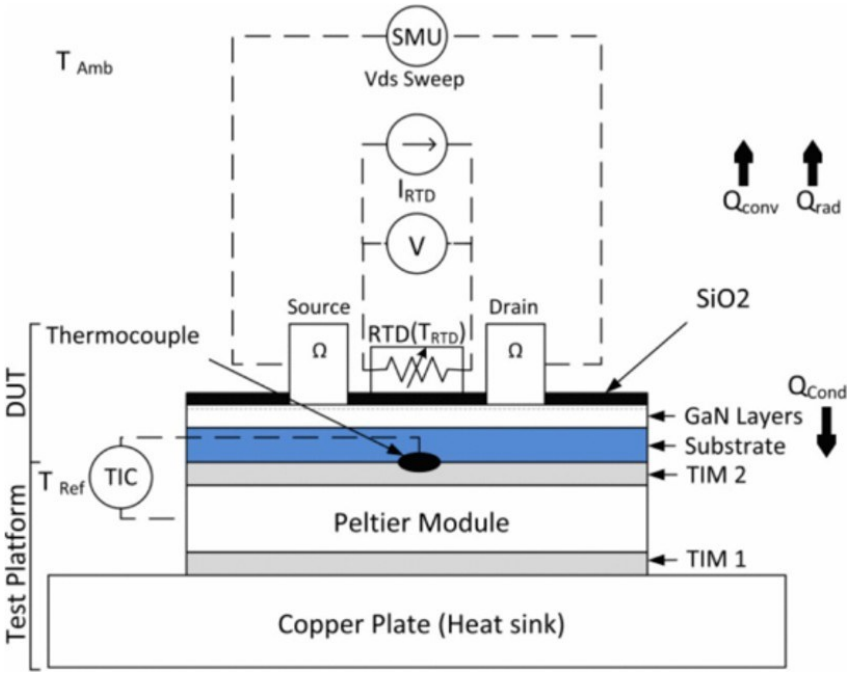

Figure 2.27: Design of DUT and testing platform for temperature measurements using the integrated µ-RTD [126].

2.3.4. Photoluminescence (PL)

Photoluminescence (PL) is a tool used to observe and study the properties of defects in the device. The procedure for photoluminescence begins with illuminating the material with light that is above the bandgap of the material (>3.4 eV). Here, light is captured by electrons in the valence band and are excited to the conduction band, emitting photons of energy that make up the difference of the valence band energy and illuminating light energy, Figure 2.28.

Conduction band electrons also capture the illuminating light where they emit excess energy and return to the bottom of the conduction band. Due to the valence band electrons becoming excited, a freely moving hole is left in the valence band. An acceptor that contains energy within the bandgap can attract and capture the hole turning it into a bound hole. From this, recombination of the bound hole and a conduction band free electron occurs whereby energy is released in the form of photons and phonons; Photon emission is known as PL. Phonons emit the remaining energy and are not of concern in this characterisation technique. There are several luminescences with different wavelengths including blue, yellow, red luminescence (BL, YL, RL) that are present due to Ga and N vacancies, oxygen or deep level impurities, and amorphous phases [127]. In Figure 2.28, the PL process is illustrated along with an example of PL intensity vs. photon energy that results from this process.

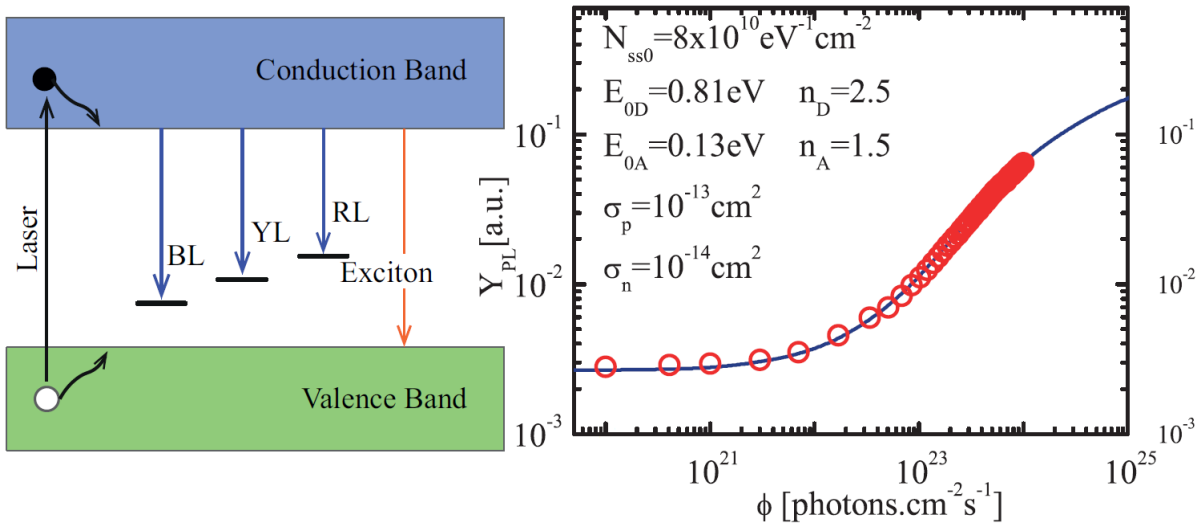

Figure 2.28: (left) PL process schematic; (right) equivalent PL intensity with respect to photon energy example.

2.3.5. X-Ray Diffraction (XRD)

X-Ray Diffraction (XRD) is used to measure strain in the AlGaN barrier layer crystal lattice or in the GaN buffer. The device is placed on an XYZ stage X-ray diffractometer of 50 nm lateral resolution. A zone plate setup focuses a 180 arc sec divergence beam to a quasi-circular illumination of X-rays of around 220 nm radius that the device is exposed to. The interaction of the X-rays with the material's crystal lattice causes diffraction patterns visible by scanning the arc of radius around the device. The device is then shifted on the mount after each measurement to cover the entirety of the device; the location of the illumination spot on the

device is monitored by Ga-K fluorescence intensities that are measured simultaneously with diffraction pattern shifts. As a material is strained, the lattice inter-planar spacing changes, which causes a shift in diffraction pattern of the X-rays. These shifts are measured by a charge-coupled device (CCD) detector, shown in Figure 2.29. The strain is then deduced from the change in inter-planar spacing via mathematical relationships that involve comparing unstressed lattice inter-planar spacing with strained inter-planar spacing [128].

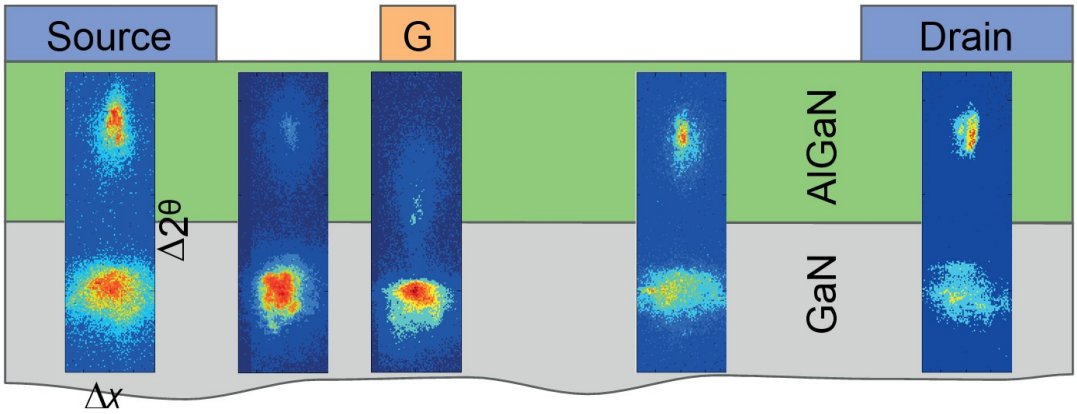

Figure 2.29: XRD CCD capture of an AlGaN/GaN device structure, showing AlGaN and GaN reflections in terms of CCD diffraction intensity.

2.3.6. Electrical Characterisation

Electrical characterisation techniques are typically used as a cost effective method of measuring various device characteristics including charge carrier density, mobility, I – V and C – V characteristics, transient current, defect density, contact resistivity. In this section, we investigate the commonly used Hall-effect technique used to measure charge carrier density and mobility as well as generic techniques typically used for current characterisation.

2.3.6.1. Hall-Effect

The Hall-effect technique is used to measure the 2DEG channel density and mobility. With current (I) flowing through the device, a magnetic field (B) perpendicular to the device is applied resulting in a transverse current. The resulting Hall voltage (V_H) is then measured across the device. Resistivity (ρ) is then measured using the van der Pauw measurement technique [129]. Both V_H and ρ measurements are repeated numerous times and then averaged due to their small values. With these four parameters as well as a measurement for wafer thickness

(t_t), the following formula is used to calculate Hall mobility (μ_H) and n_s:

$$\mu_H = \frac{|V_H|}{IB\rho} \tag{2.11}$$

$$n_s = \frac{IB}{q|V_H|} \tag{2.12}$$

Figure 2.30 shows the 2DEG n_s and μ_n with respect to temperature. The 2DEG density remains constant for temperatures below 450 K (worst-case). Due to the different piezoelectric temperature coefficients of AlGaN and GaN, an increase in temperature (> 450 K) leads to an enhancement of the strain, resulting in greater 2DEG density. This effect is known as pieroelectricity whereby the piezoelectricity changes with temperature. As temperature increases, the electron mobility decreases due to the lattice scattering and onset of polar optical phonon emission. However, this phenomenon reduces at higher temperatures. The mobility is the only quantity that strongly depends on lattice temperature.

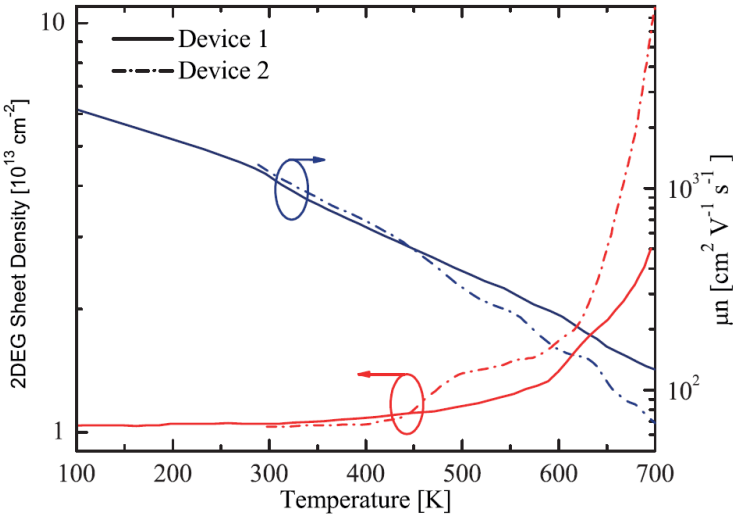

Figure 2.30: 2DEG sheet density and electron mobility vs. Temperature. The increase in 2DEG density (T > 450 K) is due to additional strain caused by pieroelectricity. Hall mobility, μ_n, decrease is due to more electron scattering as temperature increases.

2.3.6.2. DC Measurements

Typically, I – V characteristics are measured using DC measurements. This technique involves applying a DC voltage applied to all contacts of a device (i.e. drain, source, and gate contact) for a long period of time before measuring the current. This long period allows for all current

transients to settle, providing a signal that will not vary around the time that the signal is measured. The measurements are typically performed using a sigma-delta or integrating-type analog-to-digital converter (ADC). However, ambient noise is present in the power lines during measurement. In order to eliminate this noise, the signals are taken over numerous power line cycles and are then averaged in order to improve signal accuracy.

2.3.6.3. Pulse Measurements

Pulse signals provide a large number of data samples within a small time. Due to the short intervals between signals, device damage is prevented even at high voltages. One of the primary mechanisms that can degrade or damage the device over a short space of time is self-heating, as previously described in Section 2.2.6.3. Typically, for measuring I – V characteristics using this technique, a duty cycle of <10 % is applied in order to minimise the self-heating within the device. As a result, the current in I – V characteristics of pulsed measurements is larger than that of DC measurements, showing the performance of devices operating at high frequency. This measurement technique is also beneficial for devices capable of high power. The instruments used for applying high power using pulsed measurements are far more capable of reaching higher power than that of DC measurements due to the short measurement time. In addition, pulsed measurements are capable of measuring transient current with very short intervals, a beneficial technique which DC measurements are unable to perform. To fit measurements into these short windows, sigma-delta ADCs are run at sub-power-line interval integration times; sometimes, the even faster successive approximation register (SAR) type ADCs are used. However, these measurements are far noisier than DC measurements which can be an issue when high accuracy readings are required.

2.3.7. Characterisation Technique Comparison

The optical techniques IR and μ-Raman are commonly used for measuring temperature distribution. μ-Raman has the advantage of providing better spatial resolution (0.7 μm) compared to IR (~2.2 μm). However, a significant disadvantage to using the μ-Raman technique is that it takes much more time and requires a higher applied power density than IR. Therefore, it is not needed for temperature measurements of large devices. Devices grown on sapphire are difficult to be characterised using IR due to the transparency of Al_2O_3. On the other hand, devices grown on SiC are difficult to characterise using μ-Raman, due to the

bidirectional shift of the Raman signal with temperature that occurs with SiC, which complicates the calibration step.; with thermal-electrical characterisation, µ-RTD, these problems do not occur. Although, the µ-RTD technique does not provide a distribution of temperature across the device, an accurate peak temperature beneath the µ-RTD contact can be obtained. PL is commonly used to characterise defects in a material due to the high sensitivity to discrete electronic states. The benefit of this technique is that there is no change in results from when previously exposed to X-ray irradiation used in the XRD technique. Although the XRD technique is considered to measure surface strain, X-rays that are illuminated onto the device penetrate a few micrometers deep into the material. So, several values of diffraction pattern shift occur at one coordinate along the device surface with respect to depth of penetration. As the measurements are presented in 2D across the surface, the range of shift values are averaged and provide one value of strain at each coordinate on the surface. Therefore, shift/strain shown at the surface has some error due to coupling with shift/strain deeper in the material. The Hall-effect technique is commonly used for sheet density and electron mobility measurements as it is not affected by ambient conditions due to its using a magnetic field to induce traverse current; it is highly reliable and repeatable, and operates at a wide range of temperatures.

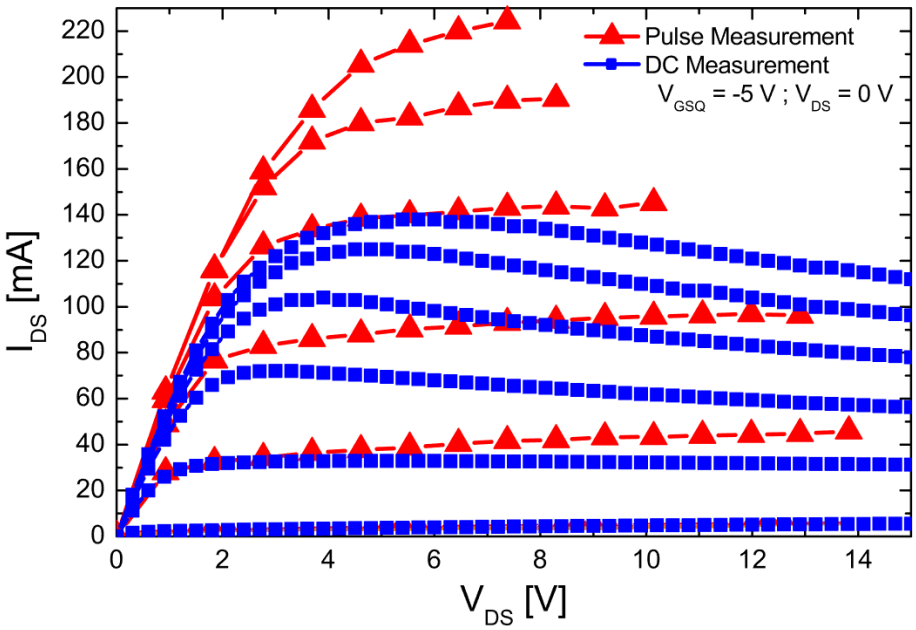

Figure 2.31: Comparison of $I_{DS} - V_{DS}$ characteristics with DC measurement (blue) and Pulse measurement (red) for V_{GSQ} = -5 V and V_{DS}= 0 V.

An important characteristic that defines the power capabilities of HEMT devices is the drain-source current (I_{DS}) vs. drain-source voltage (V_{DS}). Figure 2.31 compares the I_{DS} – V_{DS} characteristics of an AlGaN/GaN HEMT under DC (blue) and pulse (red) measurements. It is clear that current collapse occurs in DC measurements. This is primarily due to self-heating and charge trapping. The use of pulse measurements minimises this degradation due to the device being set to OFF-state for a period of time between each measurement. Current degradation due to self-heating and charge trapping still occurs during pulse measurements, although less than in DC, as described in Section 2.3.6. The decoupling of self-heating and charge trapping is investigated using pulse measurements in Chapter 4.

2.4. Development Challenges

The superior performance of AlGaN/GaN HEMTs is hampered by serious reliability issues, which remain an open problem that is holding back their widespread commercial and industrial development. These reliability issues stem from degradation mechanisms such as: (i) self-heating effects, that significantly impact the transport properties in the 2DEG, (ii) charge trapping effects, that are responsible for reducing device lifetime and reliability, (iii) source/drain (S/D) Ohmic contact resistances increase during device operation, and (iv) gate Schottky contact leakage current and barrier height, are controversial and largely unknown [60]–[62]. These accelerating factors are behind device performance degradation and persist to be limiting reliability factors. Maintaining high performance and reliability of the S/D Ohmic and gate Schottky contacts in AlGaN/GaN HEMTs is a significant challenge, particularly at high operating voltages, which hinders progress in a large-scale deployment of the technology in applications [33], [44], [45].

The strong coupling of self-heating and charge trapping mechanisms, under normal device operation, makes the quantitative contribution of each mechanism indistinct. This key performance and reliability information poses a significant challenge, particularly for AlGaN/GaN HEMTs due to their high operating temperature and relatively high density of traps, and impedes the device performance progress, an important step before large-scale deployment can be attained [60]–[62], [130].

Transient measurements, such as fast pulse characterisations described in Section 2.3.6.3, are often used to reduce self-heating effects in the device when investigating trapping effects [131].

However, it has been shown that the temperature at the channel of a conventional AlGaN/GaN HEMT can reach 70% of its maximum value within the first 2 µs, after the device is switched ON [124], [132], [133]. Lowering the applied biases conditions to prevent temperature rise is another option to decouple traps from self-heating. However, this methodology is unable to provide vital information about traps kinetics at normal device operation. Lack of standard characterisation techniques for degradation mechanisms' decoupling plays a major role in holding back the optimisation of III-N process and device technology, an important step before large-scale deployment can be attained [60]–[62], [130]. Developing such a technique and re-examining the impact each degradation mechanism has on the device, during normal device operation, will be the focus of this Thesis. This technique will contribute towards understanding the origins of device failure and the kinetics of the degradation mechanisms.

In addition, to achieve high performance, Ohmic and Schottky contacts are required to be optimised to provide lower contact resistance (R_C) and higher energy barrier (Φ_{bn}), respectively. Increasing the Al concentration in the barrier and/or using AlN exclusion layer is known to increase 2DEG confinement and to enhance 2DEG density and mobility, which enhances performance [134], [135]. However, it results in increased R_C due to low metal diffusion beneath the metal contact [136], [137]. In Section 5.2, we propose a fabrication process of ohmic contacts to reduce R_C of AlGaN/GaN HEMTs with a high Al concentration, whilst avoiding implantations that cause HF-traps and gate leakage. The optimisation of Schottky contacts is crucial for gate control in GaN-based HEMTs in order to achieve high frequency performance, good linearity and low leakage current. With the existing Schottky contact metallisation processes, the leakage current and the barrier height can be improved but needs several difficult operations, described in Section 5.3.1, before achieving this. Therefore, we propose a new and simple process of forming a TiN-based Schottky contact on an AlGaN barrier.

CHAPTER 3

STRAIN IMPACT ON SELF-HEATING IN AlGaN/GaN HEMTs

In the first section of this chapter, we investigate the self-heating and strain mechanisms in AlGaN/GaN HEMTs using Infrascope temperature mapping system (IR) accompanied by synchrotron radiation-based High-Resolution X-Ray Diffraction (HR-XRD) measurements and physically based TCAD simulations. This unique approach demonstrates that compressive and tensile strain around S/D contacts affects temperature distribution during device operation and limits its performance. In the second section of this chapter, we study electro-thermal behaviour of scaled AlGaN/GaN TLM heterostructures with low resistive Ohmic contacts to identify the relationship between device geometry and polarisation within AlGaN/GaN-based devices.

3.1. Structure of Investigated Devices

The investigated AlGaN/GaN-based device structure has been grown by molecular beam epitaxy on High-Purity HP-Si(111) substrate (Figure 3.1). The following device architecture was fabricated at the IEMN of the University of Lille. It consists, from the substrate to the top surface, of low temperature AlN(40 nm)/GaN(250 nm)/AlN(250 nm) nucleation layers, a 1.7 µm $Al_{0.10}Ga_{0.90}N$ back-barrier to reduce leakage current in the buffer and to improve the carrier

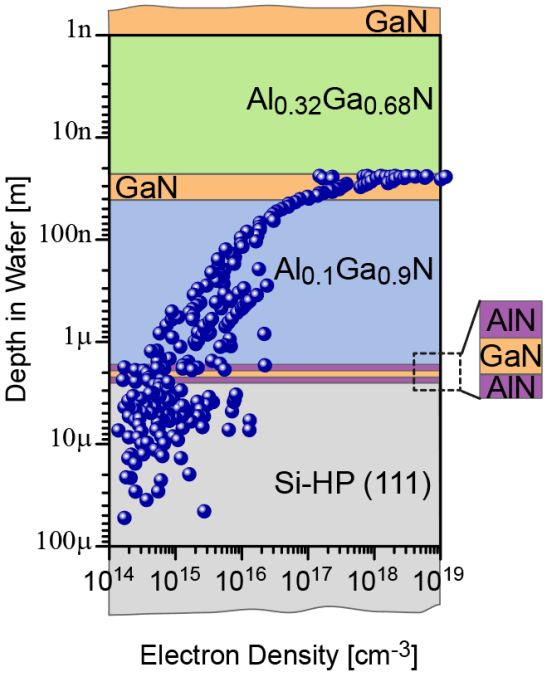

Figure 3.1: AlGaN/GaN-based device structure and measured electron density profile of the investigated wafer, GaN(1 nm)/$Al_{0.32}Ga_{0.68}N$(25 nm)/GaN(15 nm)/$Al_{0.10}Ga_{0.90}N$(1.7 µm)/NL/HP-Si(111), where NL are nucleation layers that consist of AlN(40 nm)/GaN(250 nm)/AlN(250 nm).

confinement of the 2DEG. A channel is made of a 15 nm thick unintentionally doped GaN buffer followed by a 25 nm undoped $Al_{0.32}Ga_{0.68}N$ barrier and, finally, a 1 nm GaN cap layer. Room temperature Hall measurements yield a 2DEG electron mobility of 1750 $cm^2V^{-1}s^{-1}$ and $R_{\square}$ = 310 Ω/□. The CV-technique revealed an electron sheet density of 1.18 × 10^{13} cm^{-2} in the buffer. The fabrication process flow is similar to that in [107]. To reduce the contact resistance, the S/D terminals are formed by rapid thermal annealing of an evaporated Ti(10 nm)/Al(200 nm)/Ni(40 nm)/Au(100 nm) multilayers metallisation scheme at 870 ºC for 30 s under nitrogen atmosphere. The S/D contacts resistance and specific resistivity are 0.39 Ω.mm and 3.8 × 10^{-6} Ω.cm^2, respectively. The devices are electrically isolated by He^+ ion multiple implantations.

To reduce trapping effects and dispersion, the surfaces of the devices are N_2O pre-treated for 2 min followed by SiO_2(100 nm)/Si_3N_4(50 nm) bi-layer passivation, performed by plasma-enhanced chemical vapour deposition at 340 ºC. The SiO_2(100 nm)/Si_3N_4(50 nm) bi-layer is opened by using a CHF_3/CF_4 reactive ion etching plasma. The used gate metallisation scheme is Ni(5 nm)/Pt(25 nm)/Ti(25 nm)/Mo(30 nm)/Au(250 nm). The electrical I – V characterisations were performed at DC and dark conditions at University of Swansea using the Agilent B1500A framework. The trace of drain current is reproducible showing that no permanent degradation of drain current occurs from the experiment, only recoverable degradation, i.e., charge trapping and self-heating.

3.2. Strain-Reduction Induced Rise in Channel Temperature at Ohmic Contacts

In this work, we investigate the channel temperature distribution in AlGaN/GaN-based devices using IR temperature mapping system accompanied by HR-XRD measurements and physically based TCAD simulations. We demonstrate that compressive and tensile strain around S/D affects temperature distribution during device operation which limits device performance. An overview of the used devices and performed experiments is first summarised. Then, temperature profiles in the device under different configurations as well as the physics behind the temperature rise at the source/drain contacts is examined.

3.2.1. Experimental Procedure

3.2.1.1. Device Performance

The I_{DS} – V_{DS} characteristics of the used 100 µm wide AlGaN/GaN TLMs with different source-to-drain distances, L_{SD} = 10 µm (short TLM) and L_{SD} = 30 µm (long TLM), are shown

in Figure 3.2. A lower current and a larger resistance are observed for the long TLM.

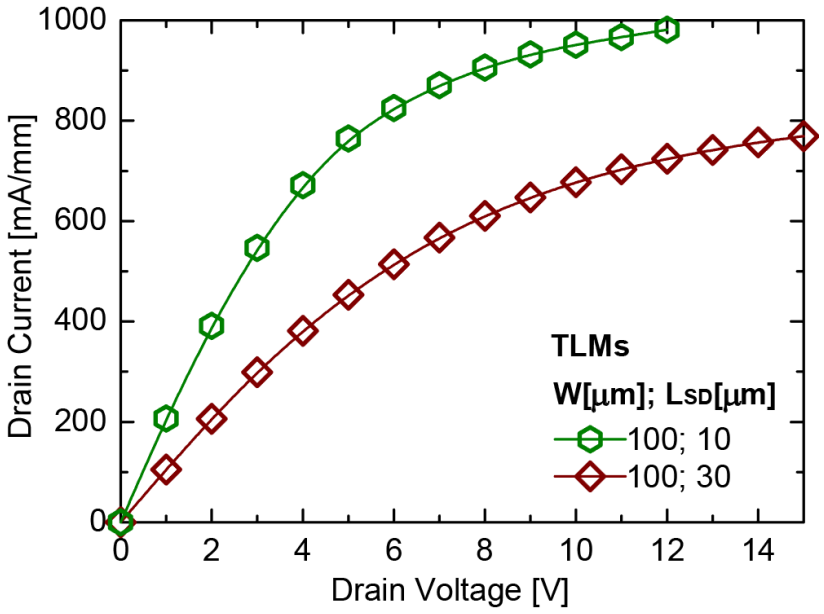

Figure 3.2: Measured $I_{DS} - V_{DS}$ characteristics of the gateless AlGaN/GaN TLMs. The source-to-drain distance of the used TLMs are L_{SD} = 10 µm (short TLM) and L_{SD} = 30 µm (long TLM).

3.2.1.2. Infrared Camera

To measure the temperature profile, the Infrascope temperature mapping system from IEMN of the University of Lille, equipped with 500 × 500 InSb detectors array, is first calibrated. A high emissivity layer is coated over the device and surface radiation of the unbiased AlGaN/GaN device is measured, whilst increasing the temperature from 50 °C to 200 °C with a step of 15 °C using a heated-stage to maintain constant uniform temperature [107], [138]. The surface temperature is then measured from the emissivity by comparing it with the instrument calibration curve (not shown). After the calibration step, each device is first placed on a constant temperature platform (40 °C or 45 °C) and biased at DC conditions using Agilent B1500A framework. Then, thermal imaging measurements are performed using the calibrated Infrascope system. Pixel resolution of the obtained IR image is about 2.3 µm, giving a total field of view of about 1 mm × 1 mm. This technique is based on measuring the IR radiations emitted at the top surface of the device that are proportional to the temperature.

3.2.1.3. High-Resolution X-Ray Diffraction

To measure the strain profile in the AlGaN barrier layer, synchrotron radiation-based HR-XRD

is used. This techniques uses 10.4 keV energy at the 2 – I_D – D micro-diffraction beamline. The sample device is mounted on an XYZ stage with a 50 nm resolution. The location of the beam spot was monitored by means of simultaneous measurement of Ga–K fluorescence intensities and the diffraction data were collected by a charge-coupled detector. The size of the quasi-circular beam spot is ≈220 nm with 180 arc sec divergence.

3.2.1.4. Simulation Methodology

The electrostatic (i.e. potential and electric field distribution) of the used devices have been investigated by Drift-Diffusion (DD) simulations. The details of the used device simulation technique can be found in [139]–[144]. In the past, this simulation technique has been successfully used to predict AlGaN/GaN based device architectures grown on various substrates (i.e., Si, 4H−SiC, diamond, Al_2O_3). The transport parameters such as electron drift velocity, energy relaxation time, and electron effective mass are obtained from Monte Carlo simulation runs at different lattice temperatures [144]. Both simulated I – V characteristics and

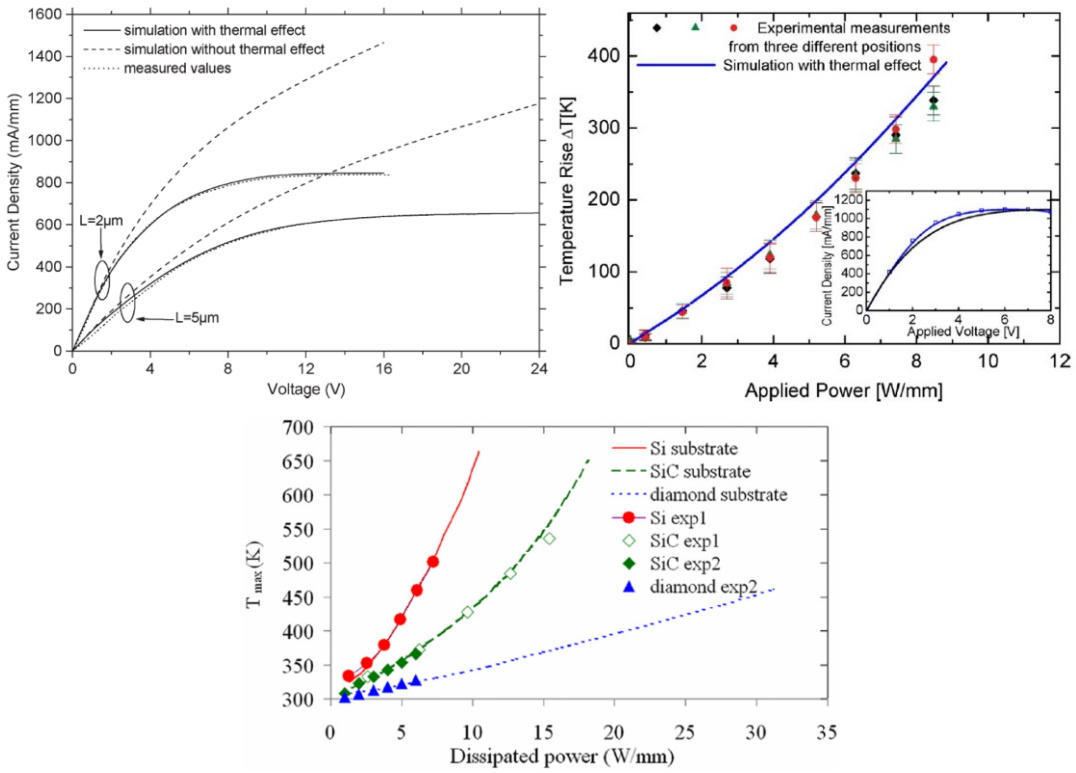

Figure 3.3: I – V characteristics and operating temperatures for different device structures (gated and gateless), showing good agreements between experimental data and our simulation results.

calculated temperatures have been compared to experimental I – V characteristics and temperature measurements, demonstrating a good agreement, as shown in Figure 3.3. Moreover, this simulation technique has been adapted to deal with both gated and gateless AlGaN/GaN devices.

3.2.2. Temperature distribution in AlGaN/GaN TLMs

3.2.2.1. Source-to-Drain Thermal Coupling

Figure 3.4 shows the IR measured temperature distributions along the surface of the short and long TLMs, L_{SD} = 10 µm and L_{SD} = 30 µm, at V_{DS} = 2 V to 12 V by step of 2 V. For the long TLM, temperature peaks are observed at the inner ends of the S/D contacts, for all applied biases (Figure 3.4(b)). These temperature peaks merge when L_{SD} decreases as a result of temperature coupling (Figure 3.4(a)). For $L_{SD} \leq$ 10 µm, the amount of thermal coupling between the source and the drain sides is even larger making it difficult to observe the temperature peaks at the inner end of the Ohmic contacts (not shown). Note that this thermal coupling induced temperature rise can significantly impact the device performance through an increase in the contact access resistance and electron mobility degradation, particularly for small devices, as a result of the source-drain thermal coupling.

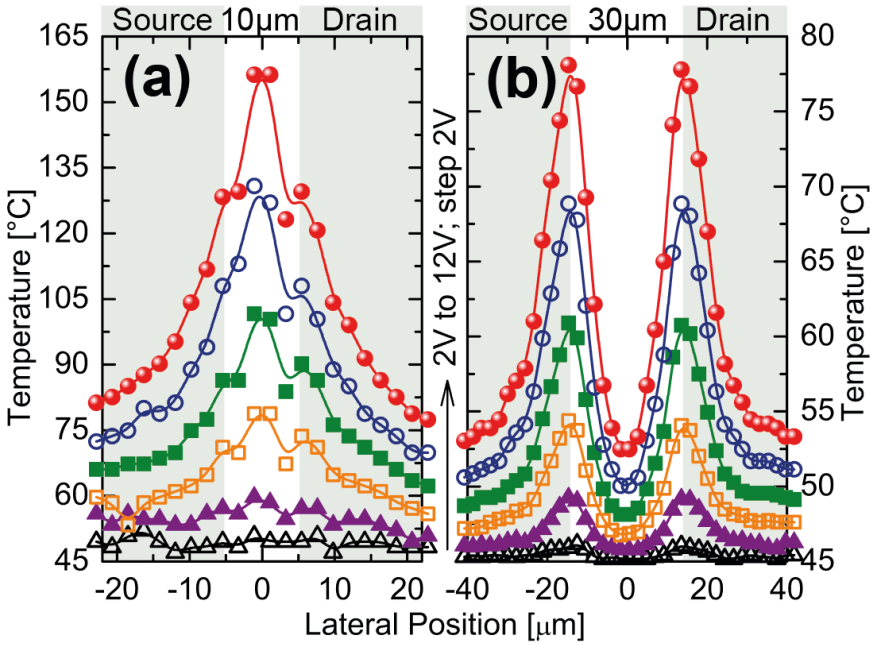

Figure 3.4: Measured temperature profiles along the top surface of the gateless AlGaN/GaN structures at different drain voltages for (a) short TLM (L_{SD} = 10 µm) and (b) long TLM (L_{SD} = 30 µm).

Unlike in the long TLM, the channel temperature is at its maximum in the centre of the short TLM (L_{SD} = 10 µm). This can be explained by a heat spread angle and a strong thermal coupling between source and drain, as illustrated in Figure 3.5(a). The temperature in the middle of the short TLM is much higher than at the inner ends of Ohmic contacts. To demonstrate the low thermal coupling in the long TLM (L_{SD} = 30 µm), we have artificially modified the measured temperature profile by reducing the source-to-drain distance from 30 µm to 10 µm (Figure 3.5(b)). It can be seen that the resultant temperature profile (modified

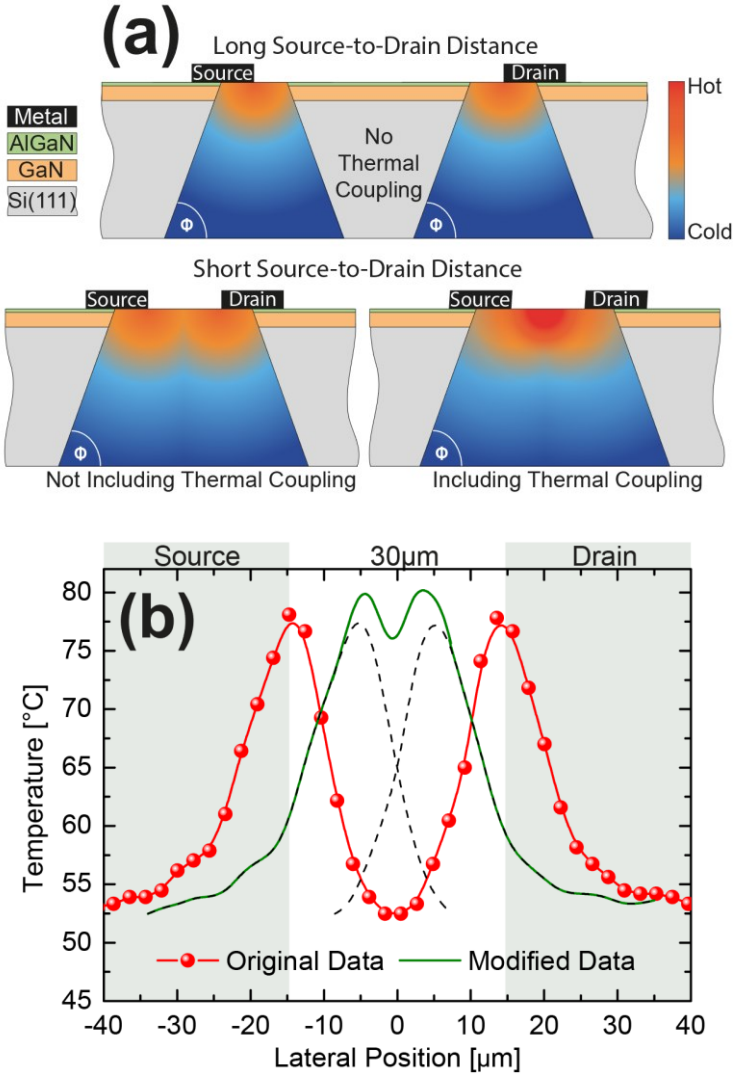

Figure 3.5: (a) Illustration of the heat spreading angle and the source-to-drain thermal coupling in the short and long TLMs. (b) Measured temperature profile along the top surface of the gateless AlGaN/GaN structure at V_{DS} = 12 V for the long TLM (L_{SD} = 30 µm). The original measured data are compared to the modified data to show a very negligible thermal coupling between the inner ends of Ohmic contacts in a long L_{SD} device.

data) is slightly larger than the original data but still present two peaks, in contrast with the measured temperature of the short TLM (L_{SD} = 10 µm).

The device temperatures of the AlGaN/GaN TLMs are plotted against dissipated power density in Figure 3.6. The dissipated power density is controlled via V_{DS}. For a given dissipated power density, the temperature is higher in the short TLM (L_{SD} = 10 µm) due to (i) a higher electric field [139] and (ii) a stronger thermal coupling between source and drain sides (Figure 3.5(a)).

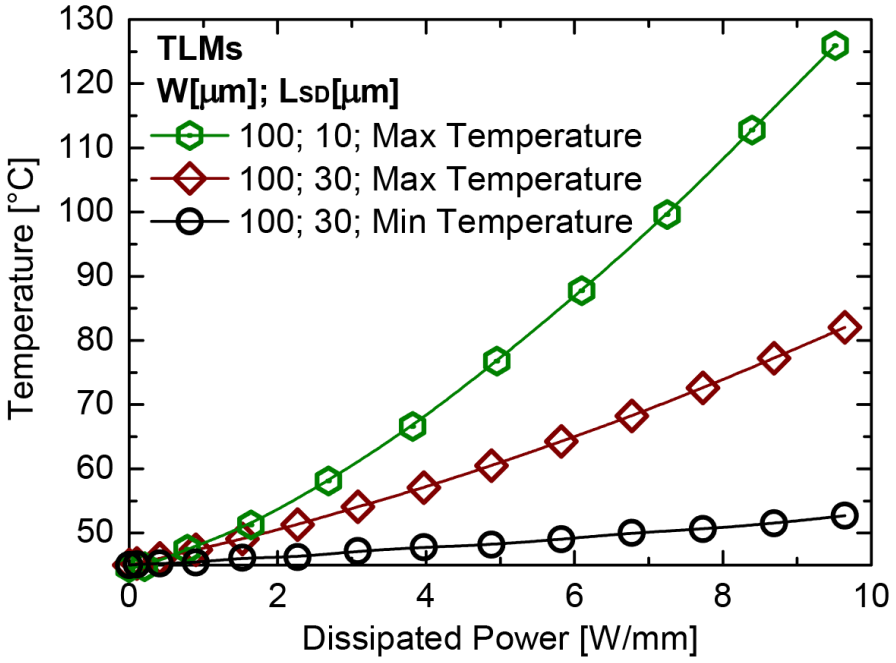

Figure 3.6: Evolution of the channel temperature versus the dissipated power density for the AlGaN/GaN TLMs (L_{SD} = 10 µm and L_{SD} = 30 µm). The Max Temperatures are extracted from the peaks at the vicinity of S/D contacts for the long TLM and at the centre of the device for the short TLM. The Min Temperature corresponds to the value of temperature at centre of the long TLM (L_{SD} = 30 µm).

3.2.2.2. Thermal Resistance

To get a rough estimate of the thermal resistance of each device, we have employed the analytical thermal model described by the following equation [145], [146]:

$$T = T_{SUB} + R_{TH} \times P_{DISS} \qquad (3.1)$$

where T is the channel temperature, T_{SUB} is the substrate temperature (45 °C), R_{TH} is the thermal resistance, and P_{DISS} is the dissipated power, which is proportional to electric field (E),

drain current (I_{DS}) and source-to-drain distance (L_{SD}):

$$P_{DISS} \approx E \times I_{DS} \times L_{SD} \quad (3.2)$$

According to this model, the increase of L_{SD} should lead to an increase in temperature, due to a larger amount of material for heat to dissipate through. This is in disagreement with experimental observations. Therefore, the temperature increase with the reduction of L_{SD} is mainly caused by the thermal resistance. With respect to the heat spreading angle model [147]–[149], as illustrated in Figure 3.5(a), the thermal resistance increases with decreased L_{SD} due to the lower substrate volume for heat to dissipate. The extracted thermal resistances are 68 ^{o}C W^{-1} and 38 ^{o}C W^{-1} for short (L_{SD} = 10 µm) and long (L_{SD} = 30 µm) TLMs, respectively. These values of R_{TH} are within the typical range of values [138], [150]. Here, we have used the maximum temperatures that occurs at (i) the inner-ends of the source and drain terminals for the long TLM (L_{SD} = 30 µm) and (ii) at the centre of the device for the short TLM (L_{SD} = 10 µm), due to thermal coupling. When using temperature values in the middle of the TLM with L_{SD} = 30 µm (minimum temperature), the extracted R_{TH} is equal to 9.0 ^{o}C W^{-1}, over three times smaller than at the inner-ends of the source and drain terminals. This is an indication of a non-uniform distribution of the electric field between source and drain contacts.

3.2.2.3. Strain Relationship with Self-Heating

It has been reported that the S/D Ohmic contacts process annealing and device operation induce mechanical stress due to (i) a mismatch in thermal expansion coefficients of III-N and Ti/Al/Ni/Au metallisation scheme, and (ii) an exacerbation of inverse piezoelectric effect at high temperatures [151]–[153]. These effects result in a change of strain at the vicinity of metal contacts. The deformation of c-plane nitride crystal under compressive and tensile strains [154] around the contacts is illustrated in Figure 3.7(b).

To support the above theory, the strain relaxation in the AlGaN barrier layer of an unbiased device is measured using synchrotron radiation-based HR-XRD [155]. The measured strain profile, given in Figure 3.7(a), reveals a reduction of strain at the inner ends of S/D contacts. The strain reduction at the inner ends of the contacts reduces the electron density at these locations which, in turn, impacts the potential distribution and increases the electric field locally [156], hence an increase in channel temperature. Some preliminary HR-XRD data shows a reduction of strain below the gate terminal as well (Figure 3.8). Further investigation

of the heating beneath the gate will be the subject of future works.

The impact of the strain reduction, at the inner ends of S/D Ohmic contacts, on the device electrostatic has been investigated by DD simulations and HR-XRD measured data. The details of the used device simulation technique can be found in [139]–[144]. In the past, this simulation

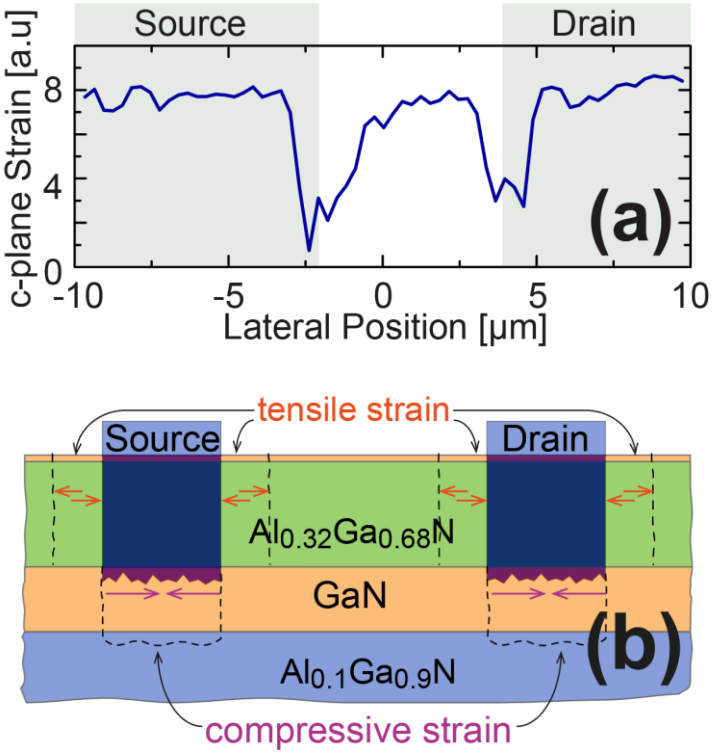

Figure 3.7: (a) Measured strain in the channel along the lateral direction of an AlGaN/GaN TLM using synchrotron radiation-based HR-XRD, showing a reduction of strain at the inner ends of S/D contacts. (b) The schematic of strain distribution at the vicinity of S/D Ohmic contacts.

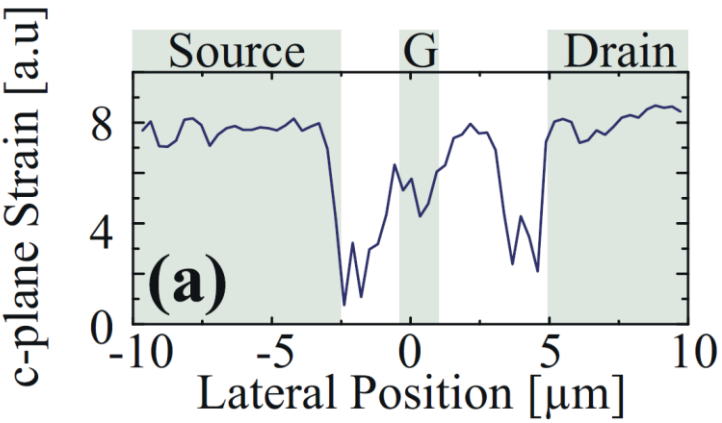

Figure 3.8: Measured strain in the channel along the lateral direction of an AlGaN/GaN HEMT using HR-XRD.

technique has been successfully used to predict AlGaN/GaN based device architectures grown on various substrates (i.e., Si, 4H–SiC, diamond, sapphire). The transport parameters such as electron drift velocity, energy relaxation time, and electron effective mass are obtained from Monte Carlo simulation runs at different lattice temperatures [144]. Both simulated I – V characteristics and calculated temperatures have been compared to experimental I – V characteristics and temperature measurements, demonstrating a good agreement [139]–[142]. Moreover, this simulation technique has been adapted to deal with both gated and gateless AlGaN/GaN devices.

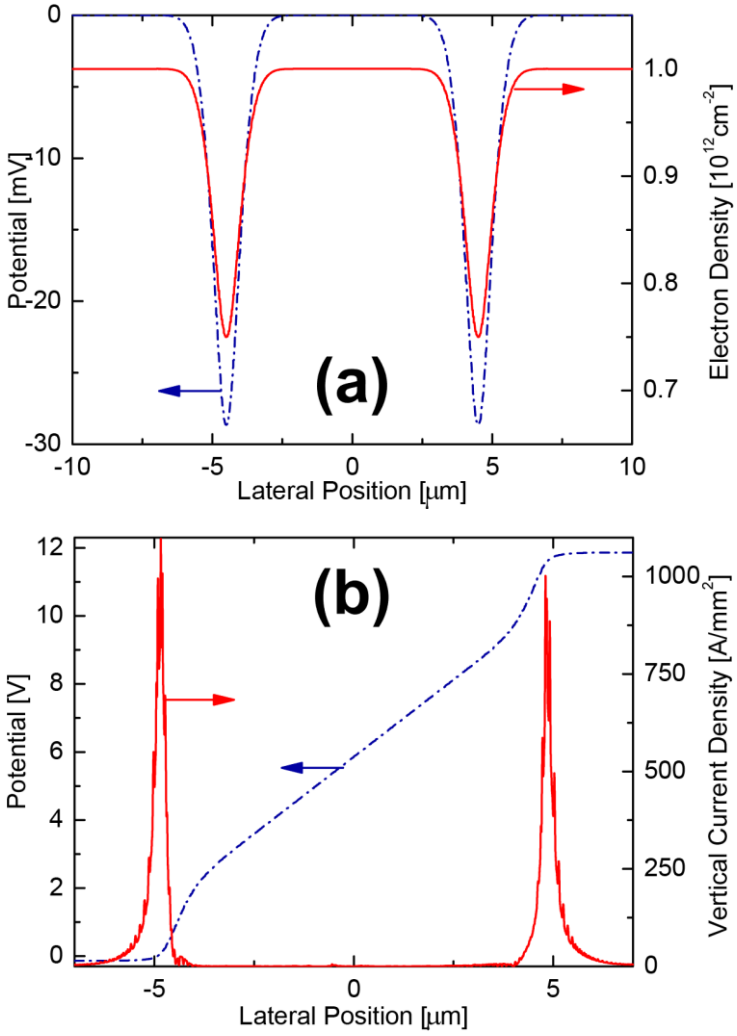

Figure 3.9: DD simulation results of the short TLM (L_{SD} = 10 µm), when taking into account the HR-XRD measured strain. (a) Lateral 2DEG profile overlapped with potential distribution at V_{DS} = 0 V in the channel of the TLM. (b) Vertical current density overlapped with potential distribution at V_{DS} = 12 V in the channel of the TLM.

The lateral 2DEG profile overlapped with corresponding potential distribution at V_{DS} = 0 V, when taking into account the measured strain, are shown in Figure 3.9(a). At least 25 % reduction in 2DEG density is observed at the inner ends of S/D contacts, as a result of strain degradation. Figure 3.10(a) and (b) compare the simulated electric field distributions with measured temperature profiles under V_{DS} = 12 V for both short (L_{SD} = 10 µm) and long (L_{SD} =

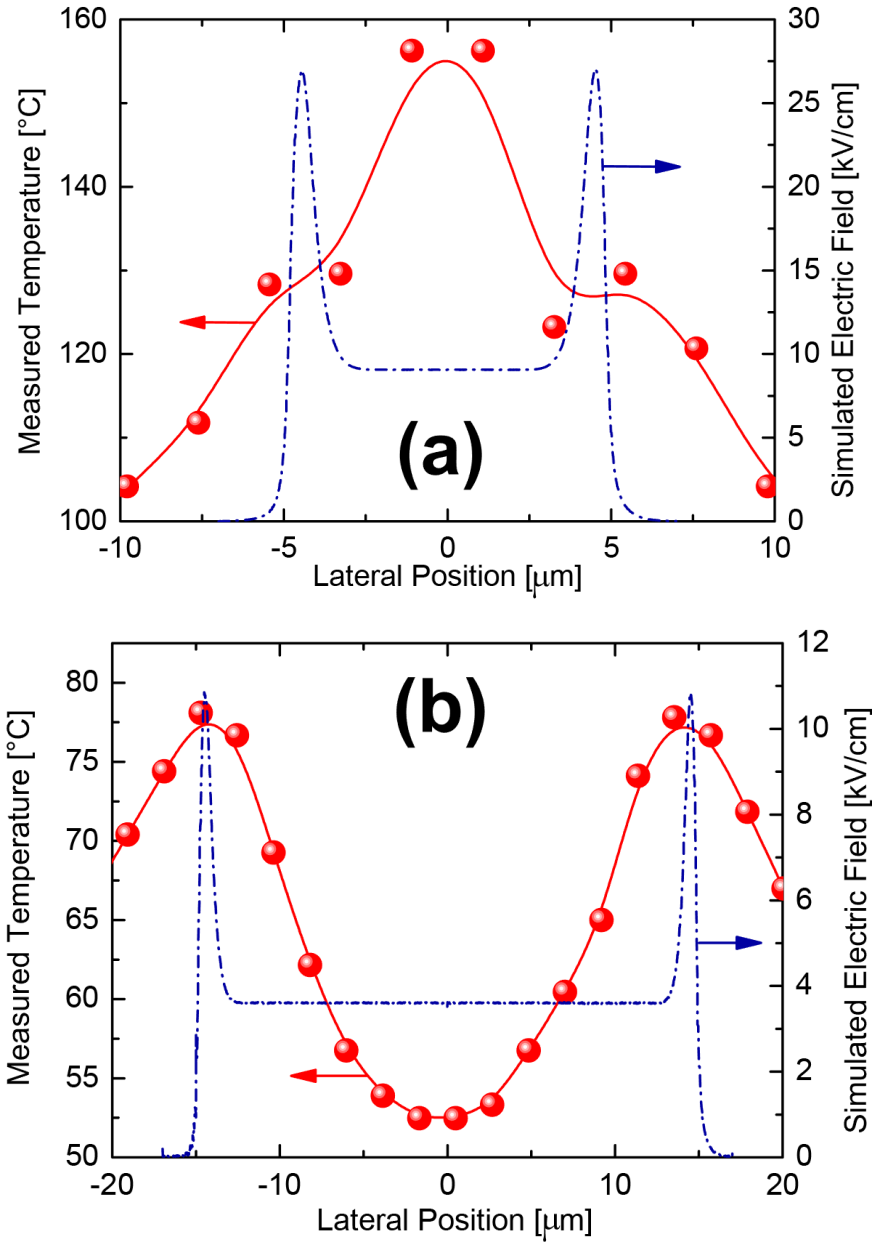

Figure 3.10: simulated electric field distributions and measured temperature profiles at V_{DS} = 12 V for (a) short TLM (L_{SD} = 10 µm) and (b) long TLM (L_{SD} = 30 µm).

30 µm) TLMs, respectively. Electric field peaks that occur at the inner ends of the S/D contacts are nearly three times larger than that at the middle of the device and directly correlate with the measured temperature profiles. As the electric field and the drain current increase proportionally with V_{DS}, the channel temperature increases near the Ohmic contacts. With the proportional relationship between electric field and temperature, the degradation of strain significantly impacts temperature peaks within the device. Furthermore, the vertical component of the current density, simulated by DD and given in Figure 3.9(b), shows that the majority of current flows in/out of the 2DEG through a small portion of the S/D contacts as suggested by Trilayer-TLM model Ohmic contacts [157]. This attribute could be a cause of a further strain degradation and channel temperature increase.

3.2.3. AlGaN/GaN HEMT

3.2.3.1. Sources of Self-Heating

It was not possible to observe the temperature peaks at the vicinity of the Ohmic contacts in AlGaN/GaN HEMTs due (i) to the strong thermal coupling between contacts when $L_{SD} \leq 10$ µm, as demonstrated in the previous section; and (ii) to the hot-spot at the end of the gate, as described in this section. However, a temperature rise near source and drain contacts still takes place in HEMTs, since the fabrication process of Ohmic contacts in gated and gateless devices are exactly the same. We shall therefore expect to observe temperature rise near the S/D contacts in HEMTs as in TLMs. The $I_D - V_G$ characteristics of two AlGaN/GaN HEMTs with

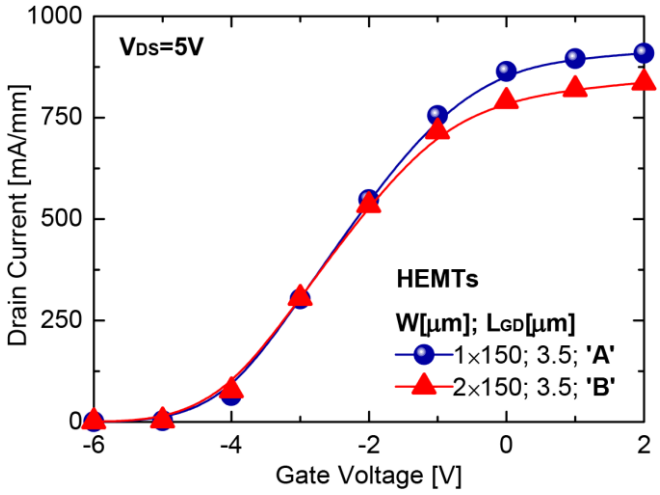

Figure 3.11: Measured $I_D - V_G$ characteristics of single and two-finger gate AlGaN/GaN HEMTs at V_{DS} = 5 V. The device dimensions are: L_{SG} = 1.0 µm, L_G = 0.5 µm, L_{GD} = 3.5 µm.

different configurations (single or two-finger gate) are presented in Figure 3.11. The two-finger gate device 'B' outputs less current than single-finger gate HEMT 'A', a point to be noted in discussion. The same temperature measurement technique is applied to a two-finger gate HEMT with L_{GD} = 2.5 µm and W = 2 × 150 µm (Figure 3.12(a)). Since L_{SD} of this device is less than 10 µm, the peaks of temperature at the inner ends of S/D contacts are merged together. This profile is similar to what has already been reported in literature using techniques such as µ-Raman [158]. The notch between the source and drain sides is caused by the metal gate. In addition, a higher temperature peak can also be seen at the end of the gate (toward the drain side, as marked by T_{SD} in Figure 3.12(b)). This peak may be slightly undervalued, due to the limited resolution of the IR System. The drain-side temperature increase as V_{GS} increases can be explained by the temperature coupling with that of the neighbouring HEMT and by the high electron kinetic energy at the end of the gate [159]. The maximum device temperatures of the AlGaN/GaN HEMTs are plotted against dissipated power density in Figure 3.13(a). The dissipated power density is controlled via V_{GS} and V_{DS}. The presence of temperature coupling between two neighbouring HEMTs (two-finger gate HEMT 'B': W = 2 × 150 µm), due to heat spreading angle as illustrated in Figure 3.13(b), leads to channel temperature increase, when compared with a single-gate HEMT ('A': W = 1 × 150 µm) [160]. As a result, the two-finger gate exhibits lower drain current, as shown in Figure 3.11 [140], opposite to the expected higher current without considering thermal coupling. This experimental observation is in good agreement with heat spreading angle models [147]–[149]. The main cause of temperature rise in AlGaN/GaN HEMT is, therefore, the high value of the electric field at the end of the gate toward the drain side. This electric field peak is observed through DD-simulation, Figure 3.14, which also shows increased electric field with reduced source-to-drain distance that increases the self-heating further. The electrons that enter the device via the source terminal and crystal lattice of AlGaN and GaN gain significant energy at the drain-side gate edge, as shown in Figure 3.15, due to the large electric field peak in the local area. Consequently, a non-uniform distribution of dissipated power produces a hot spot of temperature to be formed at this location, Figure 3.16. This phenomenon happens regardless of the strain reduction near the contact [161], [162]. Therefore, the physics behind temperature rises near the gate and near S/D contacts are very different. Both mechanisms contribute to the higher temperature at the drain side in AlGaN/GaN HEMTs. Further investigation will be needed to separate the thermal effects of the two mechanisms in this device.

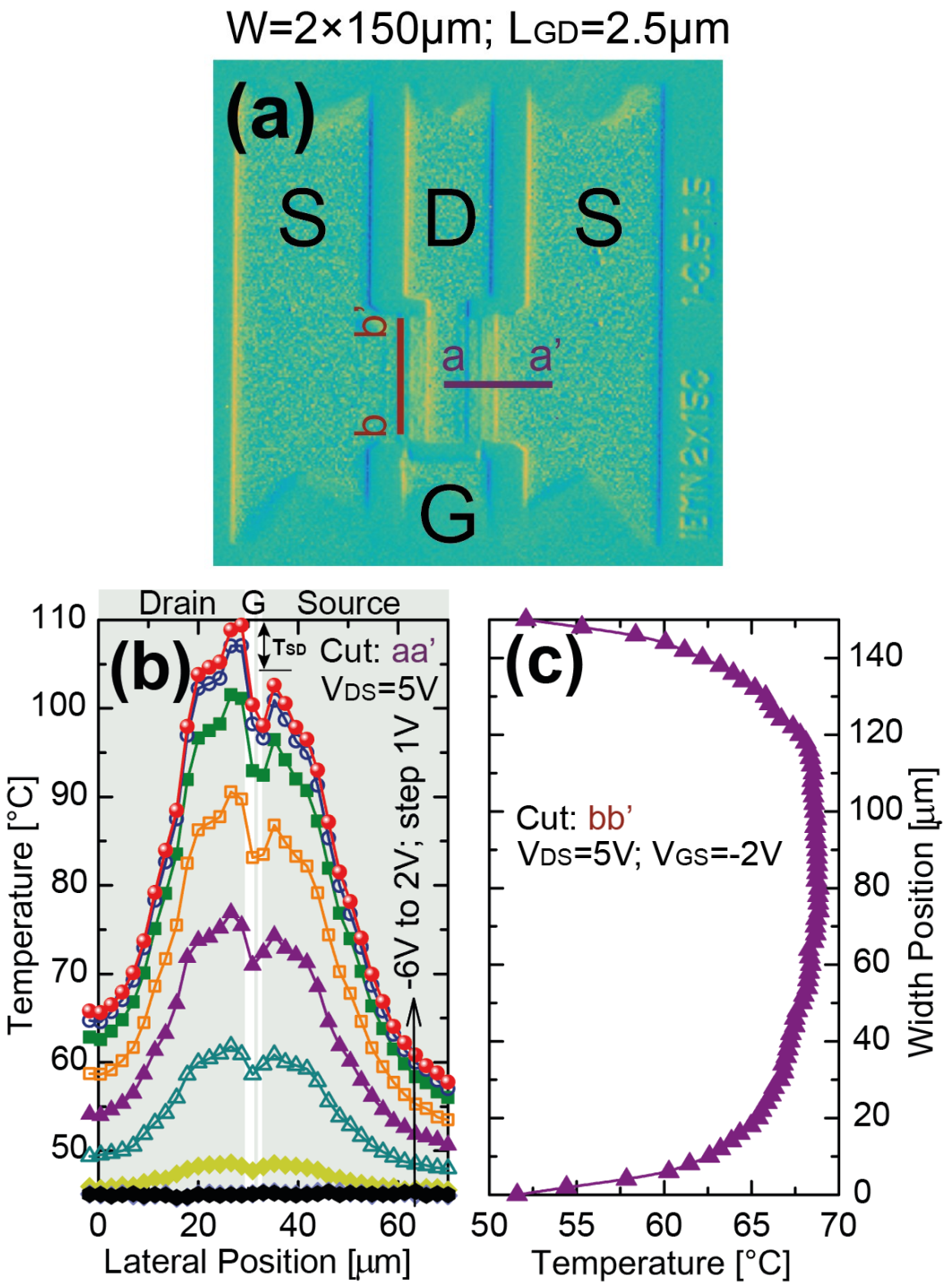

Figure 3.12: (a) Layout of two-finger gate AlGaN/GaN HEMTs. (b) Measured temperature profiles at V_{DS} = 5 V and at different gate voltages (-6 V to 2 V; step 1 V) along the lateral position (Cut: aa'). (c) Temperature distribution at V_{DS} = 5 V and V_{GS} = -2 V along the width position (Cut: bb'). The device dimensions are: L_{SG}= 1.0 µm, L_G = 0.5 µm, L_{GD} = 2.5 µm.

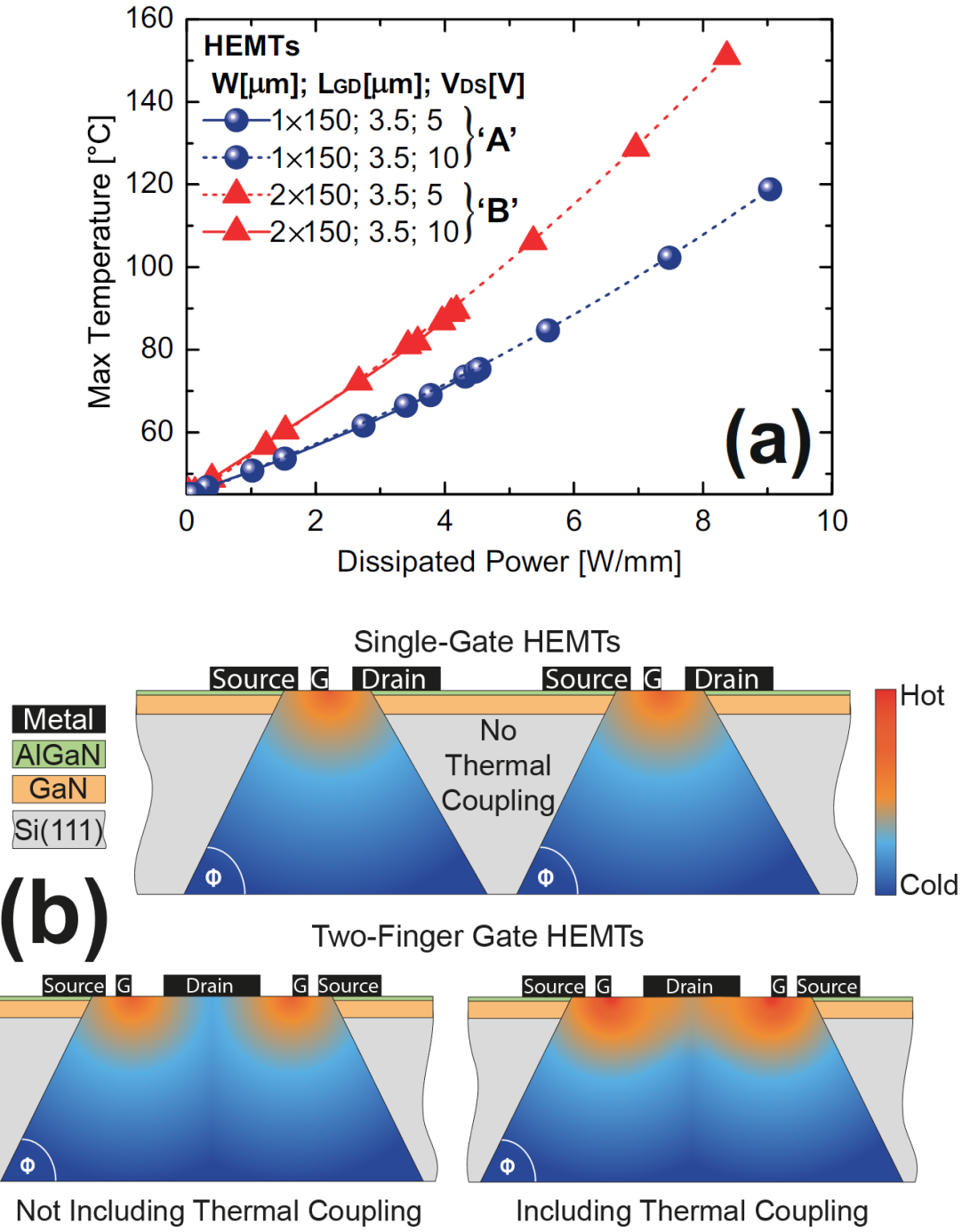

Figure 3.13: (a) Evolution of the maximum channel temperature versus the dissipated power density of single and two-finger gate AlGaN/GaN HEMTs ('A': W = 1 × 150 µm; and 'B': W = 2 × 150 µm. The device dimensions are: L_{SG} = 1.0 µm, L_G = 0.5 µm, L_{GD} = 3.5 µm. (b) Illustration of the heat spreading angle in single and two-finger gate AlGaN/GaN HEMTs.

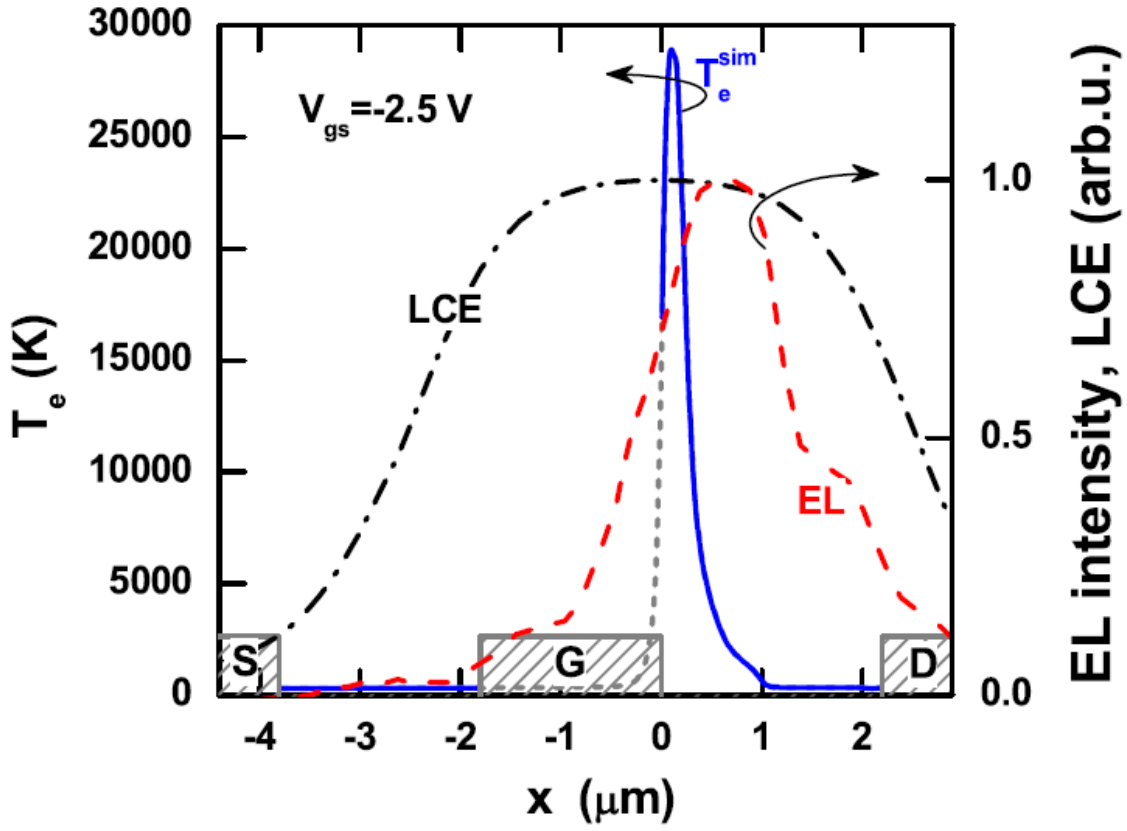

Figure 3.14: Simulated electron temperature (electron energy) distribution in an AlGaN/GaN HEMT.

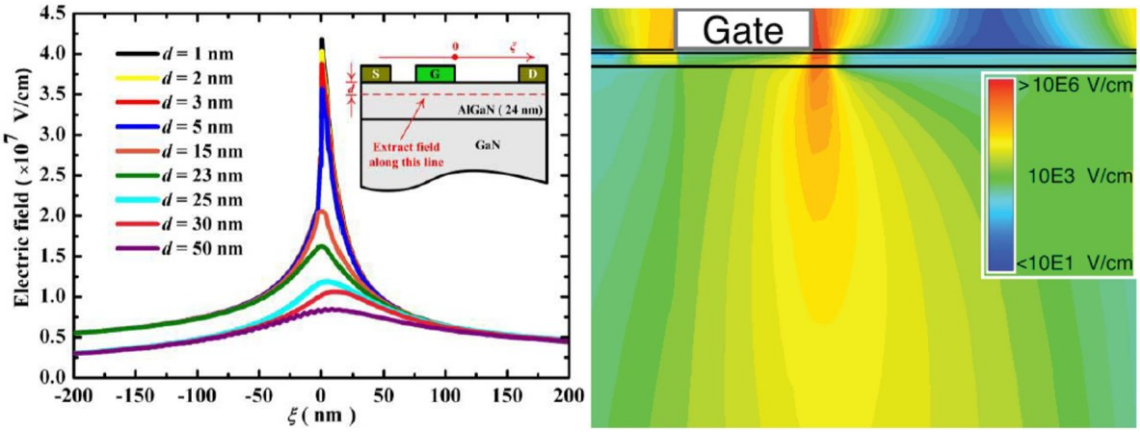

Figure 3.15: Numerical simulation of electric field distribution in an AlGaN/GaN HEMT.

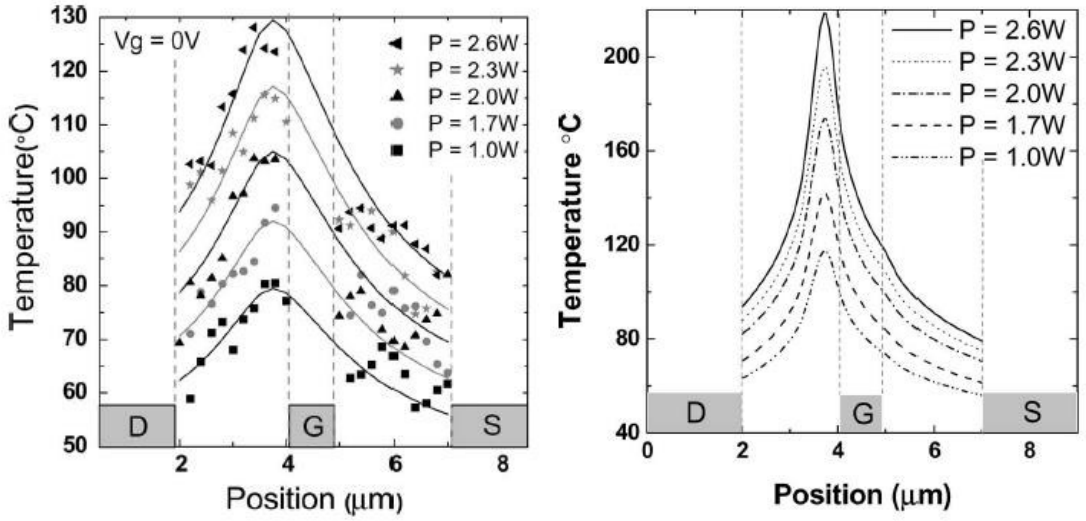

Figure 3.16: Lateral temperature profiles between source and drain contact of an AlGaN/GaN HEMT; measured using μ-Raman left, simulated right.

3.2.3.2. Thermal Management Issue

When implementing these devices into high-power system applications that require a large device density, thermal effects become an issue for the performance of these devices. As previously discussed, temperature that dissipates out of the device can increase the temperature of a neighbouring device if the temperature is high enough and the spacing between devices is too small. With large device density the accumulation of heat transfer between neighbouring devices can reduce the device performance significantly due to the large increase in temperature, thus, increasing the current collapse within each device. This shows the importance of finding solutions to reduce the self-heating within these devices whilst maintaining their high power and high frequency capabilities.

3.3. Relationship between Device Size and Polarisation in AlGaN/GaN-based Devices

The interplay of self-heating and polarisation affecting resistance is then studied in AlGaN/GaN TLM heterostructures with a scaled source-to-drain distance. This work is based on meticulously calibrated TCAD simulations against I – V experimental data using an electro-thermal model. The electro-thermal simulations show hot-spots (with peak temperature in a range of ~566 K – 373 K) at the edge of the drain contact due to a large electric field. The electrical stress on Ohmic contacts reduces the total polarisation, leading to the inverse/converse piezoelectric effect. This inverse effect decreases the polarisation by 7 %, 10

%, and 17 % during a scaling of the source-to-drain distance in the 12 µm, 8 µm, and 4 µm TLM heterostructures, respectively, when compared with the largest 18 µm heterostructure.

3.3.1. I - V Simulation Methodology

The device is simulated using TCAD simulation using an electro-thermal model. The spacing between the Ohmic contacts varies from L1 = 4 µm, L2 = 8 µm, L3 = 12 µm and L4 = 18 µm. The Ohmic contact length is LC = 50 µm for all the source-to-drain distances as depicted in Figure 3.17(a). The energy band diagram overlapped with electron concentration profile in the heterostructure cross-section is illustrated in Figure 3.17(b). The described Ti/Al/Ni/Au multilayer metallisation scheme was used for Ohmic contacts to create TLM heterostructures with various source-to-drain distances. Hall-effect measurements indicate a 2DEG electron mobility of 1950 $cm^2\ V^{-1}s^{-1}$, at room temperature. A C – V technique has revealed an electron sheet density of $n_s = 1.5 \times 10^{13}\ cm^{-2}$. The Ohmic contacts were implemented to the structures by using heavily doped GaN regions with a measured contact resistance of 0.3 Ω.mm.

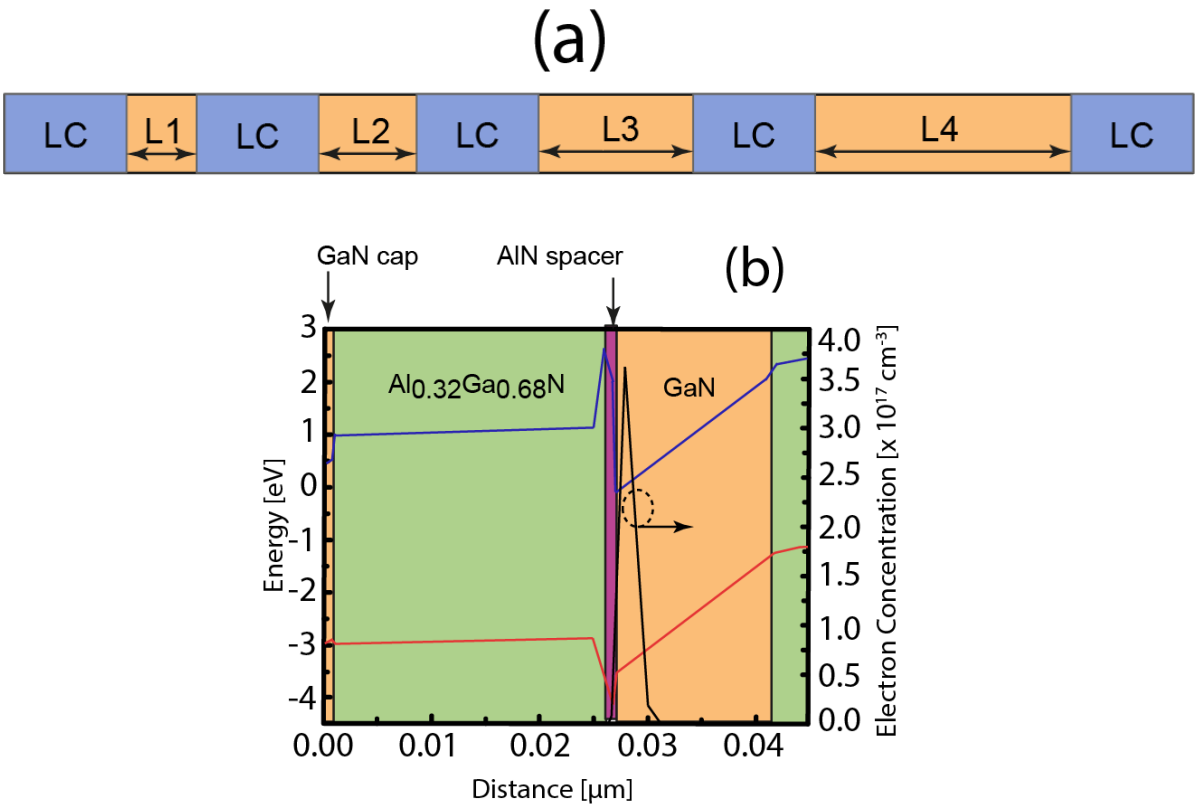

Figure 3.17: (a) Top-down view of the AlGaN/GaN TLM and (b) energy band diagram and electron concentration profile at equilibrium.

The I – V characteristics of the 100 µm wide TLM structures with the described source-to-drain distances plotted in Figure 3.18 are measured at DC and dark conditions using Agilent B1500A framework. For the shortest distance of 4 µm, the voltage applied on the contact is restricted to 15 V to prevent contacts damage, while for other spacing lengths of 8 µm, 12 µm and 18 µm, the maximum applied voltage is set to 20 V. The arrows point to bias points at which a temperature is measured at the structure (18 µm and 4 µm TLM structures only) surface close to the drain.

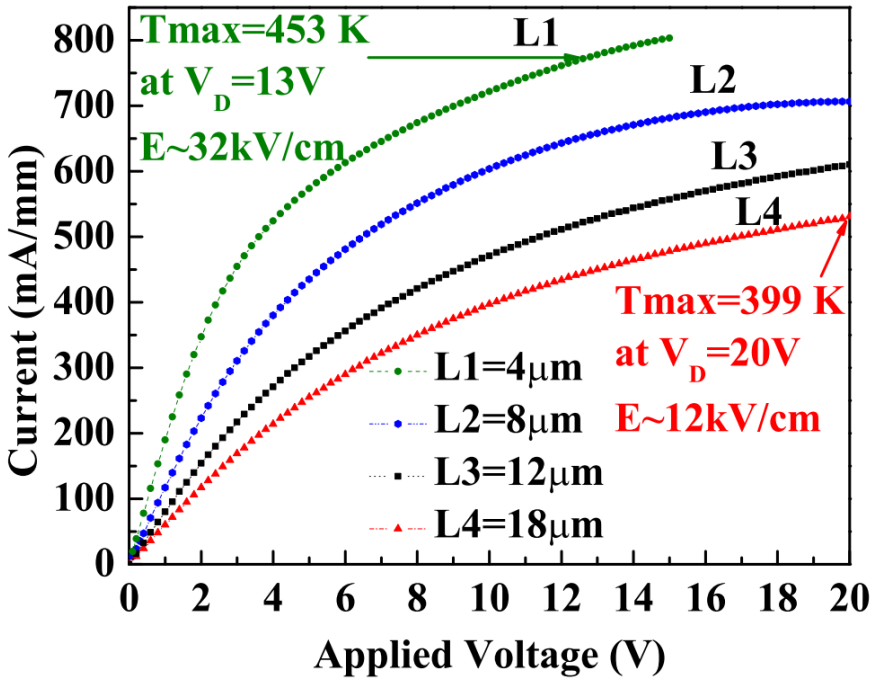

Figure 3.18: DC I – V measured characteristics of the AlGaN/GaN TLM structures. The arrows indicate the bias at which temperature of the structure shown at the given electric field is measured at the surface.

3.3.2. Electro-thermal Simulation and Calibration Methodology

The electro-thermal model used to simulate electron transport in the TLM heterostructures combines two-dimensional (2D) DD simulations with 2D heat transport model. In the calibration at a low electric field shown in Figure 3.19(a), we have used a low-field electron mobility of 1950 $cm^2\ V^{-1}s^{-1}$, a saturation velocity of 1.9×10^7 cm s^{-1} [163] within the concentration dependent mobility model, and a contact resistance of 0.3 Ω.mm. At a high electric field, a combination of the nitride specific field dependent mobility model [164] with Shockley-Read-Hall (SRH) recombination and Fermi-Dirac statistics is used. The Poisson and

current continuity equations are solved in all simulations [165]. Specifically, the low-field analytic mobility model based on Caughey and Thomas [166] and Selberherr [167] is employed in the simulation, given by:

$$\mu_n(N, T_L) = \mu_{min}\left(\frac{T_L}{300}\right)^{\alpha} + \frac{\mu_{max}\left(\frac{T_L}{300}\right)^{\beta} - \mu_{min}\left(\frac{T_L}{300}\right)^{\alpha}}{1 + \left(\frac{T_L}{300}\right)^{\gamma}\left(\frac{N}{N_{crit}}\right)^{\delta}} \quad (3.3)$$

where N and T_L are the total doping concentration and the temperature in Kelvin, μ_{max} and μ_{min} are the mobility of undoped samples, where lattice scattering plays a dominant role and the mobility of highly doped materials, where impurity scattering is the main scattering mechanism. N_{crit} is the doping concentration when the mobility reaches the average value of μ_{max} and μ_{min}, δ is a measure of how quickly the mobility changes from μ_{max} and μ_{min}, δ, β and γ are temperature dependent coefficients. The AlGaN/GaN TLM heterostructures have a background doping concentration of 1×10^{16} cm^{-3}. Carbon traps density of 1×10^{17} cm^{-3} at an energy level $E_{TC} = E_V + 0.9\ eV$ and iron traps concentration of 4×10^{18} cm^{-3} at $E_{TI} = E_V + 0.6\ eV$ are considered in the GaN buffer and $Al_{0.1}Ga_{0.9}N$ back barrier, respectively [168]. HP-Si (111) substrate is a p-type doped [169] with a concentration density of 5×10^{18} cm^{-3}. The GaN cap donor concentration was set to be 5×10^{20} cm^{-3}, which is similar to that reported in [170] with an energy level of $E_T = E_C - 0.5\ eV$ [171]. We simulate an 8 µm thickness of the Si substrate with a bottom thermal contact at T = 300 K but do not introduce additional thermal resistance at the bottom of the simulated structure. To investigate the impact of self-heating on the device performance, the temperature variations for different source-to-drain distances have been considered. The I – V characteristics of TLM structures are firstly simulated using the DD transport model without considering the self-heating effects to accurately calibrate the low-field mobility and saturation velocity [172] in the linear region of the device, where the self-heating effect is negligible. Later, self-heating effect is taken into consideration to reproduce the output characteristics as shown in Figure 3.19(b).

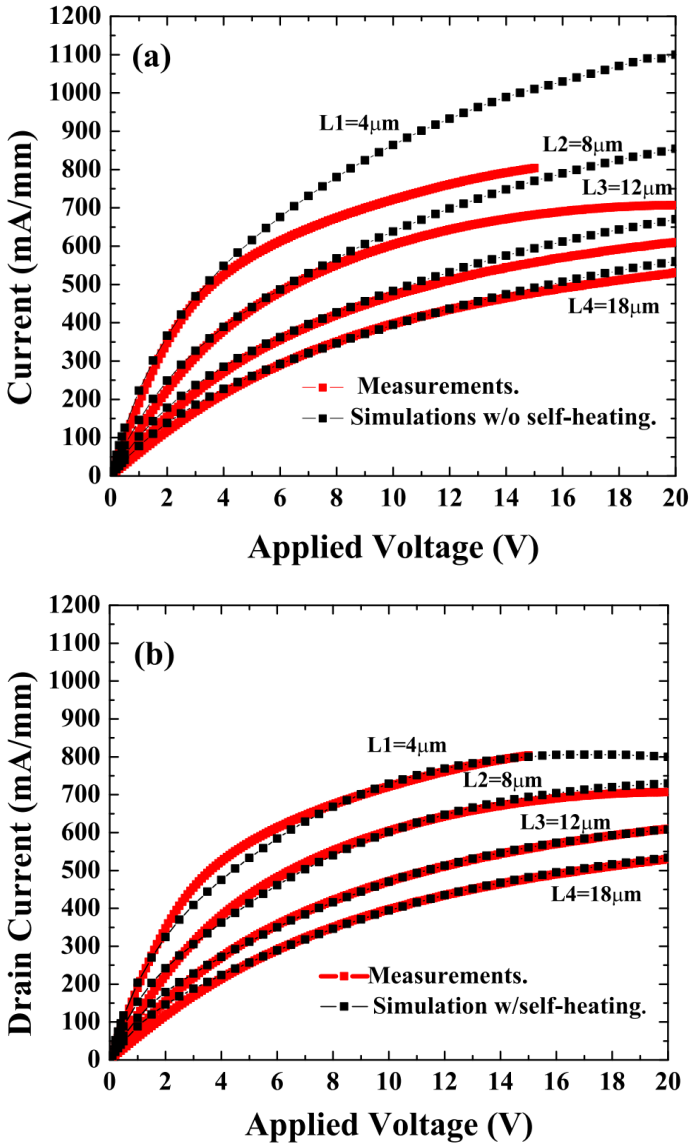

Figure 3.19: I – V characteristics of AlGaN/GaN TLM structure: (a) DD simulations of the AlGaN/GaN TLM without a self-heating effect, (b) electro-thermal (ET) simulations of the AlGaN/GaN TLM (with a self-heating effect). Note that the mobility model in the DD and the ET simulations has been calibrated at a low-electric field only.

The thermal modelling is activated by Giga module accounting for lattice heat flow in the device [173]. The used values of thermal conductivity of the different layers were taken from [174], [175]. Giga module in Atlas [165] solves the lattice heat flow equation in addition to the DD and Poisson equations making the overall simulations to be electro-thermal. The heat flow equation is given by:

$$C\frac{dT_L}{dt} = \nabla(\lambda \nabla T_L) + H \tag{3.4}$$

where C denotes the heat capacitance per unit volume, λ is the thermal conductivity of the respective materials, H is the heat generation term, and T_l is the local lattice temperature. Thermal conductivity for GaN and AlN has been fit against measured experimental data as presented in Figure 3.20. Here, we have used a power function in the form:

$$\lambda(T_L) = \alpha_\lambda \left(\frac{T_L}{300}\right)^{-\beta_\lambda} \tag{3.5}$$

To fit a dependence of thermal conductivity on temperature with experimental data [174] for GaN and AlN [175] shown in Figure 3.20, respectively, that have been used in the simulations. α_λ and β_λ are the respective fitting coefficients for GaN and AlN summarised in Table 3.1 The heat generation term is given by the equation [173]:

$$H = \left[\frac{|\overrightarrow{Jn}|^2}{q\mu_n n} + \frac{|\overrightarrow{Jp}|^2}{q\mu_p p}\right] + q(R - G_c)$$
$$\left[\varphi_p - \varphi_n + T_L(P_p - P_n)\right] - T_L\left(\overrightarrow{Jn}\nabla P_n + \overrightarrow{Jn}\nabla P_p\right) \tag{3.6}$$

where $|\overrightarrow{Jn}|$, $|\overrightarrow{Jp}|$ are the current densities of electrons and holes, μ_n, μ_p are the mobility of electrons and holes. n, p are the electron and hole concentrations; φ_n, φ_p are the quasi-fermi levels of electrons and holes; P_n, P_p are the thermoelectric powers of electrons and holes, R is the bulk recombination rate of carriers; G_c is the carrier generation rate; T_L is the local lattice temperature; and q is elementary charge of an electron.

Table 3.1: The fitting coefficients for GaN and AlN used in the relation (3.2). Note that the coefficient α_λ has units of W/mK while β_λ is unitless.

Materials	Coefficient (α_λ) [W mK^{-1}]	Coefficient (β_λ)
GaN	2.2132	1.447
AlN	2.83	1.529

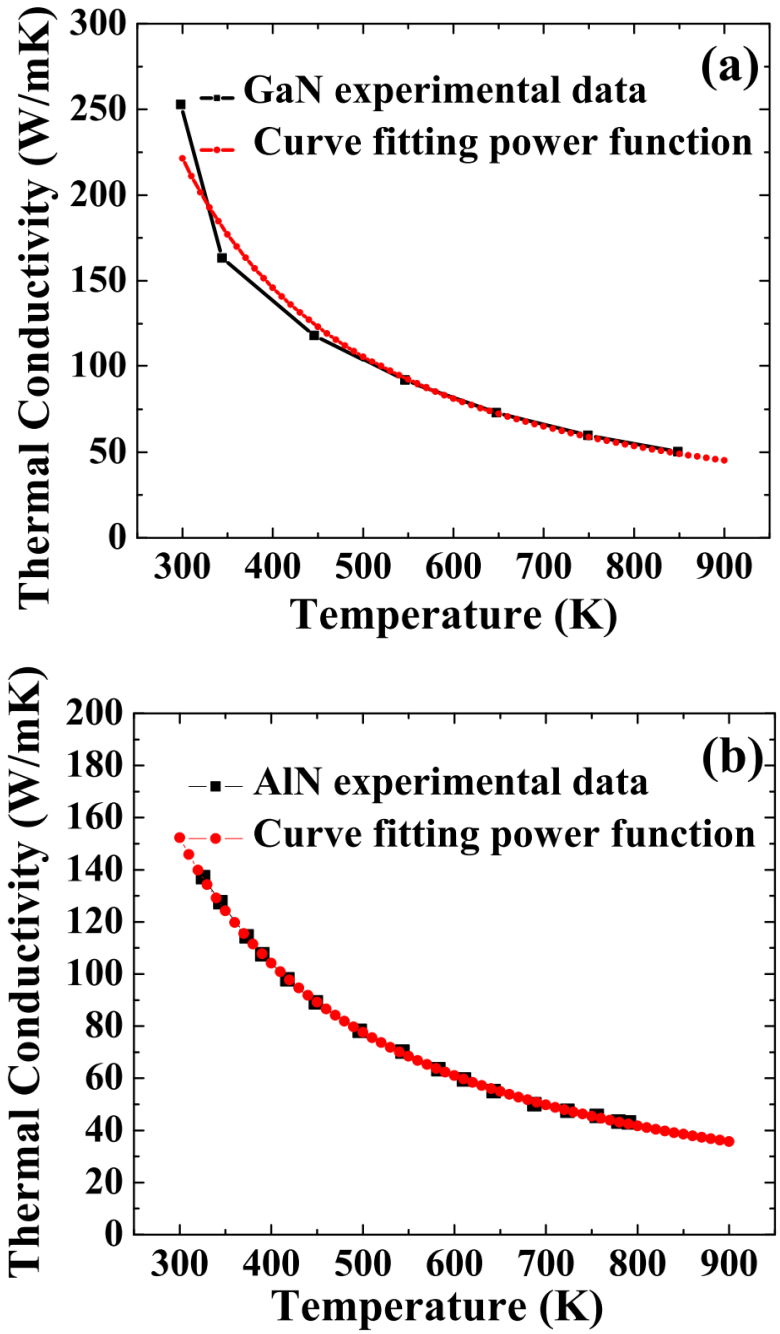

Figure 3.20: Thermal conductivity as a function of temperature compared with a fitting power function for (a) GaN [174] and (b) AlN [175].

3.3.3. The Role of Self-Heating and Polarisation

Figure 3.19(a) presents the calibration of the TLM structure against the experimental measurements without self-heating. A larger difference between the measurement results and the simulations, that is caused by the self-heating effect, is seen for the shortest contact spacing

of L1 = 4 µm at V_{DS} = 20 V. The difference between the experimental measurements and the simulation data reduces when the source-to-drain distance increases. Figure 3.19(b) compares the simulation results obtained from electro-thermal simulations, while using the calibration of thermal conductivity from Figure 3.20. A stronger self-heating effect is observed for the shortest source-to-drain distance TLM, L1 = 4 µm, when compared with longest TLM, L4 = 18 µm. This is due to the higher electric field between the contacts in the shortest TLM compared with larger TLMs. The drain current reduction occurs due to mobility degradation caused by the self-heating. The simulation agreement improves as the distance between the source and drain is increased as expected so a very good agreement between simulation results and measurement data can be observed.

The lattice temperature profiles in the 2DEG along the channel and its 2D distributions for all the structures (L1, L2, L3, and L4) are presented in Figure 3.21 and Figure *3.22*, respectively. When the spacing between the source and the drain decreases, which increases the electric field at the vicinity of the drain [176] in a TLM structure, the lattice temperature increases and hence degrades the transport properties [140]. The GaN channel temperature increase is due to more

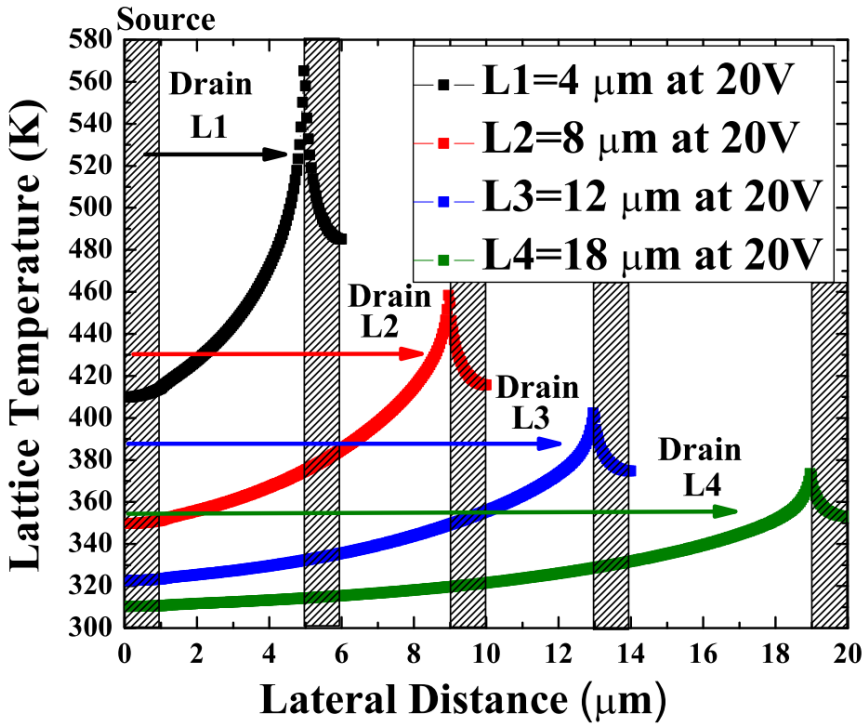

Figure 3.21: Lattice temperature profiles in the 2DEG along the channel for different source-to-drain distances at V_{DS} = 20 V.

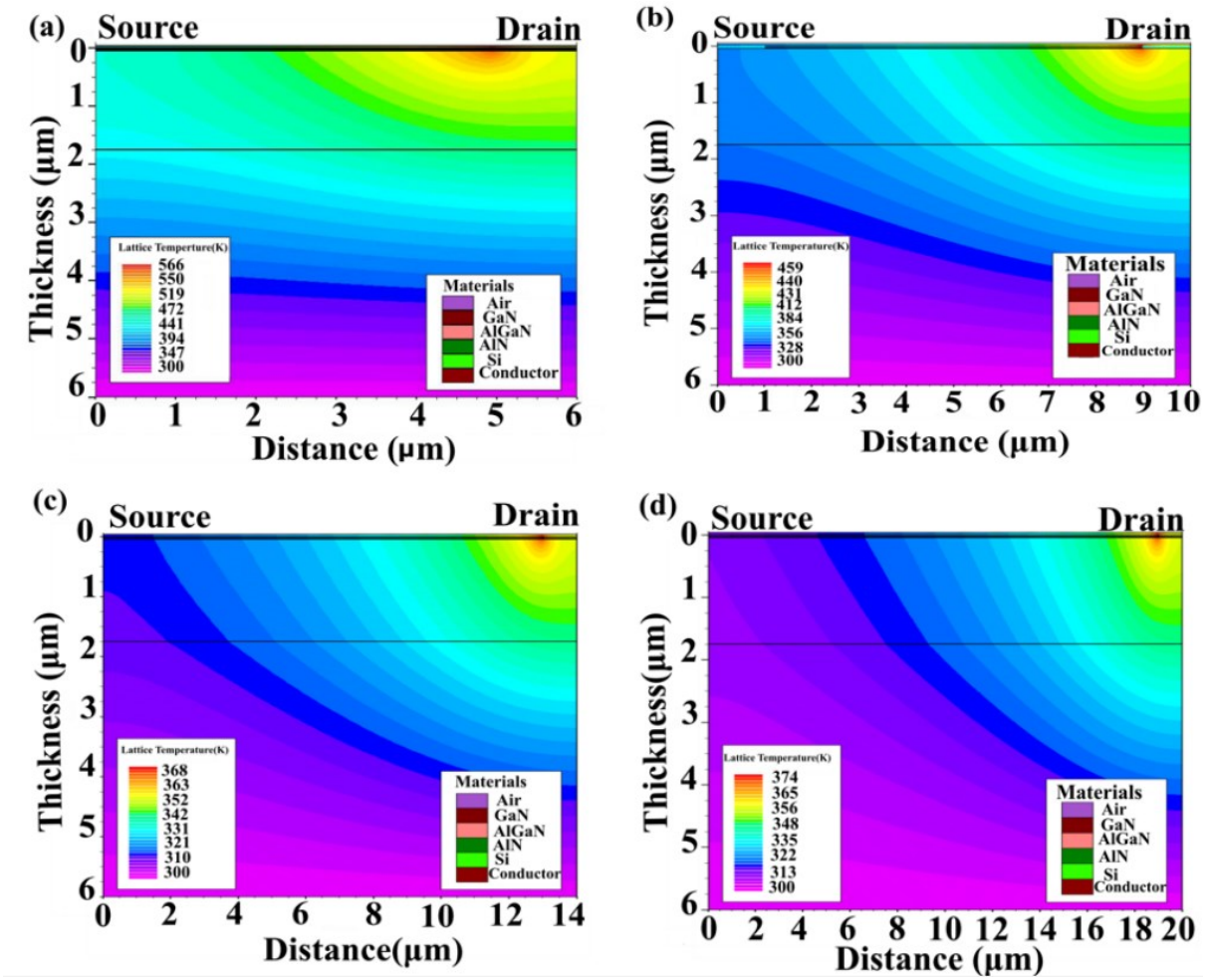

Figure 3.22: 2D Lattice temperature distributions for TLM heterostructures with a source-to-drain distance of (a) L1 = 4 µm, (b) L2 = 8 µm, (c) L3 = 12 µm, and (d) L4 = 18 µm, at applied biases of 20 V.

energetic carriers in the channel with a larger kinetic energy accelerated by the increasing electric field [140], [177], [178]. The hot spot is located next to the drain contact for all structures [179]. At an applied drain-to-source bias of 20 V, the shortest structure (L1 = 4 µm) exhibits a peak lattice temperature of 566 K which is reported similarly in [177]. When the source-to-drain distance increases to 8 µm (L2), a peak of lattice temperature decreases to 459 K in the structure and then to 403 K and to 374 K in the 12 µm and 18 µm structures (L3 and L4). The hot spot remains at the drain side for all TLM structures [180], [181]. The maximum simulated lattice temperature of 374 K at applied bias of 20 V in the 18 µm TLM structure is in a reasonable agreement (~7 %) with a measured temperature of 399 K indicated in Figure 3.18. In the smallest, 4 µm TLM structure, the simulations give a lattice temperature of 434 K

at applied bias of 13 V (used in the experiment) which is also in a good agreement (~4 %) with experimentally measured temperature of 453 K (Figure 3.18).

The drain current in the largest TLM structure with a drain-source distance of L4 = 18 µm is compared against the scaled structures at an applied voltage V_{DS} = 15 V excluding and including the self-heating effects. The self-heating effect has a very small impact on the current of the 18 µm TLM structure. When the distance between the source and drain contacts is reduced to L3 = 12 µm, the drain current increases by 31.7 % (self-heating included) and by 40.7 % (self-heating excluded). With further scaling of the distance between the source and drain contact to L2 = 8 µm, the drain current increases by 61.7 % in the simulation with self-heating and 88 % without self-heating. Finally, for the shortest TLM structure of L1 = 4 µm, the drain current increases by 109.6 % with self-heating included and by 210.9 % with self-heating excluded in the simulation as compared to the largest TLM structure (L4 = 18 µm), which serves here as a reference to the comparison. When applying an external electrical stress on the TLM structure (applied voltage) via contacts, the wurtzite crystal structure of III-Nitrides suffers from the stress. This affects the polarisation along with different spacing

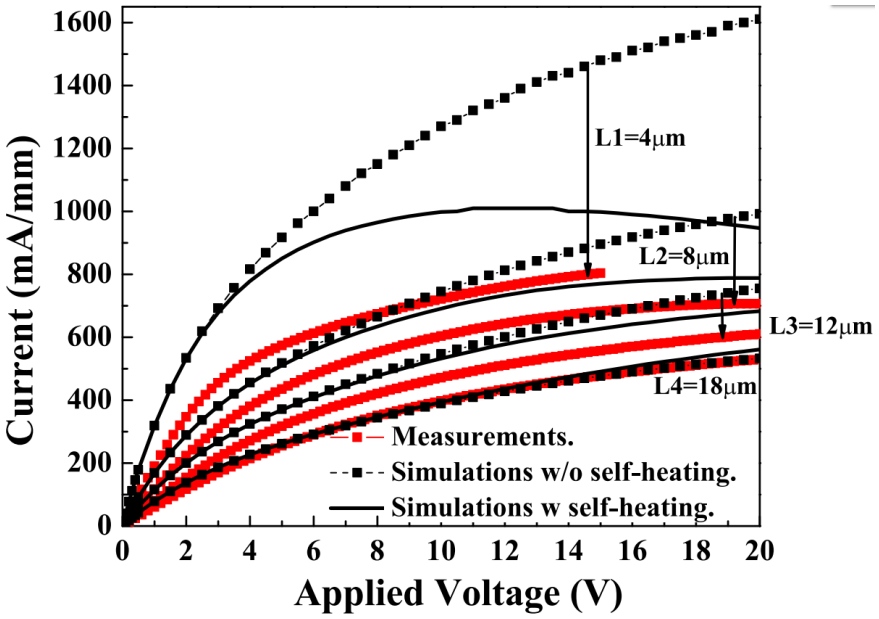

Figure 3.23: Measured I – V characteristic of TLM structure (red lines) plotted against the hypothetical low-field calibrated results. The black dashed lines represent the simulations without self-heating while the black solid lines are the simulation results including self-heating effects. In all simulations, the polarisation value of the largest structure (L4 = 18 µm) is used.

between the contacts. This phenomenon is known as the inverse or converse piezoelectric effect [181], [182]. To study this phenomenon, we altered the polarisation factor for TLM structures to mimic the electrical stress that is applied after each measurement thus changing the total value of polarisation. Figure 3.23 illustrates hypothetical I – V characteristics if the polarisation factor would be fixed at a value calibrated for the TLM structure with L4 = 18 µm, the largest source-to-drain distance. By applying this value on L1 = 4 µm, the drain current has increased by 66.8 % in the simulation, which clearly disagrees with experimental observations.

Electrical and mechanical strain/stress and its relationship with the electric field in GaN HEMTs has a tremendous impact on GaN based devices in general [181]. Nitride materials like GaN which have unique properties due to the lack of inversion symmetry and high iconicity exhibit inverse/converse piezoelectric effect due to strain/stress generated by the electric field [183]. When applying an external electrical and mechanical stress on the TLM structure via contacts (applied voltage), the wurtzite crystal structure of III-Nitrides suffers distortion and deformation from mechanical stress on GaN and AlGaN layers. This affects the polarisation along with different spacing between the contacts. The electrical stress caused by an applied voltage on Ohmic contacts induces a lattice deformation at the vicinity of the drain as illustrated in Figure 3.24. The total polarisation value decreases when compared to the largest contact of 18 µm for 12 µm, 8 µm, and 4 µm by 7 %, 10 %, and 17 %, respectively.

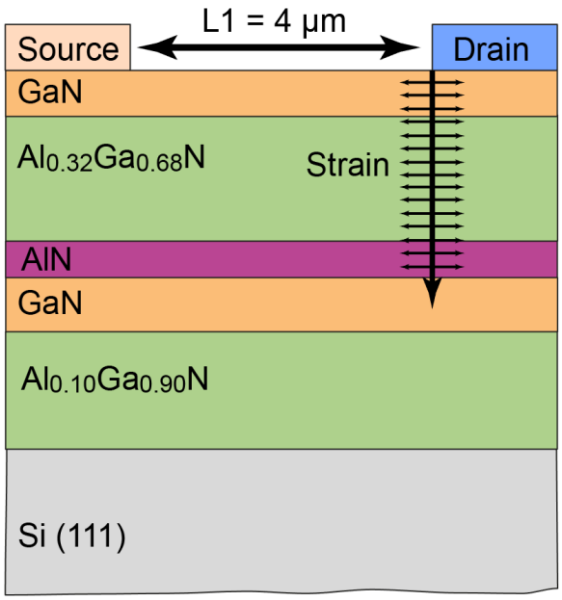

Figure 3.24: Schematic diagram of the TLM structure that illustrates the strain induces by applied electrical stress.

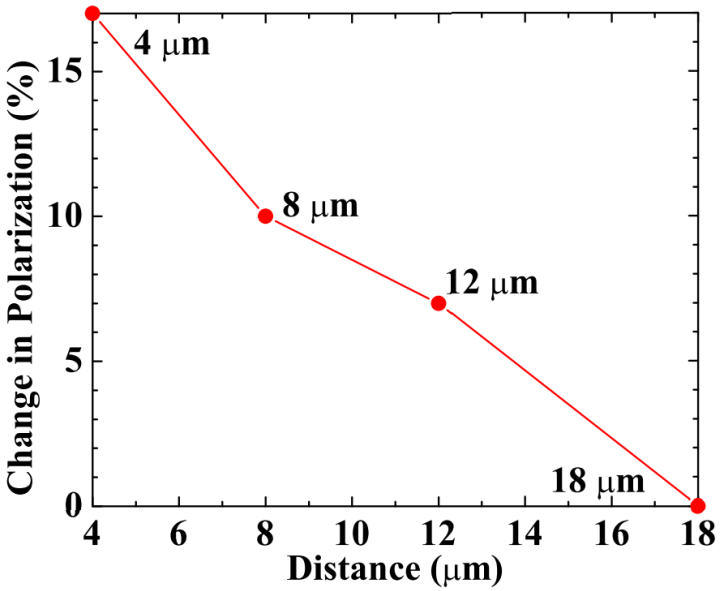

Figure 3.25: The total polarisation value decreases when compared to the total polarisation used in the largest 18 μm TLM structure.

Finally, the relationship between the change in polarisation and the source-to-drain distance is almost linear, as shown in Figure 3.25.

3.4. Summary

Infrascope temperature mapping system measurements have shown a large increase in temperature at the S/D contacts of AlGaN/GaN-based devices at operating conditions. Temperature coupling of a high conductivity tensile region to the lower conductivity regions is responsible for the temperature rise observed in both short and long gateless devices. The thermal coupling also enhances the peak of temperature at the end of the gate in the AlGaN/GaN HEMTs. In addition, the HR-XRD measurement supported by DD simulations have revealed that the change of the strain at the vicinity of S/D Ohmic contacts, due to a difference in expansion coefficients of III-N and S/D metallisation, is the reason behind this temperature rise.

We have studied $Al_{0.32}Ga_{0.68}N/AlN/GaN/Al_{0.1}Ga_{0.9}N$ TLM heterostructures with a GaN cap layer grown on a p-type doped HP-Si (111) substrate. Their I – V characteristics from experimental measurements were simulated via a 2D drift-diffusion transport model using Fermi-Dirac statistics and the SRH recombination model by commercial tool Atlas-Silvaco [184]. A thermal model was employed to study the self-heating effects with the thermal

conductivity approximated by a power function and calibrated to experimental data. We have found that the current soon becomes limited by increase in a lattice temperature with the increase in applied bias up to 13% (the 4 µm structure) and that this limitation occurs sooner in shorter structures. We have demonstrated a good agreement of the electro-thermal simulations predicting a lattice temperature of 374 K against experimental temperature of 399 K at applied bias of 20 V in the largest, 18 µm structure as well as in the smallest, 4 µm structure, predicting a lattice temperature of 434 K against experimental temperature of 453 K at applied bias of 13 V. The maximum lattice temperature for each TLM was predicted in the vicinity of the drain, when constant strain profile is assumed. In addition, we have observed that the total polarization value in heterostructure reduces when compared to the largest contact distance of 18 µm for 12 µm, 8 µm, and 4 µm by 7 %, 10 %, and 17 %, respectively. This decrease in the total polarization is due to the inverse piezoelectric effect, or also called the converse piezoelectric effect, caused by the additional stress induced by the applied electric field on contact. The inverse piezoelectric effect changes the total polarization thus affecting a 2DEG density in the channel [185]–[187].

CHAPTER 4

A PARAMETRIC TECHNIQUE FOR TRAP CHARACTERISATION IN AlGaN/GaN-BASED DEVICES

This chapter is dedicated towards the development of a parametric technique for characterisation of bulk and surface trapping mechanisms in AlGaN/GaN-based devices. There is a widespread agreement that both self-heating and charge trapping are contributing factors in transient current degradation [188]–[191], which has led our study towards investigating the kinetics of charge trapping mechanisms. Our focus lies within gaining insight into analysing the degradation of both source and drain transient current with the complete exclusion of self-heating and under normal device operation. We use the knowledge gained in Section 2.2.6.3, describing the physical mechanisms of both bulk and surface trapping, to contribute towards the understanding of our analysis. In the coming sections: the equipment used to perform measurements and the hardware calibration is detailed; the influence that electrostatic potential has on charge trapping is investigated; the mechanisms of bulk and surface trapping under various biasing conditions is analysed; and the influence that surface trapping has on current degradation compared to self-heating is investigated.

4.1. Degradation of Current Misconceptions

Several studies investigating the current degradation in AlGaN/GaN HEMTs have resulted in differing conclusions [192]–[194]. It is widely agreed upon that transient current degradation involves self-heating and charge trapping [188]–[191]. Some studies of transient drain current suggest that two mechanisms of current degradation of different time constant in AlGaN/GaN HEMTs are caused by both bulk and surface trapping [192], [193]. Other investigations suggest that the two current degradation trends are proportional to self-heating effects that occur at two different times in AlGaN/GaN HEMTs [194]. With the significant impact of the current degradation time constant and magnitude on device reliability and RF performance, it is vital to address its mechanisms and kinetics.

Based on the works of [192], [193], the research fails to sufficiently exclude self-heating mechanisms or, at least, provide proof that self-heating is a negligible degradation mechanism. Although these works are more applicable than the commonly used deep-level transient spectroscopy (DLTS) [195], trap properties are gathered through an adaptation of DLTS and the issue of not excluding self-heating persists. The techniques used in these works are to identify the current transient time-constant spectra using pulse measurements under the assumption that the change in current stems from the change in trapping in the device alone. It

is stated that the current collapse is strictly related to charge trapping at deep levels that are generated through electrical and thermal stress within the device. An example of the results found by using this methodology are given in Figure 4.1(a), whereby the transient current is measured under ON-state conditions, e.g. $(V_{GM}; V_{DM})$ = (1 V; 2 V), with particular quiescent OFF-state biasing conditions, e.g. $(V_{GF}; V_{DF})$ = (-6 V; 27 V). Then, shown in Figure 4.1(b), the differential of the transient current measurements $(\partial I_{DS}/\partial log_{10}(t))$ is calculated to show

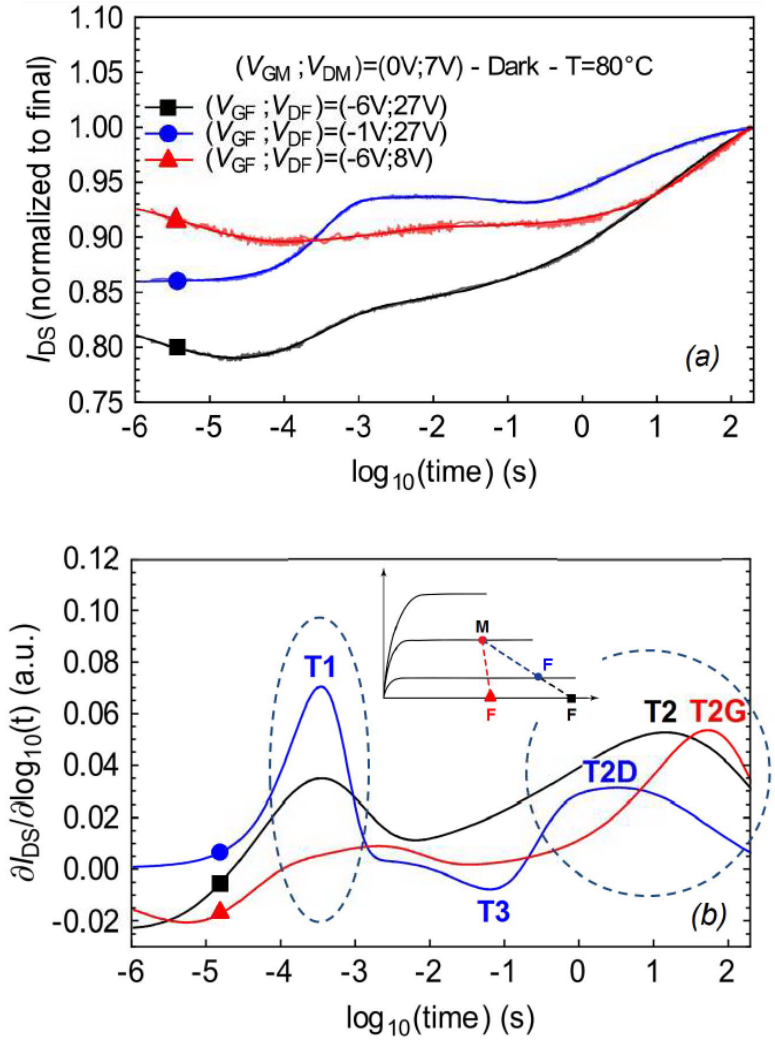

Figure 4.1: (a) Drain current transients recorded after different trapping conditions and (b) related differential signals: T1 amplitude is enhanced by the combination of drain voltage and drain current experiencing his maximum after semi-on trapping condition, whereas broad T2 spectrum is composed by one drain-influenced component (T2D) and one gate-influenced component (T2G). Finally, T3 is a detrapping process [200].

several peaks in the differential signal. According to this work, the peaks are described as the degradation in current due to the time dependent trapping processes; i.e. bulk trapping is T1, surface and second bulk trapping is T2 and detrapping is T3. Although this may be true for devices operating at low power, this still does not answer the question of how trapping can be decoupled from self-heating under normal device operation.

The works of [194] ignore the trapping processes and focus on the cause of current degradation to be self-heating. To measure the temperature within the device, they monitor the changes in the forward Schottky gate voltage $(|\sigma V_g|)$ of several Schottky diodes that are placed on top of the wafer and at different distances away from the device. By applying a low enough test current through the Schottky diodes to avoid self-heating, the transient change in $|\sigma V_g|$ is measured when the device is set to the active region. Apparently, $|\sigma V_g|$ changes linearly with temperature rise. As a result, it is observed by this work that the two temperature rises occur, as seen in Figure 4.2. Although this may be true, it neglects any analysis of transient current degradation within the device as a result of both self-heating and charge trapping together.

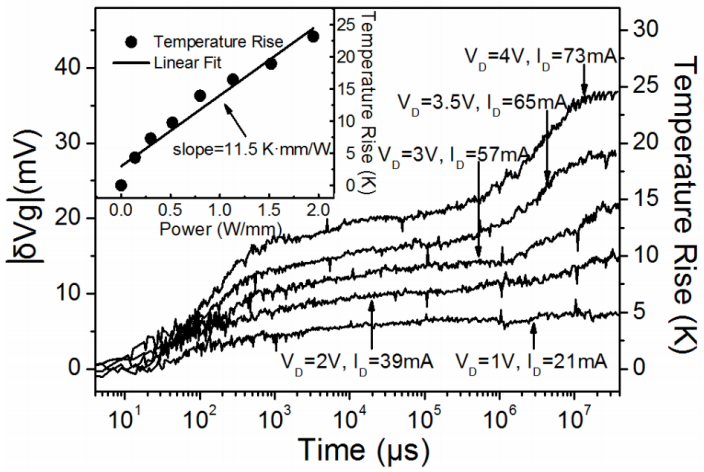

Figure 4.2: Transient temperature rise curves of the device under different electrical bias conditions. (inset) relationship between temperature rise and power density [194].

4.2. Self-Heating Model

Self-heating is a fundamental reliability issue in AlGaN/GaN-based devices. As AlGaN/GaN-based devices typically operate at high power (> 2 W/mm), maintaining high performance and reliability is a significant challenge. This is particularly true given how quickly the increase in

temperature occurs with respect to time, as described in Section 2.2.6.3. Therefore, to begin our investigation into characterising the degradation mechanisms within AlGaN/GaN HEMTs we model the thermal behaviour within the device. In particular, we use the RC thermal model provided by [194], [196]. The described RC thermal model used to extract the self-heating characteristics, provided in Figure 4.3, is given as:

$$\Delta T(t) = P_{DISS} \times \sum_{i=1}^{n} R_{TH,i}\left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{4.1}$$

Where $\Delta T(t)$ is the temperature rise with respect to time, P_{DISS} is the dissipated power, $R_{TH,i}$ is the thermal resistance at the i-th stage of the Foster RC network. Additionally, $\tau_i = R_{TH,i} \times C_{TH,i}$ is the thermal time constant, where $C_{TH,i}$ is the thermal capacitance at the i-th stage of the Foster RC network. The first stage of i defines the thermal parameters where the temperature has not thermally coupled, occurring during a short period. The second stage of i defines the thermal parameters for when the temperature has thermally coupled through (i) coupling of heat from source, gate and drain peaks, and (ii) heat that is diffused back into the device at the semiconductor/substrate interface. This second stage takes a longer time due to

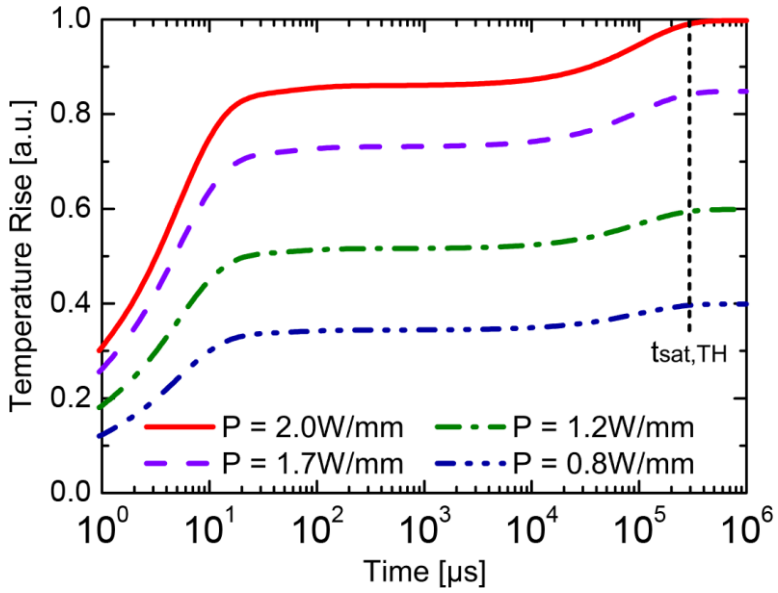

Figure 4.3: Transient heating characteristic at various power densities (P) using the RC thermal model [194], [196].

Table 4.1: Parametric values applied to RC Thermal Model.

i	$R_{TH,i}$ [Ω]	τ_i [s]
1	0.32	300 n
2	1	5 µ
3	0.05	50 µ
4	0.22	100 m

the thermal diffusion process. The calculated transient temperature at different dissipated power (0.8, 1.2, 1.7 and 2.0 W mm^{-1}) is shown in Figure 4.3. The $R_{TH,i}$ and τ_i parameters used for the calculation of Equation (4.1) is given in Table 4.1. We observe two time constants of self-heating mechanisms, at 1 ms and $t_{sat,TH} = 1$ s. It is important to note that regardless of the power applied, the temperature time constant ($t_{sat,TH}$) is unchanged.

4.3. Electrostatic Trapping

The impact of trapped charges on the device electrostatic, described as the charge trapping that occurs as a result of changing an applied voltage, is first investigated. In order to induce electrostatic trapping with no self-heating and hot carrier injections, the pulse waveform shown in Figure 4.4 has been applied to the source (V_S) and drain (V_D) terminals of a TLM ($L_{SD} = 8$ µm). This provides low $V_{DS} = V_D - V_S$, to negate self-heating effects and high V_D, V_S, to induce electrostatic trapping. V_S and V_D are given in respect to the ground, 0V, of the used semiconductor analyser framework.

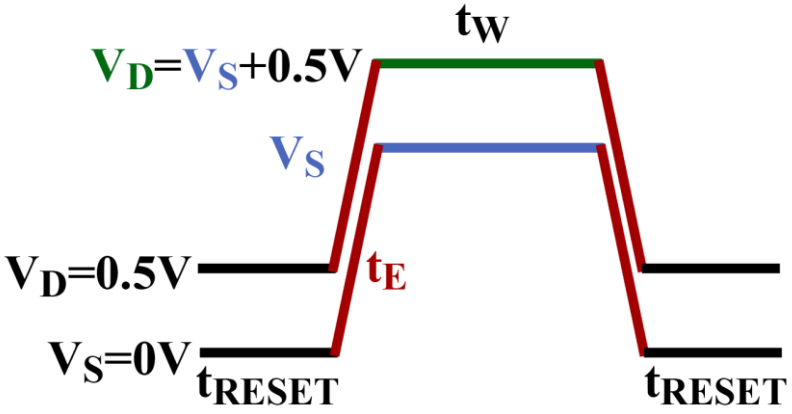

Figure 4.4: Voltage waveforms applied on source (V_S) and drain (V_D) terminals for characterising

electrostatic trapping; where t_{RESET} = 10 s, t_E = 200 ns, and t_W = 1 s.

The resulting transient I_D at different V_S are presented in Figure 4.5. The degradation of I_D is caused by the amount of trapped charges under different V_S and V_D conditions, where V_{DS} is constant. The trapping process is completed within a few micro seconds, independently of the applied voltages. In contrast to the trapping, the discharge mechanism is very slow. It takes a few milliseconds for the trapped charges to begin discharging. It is very important to note that minimal variation of I_D is observed between 10 µs and 1 ms. From this figure, we can observe that the trapped charge can impact the device electrostatic quite significantly.

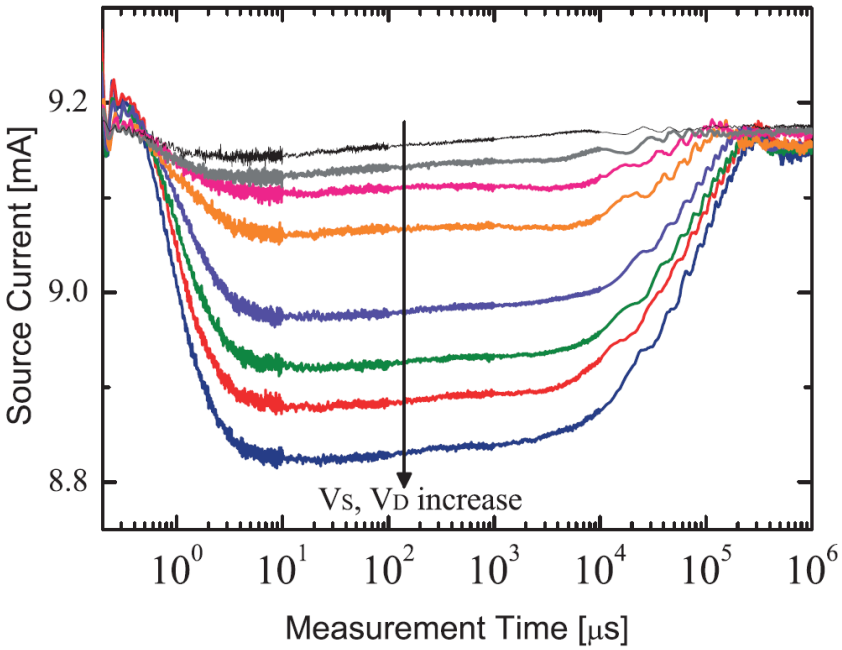

Figure 4.5: Transient I_D at different V_S (from 1 V to 9 V; step = 1 V) showing the impact of the trapped electrons on the electrostatic. The experiment conditions and used pulse waveform are summarised in Figure 4.4.

4.4. Device and Instruments

4.4.1. Device Performance

The investigated epi-structures of the AlGaN/GaN TLM and HEMT were grown via MBE on HP-Si (111) substrate of a resistivity of 2000 Ω.cm, Figure 4.6(a) and (b), respectively. The AlGaN/GaN TLM consists, from the substrate to the top, of low-temperature AlN/GaN/AlN (250/250/40 nm) nucleation layers, a 1.7 µm $Al_{0.10}Ga_{0.90}N$ back-barrier to reduce alloy

scattering and to improve the carrier confinement of the 2DEG. A channel is made of a 15 nm thick unintentionally doped GaN buffer followed by a 25 nm undoped $Al_{0.32}Ga_{0.68}N$ barrier and, finally, a 1 nm GaN cap layer. Room temperature Hall measurements yields a sheet resistance of $R_{\square}$ 398 Ω sq^{-1}. The CV-technique revealed an electron sheet density of 1.5 × 10^{13} cm^{-2}.

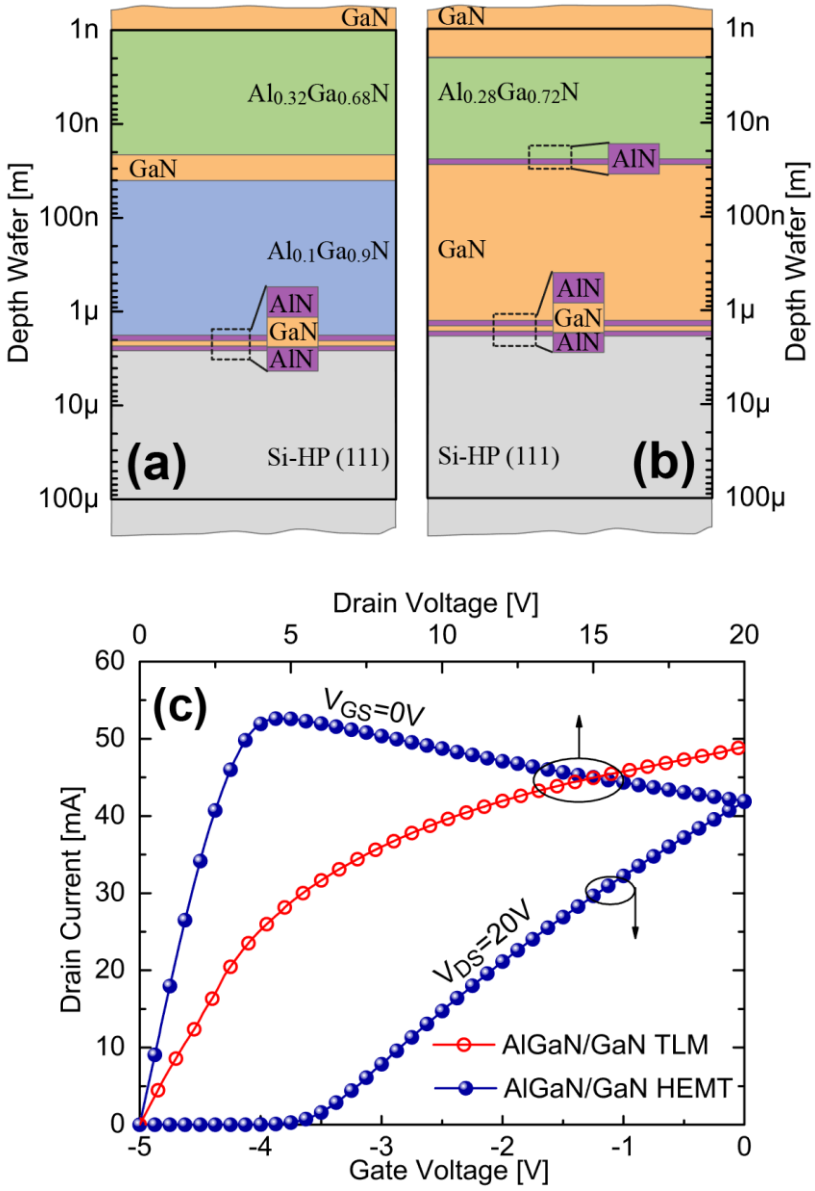

Figure 4.6: Schematic cross-section of the epi-structures grown on Si-HP (111) substrate for AlGaN/GaN (a) TLM and (b) HEMT. The source-to-drain distance and device width are 5 µm and 100 µm, respectively. (c) I_{DS} - V_{DS} and I_{DS} - V_{GS} characteristics at V_{GS} = 0 V and V_{DS} = 20 V, respectively, of the used AlGaN/GaN HEMT.

The investigated epi-structure of the AlGaN/GaN HEMT was also grown by MBE on HP-Si (111) substrate, as shown in Figure 4.6(b). MBE was performed using NH_3 for the Nitrogen precursor. The HEMT structure consists, from the substrate to the top, of low-temperature AlN/GaN/AlN (250/250/40 nm) nucleation layers, a 1.1 µm GaN back-barrier and 1 nm AlN exclusion layer to reduce alloy scattering and to improve the carrier confinement of the 2DEG. A 25 nm undoped $Al_{0.28}Ga_{0.72}N$ barrier and, finally, a 1 nm undoped GaN cap layer. Room temperature Hall measurements yields a sheet resistance of $R_{\square}$ = 340 Ω/sq, an electron sheet density of 1.25×10^{13} cm^{-2}, electron mobility of 1480 cm $V^{-1}s^{-1}$, and dislocation density of ~$5\times10^{9}cm^{-2}$. The gate metallisation scheme is Ni/Pt/Ti/Mo/Au (5/25/25/30/250 nm), where Ti/Al/Ni/Au (10/200/40/100 nm) multilayers were used for the source and drain terminals. The contact resistance and specific resistivity are 0.39 Ω.mm and 3.8×10^{-6} $\Omega.cm^2$, respectively. The fabrication process flow is similar to that in [107] with additional Si_3N_4 passivation. The I_{DS} – V_{DS} at V_{DS} = 20 V and I_D – V_G at V_{GS} = 0 V characteristics of the used AlGaN/GaN TLM and HEMT are plotted in Figure 4.6(c).

4.4.2. Device Reset Conditions

At high voltages, e.g. V_{DS} = 20 V, both self-heating and charge trapping occur within the device. It takes some time for the device to cool down and trapped charges to discharge after a high voltage pulse has been applied. To ensure each measurement on the device can be carried out under identical conditions, electrical reset/refresh condition is required to be applied to the device between each measurement that is taken. Otherwise, heat and trapped charges that have not recovered will influence the measurements on the following experiments.

The waveform shown in the Figure 4.7 has been applied on the source and drain terminals for different pulse widths ranging from 300 µs up 1 s. It is found that V_S = 0 V and V_D = 0 V needs to be applied before each measurement for a period of time, t_{RESET} > 10 s, in order to fully recover the device from degradation mechanisms (self-heating and charge trapping) that would cause an unwanted influence on further measurements. Figure 4.8 shows 20 repeated measurements of this pulse waveform (cycles) for AlGaN/GaN (a) TLM and (b) HEMT. No change occurs in initial current or trend of current degradation over time with each cycle of the measurement. The advantage of this reset technique is much easier to control compared to the commonly used device reset using light/dark conditions due to there being less variability that

can cause error; e.g. light intensity and time, dark time.

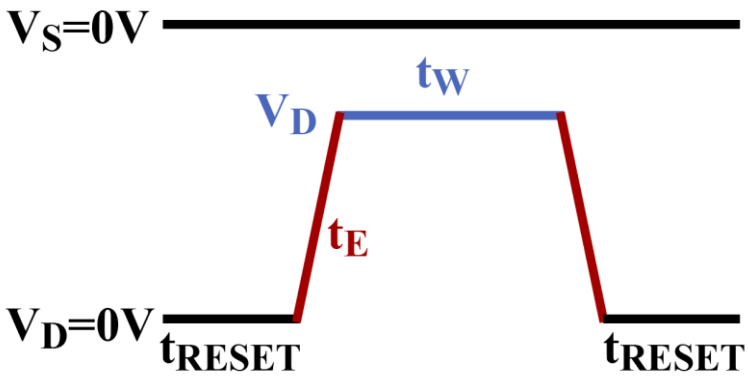

Figure 4.7: Pulse waveform used for testing device reset condition.

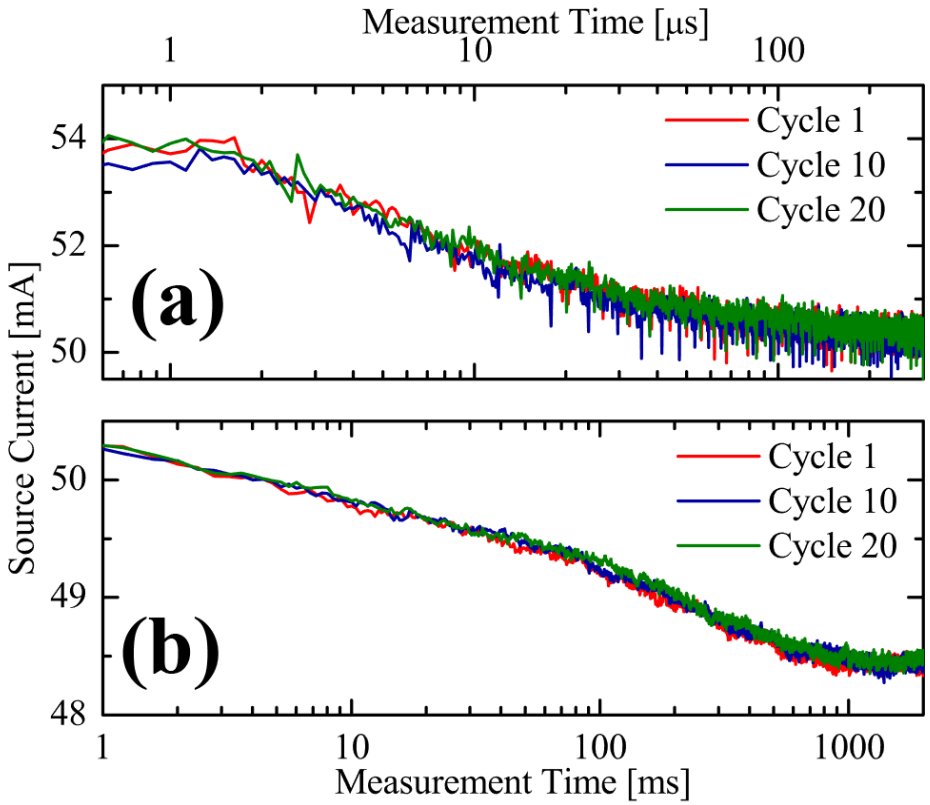

Figure 4.8: Transient I_S at V_{DS} = 20 V for (a) t_W = 300 µs and (b) t_W = 1s; t_{RESET} = 10 s, t_E = 300 ns on AlGaN/GaN TLM. I_S produces the same degradation trend through each cycle of the test, showing complete device reset.

4.5. Transient Current Degradation

For the first time, a parametric technique that measures both source and drain transient currents is developed to extract bulk trapping kinetics under normal device operation with the exclusion of self-heating. We describe the developed experimental methodology and then discuss our investigation into the time constant and magnitude of bulk and surface traps under various biasing conditions. These results are then compared with existing works in order to verify our findings.

4.5.1. Experimental Methodology

In order to investigate the charge trapping involved in the AlGaN/GaN HEMT structure, we propose the experiment given in Figure 4.9. The experiment condition for the AlGaN/GaN HEMT, V_{DS} = 0 V and V_{GS} = 0 V were pulsed to V_{DS1} = 10 V, 15 V, and 20 V and V_{GS1} = 0 V, -1 V, -2 V, and -3 V, respectively, were pulsed for a measurement time of $t_{meas,1}$ = 1 s. These conditions place the device in a semi-ON state. The time to refresh/reset the device, for purposes described in Section 4.4.2, is set to be t_{RESET} = 10 s. While the edge time, t_E, is set to be 200 ns in order to reduce parasitic capacitance and avoid diffusion current. The AlGaN/GaN TLM uses the same conditions without the gate pulse as there is no gate terminal.

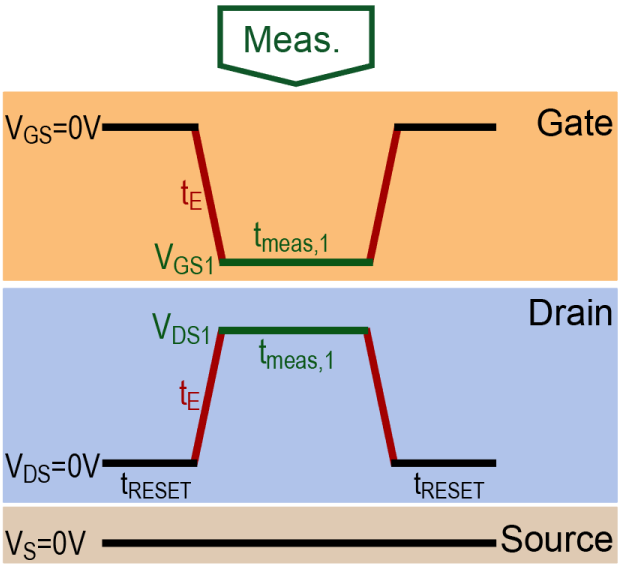

Figure 4.9: Pulse waveforms used for I_S and I_D transient measurements for investigating the transient bulk trapping behaviour in AlGaN/GaN HEMTs. For AlGaN/GaN TLMs, only V_S and V_{DS} waveforms are used.

Using this experimental methodology, the source and drain currents are measured on both AlGaN/GaN TLM and HEMT devices that are grown on different wafers. Figure 4.10 shows the current transients, I_S and I_D, monitored at V_{DS} = 20 V for both the AlGaN/GaN (a) TLM and (b) HEMT devices. This shows that similar trends of degradation phenomena persist regardless of the device architecture (TLM or HEMT) and the wafer. Therefore, the later described analysis of these current transients is not limited to only AlGaN/GaN HEMT devices.

The transient behaviour of source and drain current (I_S and I_D) can be broadly split into two phases, namely a fast degradation (DEG1 for ≤ 1 ms) and a slow degradation (DEG2 for ≥ 1 ms). The following sub-sections analyse the behaviour of bulk and surface trapping for both fast and slow degradation under the remaining experimental conditions.

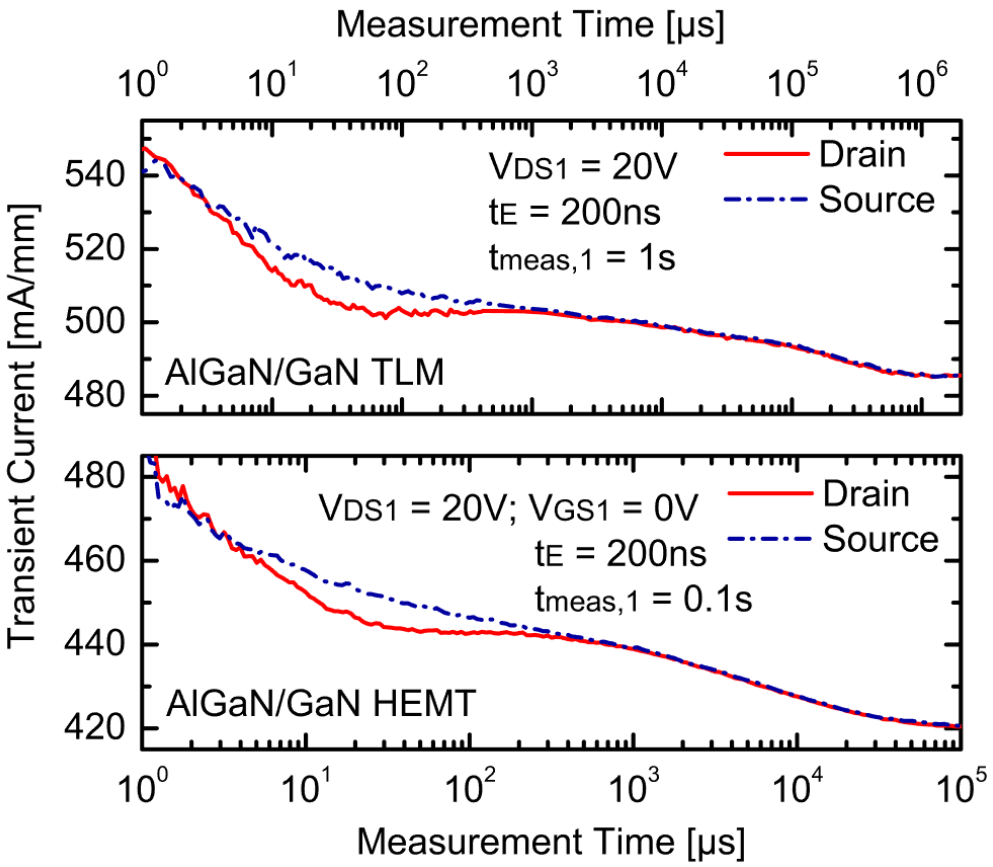

Figure 4.10: Transient source and drain currents, I_S and I_D. Very similar degradation characteristics mechanisms, i.e. charge trapping and self-heating effects, are observed for the (i) AlGaN/GaN TLM and (ii) AlGaN/GaN HEMT. The experiment conditions and the used pulse waveform are summarised in Figure 4.7.

4.5.2. Bulk Trapping

We investigate the bulk trapping that occurs within the AlGaN/GaN HEMT. Bulk traps are identified as the fast charge trapping mechanism that contributes to DEG1 [140]. Electrons that flow through the source terminal and become trapped within the bulk, e.g. GaN buffer, are not collected by the drain terminal, resulting in a difference between I_S and I_D ($I_S - I_D > 0$ mA mm^{-1}). It is important to note that self-heating does not influence this difference, $I_S - I_D$, as it degrades both I_S and I_D proportionally. Similar to the gated device, $I_S - I_D > 0$ mA mm^{-1} occurred in ungated device, as shown in Figure 4.10. This indicates that $I_S - I_D$ is not caused by gate terminal.

4.5.2.1. Fast Degradation – DEG1

During the fast degradation ($\leq$ 1 ms) phase, a maximum magnitude of $I_S - I_D$ is observed, which indicates that majotity (> 90%) of bulk trapping occurs during this phase. This stems from the high electric field applied within the device that provides enough energy for charge carriers to be trapped within the bulk. However, it is well documented that self-heating does occur over this period and contributes towards the degradation of current, as previously described in Section 2.2.6.3. It is important to note that the degradation of I_D saturates towards the end of this fast degradation phase, indicating the saturation of the first self-heating.

4.5.2.2. Slow Degradation – DEG2

During the slow degradation ($\geq$ 1 ms) phase, current begins to degrade a second time after bulk trapping and self-heating saturation. Trace $I_S - I_D$ is observed in this phase showing that insignificant bulk trapping occurs. According to the RC model, given in Section 4.2, a second self-heating phase can occur at this time constant ($\geq$ 1 ms).

4.5.2.3. Dependency on Bias Conditions

Now that bulk trapping has been measured, $I_S - I_D$, shown in DEG1, we investigate its kinetics under various biasing conditions. Using the same pulse waveform given in Figure 4.7, we apply V_{DS1} = 20 V, 15 V and 10 V, V_{GS1}= 0 V to -3 V (step -1 V) to the AlGaN/GaN HEMT. The current transients for each gate biasing condition are shown in Figure 4.11 for (a) V_{DS1} = 20 V, and (b) V_{DS1} = 10 V. Focusing only on DEG1 for this section, we observe $I_S - I_D$ for each condition. To analyse the dependency of $I_S - I_D$ on bias conditions, we provide Figure 4.12,

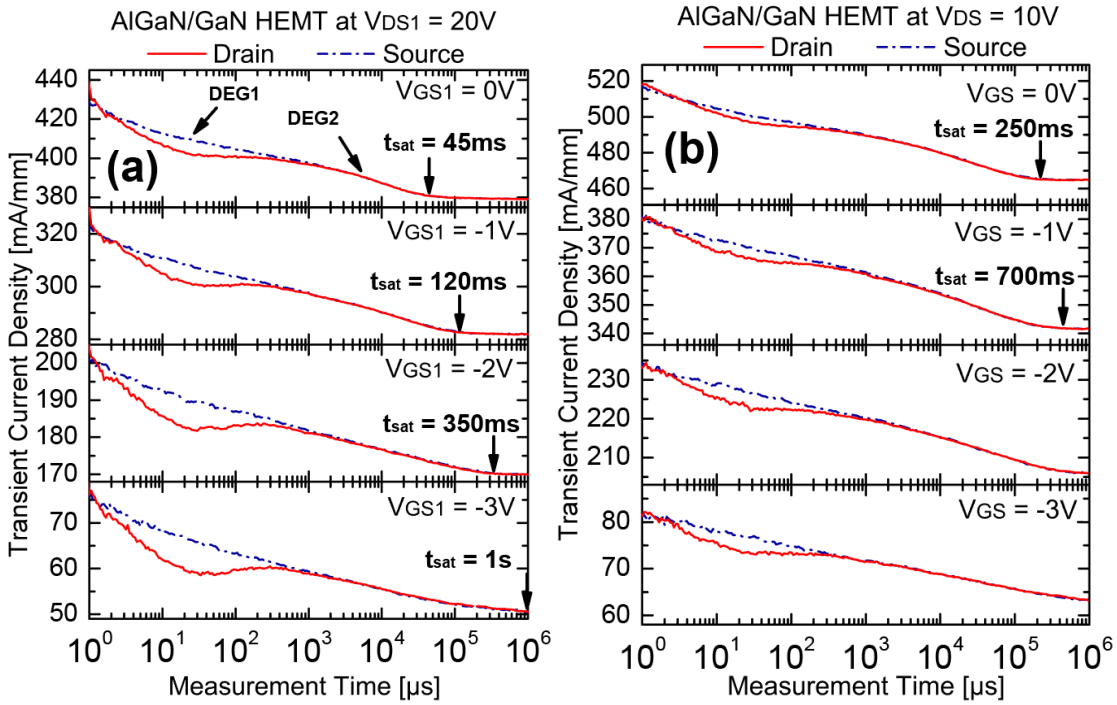

Figure 4.11: Transient behavior of the drain, I_D, and source, I_S, currents, versus measurement time on log scale using the pulse waveforms given in Figure 4.7 with (a) V_{DS1} = 20 V and (b) V_{DS1} = 10 V, at V_{GS1} = 0 V to -3 V. Two degradations of current are observed at different time constants, DEG1 and DEG2.

showing the measurement of $I_S - I_D$ with respect to measurement time for each bias condition. From this, we can deduce two points:

i. The magnitude of $I_S - I_D$ is only dependent on drain bias. This could suggest that the small change in gate bias does not provide a significant enough change in electric field to induce greater bulk trapping. Although, given this suggestion, the drain bias step of 5 V should not impact the bulk trapping significantly. The more likely suggestion is that fewer bulk traps occur beneath the gate due to the lack of strain reduction directly beneath the gate. This lack of strain reduction contributes towards fewer threading dislocations resulting in fewer bulk traps [197].

ii. There is no change in $I_S - I_D$ peak in terms of time regardless of the bias condition. Therefore, the timing characteristic of $I_S - I_D$ is independent on both drain and gate bias. This suggests that rate of bulk charge trapping peak does not change as this is dependent on the density of threading dislocations within the bulk for charge carriers

to trap into and not dependent on biasing conditions. Increasing drain bias simply provides more energy to charge carriers to reach deeper traps and does not impact the speed in which these charge carriers are trapped.

To further visualise the dependence of $I_S - I_D$ against drain and gate bias, we take the maximum $I_S - I_D$ value from Figure 4.12 ($t \approx 35$ µs) and plot this against each drain and gate biasing condition, shown in Figure 4.13. Here, with the inclusion of V_{DS1} = 15 V for V_{GS1} = 0 V to -3 V, we observe a linear increase of bulk trapped charge density magnitude with respect to V_{DS1} increase. As the electric field between the gate and the drain contacts increases linearly with linear increase of V_{DS1} , greater energy is provided to charge carriers within the channel

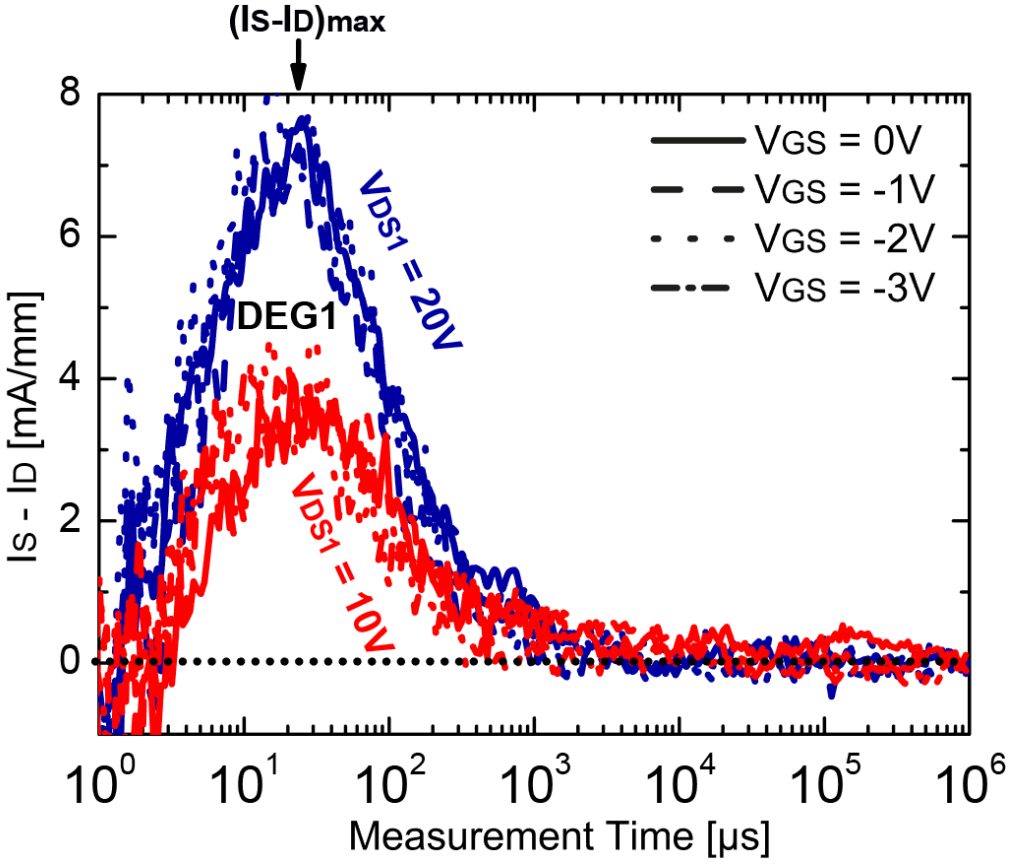

Figure 4.12: I_S and I_D difference ($I_S - I_D$) versus the measurement time at V_{DS1} = 20 V and 10 V for different gate voltages (V_{GS1} = 0 V to -3 V); indicating the bulk trapping process (DEG1). Showing (i) I_S – I_D magnitude dependence on drain bias only, and (ii) I_S – I_D timing characteristic independent of both drain and gate bias.

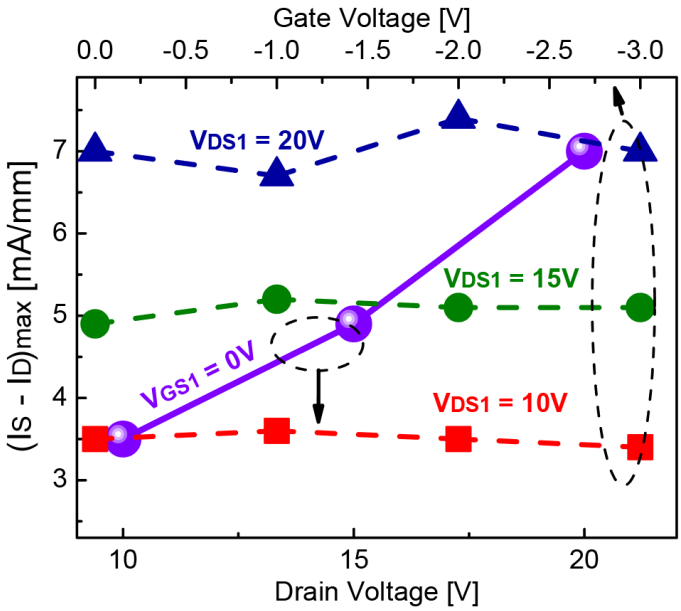

Figure 4.13: The impact of drain voltage, V_{DS1}, and gate voltage, V_{GS1} on $(I_S - I_D)_{max}$ given at $t \approx 35$ µs showing linear proportionality of bulk trapped charge density and V_{DS1}. Unlike V_{DS1}, V_{GS1} shows a negligible impact on bulk trapping characteristics.

that results in a linearly increasing bulk trap charge density. This is potentially due to the near-uniform distribution of threading dislocations within the bulk. V_{GS1}, however, has no impact on bulk trapped charge density as previously discussed.

4.5.3. Surface Trapping

Surface trapping is also known to degrade the current within AlGaN/GaN HEMTs as described in Section 2.2.6.3. Two mechanisms of surface trapping occur that contributes towards current degradation, namely accumulation and redistribution of surface traps. Unlike bulk trapping, where $I_S - I_D > 0$ mA mm^{-1}, the surface trapping contributes towards the transient current degradation of both I_S and I_D proportionally, where $I_S - I_D = 0$ mA mm^{-1}. Here, surface trapping changes the electrostatic within the device and, thus, degrading the current. In the following, we analyse the current degradation of the AlGaN/GaN HEMT and the time to current degradation saturation (time constant) of DEG2, shown in Figure 4.14, due to surface trapping accumulation and redistribution.

4.5.3.1. Fast Degradation – DEG1

It is unclear as to whether surface trapping accumulation or redistribution contributes towards

DEG1. However, for surface trapping accumulation, it is known to occur within 1 µs [198]. Due to the large electric field between the gate and drain, charge carriers are trapped at the surface of the device as a result of dangling bonds. As the surface trapping accumulation occurs within a short period, the degradation of current as a result of this begins before our first measurement sample is taken.

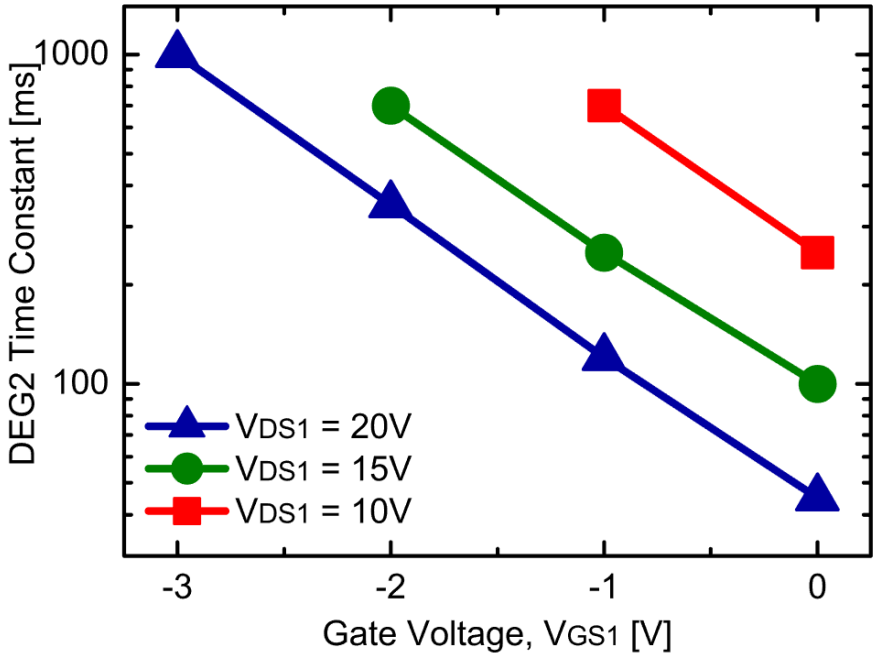

Figure 4.14: Time constant of DEG2, t_{DEG2}, at V_{DS1} = 20 V, 15 V, and 10 V and V_{GS1} = 0 V to -3 V; showing the dependence of t_{DEG2} with both V_{DS1} and V_{GS1}.

4.5.3.2. Slow Degradation – DEG2

As we observe a second degradation that does not include bulk trapping ($I_S - I_D$ = 0 mA mm^{-1}), therefore, DEG2 must be at least partlially due to surface trapping redistribution. The time constant of DEG2 corresponds with that of other works, which validates this theory [194], [199]. Similarly to DEG1, the slow degradation (DEG2) is coupled with the second phase of self-heating, described in Section 4.2.

4.5.3.3. Dependency on Bias Conditions

By analysing the transient current degradation under different bias conditions (drain and gate bias), shown in Figure 4.11, we decouple the surface trapping and self-heating by observing

the bias dependency of DEG2. Firstly, we examine the time constant of DEG2 (t_{DEG2}). In contrast to the time constant of DEG1, t_{DEG2} is both drain and gate bias independent. Figure 4.14 shows the behaviour of t_{DEG2} extracted from Figure 4.11 with respect to both drain and gate biasing conditions. It is clear that t_{DEG2} can be influenced by both V_{DS1} and V_{GS1}. With consideration of Figure 4.3, where the self-heating time constant does not change with bias conditions, this leads us to believe that surface trapping is the cause of t_{DEG2} variation.

With the knowledge that t_{DEG2} is surface trapping dependent for semi-ON state conditions, explanations to its behaviour under these conditions can be made (Figure 4.14). On one hand, the increase of the magnitude of V_{GS1} induces greater surface trapping density, leading to a larger time for the redistribution process to complete. On the other hand, the required time to redistribute the trapped electrons at the surface and extend the 'virtual gate' towards the drain side reduces when increasing V_{DS1}. Larger V_{DS1}, which induces higher electric field, provides more energy to surface traps to distribute more quickly [200]. The redistribution of surface traps alter the electrostatic integrity and channel resistance in the device. As a result, both source and drain current degrade proportionally.

We cannot determine the dependency of surface trapping magnitude with the pulse waveform of Figure 4.9, as it is strongly coupled with self-heating. This leads us onto the investigation of Section 4.6, where we conclude whether surface trapping or the second phase of self-heating is the primary cause of DEG2 magnitude.

4.6. Self-Heating & Charge Trapping Mechanisms

The primary mechanism, t_{DEG2}, is stated to be dependent on surface trapping during the semi-ON state. In this section, we investigate the primary mechanism of the magnitude of DEG2. The experimental methodology behind how we identify the dominant degradation mechanism is described. The severity of increasing the magnitude of gate bias when the device is in the OFF-state is investigated. Finally, we conclude on the primary cause of DEG2 and explain the importance of reducing the degradation mechanism.

4.6.1. Experimental Methodology

In order to investigate the surface trapping influence on degradation in AlGaN/GaN HEMTs, we propose the experiment illustrated in Figure 4.15. Quiescent biasing conditions, V_{DSQ} = 10 V and V_{GSQ} = -10 V, -8 V, -5 V, -3 V, and -1 V, were set at t_Q = 1 µs, 10 ms, and 1 s, whereby pre-charging of surface trapping and redistribution occurred. To note, V_{TH} = -3.5 V is the threshold voltage of this investigated device.

When $V_{GSQ} < V_{TH}$, there is no self-heating as the device is in the OFF-state. Otherwise, self-heating occurs due to the device being in a semi-OFF state when $V_{GSQ} > V_{TH}$. Also, bulk trapping occurs within the device during this condition due to the high V_{DSQ} of 10 V, as a result of the mechanisms described in Section 4.5. After the device is pre-charged, the measurements were then taken at V_{DS2} = 10 V and V_{GS2} = 0 V for a time $t_{meas,2}$ = 1 s. During this measurement phase, surface traps begin to redistribute in the opposite manner to the quiescent conditions and surface trapping density reduces. This is the consequence of the decreased magnitude of gate voltage from the quiescent to the measured condition. Self-heating increases as the device is switched from the OFF/semi-OFF state to the ON-state. The bulk trapping saturates during the pre-charging conditions and no further bulk trapping occurs during the measurement phase, $t_{meas,2}$. As discussed in Section 4.5.2.3, keeping the same drain voltage

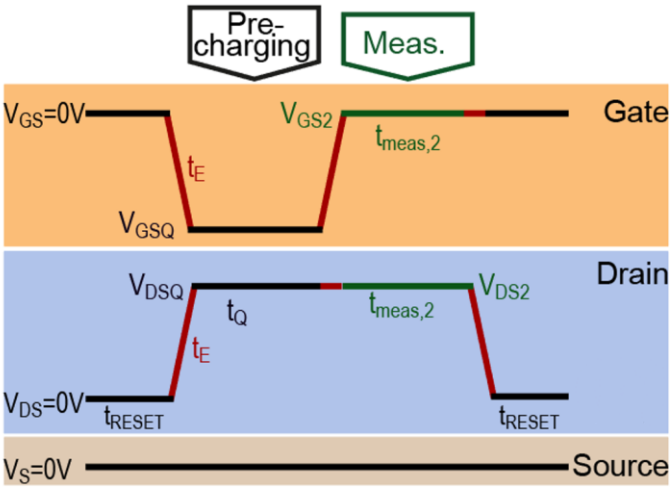

Figure 4.15: Pulse waveforms used for I_S and I_D transient measurements where surface and bulk traps are pre-charged during the pre-charging condition at V_{DSQ} and V_{GSQ} for a time t_Q. Transient current measurements are then taken at V_{DS2} and V_{GS2} for a time $t_{meas,2}$.

condition ($V_{DSQ} = V_{DS2}$ = 10 V) and changing the gate voltage ($V_{GSQ} \neq V_{GS2}$) does not impact the bulk trapping process.

4.6.2. Primary Slow Degradation (DEG2) Mechanism

To explore the primary mechanism of DEG2, we first need to decouple bulk trapping from self-heating and surface trapping in our measurement phase ($t_{meas,2}$). A pre-charging condition of V_{GSQ} = -1 V is used for comparison purposes. For all pre-charging bias conditions where $t_Q >$ 1 ms, bulk trapping is saturated at the same amount as found in Figure 4.11(b). However, surface trapping and redistribution are controlled by V_{GSQ} and V_{DSQ}. From Figure 4.16 and when $t_Q \geq$ 10 ms, two mechanisms of transient current occur when reducing $|V_{GSQ}|$ to $|V_{GS2}|$: (i) recovery of surface trapping redistribution occurs whereby 'virtual-gate' length is reduced, reducing channel resistance and recovering the current, and (ii) self-heating occurs that increases channel resistance and degrades the current. The behaviour of transient current is analysed for each pre-charging condition:

- $t_Q = 1\ \mu s$ – Negligible surface trapping redistribution is induced during this pre-charging condition due to its short pre-charging time. As a result, no recovery of surface trapping occurs during measurement. Instead, bulk trapping, self-heating and surface trapping degrade the current. Therefore, the current transient behaviour is similar to that of Figure 4.11(b) at V_{GS1} = 0 V; this occurs for all V_{GSQ} conditions.
- $t_Q = 10\ ms$ – During the pre-charging time, surface trapping accumulation/redistribution and complete bulk trapping occur. In addition, no self-heating is induced during the pre-charging time for V_{GSQ} = -5 V and -10 V. As a result, the primary cause of the degraded current at $t_{meas,2}$ = 1 µs is surface trapping. This initial degradation increases with greater $|V_{GSQ}|$ as greater surface trapping density is accumulated/redistributed. A recovery of current is then observed during measurement from ~10 ms to ~40 ms for V_{GSQ} = -1 V to -10 V, respectively. This shows that surface trapping recovery has a greater impact on the current behaviour than the degradation of current due to self-heating. As t_Q is less than the time constant of surface trapping that is observed in Figure 4.11(b), surface trapping recovery ends premature to the saturation of current degradation. Hence, a degradation of current is observed beyond ~40 ms as a result of self-heating.

- t_Q = *1 s* – Unlike t_Q = 10 ms, pre-charging of surface traps is complete and occurs at a greater magnitude at this pre-charging time. Therefore, the current recovers throughout the entirety of the measurement window. In addition, degradation of current is shown to be greater when comparing the same V_{GSQ} at less t_Q at the initial measurement of transient current. Large recovery of current is then observed, clearly showing the dominance of recovery of surface trapping over self-heating degradation.

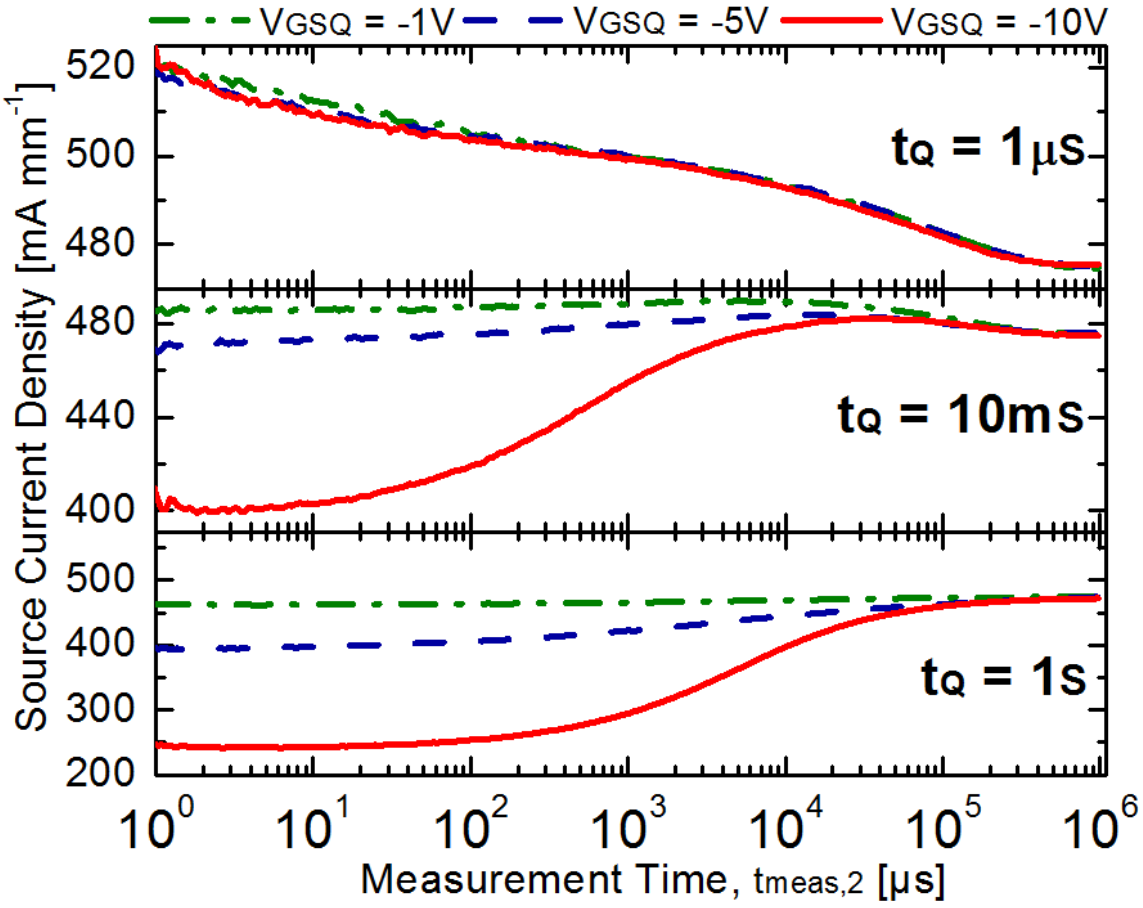

Figure 4.16: Transient behavior of the drain, I_D, and source, I_S, currents, versus measurement time using the pulse waveforms given in Figure 4.15 with V_{DSQ} = V_{DS2} = 10 V, V_{GSQ} = -1 V, -5 V, and -10 V, and V_{GS2} = 0 V. The effect of current recovery is shown to increase with greater V_{GSQ} and t_Q due to greater surface trapping density and redistribution.

4.6.3. Bulk Trapping vs. Surface Trapping

It is evident from the previous analyses that surface trapping degradation has a much greater impact on DEG2 compared to self-heating. To show how the bulk trapping compares to surface trapping with respect to overall current degradation, bulk-trapping is required to be induced during measurement whilst maintaining the surface trapping degradation during pre-charging. Therefore, during the measurement, there will be degradation due to bulk trapping and self-heating but recovery of current due to surface trapping under certain conditions. To achieve this, V_{DSQ} = 0 V at V_{GSQ} = -1 V, -3 V, -8 V and -10 V for t_Q = 1 s are used during pre-charging (Figure 4.15). The pre-charging conditions are then stepped up to V_{DS2} = 20 V and 10 V and V_{GS2} = 0 V for $t_{meas,2}$ = 1 s during transient current measurement; shown in Figure 4.17(a) and (b), respectively. We observe similar behaviours to changes in bias given in Figure 4.11. The

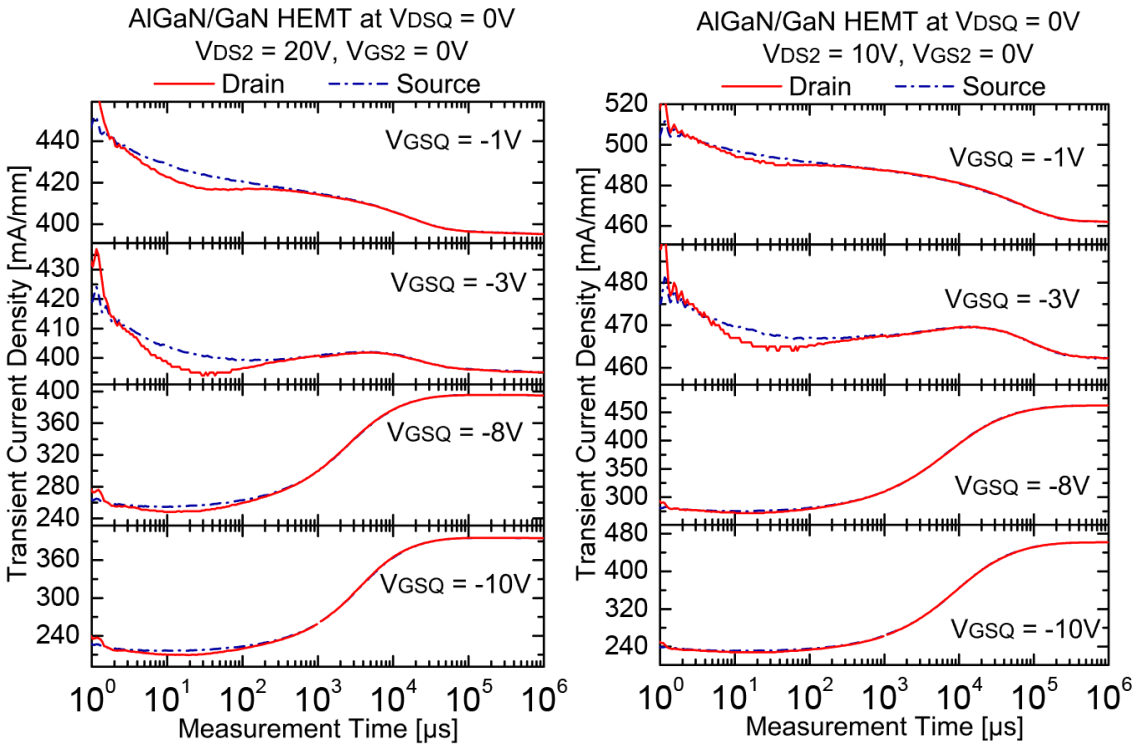

Figure 4.17: Transient behavior of the drain, I_D, and source, I_S, currents, versus measurement time using the pulse waveforms given in Figure 4.15 with (a) V_{DS2} = 20 V and (b) V_{DS2} = 10 V, at V_{DSQ} = 0 V, V_{GSQ} = -1 V, -3 V, -8 V, and -10 V, and V_{GS2} = 0 V at t_Q = 1 s. The inclusion of bulk trapping has minimal impact on the recovery of current degradation when pre-charging conditions set the device to the OFF-state; $|V_{GSQ}| > V_{TH}$.

large recovery shown in higher $|V_{GSQ}|$ shows the significant dominance of surface trapping over both self-heating and bulk trapping. To note, the surface trapping redistribution is gate-to-drain voltage (V_{GD}) and t_Q dependent.

The difference between I_S and I_D is extracted from Figure 4.17 and is shown in Figure 4.18. This shows near identical characteristics to Figure 4.12 which validates that (i) current is not degraded due to bulk trapping during pre-charging and (ii) bulk trapping is not impacted by gate bias, only by drain bias.

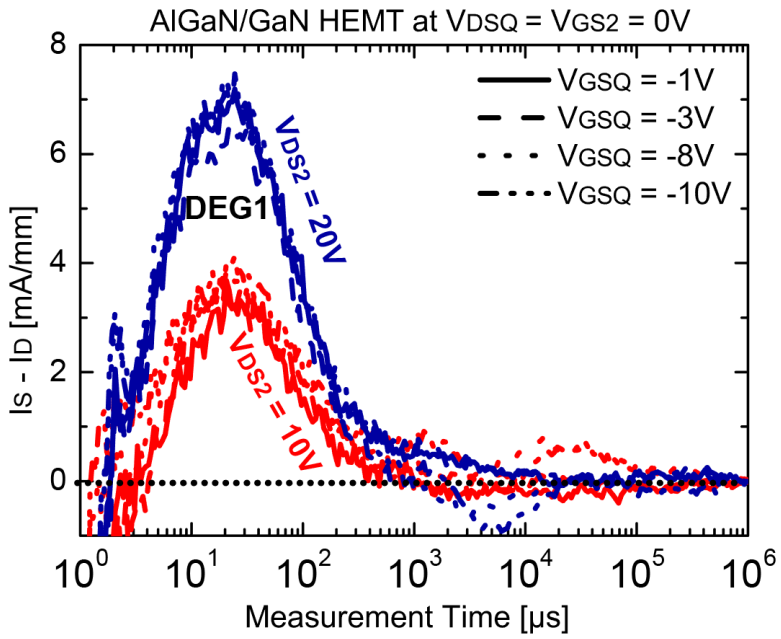

Figure 4.18: I_S and I_D difference ($I_S - I_D$) versus the measurement time at V_{DS2} = 20 V and 10 V for different gate voltages (V_{GS2} = -1 V, -3 V, -8 V, and -10 V). When compared with Figure 4.12, this validates that no charge carriers are trapped in the bulk during pre-charging.

4.7. Summary

In this chapter, a new source and drain transient currents, I_S and I_D, technique for charge trapping characterisation in AlGaN/GaN HEMTs, under normal device operation, has been developed. Using this technique, charge trapping behaviours, with the exclusion of self-heating, have been analysed. Two types of charge trapping mechanisms have been identified: (i) bulk trapping occurring on a time scale of < 1 ms, followed by (ii) surface trapping and redistribution beyond 1 ms. The bulk trapping and surface trapping corresponds to fast and slow current

degradations, respectively.

Through monitoring the difference between I_S and I_D, bulk trapping time constant is shown to be independent of V_{DS} and V_{GS}. Although, V_{DS} is found to affect the bulk trap density. V_{DS} is found to be a cause of bulk charge trapping during both ON and OFF states of the device.

Surface trapping is found to have a much greater impact on slow degradation when compared to self-heating and bulk trapping. This is an important step to understanding the priority of device engineering, whereby the focus should be aimed towards reducing surface trapping accumulation and redistribution in order to minimise current degradation.

CHAPTER 5

OHMIC/SCHOTTKY CONTACT OPTIMISATION & DEVICE ENGINEERING

The focus of this chapter is to apply the knowledge gained from the research conducted in previous chapters in order to propose new optimisations for the AlGaN/GaN HEMT Ohmic contacts, Schottky contact, and device architecture. Through deep understanding of thermal management issues at the Ohmic contacts, Chapter 3, we are able to focus on optimising the performance of the Ohmic contacts and propose an option to reduce the self-heating effects, Section 5.2. The insight gained from the newly developed characterisation technique, Chapter 4, showing a very small impact of gate voltage on bulk trapping gave us reason towards optimising Schottky contact fabrication process, Section 5.3. Finally, the performance of our devices were enhanced through several modifications to its architecture, discussed in Section 5.4. The output of this research is the result of collaborations with University of Lille, Swansea University and University of Malaya.

Through recessing the Ohmic contacts of our device into the AlGaN barrier layer, we reduce the access resistance. We propose a fabrication process of ohmic contacts to reduce R_C of AlGaN/GaN HEMTs with a high Al concentration, whilst avoiding implantations that cause HF-traps and gate leakage. The optimisation of Schottky contacts is crucial for gate control in GaN-based HEMTs in order to achieve high frequency performance, good linearity and low leakage current. The gate leakage of the device is minimised through the implementation of a TiN layer within the Schottky contact, which alters the state of the AlGaN barrier layer and forms quasi-p-type doping directly beneath the Schottky contact. Finally, we propose to replace the conventional HEMT with several new structures (i.e. step-graded AlGaN barrier layer, AlN exclusion layer, and InGaN channel layer) to improve 2DEG density and mobility within the device.

5.1. Device Structure

A schematic cross-section of the AlGaN/GaN epi-structures used for Ohmic contact optimisation is illustrated in Figure 5.1(a) without exclusion layer and (b) with exclusion layer. This structure is grown by MBE on a High-Purity (HP) and highly-resistive (ρ > 5 kΩ.cm) Silicon substrate with (111) orientation. It consists, from the substrate to the top, of low-temperature AlN/GaN/AlN nucleation layers for stress accommodation, and a 1 µm $Al_{0.07}Ga_{0.93}N$ back-barrier to reduce alloy scattering and to improve the carrier confinement of the 2DEG. A channel is made of a 100 nm thick unintentionally doped GaN buffer followed by a 1 nm AlN exclusion and a 20 nm undoped $Al_{0.28}Ga_{0.72}N$ layer to increase the electron density

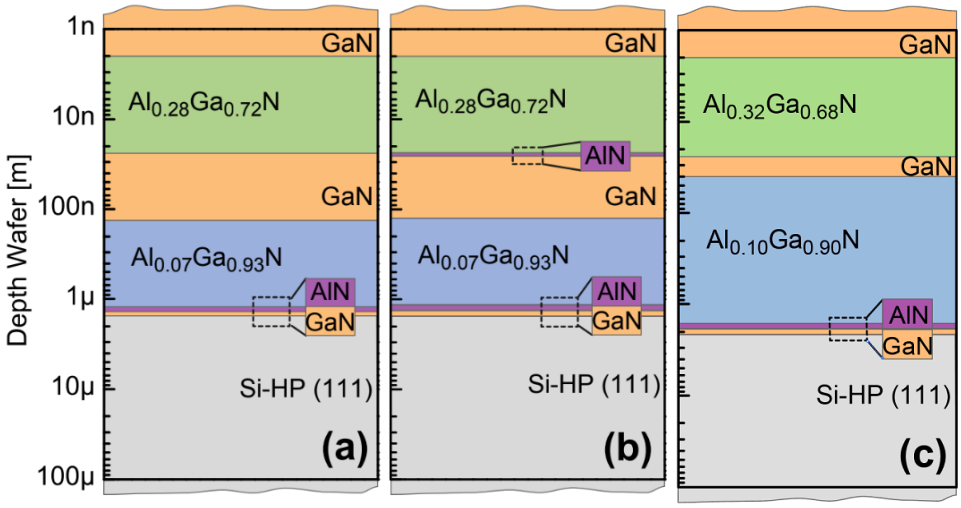

Figure 5.1: Schematic cross-section of AlGaN/GaN epi-structures grown on the Si-HP (111) substrate with Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) contact metallisation for Ohmic contact optimisation (a) without exclusion layer, (b) with exclusion layer and (c) for Schottky contact optimisation.

in the 2DEG and to reduce alloy disorder scattering [201]. Finally, a 2 nm GaN cap layer is grown in order to reduce surface traps [202]. The material growth process and conditions to form this epi-structure are similar to those given in previous works by Cordier [203].

The AlGaN/GaN epitaxial structures used for Schottky contact optimisation are grown using a Riber reacture on a highly resistive (111)-oriented silicon substrate (10 to 20 kΩ.cm) by MBE, shown in Figure 5.1(c). A 0.54 µm-thick stress accommodation layer of AlN/GaN is deposited initially, followed by a 1.7 µm-thick buffer of $Al_{0.1}Ga_{0.9}N$, a 15 nm-thick channel of GaN, a 25 nm-thick barrier of $Al_{0.32}Ga_{0.68}N$, and a 1 nm GaN cap layer. In a first step, the surface is ultrasonically cleaned and de-greased by 1 min dip in HNO_3:H_2O (1:1), 1 min wet etch in HCl:H_2O (1:1), and then drying by nitrogen. Ti/Al/Ni/Au (12/200/40/100 nm) evaporation is then performed, followed by a rapid thermal annealing at 900 °C for 30 s in order to form ohmic contacts, [204]. Components are isolated by He^+ ion implantation. As a result, an isolation current density of 850 nA mm^{-1} is measured at +150 V with an 8 µm space between the two contacts.

5.2. Ohmic Contact Optimisation for Access Resistance Lowering

The issue of current reduction through AlGaN/GaN-based devices as a result of Ohmic contact limitations is addressed in this section. We propose two solutions towards improving the current

flow through these devices. Firstly, we advise etching the AlGaN barrier layer beneath the Ohmic contacts prior to deposition and annealing of Ohmic contacts in order to reduce access resistance. Secondly, we contest the temperature rise at the Ohmic contacts with a proposition to overgrow the AlGaN barrier layer at the Ohmic contacts by reducing the vertical electric field between the channel and contact metal.

5.2.1. Ohmic Contact Optimisation for AlGaN/GaN HEMTs

To fully benefit from the properties of AlGaN/GaN HEMTs, reduction of extrinsic R_C of AlGaN/GaN HEMTs is essential to enhance their DC/RF performance. To achieve this, several methodologies have been previously proposed [134], [135], [205]–[207]. Firstly, implanting Si into the AlGaN barrier is known to reduce ohmic contact, R_C. However, annealing contacts at high temperatures, to activate dopants, results in diffusion of the Si dopants away from the contacts. The result is increased high-frequency (HF) charge trapping and gate leakage current [208]. Secondly, increasing the Al concentration in the barrier and/or using AlN exclusion layer is known to increase 2DEG confinement and to enhance 2DEG density and mobility, which enhances performance [134], [135]. However, it results in increased R_C due to low metal diffusion beneath the metal contact [136], [137].

In this section, we propose a fabrication process of ohmic contacts to reduce R_C of AlGaN/GaN HEMTs with a high Al concentration, while avoiding implantations that cause HF-traps and gate leakage. This is essential for enhancing device DC and RF performance. For this new proposal, the outer edges of an AlGaN/GaN HEMT, where the source and drain ohmic contacts are to be placed, are etched from the surface of the device down into the AlGaN barrier layer. Contact metal is then evaporated onto the etched locations and rapidly annealed under high temperatures. During the annealing process, contact metal diffuses into the AlGaN barrier layer to form an alloy beneath the metal contact. The change in R_C at different etching depths at various annealing conditions is investigated to identify the optimal etching depth given by the lowest R_C.

5.2.1.1. Technological Process of Ohmic Contact

To optimise the metallisation scheme, particularly the Ti/Al ratio, Ti metal is first evaporated on the epi-structure shown in Figure 5.1(a), without AlN exclusion layer. The contact is then annealed at two different temperatures, one sample (S1) at 750 °C and another one (S2) at 900 °C. The Ti/AlGaN/GaN interfaces are then examined using High-Resolution Transmission

Electron Microscopy (HRTEM) images. The HRTEM image of S1, annealed at 750 °C, shows few Ti-Al alloy clusters and an abrupt interface (Figure 5.2(a)). Here, the reactivity of Ti with AlGaN is low and, therefore, the formed alloy is small. However, S2, annealed at 900 °C, has a larger alloy formation (Figure 5.2(b)). Multiple compositions of alloy are formed, consisting of (i) Ti-Ga on the top, (ii) TiN at the interface, and (iii) Al + Ti + N + Ga. The formation of the alloy stems from N atoms reacting with Ti, to create a TiN alloy. This is observed below the contact metallisation. The greater reactivity between Ti and N can be seen at high annealing temperatures, which produces a greater TiN alloy formation. However, as a result of higher annealing temperature, a greater void formation is observed. This void formation can be reduced with incorporation of Al through the metallisation scheme. Al concentration in the barrier layer also increases reactivity of Ti from the metal contact and N from the barrier layer to form an $AlTi_2N$ alloy [119], [209].

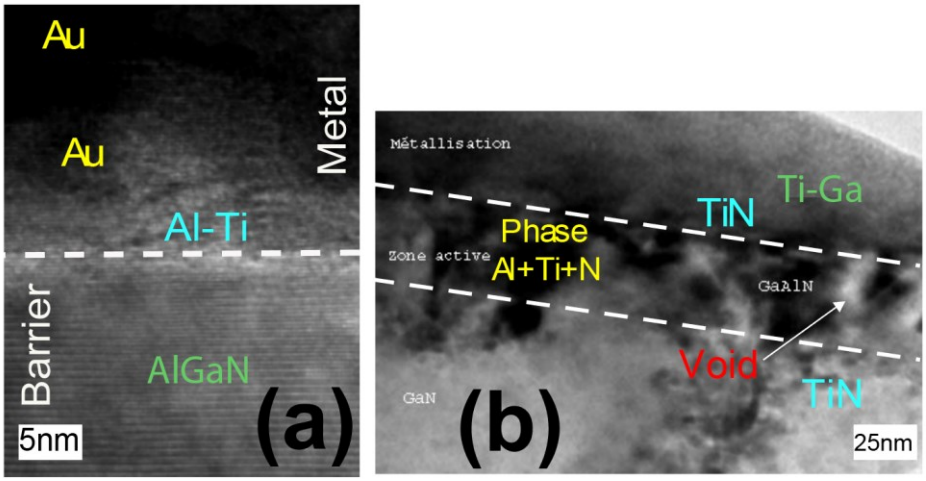

Figure 5.2: HRTEM images from University of Lille of Ohmic contacts at the $Ti/Al_{0.28}Ga_{0.72}N$ interface after rapid thermal annealing, forming an alloy compositions at (a) 750 °C and (b) 900 °C.

The addition of Al into the metallisation scheme is observed in Figure 5.3 with HRTEM imaging at 900 °C annealing temperature to clearly show alloy formation. At such high temperatures, (i) Al diffuses into the Ti layer of the metallisation to form Ti-Al bonds, and (ii) there is a high reactivity with oxygen at the Ti/Al interface which causes an AlO_X-TiO_X alloy to form. The increase in the Ti/Al ratio allows the formation of TiN layer, which is favourable to obtain a good ohmic contact. Decreasing the Ti/Al ratio, however, reduces the reactivity of Ti at the interface and, consequently, leads to the formation of voids. Therefore, a compromise between these two has to be found. A Ti/Al ratio of 6% has been found experimentally to be

the best Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayers for the ohmic contact metallisation [210].

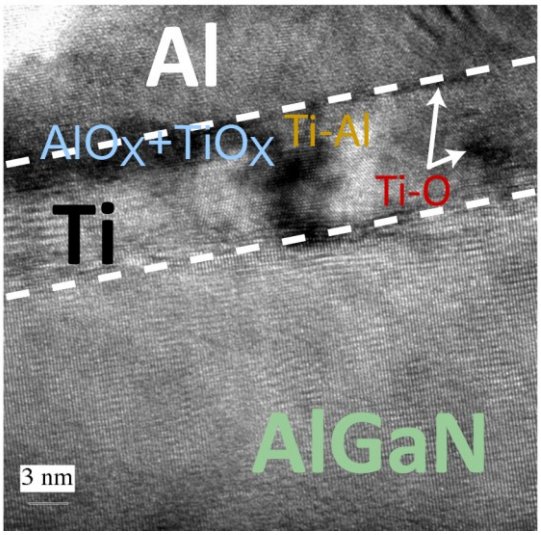

Figure 5.3: HRTEM image of ohmic contact at the Al/Ti/$Al_{0.28}Ga_{0.72}N$ interface after rapid thermal annealing forming alloy compositions at 900 °C.

The challenge is how to form a good ohmic contact with a low R_C for the epi-structure shown in Figure 5.2(b), including the AlN exclusion layer. We have observed that the presence of high Al concentration in the barrier and/or AlN exclusion layer, reduces the diffusion of metal in the barrier and significantly degrades R_C. To overcome this difficulty, we used the same metallisation scheme as described above and recessed the source/drain metallisation at different depths to find an optimum contact as summarised in the following section.

5.2.1.2. Experimental Procedure

In order to identify an optimal contact formation that provides lowest R_C, various ohmic contact configurations are tested. The GaN/$Al_{0.28}Ga_{0.72}N$/AlN barrier layers of the epi-structure (Figure 5.2(b)) are dry etched using an Ar^+ ion ebeam evaporation at different depths ranging from 0 % to 100 %, as illustrated in Figure 5.4. The condition used for the etching is Ar flow of 12 sscm and ion energy of 300 eV. The etching rate of the barrier is around 4 nm min^{-1}. The source and drain contact metallisation, which consists of Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayers, are then evaporated onto this epi-structure. The metallisation for each etched depth is rapidly annealed at various temperatures ranging from 750 °C to 900 °C for 30 s in a nitrogen atmosphere.

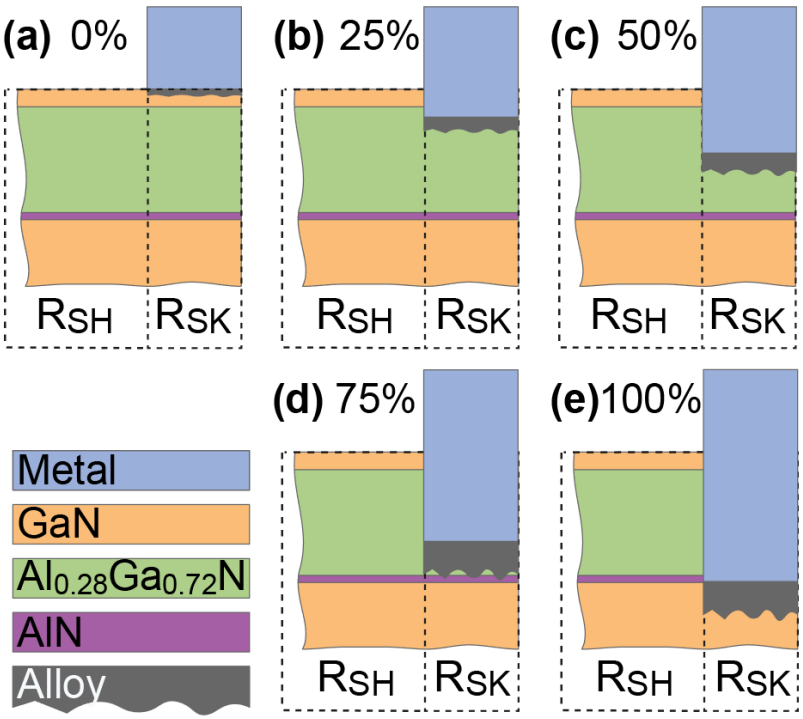

Figure 5.4: Illustration of alloy thickness under different etching depths. Greater quantity of Al beneath the metal results in less alloy thickness (a) 0%, (b) 25%, (c) 50%, (d) 75% and (e) 100% (not to scale). R_{SK} is the sheet resistance beneath the metal contact and R_{SH} is the sheet resistance outside of the contact area.

Upon annealing the contacts, an alloy forms due to metal diffusion. The alloy thickness is dependent on the Al volume beneath the metal. When the epi-structure is etched further into the GaN/$Al_{0.28}Ga_{0.72}N$/AlN layers, there is less Al volume beneath the metal contact. As a result, a greater quantity of alloy, and therefore greater alloy thickness, is formed during the annealing process; i.e. 75 % etching depth has greater alloy thickness than 0 % (no etching).

Two analytical methods (TLM and Tri-layer TLM) are used in order to fully understand the mechanisms of contact resistance reduction through the proposed Ohmic contact optimisation.

A. Transmission Line Model (TLM)

The TLM makes use of an ungated HEMT, consisting of only Ohmic contacts (i.e. source and drain terminals), in order to measure its electrical properties and the quality of its Ohmic contacts [211]. The ungated HEMT shares the same name as the model used for measurement and will be referred to as an AlGaN/GaN TLM.

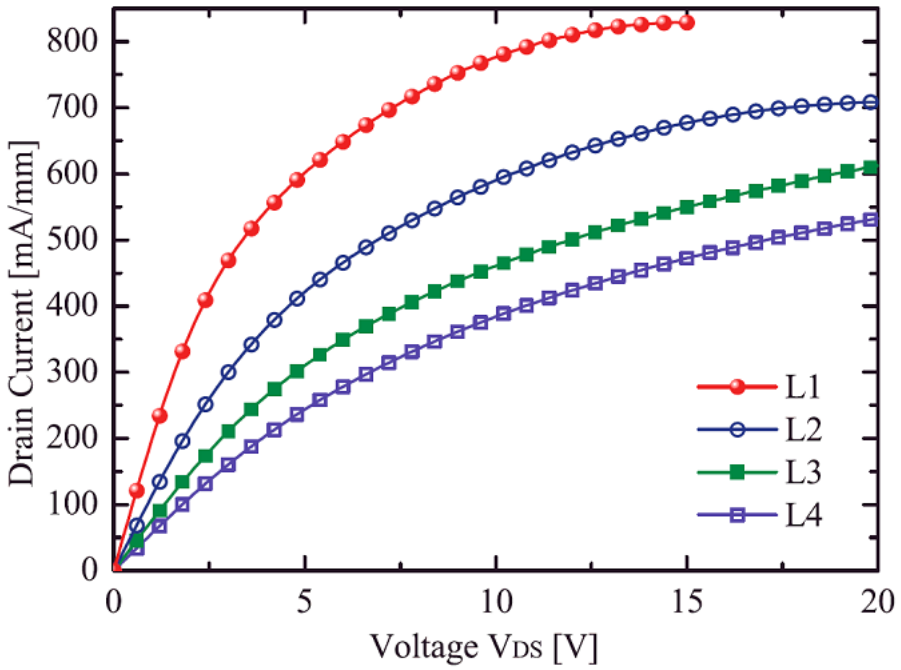

Figure 5.5: An example of the I_{DS} – V_{DS} characteristics of an ungated HEMT and gated HEMT with similar structure. Negative resistance is seen in the gated HEMT due to the increased temperature induced by the increased electric field peak.

The total resistance between the two Ohmic contacts of an AlGaN/GaN TLM, R_T, is extracted from the linear region of the I – V characteristics of devices at different lengths, Figure 5.5. The total resistance (R_T) is given by the following equation:

$$R_T = 2R_C + \frac{R_{sh}L_{SD}}{W} \tag{5.1}$$

where R_C is the Ohmic contact resistance, R_{sh} is the semiconductor sheet resistance between the Ohmic contacts, and W is the width of the Ohmic contact. To note, the current flow outside the device width (W) is eliminated via device-to-device isolation via implantation.

In order to calculate R_C, the R_T is extracted for various L_{SD}. An illustration of the resultant graph is given in Figure 5.6(a). The slope of the resulting R_T vs. L_{SD} graph is given as R_{sh}/W and the y-intercept is given as $2R_C$.

R_C is then given by:

$$R_C = \frac{R_{sk}L_T}{W} \tag{5.2}$$

where R_{sk} is the semiconductor sheet resistance beneath one Ohmic contact, and L_T is the transfer length. Current flow beneath the contact decays exponentially from the inner end of the contact towards the outer end. Therefore, L_T is the length in which the current beneath the contact falls to $1/e$ of the highest current, given at the inner ends of the contacts, as it transfers to the metal layer. The transfer length $\left(L_T = \frac{R_C W}{R_{SK}}\right)$ is proportional to R_C.

In order to identify and analyse the influence of the etched depth on alloy thickness and R_C, the TLM model, illustrated in Figure 5.6(a), is used [211]. R_C is extracted for each etched depth and at different annealing temperatures ranging from 750 °C to 900 °C. To apply the TLM, the spacing between the ohmic contacts, L_{SD}, is varied from 5 µm to 50 µm as shown in Figure 5.6(b).

B. *Tri-Layer Transmission Line Model (TLTLM)*

In the case of AlGaN/GaN Ohmic contacts, where an alloyed layer can be formed, a more comprehensive model is needed. This model is known as a Tri-layer Transmission Line Model (TLTLM). The two interfaces, (i) alloy/semiconductor and (ii) metal/alloy, are considered in this model. The TLTLM allows for current distributions to be extracted by modelling the alloyed layer and the non-alloyed semiconductor layer to have separate and identifiable sheet resistances.

The schematic cross section of an alloyed Ohmic contact and its corresponding TLTLM electrical network representation is given in Figure 5.7. Here, the specific contact resistance of the alloy/semiconductor interface (ρ_{cu}) and of the metal/alloy interface (ρ_{ca}) has a voltage drop across each interface. The current, therefore, flows laterally through the sheet resistance of the alloy/semiconductor interface (R_{su}) and of the metal/alloy interface (R_{sa}); represented as i_1 and i_2, respectively. The vertical current through the contact at the metal/alloy interface is given by i_3. The total contact current flowing in/out of the contact (i_0) is given as:

$$i_0 = i_1(x) + i_2(x) + i_3(x) \qquad (5.3)$$

where x is the distance between the leading edge of the contact ($x = 0$) and the desired current extraction location within the contact. i_0 is independent of x and is a unit value.

An important factor for the distribution of current throughout the contact is the resistance of

the alloy sidewall of the contact (R_f). A fraction of total current enters the sidewall ($i_0(1-f)$), which is a function of the alloy depth (t_d). Assuming that the current density across the area of the sidewall ($W \cdot t_d$) is uniform, R_f is calculated as:

$$R_f = \rho_{cu}/(W \cdot t_d) \qquad (5.4)$$

In order to calculate the current division factor (f), the two entry points at the alloy/semiconductor interface ($i_0 f$) and metal/alloy interface ($i_0(1-f)$) are extracted through R_f. The resistive network is then solved to find i_1, i_2, and i_3 from the derivation of current flow given in [211].

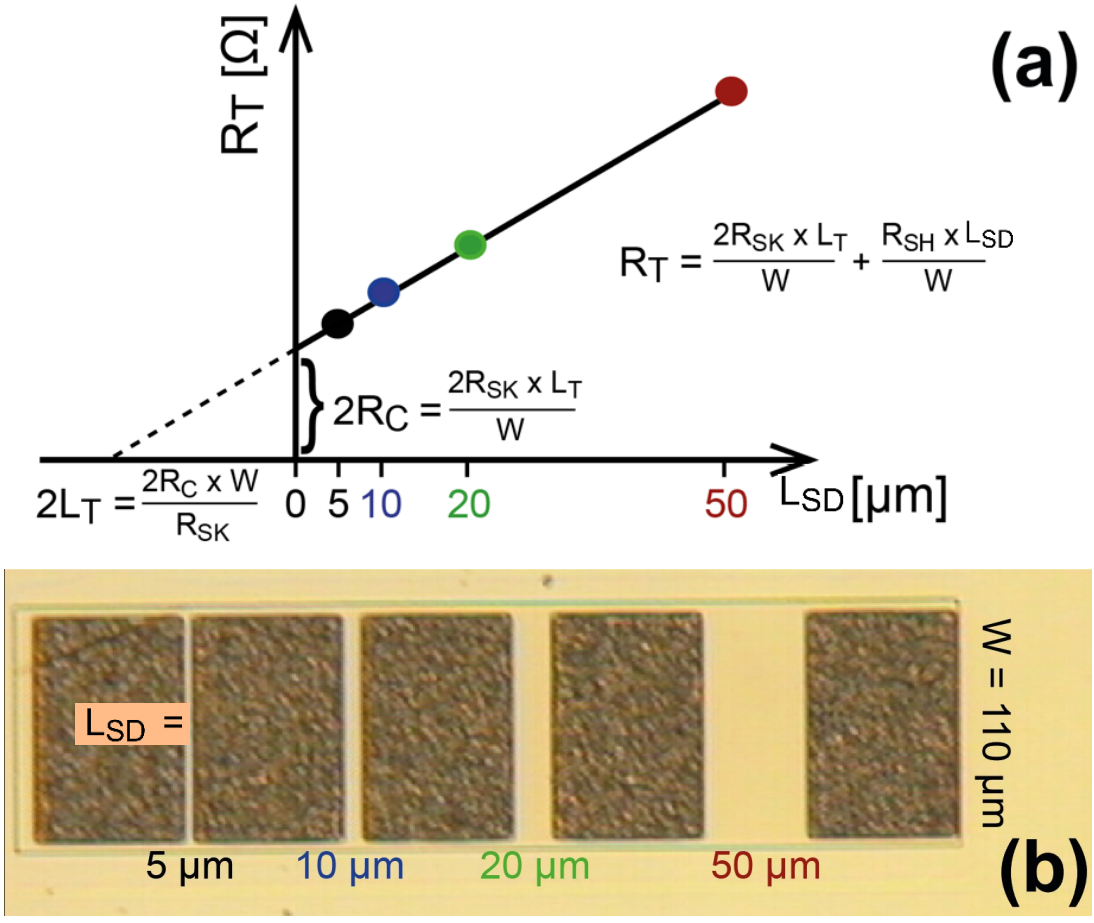

Figure 5.6: (a) Illustration of the TLM model, showing equations for extraction of its parameters (R_C, R_{SH}, R_{SK}, L_T). (b) top-down view of used TLM and dimensions for parameters extraction.

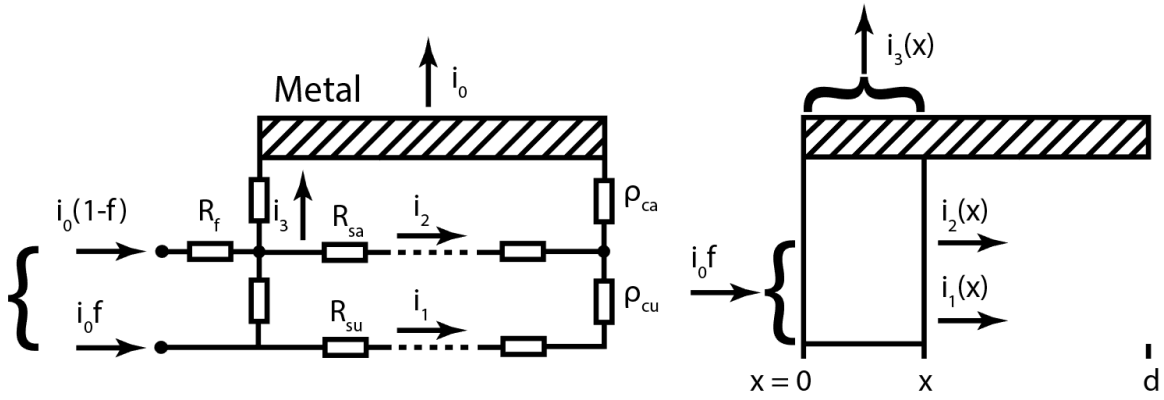

Figure 5.7: TLTLM electrical network, showing alloy/semiconductor and metal/alloy sheet resistances (R_{sa} and R_{su}), resistivities (ρ_{ca} and ρ_{cu}), and current flow ($i_0 f$ and $i_0(1-f)$), respectively. Additionally, R_f is shown [211].

5.2.1.3. Optimal Contact Resistance

Figure 5.8 represents the R_{SK}/R_{SH} ratio as a function of R_C to denote the impact of sheet resistance beneath the contact extracted using the TLM method. The different data points at each recess depth correspond to different annealing temperatures. At recess depth of 0 %, 25 % and 50 %, there is relatively a small metal diffusion and, consequently, the contact metal is away from the 2DEG. This is due to the large Al volume beneath the metal contact, which induces less reactivity in Ti as described in Section 5.2.1.1. Therefore, the AlGaN barrier layer is the limiting factor for current to flow and hence $R_{SK} \approx R_{SH}$. R_{SK} is only greater than R_{SH} at 75 % etching depth, where only 25 % of the barrier is left. This occurs due to bombardment of Ar^+ ions that partially destroys the crystal alignment near the 2DEG during the etching process [210]. However, in this case, there is a small distance between the diffused metal and the 2DEG due to the large alloy thickness that has formed. Hence, there is an overall reduction of R_C. Like all etching depth configurations, the ohmic contacts for '75 % etching depth' are annealed at different temperatures (blue sphere symbols in Figure 5.8). As the annealing temperature increases, the alloy thickness increases as well as the void formation. This results in poorer alloy quality which increases R_{SK} but the alloy becomes increasingly closer to the 2DEG, reducing R_C further. For '75 % etching depth' configuration, the optimal annealing temperature, to provide lowest $R_C \approx 0.3$ Ω.mm, that forms an alloy close enough to 2DEG with less crystal alignment damage, is found to be 850 °C. It is noted that the annealing temperature has a greater impact on '75 % etching depth' devices, when excluding the non-ohmic contacts.

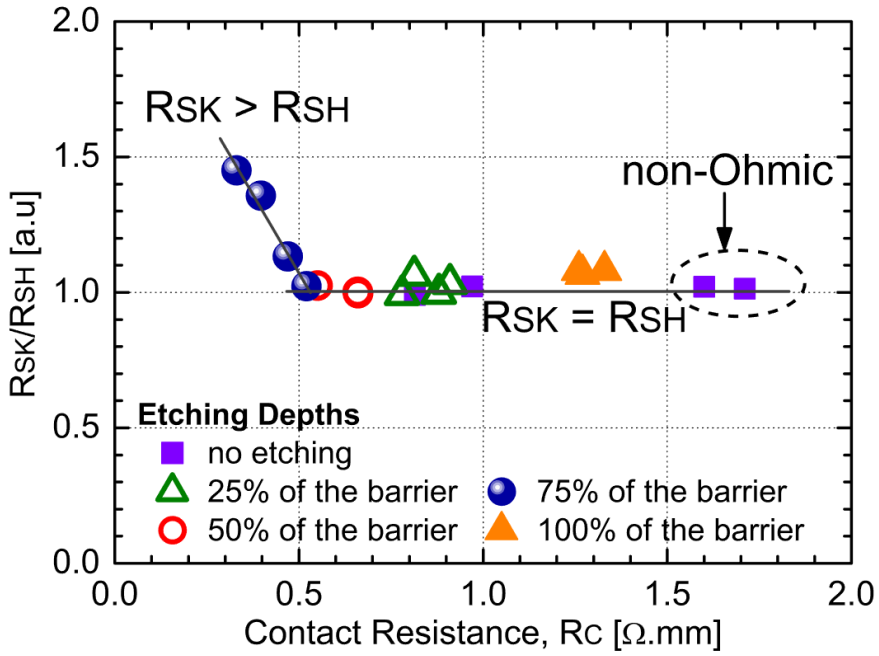

Figure 5.8: Ratio of R_{SK}/R_{SH} versus R_C. The different data points at each etching depth correspond to different annealing temperatures. 75 % etching depth provides $R_{SK} > R_{SH}$ whereas other etching provides $R_{SK} \approx R_{SH}$. This is due to (i) minimal diffusion of alloy and a large volume of AlGaN barrier beneath the contact in 0 %, 25 % and 50 % etching, and (ii) damage to the 2DEG in 100 % etching.

It could be expected that at 100 % etching depth there would be the lowest R_C and $R_{SK} > R_{SH}$, which is not the case. As the GaN/$Al_{0.28}Ga_{0.72}$N/AlN layers are completely etched at the contact locations (see Figure 5.4(e)), the 2DEG at the contact is destroyed. On top of this, current flow can only access the contact at its inner edge as opposed to the whole contact width of the alloy/AlGaN interface. These contribute toward the significant increase of R_C. To note, R_{SK} is slightly larger than R_{SH} for 100 % etching as the AlGaN barrier has been completely etched. Therefore, in this instance, R_{SK} only considers the sheet resistance of the alloy and GaN buffer layer; both of which have higher resistance than AlGaN.

5.2.1.4. Current Distribution throughout Ohmic Contact

The current distributions in the contact of '75 % etching depth' with the lowest R_C is calculated using the TLTLM model, previously described. Figure 5.9 presents the lateral current distributions at the alloy/AlGaN interface (i_1), the metal/alloy interface (i_2), and the vertical current at the metal/alloy interface (i_3). These results show an exponential decrease in current dispersion which occurs in i_1 as the majority of current enters the inner edge of the contact.

The current density at the inner edge is at its peak across the lateral span of the contact. The high resistance alloy limits the current flowing through to the metal contact at the inner edge. Current flows laterally away from the inner edge in the alloy/AlGaN interface to where lower resistance alloy clusters have formed. Then current is able to flow vertically through the metal layer and therefore an exponential increase in i_3 occurs.

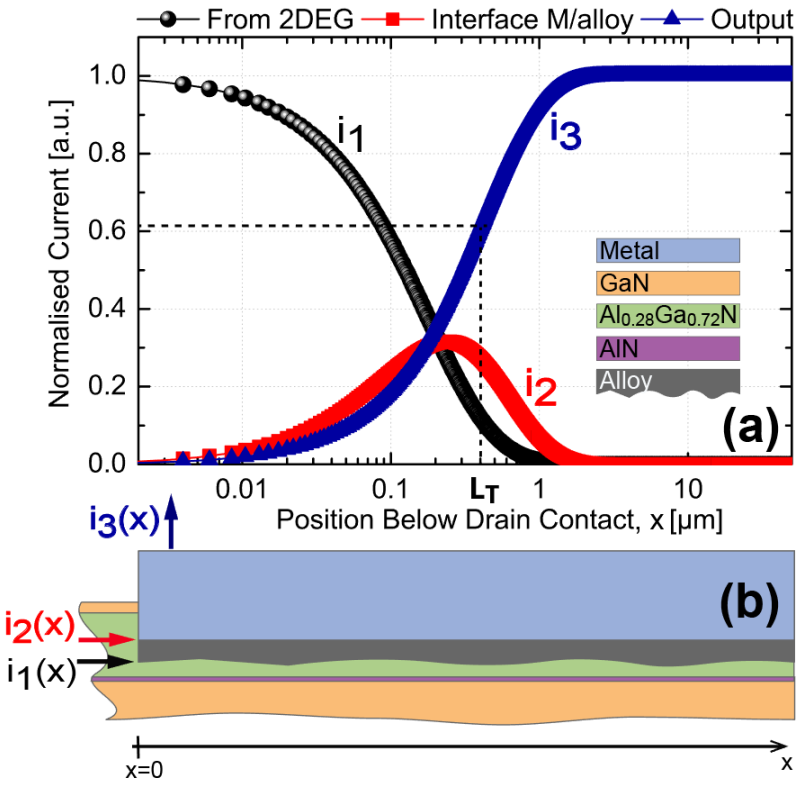

Figure 5.9: (a) Lateral current distribution at the alloy/AlGaN interface (i_1), at the metal/alloy interface (i_2), and the current entering/exiting in/out of the contact (i_3). (b) Illustration of the corresponding current distributions for i_1, i_2, and i_3.

5.2.1.5. Transfer Length of Ohmic Contact

The transfer length (L_T), that characterises the current distribution beneath the contact [212], is found to be ~0.4 μm for the lowest R_C configuration. To illustrate the relationship between L_T and etched barrier depth, 2D drift-diffusion simulations have been carried out. 2D distributions of the current density for 0 % and 75 % etched barrier depths are shown in Figure 5.10. This shows that with increased etching depth (e.g. 75 %) then L_T reduces. With deeper etching depth, a greater electric field is induced between the metal/alloy and the 2DEG and more energy is induced for charge carriers to enter/exit into or

out of the contact at its inner edge, not shown. Hence, the current density at the inner edge of the contact will be higher, reducing R_C.

Using the TLM model, L_T is extracted and compared with R_C for each ohmic contact configuration, etching depth and annealing temperature, in Figure 5.11. As expected, L_T is generally proportional to R_C, independently of the contact configuration. However, a significant issue may occur with low L_T. A high current density at the inner edges of the contact could result in a large increase in self-heating at this location, this was investigated in more details in Chapter 3. The heat dissipates throughout the device and contributes to degradation and potential failure of the device [140].

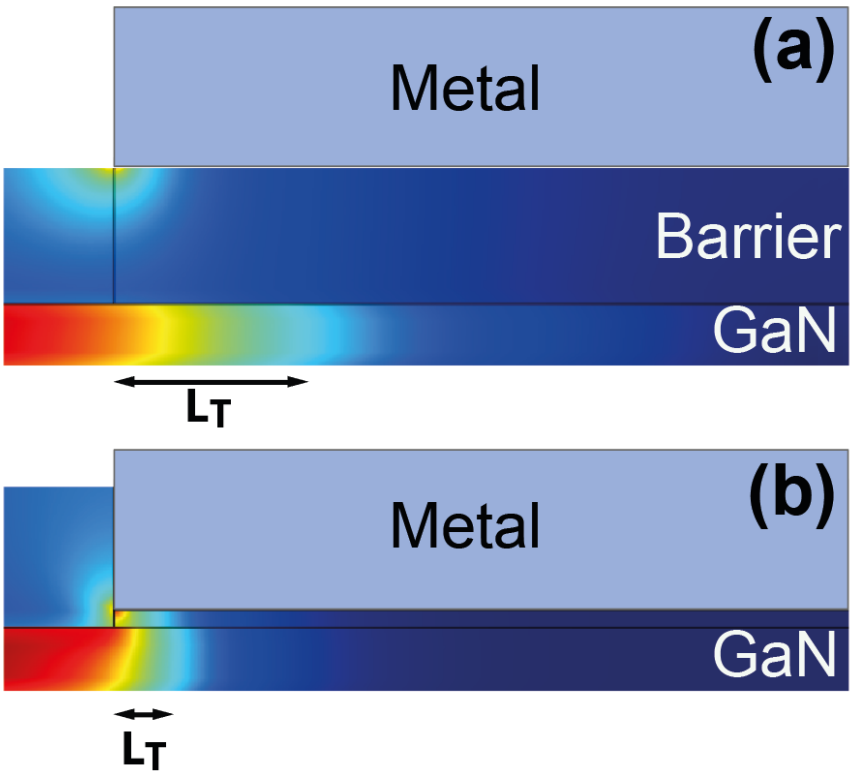

Figure 5.10: 2D current density distributions of two Ohmic contact configurations (a) 0 % and (b) 75 % etched barrier depths. The L_T decrease as etching depth increases is caused by larger electric field between the contact metal and 2DEG.

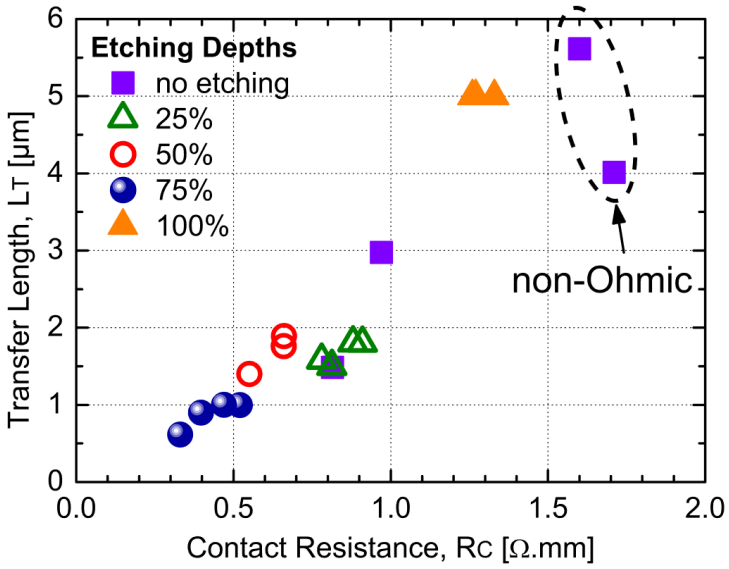

Figure 5.11: Calculated L_T versus measured R_C. Device with 75 % etching depth has the lowest R_C at 850 °C annealing temperature [211].

5.2.2. Contact Overgrowth for Self-Heating Reduction

Although low R_C has been achieved through etching Ohmic contacts to 75 % of the barrier layer, Section 5.2.1, the issue of increased temperature due to reduced L_T is now addressed. The reduced L_T with reduced R_C results in larger peaks in temperature at the inner ends of the Ohmic contacts due to the increased electron density in the local area. We aim to reduce this electron density whilst maintaining the low R_C achieved from Section 5.2.1.3. To manage the thermal issue, we propose an enhanced device architecture.

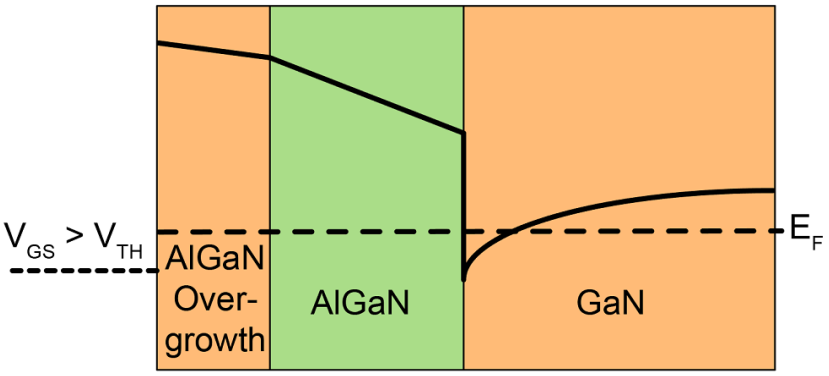

Figure 5.12: Conduction band through the metal/overgrowth layers showing the difference in conduction between the two.

The effect that this overgrowth layer has on its vertical conduction band is illustrated in . From this, we can see that from the metal/overgrowth interface onwards that the conduction band slightly increases, maintaining negligible increase in resistance.

In order to confront the issue of small L_T that causes high current density at the inner-end of the contact, and therefore high temperature in the local area, we extend the overgrowth layer from the metal towards the AlGaN barrier at an angle, illustrated in Figure 5.13. With this modification, the vertical electric field significantly reduces from the inner edges of the overgrowth/channel interface towards the inner edges of the metal/overgrowth interface when compared to the conventional HEMT. Therefore, with increased L_T, the temperature peaks at the inner edges of the S/D contacts, discussed in Chapter 3, can be reduced.

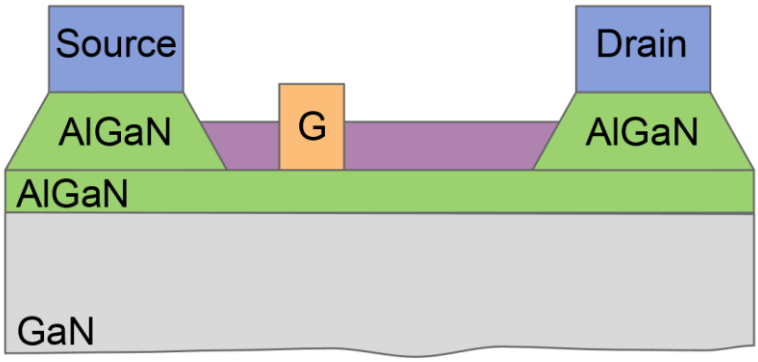

Figure 5.13: Enhanced overgrowth architecture whereby overgrowth layer is grown at an angle to reduce lateral electric field peak.

5.3. Schottky Contact Optimisation for Gate Leakage Reduction

The optimisation of Schottky contacts is crucial for gate control in GaN-based HEMTs in order to achieve high frequency and power performance. To realise this aim, the gate leakage current is required to be reduced in order to reduce breakdown voltage and, thus, improve microwave power performance. Normally-ON devices suffer from large gate leakage that stems from low Schottky barrier height, which is enhanced with the high negative gate bias required to switch the device to the 'OFF' state. For the AlGaN/GaN HEMTs, the threshold voltage is V_{TH} < -3 V.

In ideal devices, the Schottky barrier is defined as the difference between the work function of the gate metal and the electron affinity of the semiconductor, as described in Section 2.2.5.2. However, the above theory is not always true, as demonstrated in Figure 5.14, showing the Schottky barrier height of various metals deposited on AlGaN against their work function.

Therefore, using high metal work function to improve Schottky barrier height may not always be the solution towards optimising Schottky contact metallisation. This can be seen when comparing the theoretical results extracted from Eqn (2.10) where $x_{Al_{0.3}Ga_{0.7}N}$ = 2.3 kJ mol^{-1}. Refractory metals with high work function such as Mo, Ni, or Pt are commonly deposited after the native oxide of the AlGaN top surface is removed to fabricate rectifying contacts [213], [214]. However, these high work function metals do not necessarily increase the Schottky barrier height. Metals that have high Schottky barrier height such as Cu, however, have relatively high leakage current due to roughness at the metal/AlGaN interface. Instead, a new TiN Schottky contact metallisation is proposed in order to provide high Schottky barrier height and linearity and low gate leakage of AlGaN/GaN HEMT devices. The purpose for using TiN is due to its thermal stability and its low interface roughness when annealed to AlGaN. TiN has a low work function, which would be an issue in terms of obtaining a high Schottky barrier if the theoretical relationship between Schottky barrier height and work function was true experimentally. However, since Figure 5.14 shows that this relationship is not the case experimentally then the work function is not relevant towards our aim of increasing Schottky barrier height. Instead, the Schottky barrier height is increased by creating a Schottky diode at the TiN/AlGaN interface through quasi p-type dopants, described in Section 5.3.4.1.

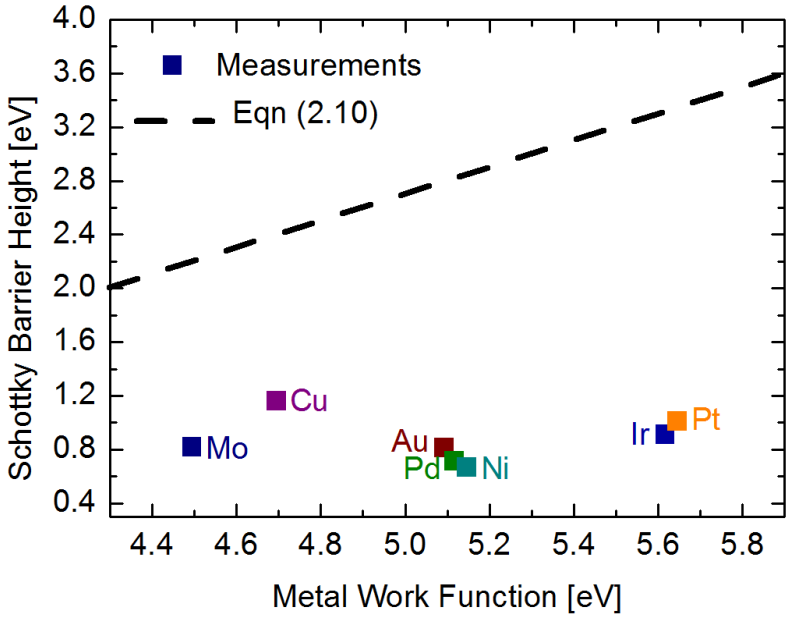

Figure 5.14: Relationship between Schottky barrier height and work function for various metals that are deposited on AlGaN layer obtained via I – V. No clear correlation is shown compared to theoretical results from Eqn (2.10) where $x_{Al_{0.3}Ga_{0.7}N}$ = 2.3 kJ mol^{-1}.

5.3.1. Current Schottky Contact Technology

On AlGaN/GaN epitaxies, the Schottky contact constitutes a difficult technological step; especially on epitaxies grown by MBE. In the past, several works were carried out to optimise the Schottky contact and understand the contact formation and conduction mechanisms. Post annealing at high temperature after depositing metal is the common method used to improve the Schottky contact behaviour [204], [215]–[219]. Some authors proposed to deposit a material such as copper (Cu), Al or SiN between the Schottky metal and the semiconductor to pump the surface oxygen. This generates n-type doping at the metal/semiconductor interface, which forms an ultra thin interfacial oxide layer (~1 nm) such as CuOx, AlOx and SiOx after applying high temperature annealing in a vacuum [216], [217], [220]–[222]. Other propositions add nitrogen on surface to fill in the nitrogen vacancies. This forms n-type doping, which results in the reduction of Φ_{bn} via the shift of Fermi level near to the conduction band [204], [216]–[219], [222]–[225]. Other works proposed to deposit a thin oxide layer such as TiO_2, Al_2O_3 [16], [107], [140], [199], [200], [204]–[207], [209]–[212] or to form an oxide layer from an O_2 annealing [218] or a chemical treatment [223]. Another method consists of removing the native oxide at the surface of AlGaN by a chemical pre-treatment [213], [214], [222]. Lastly, a low temperature GaN cap can be grown [226]. With these works, $I_{leakage}$ and the Φ_{bn} can be improved but it requires a complicated technological process. Therefore, we propose a new and simple method of forming a TiN-based Schottky contact on an AlGaN barrier.

5.3.2. TiN Gate Technology

5.3.2.1. Device Fabrication

We propose a rectifying contact that is formed by Au/TiN sputtering and then lift-off using optical and e-beam lithography for a 2 µm and 100 nm gate length, respectively. The optical lithography is a quick process that is easy to perform and cost-effective for technological optimisation. As for e-beam lithography, this process is more accurate for devices with gate lengths of a few hundred nanometers. The e-beam lithography is performed under the following conditions: 100 W radio frequency power at 13.56 MHz, 30 sccm argon (Ar) flow, and 220 V DC bias for an initial pressure of 3×10^{-7} mbar. The deposition rate is around 3.4 nm min^{-1}.

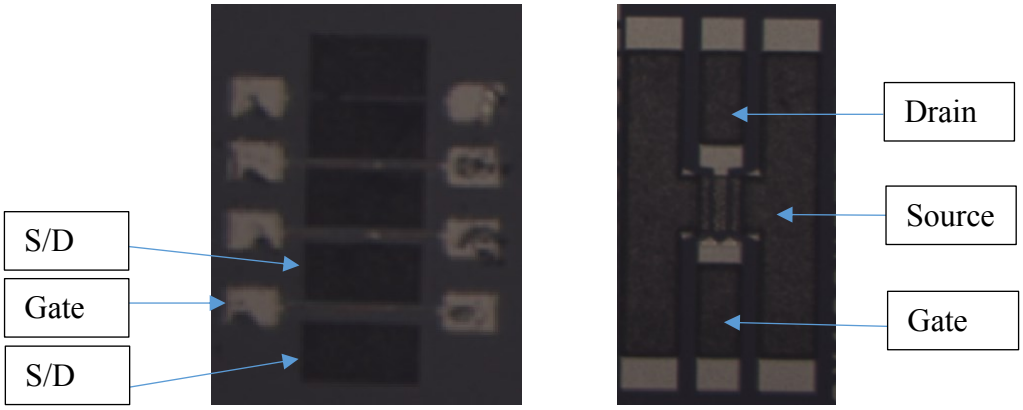

Figure 5.15: Overview of AlGaN/GaN G-TLM (left) and HEMT (right).

The fabricated structures are known as Gate Transmission Line Method (G-TLM), where the source-to-gate distance is 1 µm. An overview of an AlGaN/GaN G-TLM and HEMT is given in Figure 5.15 The average value of R_C is 0.7 Ω.mm and is associated to ρ_C of 9×10^{-6} Ω.cm^2. From Hall measurements, a 2DEG sheet density of 8×10^{12} cm^{-2}, a carrier mobility of 1670 cm^2 $V^{-1}s^{-1}$ and a sheet resistance of 490 Ω sq^{-1} are obtained. The threshold voltage, $V_{TH} \approx$ -2.7 V. Before the gate metallisation, samples are deoxidised using a HCl:H_2O (1:1) solution for 90 s, followed by in-situ Ar^+ plasma etching at 150 W for 20 s, corresponding to 510 V DC bias, with an argon gas flow keep at 25 sccm.

5.3.2.2. TiN Conduction Mechanisms

We aim to achieve a gradient of strain within the AlGaN barrier layer in order to induce quasi p-type dopants that act as a Schottky diode around the TiN/AlGaN interface as shown in Figure 5.16(a). Firstly, AlGaN is succumb to tensile strain when grown upon GaN. In order to compensate for this, the TiN layer is required to have compressive strain with the same

amplitude as the tensile strain of the AlGaN barrier layer as shown in Figure 5.16(b). This achieves a high preservation of strain within the TiN layer. Finally, Figure 5.16(c) shows that a high strain preservation can be achieved by lowering the TiN thickness. In addition to this, the target-substrate distance can be changed to preserve the strain.

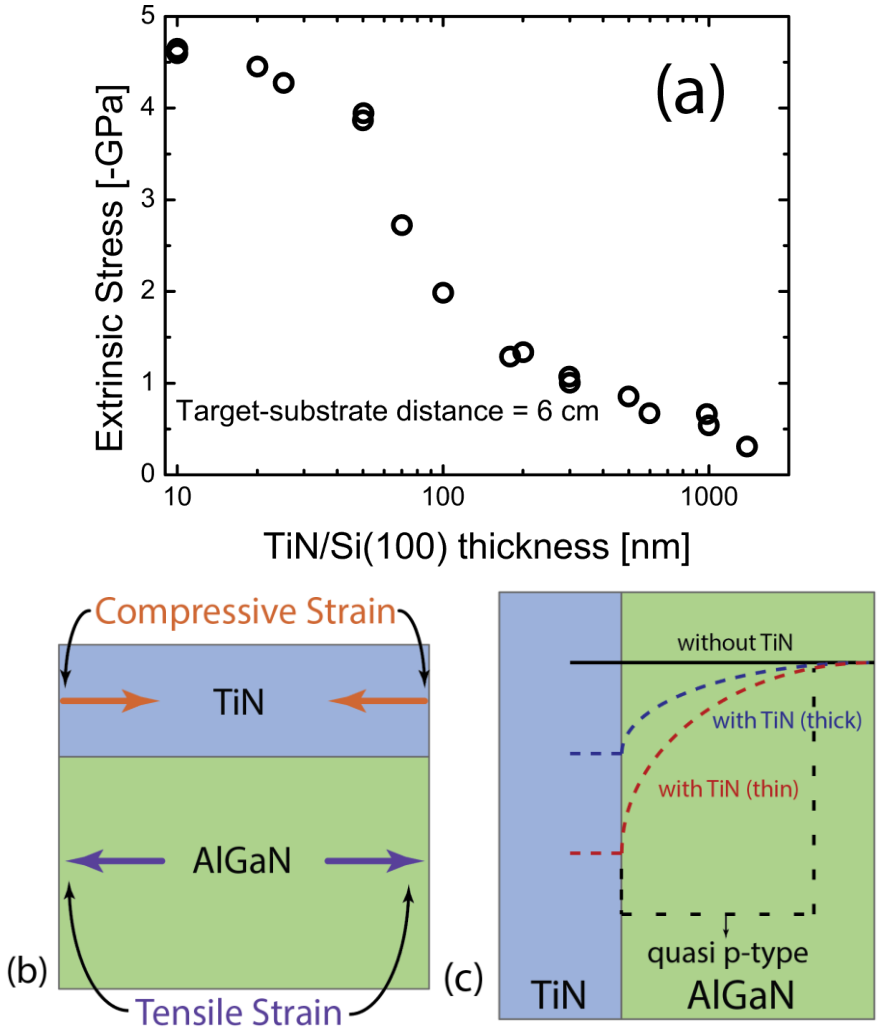

Figure 5.16: (a) Impact of TiN thickness on extrinsic stress within TiN layer, (b) types of strain occurring within TiN and AlGaN layers, (c) strain gradient within AlGaN layer with thinner TiN layer that generates quasi p-type dopants.

It is well known that TE and TFE conduction mechanisms are dominant for TiN Schottky contacts. The two probable conduction mechanisms for Schottky contacts are TE and TFE, indicated by ① and ②, respectively, in Figure 5.17, the annealing effect alters the state of the AlGaN surface. This has been suspected to form a TiO_2 layer between TiN and AlGaN (Figure 5.17(b)) However XPS data given in Section 5.3.4 shows that there is no TiO_2 layer. Instead,

after annealing the TiN metallisation, the strain at the surface of the AlGaN barrier layer is reduced, as described in Section 3.2.2.3. This reduction causes a strain gradient in the AlGaN barrier that leads to quasi-p-type doping due to conduction band edge lowering at the AlGaN barrier surface, as illustrated in Figure 5.16(c). The effect of this conduction band lowering is a Schottky diode-like behaviour (Figure 5.17(c)) whereby leakage current is severely limited.

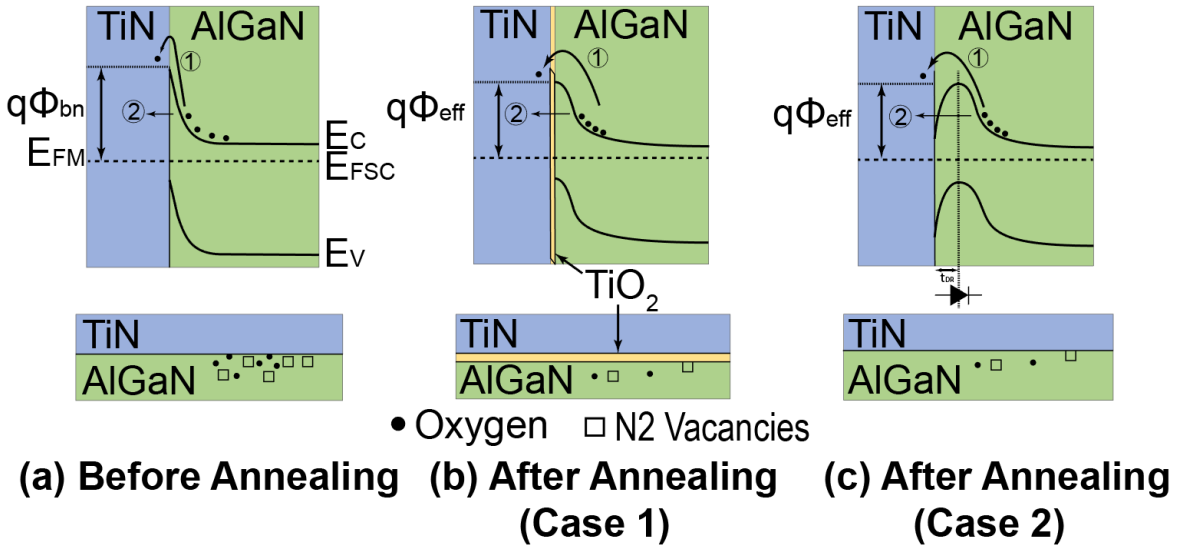

Figure 5.17: Conduction mechanism of TiN Schottky contact on $Al_{0.32}Ga_{0.68}N$/GaN HEMT (a) before annealing, (b) after annealing with TiO_2 layer, and (c) after annealing without TiO_2 layer, where t_{DR} is the depletion region thickness.

5.3.3. Device Performance

Measurements of Φ_{bn}, ideality factor (η) and gate leakage current ($I_{leakage}$) are taken at various annealing and deposition stages for a range of TiN thicknesses from 2.5 to 60 nm. The $I_{GS} - V_{GS}$ is usually used to extract η of Schottky barrier diodes where the slope of the linear region gives $q/\eta kT$. The gate leakage current is given at V_{GS} = -30 V. A summary of the process and measurements for each TiN thickness for L_G = 2 µm is given in Table 5.1 – Table 5.3. To note, the fabrication process for all TiN thicknesses have been optimised for 5 nm. This was done because it was known that strain preservation, later described in this Section, could be achieved at low TiN thicknesses. To note, the process could be optimised for 2.5 nm TiN thickness to potentially achieve better properties than shown in Table 5.1.

Prior to annealing, a relatively low Φ_{bn} with $I_{leakage}$ in the order of uA is observed for all TiN

thicknesses. In addition, the Schottky contact also has the behaviour of a quasi-Ohmic contact, since η is greater than 4 for all devices. After annealing at 500 ºC for 40 mins in an N_2 atmosphere, good results have been obtained when the TiN thickness is less than 10 nm. It appears that for these TiN thicknesses (< 10 nm), SiO_2/Si_3N_4 passivation does not help to improve the Schottky contact, it instead degrades. To recover these degraded properties, the devices were annealed at 350 ºC for 72 hours under N_2 conditions. From the above tables, it is clear that annealing at higher temperature (> 690 ºC) causes significant degradation of the Schottky contact properties.

Table 5.1: The impact of annealing and passivation on Schottky barrier height, linearity and gate leakage for TiN thicknesses of 2.5 nm and 5 nm at L_G = 2 µm.

	TiN Thickness 2.5 nm			TiN Thickness 5 nm		
	Φ_{bn} [eV]	η	$I_{leakage}$ [A/mm]	Φ_{bn} [eV]	η	$I_{leakage}$ [A/mm]
Before Annealing	0.584	14.31	810 µ	0.507	9.69	3 m
Annealing 500 ºC for 40 mins in N_2	0.878	2.17	70 n	**1.059**	**1.60**	**60 n**
SiO_2/Si_3N_4 Passivation deposition	0.821	2.05	4 µ	0.869	1.99	370 n
Annealing 350 ºC for 72 h in N_2	0.769	2.57	560 n	1.064	1.46	100 n
Annealing 350 ºC for 3 weeks in N_2	0.695	7.64	270 n	0.905	1.87	130 n
Annealing 690 ºC for 40 mins in N_2	0.433	14.42	840 µ	0.386	15.84	2 m

Table 5.2: The impact of annealing and passivation on Schottky barrier height, linearity and gate leakage for TiN thicknesses of 10 nm and 20 nm at L_G = 2 µm.

	TiN Thickness 10 nm			TiN Thickness 20 nm		
	Φ_{bn} [eV]	η	$I_{leakage}$ [A/mm]	Φ_{bn} [eV]	η	$I_{leakage}$ [A/mm]
Before Annealing	0.637	8.70	150 µ	0.635	4.15	70 µ
Annealing 500 ºC for 40 mins in N_2	**0.810**	**2.37**	**210 n**	0.800	1.97	910 n
Annealing 690 ºC for 40 mins in N_2	0.896	1.61	150 n	0.793	2.23	370 n
Annealing 800 ºC for 40 mins in vacuum				0.477	6.53	380 µ
SiO_2/Si_3N_4 Passivation deposition	0.892	1.60	850 n			
Annealing 350 ºC for 72 h in N_2	0.889	1.63	130 n	0.777	2.07	2 µ
Annealing 350 ºC for 3 weeks in N_2	0.899	1.61	120 n	0.717	2.63	660 n

Table 5.3: The impact of annealing and passivation on Schottky barrier height, linearity and gate leakage for TiN thicknesses of 40 nm and 60 nm at L_G = 2 µm.

	TiN Thickness 40 nm			TiN Thickness 60 nm		
	Φ_{bn} [eV]	η	$I_{leakage}$ [A/mm]	Φ_{bn} [eV]	η	$I_{leakage}$ [A/mm]
Before Annealing	0.661	4.21	90 µ	0.644	4.66	40 µ
Annealing 500 °C for 40 mins in N_2	0.829	1.97	150 n	0.796	2.13	40 µ
Annealing 690 °C for 40 mins in N_2	0.819	2.04	370 n	0.811	2.33	130 n
SiO_2/Si_3N_4 Passivation deposition	0.845	1.95	340 n	0.809	2.39	130 n
Annealing 350 °C for 72 h in N_2	0.845	1.91	570 n			
Annealing 350 °C for 3 weeks in N_2	0.832	1.98	360 n			

The optimal Schottky contact is obtained for when the TiN thickness is < 10 nm is marked in red. This is potentially due to the higher preservation of the strain within the TiN as its thickness is reduced, as shown in Figure 5.16(a). This is a strong indication that the obtained performance is related to the quality of the strain within the gate metal.

5.3.3.1. Charge Trapping

The overall performance of our optimal device (TiN thickness of 5 nm and L_G = 2 µm) is provided via Capacitance-Voltage (C – V), Conductance-Voltage (G – V) and I_D – V_D measurements. Figure 5.18 displays the C – V and G – V profiles. The measurement frequency range varies from 10 kHz to 1 MHz with an AC voltage amplitude of 10 mV. A time delay of 100 ms after setting the DC bias is used for all measurements. In enhancement regime, the capacitance is constant regardless of the frequency. This suggests that a negligible TiN diffusion forms within the AlGaN barrier layer, even at annealing at 500 °C. Furthermore, both forward and reverse DC bias sweeps were made and no hysteresis was observed. This indicates that very low trapping density forms at the TiN/AlGaN interface. The frequency dispersion of the corresponding conductance at $V_{GS} \approx$ -2 V suggests that deep traps are potentially located within the GaN buffer [204].

In order to test the effects of drain and gate lag at higher frequencies that are not reachable by the C – V technique, the I_{DS} – V_{DS} characteristics with several quiescent conditions are measured for V_{GS} = 0 V to -3 V with -1 V step, shown in Figure 5.19. The following quiescent biases are used (i) V_{DS0} = 0 V and V_{GS0} = 0 V used as a reference, (ii) V_{DS0} = 0 V and V_{GS0} = -3 V used to induce surface trapping, and (iii) V_{DS0} = 10 V and V_{GS0} = -3 V used to induce bulk

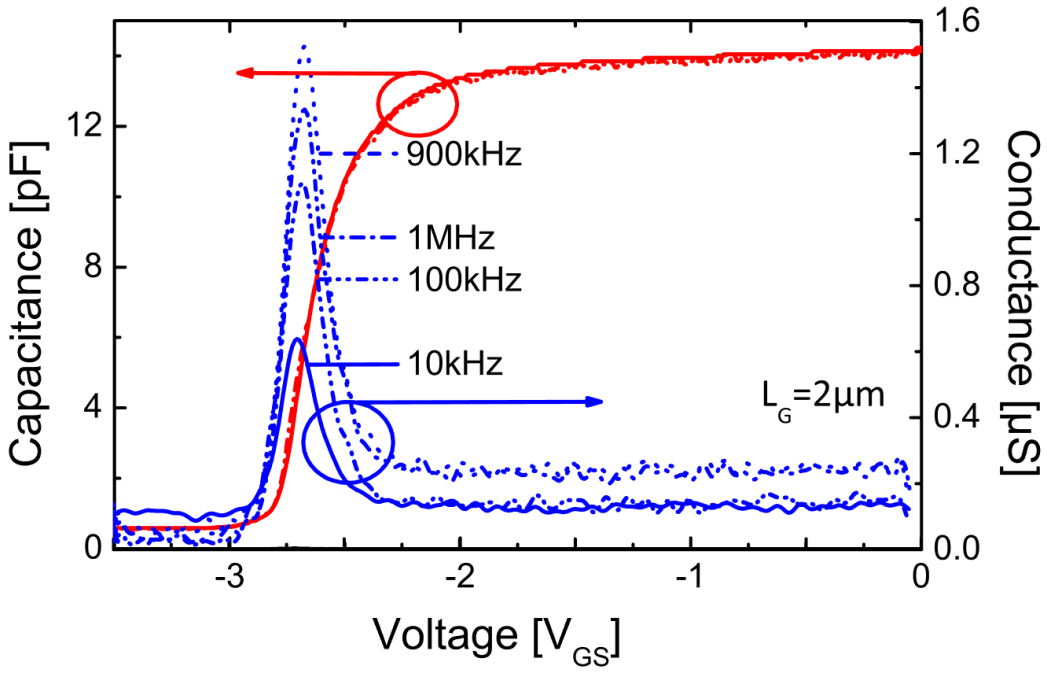

Figure 5.18: Post-annealing C – V and G – V characteristics of AlGaN/GaN HEMT with new TiN Schottky contact metallisation and TiN thickness of 5 nm as a function of frequency from 10 kHz to 1 MHz.

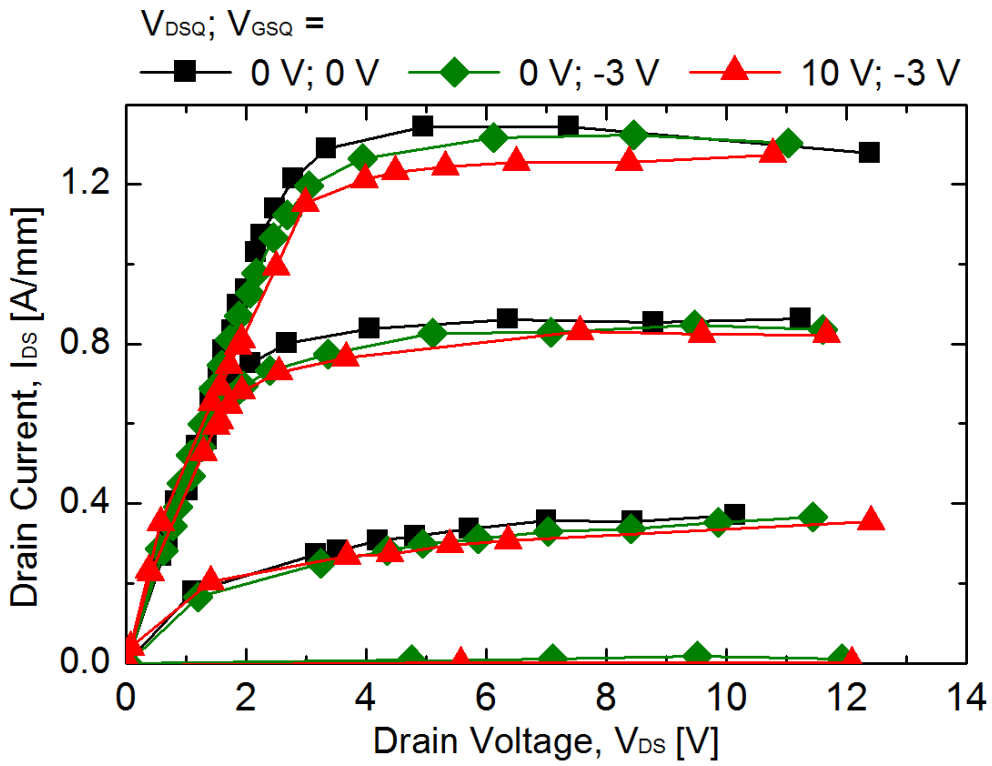

Figure 5.19: Post-annealing I_{DS} – V_{DS} characteristics of AlGaN/GaN HEMT with new TiN Schottky contact metallisation.

trapping and surface trapping. Each measurement is taken with a 200 ns pulse width and 20 % duty cycle (i.e. 1 µs period). From these results, we observe little degradation in current for all conditions, which shows that little bulk and surface trapping occurs within this device. The degradation of current has been significantly reduced as a result of implementing this new gate technology when compared to devices used in previous chapters.

5.3.3.2. Gate Length Consideration

This new Schottky process has first been tested using optical lithography (L_G = 2 µm) and then adjusted to analyse sub-micrometer gate length (L_G = 100 nm) devices using e-beam lithography.

For TiN thickness of 5 nm, a comparison between L_G = 100 nm and 2 µm before and after annealing is given in Figure 5.20. A large drop of the leakage current is observed after annealing with a great enhancement of Φ_{bn}. For L_G = 2 µm, the optimum values are obtained at 500 °C with a reverse leakage current of 10 nA mm^{-1} and Φ_{bn} of 1.06 eV associated to an ideality factor of 1.46. With regards to the 100 nm gate length, the optimum values are obtained at 600 °C with a reverse leakage current of 10 pA mm^{-1} and a Φ_{bn} of 0.94 eV associated to an ideality factor of 1.41. This shows a significant drop of $I_{leakage}$ (3 orders of magnitude) with respect to L_G = 2 um. This shows that this technique can be used for both small and large gate lengths.

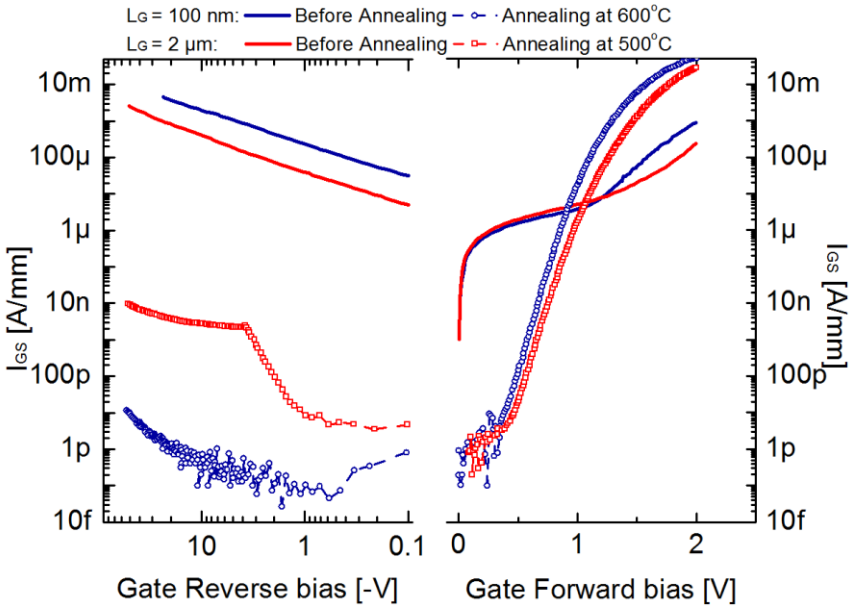

Figure 5.20: I_{GS} – V_{GS} measurement for different annealing temperature and gate length for TiN/Au Schottky contact and W = 100 µm [227], [228].

To note, the annealing temperature for each gate length is different to account for the difference in metal contact surface.

5.3.4. TiN Diffusion

X-ray photoelectron spectroscopy (XPS) data given by Figure 5.21 revealed two peaks of intensity at binding energies of 459 eV and 454.5 eV representing TiN at different orientations within (a) AlGaN barrier and (b) TiN layer. It is shown from Figure 5.21(a) that TiN diffuses into the AlGaN barrier layer, which contributes towards the strain gradient illustrated in Figure 5.16(c). This strain gradient is depicted through XPS data by the decrease in Ti2p intensity below 454.5 eV. As there is no change in characteristic of Figure 5.21(b) and no additional peak of intensity at 457.5 eV (binding energy of TiO_2) occurs, we determine that no oxidation of the TiN layer at the AlGaN surface occurs.

The XPS experiments are performed with a system based on 5600 Physical Electronics model operating at a base pressure of 2.5×10^{-10} mbar, employing a hemispherical analyzer and a monochromatic Al Kα excitation source (hν = 1486.6 eV). The pass energy is set at 12 eV. Under these conditions, the overall resolution as measured from the FWHM of the Ag $3d_{5/2}$ line is 0.45 eV. All XPS spectra are collected at an emission angle of 45 ° with respect to the surface normal. The Binding Energy (BE) scale is calibrated using the Au $4f_{7/2}$ peak position at 84 eV for a polycrystalline gold foil reference.

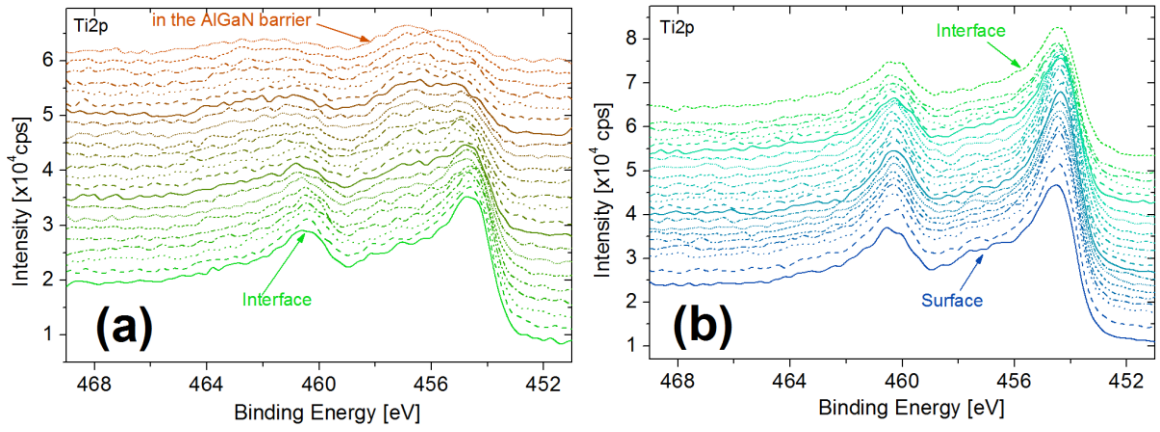

Figure 5.21: Ti2p spectrum in the (a) AlGaN barrier layer and (b) TiN layer.

5.3.4.1. Quasi-p-type Doping Layer

The log – log plot of the I_{GS} – V_{GS} characteristics, given in Figure 5.22(a), reveals two behaviours: (i) Ohmic contact behaviour ($V^{1.1}$ slope), followed by (ii) rectifying behaviour

($V^{18.5}$ slope). As the AlGaN layer is unintentionally n-type doped, the rectifying behaviour ($V^{18.5}$ slope) leads us to believe that doping modulation (quasi-p-type doping) occurs beneath the TiN layer. In addition, the beginning of this rectifying regime is shown to be temperature dependent (Figure 5.22(b)), which supports the theory of quasi-p-type doping. The raw data from which Figure 5.23(b) is extracted from is given in Figure 5.23. Finally, in support of Figure 5.24(a), the model given in [229] is used with the assumption of a depletion layer thickness of 5 nm to extract the n and p concentrations (Figure 5.24), which shows Schottky diode-like characteristics.

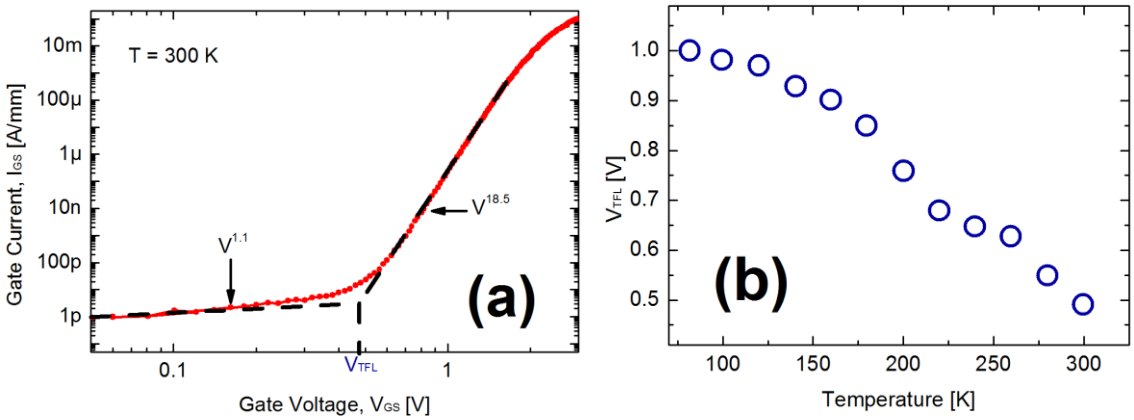

Figure 5.22: (a) $I_{DS} - V_{GS}$ characteristics, showing a rectifying behaviour with two mechanisms of current increase as a result of quasi-P/N junction of TiN/AlGaN. (b) Reduction of V_{TFL} with increased temperature, showing that these mechanisms impact the $I_{GS} - V_{GS}$ characteristics.

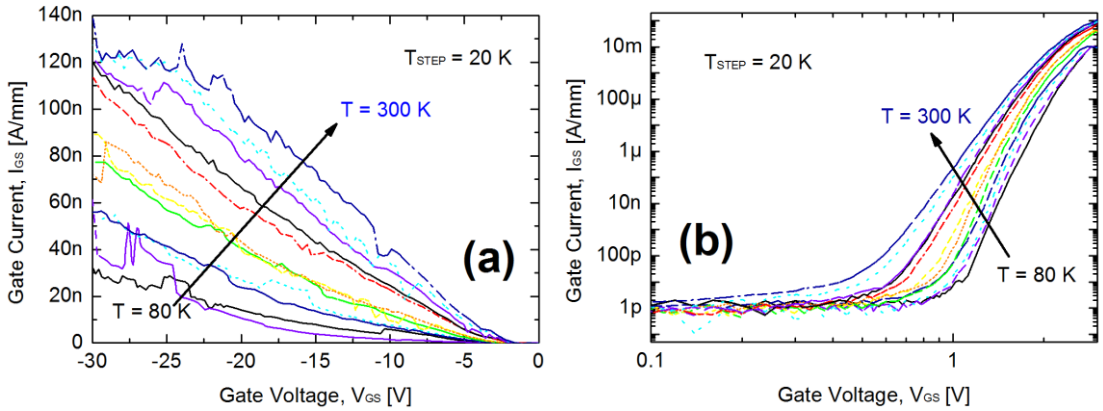

Figure 5.23: Raw data of (a) reverse current and (b) forward current under various temperatures.

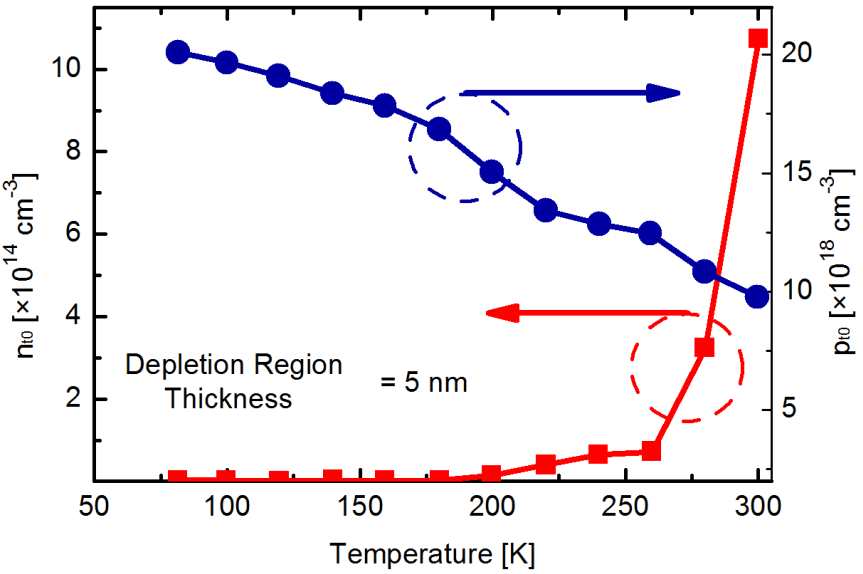

Figure 5.24: Extracted n and p concentration using the model given in [229] with Figure 5.22(b) whilst assuming a depletion layer of 5 nm, showing Schottky diode characteristic.

5.4. Step-Graded AlGaN Barrier with AlN spacer and InGaN channel Structure

New AlGaN/GaN HEMT structures are proposed to improve the performance and current handling capabilities. These device structures are simulated using Synopsys' Sentaurus TCAD to characterise their electronic properties. Through material and geometric optimisation, these structures achieve increased thermal conductivity, 2DEG density and charge carrier mobility compared to conventional AlGaN/GaN HEMT structures.

5.4.1. Device Structures

A conventional AlGaN/GaN HEMT structure is used to compare with the optimised structures, illustrated in Figure 5.25(a). Architectural additions to the conventional AlGaN/GaN HEMT are constructed to form optimised AlGaN/GaN HEMT structures. These newly proposed structures are illustrated in Figure 5.25(b)-(d) and descriptions of their architecture are provided in the following:

i. *Conventional HEMT* – A conventional $Al_xGa_{1-x}N$/GaN HEMT, where x = 0.25 are grown in the [0001] Ga-face direction on a Si substrate. The epi-structure consists of a 10 nm AlN nucleation layer formation after the substrate and an undoped GaN buffer layer with a thickness of 2.0 µm is grown after. Then, a thin channel layer of 5 nm is defined inside the buffer layer, followed by the growth of a thin AlGaN interfacial spacer layer of 2 nm. Finally, an 18 nm barrier layer of the device was

deposited with a 1 nm GaN cap layer and SiN passivation above the cap layer.

ii. *Structure 1* – Based on the structure of the conventional AlGaN/GaN HEMT, an additional step-graded $Al_xGa_{1-x}N$ barrier is formed in place of the AlGaN barrier, where x = 0.2 in the first layer, x = 0.35 in the second, and x = 0.5 in the third (from top to bottom). Each step-graded layer has a thickness of 6 nm. The increasing concentrations increase the strain within the barrier layer, due to increased lattice mismatch between the AlGaN barrier and GaN buffer, without succumbing to strain relaxation.

iii. *Structure 2* – Based on the structure of Structure 1, an AlN spacer is implemented into Structure 2 to improve the electron mobility. The implementation of the AlN spacer layer reduces the strain along the AlN/GaN interface [76], whilst improving the lattice of the AlGaN barrier layer. The strain reduction is a result of the larger lattice mismatch between the spacer and channel layer when compared with Structure 1.

iv. *Structure 3* – Based on the structure of Structure 2, an InGaN channel is implemented in Structure 3 to the lower conduction band energy compared to GaN, providing greater conduction band discontinuity between the channel and spacer layers. As a result, carrier confinement and high power capabilities are increased.

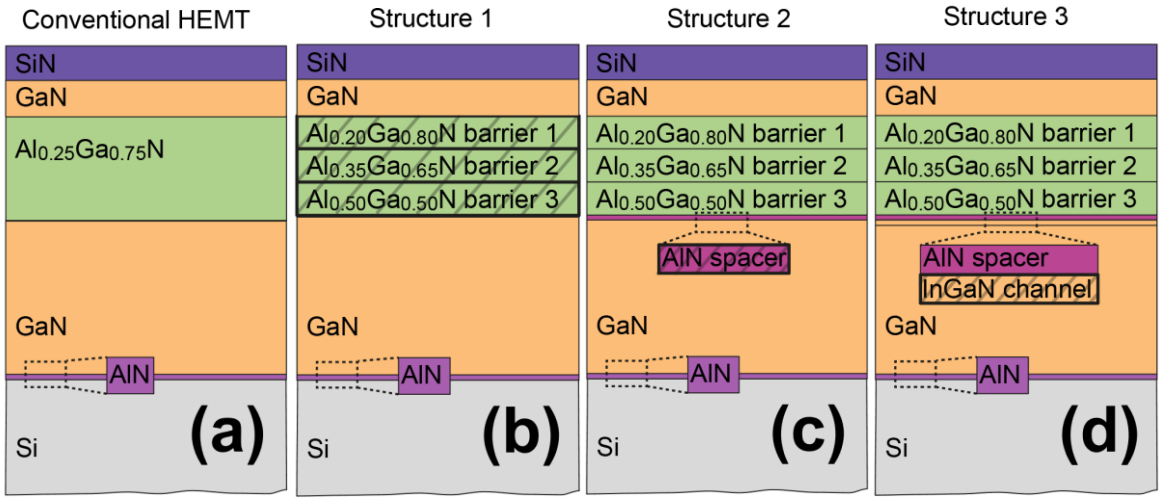

Figure 5.25: Schematic diagram of simulated GaN-based HEMT showing (a) conventional AlGaN/GaN HEMT; (b) step-graded AlGaN barrier layer – Structure 1; (c) AlN spacer layer – Structure 2; (d) InGaN channel layer – Structure 3. For conventional AlGaN/GaN HEMT: x = 0.25; for Structure 1 – 3: $x_1 = 0.2$, $x_2 = 0.35$, $x_3 = 0.5$.

5.4.2. Simulation Methodology

The new structures are simulated using the commercial 2D device simulation software Sentaurus Synopsys TCAD. The dimension and doping parameters used to build these structures are given in Table 5.4, where the gate contact of the device is set to be Schottky type with a metal work function, Φ_{MG} = 4.4 eV. The simulation flow for these structures is illustrated in Figure 5.26. The control parameters [230], namely the structure geometry, doping concentrations and Al mole fractions inside the barrier layer are defined. The layer epi-structure is then defined along with the type of materials, doping levels, mole fractions, and the meshing criteria of each region. Subsequently, emulations of source, drain and gate metallisation patterning is done and is used for interpreting electrodes and thermode of the devices followed by 2D doping profiles of the doping around the source and drain electrodes. The final meshing is applied in order to ensure the heterointerfaces to be in a sufficiently tight configuration, especially where large variations in 2DEG concentration are observed within the short distances. Sentaurus Visual is used to extract electrical properties such as 2DEG concentration and mobility, electric fields, and carrier velocity. To generate the I_{DS} – V_{DS} and I_{DS} – V_{GS}

Table 5.4: Parameters used for the simulation of devices.

Parameters	Conventional AlGaN/GaN HEMT	Proposed Final Structure (Structure 3)
Gate Length, L_G	0.8 µm	0.8 µm
Source-gate length, L_{SG}	1.0 µm	1.0 µm
Gate-drain length, L_{GD}	3.0 µm	3.0 µm
GaN cap thickness, t_c	3 nm	3 nm
GaN cap doping, N_c	5×10^{18} cm^{-3}	5×10^{18} cm^{-3}
AlGaN barrier layer	Ungraded – 25 % Al	Step-graded (3 layers) – 50 %, 35 %, and 25 % Al
***AlGaN barrier thickness, t_{br}**	18 nm	18 nm, 21 nm, 24 nm, 27 nm, 30 nm
AlGaN barrier doping	2×10^{18} cm^{-3}	2×10^{18} cm^{-3}
Spacer layer	AlGaN	AlN
***Spacer thickness, t_{sp}**	2 nm	2 nm, 3 nm, 4 nm, 5 nm
Spacer doping, N_{sp}	1×10^{14} cm^{-3}	1×10^{14} cm^{-3}
Channel layer	GaN	InGaN
Channel thickness, t_{ch}	5 nm	5 nm
***GaN Buffer thickness, t_{bf}**	2 µm	2 µm, 2.5 µm, 3 µm
GaN Buffer doping, N_{bf}	1×10^{15} cm^{-3}	1×10^{15} cm^{-3}

characteristics, a drain bias of V_{DS} = 36 V was applied for all simulation conditions. For the I_{DS} – V_{DS} characteristics, two levels of gate voltage were applied, V_{GS} = ±2 V. Spontaneous and piezoelectric components were taken into account for the built-in polarisation model which computes the formation of interface charges at the heterointerfaces due to the polarisation divergence [231]. The anisotropic dielectric tensor is used concerning the reduction in polarisation due to converse piezoelectricity [232].

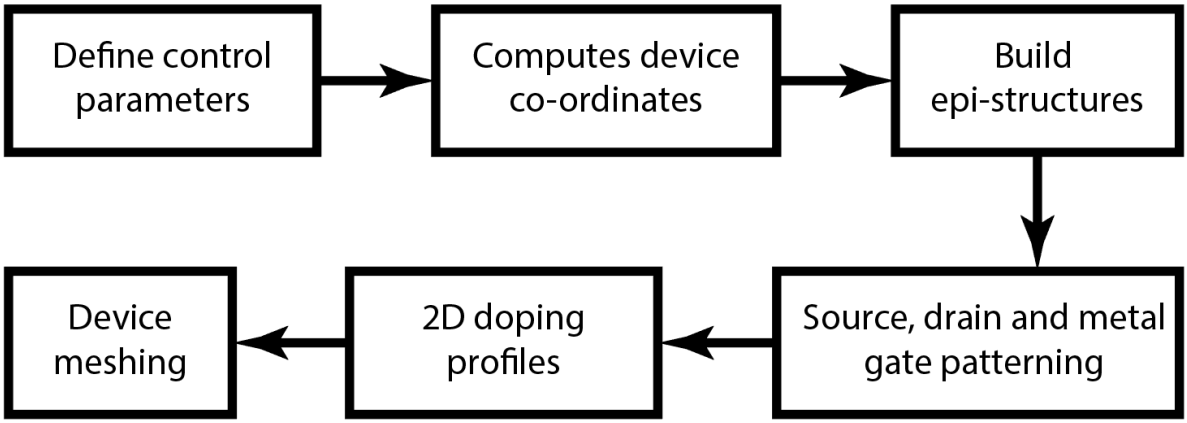

Figure 5.26: Simulated structure formation flow for GaN-based HFET design.

5.4.3. Process Design Considerations

The influence of barrier spacer and channel layer modification to the conventional AlGaN/GaN HEMT on DC output and transfer characeteristics is given in Figure 5.27(a)-(c) and Figure 5.28(a), (b), respectively. The following sub-sections will discuss the impact that each proposed structure has on these characteristics. A comparison of the improved electronic properties for each structure to be discussed is provided in Table 5.5.

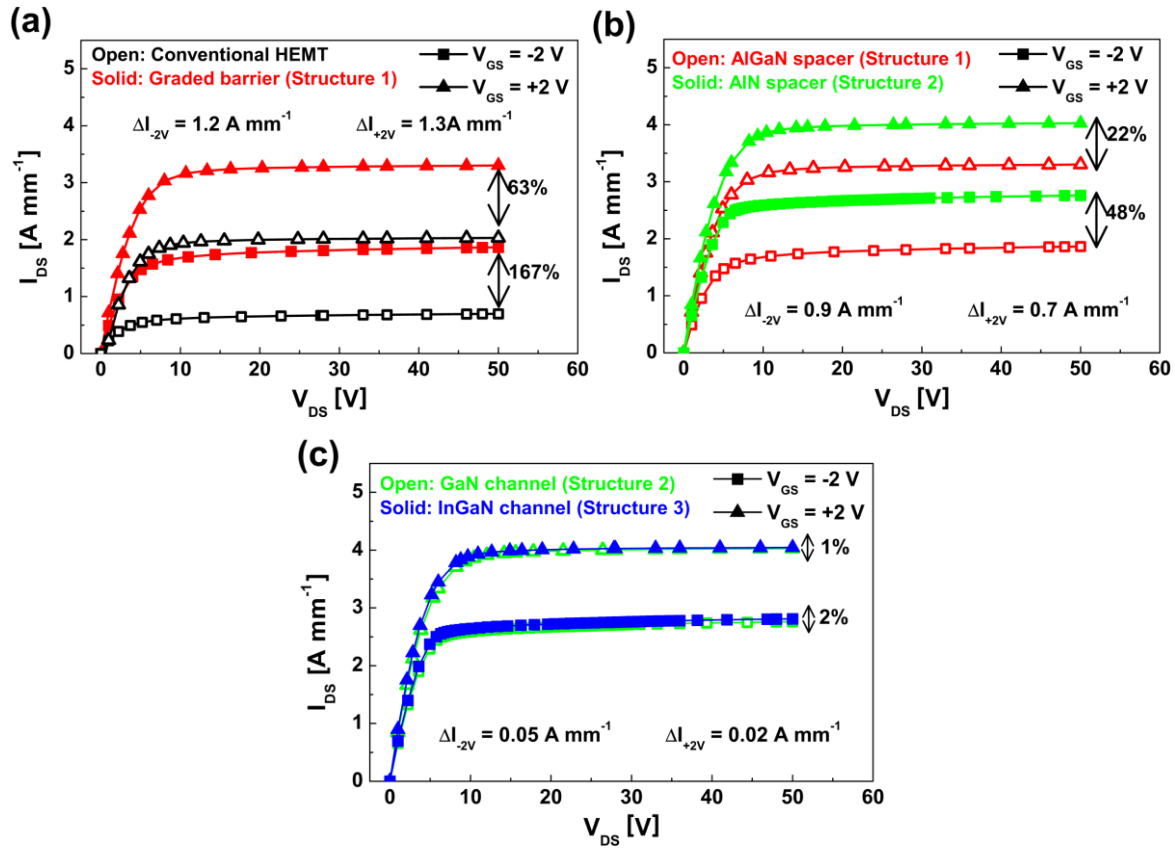

Figure 5.27: I_{DS} – V_{DS} characteristics at V_{GS} = ±2 V for (a) conventional and step-graded AlGaN barrier HEMT (Structure 1); (b) AlN spacer HEMT (Structure 2); and (c) InGaN channel HEMT (Structure 3).

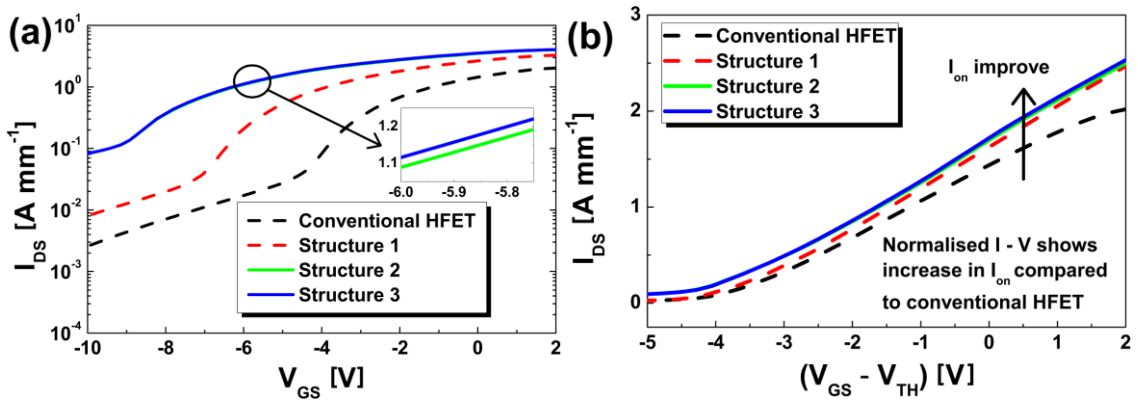

Figure 5.28: (a) I_{DS} – V_{GS} characteristics at V_{DS} = 36 V in logarithmic scale and (b) normalised I_{DS} versus (V_{GS} – V_{TH}) curves for all structures.

Table 5.5: Simulated results of DC characteristics for each device structure.

HEMT Structures	$\|V_{TH}\|$ [V]	I_{on} [A mm^{-1}]	I_{off} [A mm^{-1}]	R_{on} [Ω mm^{-1}]	R_{out} [Ω mm^{-1}]
Conventional	3.509	1.944	1.175	2.588	616.2
Structure 1	6.208	3.288	2.659	2.294	226.8
Structure 2	8.368	4.014	3.410	2.219	40.19
Structure 3	8.415	4.035	3.505	2.202	38.69

5.4.3.1. Step-Graded Barrier Layer – Structure 1

It is known that a step-graded AlGaN barrier layer can significantly improve device performance [233]–[235]. To support this, Figure 5.27(a) shows the DC output characteristics at V_{GS} = ±2 V Structure 1 compared to the conventional AlGaN/GaN HEMT. With this structure, a 63 % increase in peak current density (up to 3.3 A mm^{-1}) is achieved at V_{GS} = +2 V. From Figure 5.29(a), the transfer characteristics depict the increase in current density by 1.26 A mm^{-1} with Structure 1. This is a result of larger band discontinuity at the AlGaN/GaN interface from the increased Al concentration in Structure 1 compared to the conventional AlGaN/GaN HEMT. This induces greater 2DEG sheet density in the channel region due to enhanced P_{PE} effect that stems from the increased lattice mismatch between $Al_{0.5}Ga_{0.5}N$ and GaN. This increase in 2DEG sheet density from the conventional AlGaN/GaN HEMT to Structure 1 is shown in a 2D-DD simulation given in Figure 5.30(b). Although this increase in Al concentration is proven to be beneficial for device performance, the reliability of the device will degrade as the crystal

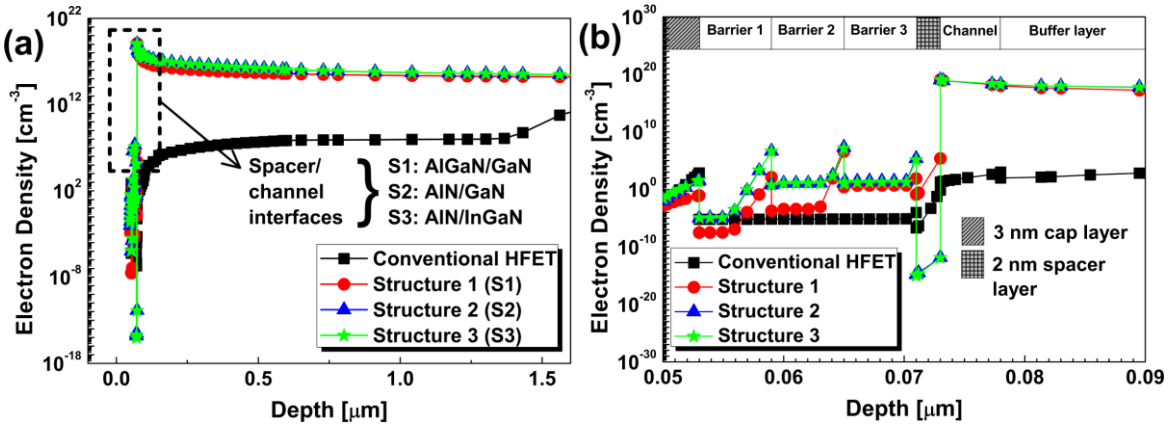

Figure 5.29: (a) Depth profile for electron density for conventional AlGaN/GaN HEMT and Structures 1-3. (b) Closer visual focusing on the density at the interfaces from the depth of 50 nm and 90 nm.

quality of the interface, and thus electron mobility, will degrade [236]. The electronic characteristic simulation of these devices, given in Figure 5.30, clearly shows this degradation in electron mobility and increase in 2DEG sheet density.

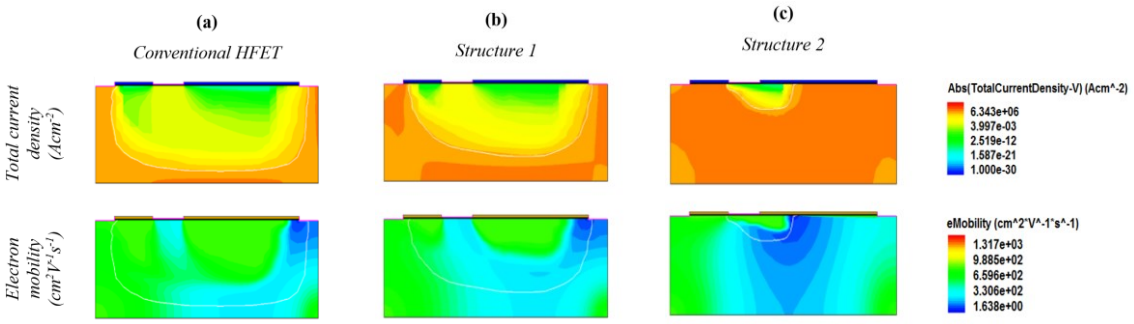

Figure 5.30: Current density and electron mobility distribution for (a) conventional AlGaN/GaN HEMT; (b) Structure 1; and (c) Structure 2.

A deeper investigation into the profile of electron density throughout the device is provided in Figure 5.29(b). A large increase in maximum sheet density is found for Structure 1 (1.66×10^{18} cm^{-3}) compared to the conventional AlGaN/GaN HEMT (0.39×10^{3} cm^{-3}). Interestingly, large numbers of electrons flow through the interfaces of each step-graded barrier layer. This significantly minimises the surface trapping redistribution due to an increase in trap energy induced by the repulsion of mobile electrons in the step-graded barrier. As a result, current collapse is significantly reduced, which allows for vast improvements in device performance.

5.4.3.2. AlN Spacer Layer – Structure 2

Structure 2 is a modification of Structure 1 whereby an AlN spacer layer is implemented. The addition of this layer is designed to improve electron mobility as well as surface lattice arrangements. However, for graded structures, the total strain inside the barrier will decrease due to the reduction in lattice mismatch between the AlGaN and AlN configurations. Despite this, significant improvements to the 2DEG concentrations and electron mobility are observed through the following simulation results. The $I_{DS} - V_{DS}$ curves given in Figure 5.27(b) shows a 22 % increase in I_{on} (4.014 A mm^{-1}) and 48 % increase in I_{off} (3.410 A mm^{-1}) when compared with Structure 1 at V_{GS} = +2 V and V_{GS} = -2 V. The transfer characteristics in Figure 5.28 also show improvement in device performance. This behaviour is strongly related to the increment of mobility caused by the lowering of alloy scattering [237], [238].

The electron density within the channel layer is enhanced to 2.2 × 10^{18} cm^{-3} in Structure 2, as shown in Figure 5.29(b) and Figure 5.30(c). The potential differences across the AlN spacer layer produces larger effective conduction band offset:

$$\Delta E_{c,2} - \Delta E_{c,1} = \exp\left(\frac{\sigma_2 - N_{D,2}}{\varepsilon_r}\right) t_{br} \qquad (5.5)$$

Where $\Delta E_{c,2}$ and $\Delta E_{c,1}$ are the effective conduction band offsets between the interfaces of Structure 2 and Structure 1, respectively; σ_2 is the polarisation induced charge at the heterointerfaces, $N_{D,2}$ is the sheet carrier concentration of Structure 2, ε_r is the dielectric constant, and t_{br} is the thickness of the barrier layer. This increase in effective conduction band offset further increases the polarisation field when compared to Structure 1. The increase of electron mobility from 1102 cm^2 $V^{-1}s^{-1}$ in Structure 1 to 1317 cm^2 $V^{-1}s^{-1}$ in Structure 2 is also shown in Figure 5.30(c). The improvement in both electron density and mobility is owed to the higher quantum well depth which in turn lowers the alloy scattering. Additionally, the effective Schottky barrier of the quaternary structure will increase with the presence of the AlN spacer barrier, which reduces the gate leakage within the device [239]. This reduces the forward Schottky gate current, thus enabling high gate voltage operation. The trend of current density, shown in Figure 5.27(c), indicates that there is essential reduction in the current density below the gate region. This is a result of reduced electric field within the device, shown in Figure 5.31 (a),(b), that leads to reduction in channel leakage into the buffer. Although the electric field at the AlN/GaN interface is higher in Structure 2 (9.8 × 10^6 V cm^{-1}) compared to Structure 1 (3.38 × 10^6 V cm^{-1}), there is a greater drop in electric field away from this interface.

5.4.3.3. InGaN Channel Layer – Structure 3

InGaN has been widely used as the channel material due to its low band gap, which can enhance the high frequency characteristics, reducing 1/f noise and RF current collapse [240]–[242]. Therefore, in Structure 3, InGaN replaces the GaN channel layer in Structure 2. The output characteristics for Structure 3 is given in Figure 5.27(c), showing a 1 % increase in I_{on} (4.035 A mm^{-1}) and a 2 % increase in I_{off} (3.505 A mm^{-1}) when compared to Structure 2 at V_{GS} = +2 V and V_{GS} = -2 V, respectively.. A similar trend of transport characteristics can also be seen in Figure 5.28(a). The narrower band gap of InGaN increases the quantum well depth. This improves the carrier confinement within the channel. This is shown from Figure 5.29(b) where

the carrier density is higher compared to previous structures.

InGaN is beneficial due to its relatively low electron effective mass, leading to increased carrier velocity. This is shown in Figure 5.32(a),(b) where the carrier velocity is increased by 13.9 × 10^3 cm s^{-1} compared to the conventional AlGaN/GaN HEMT. As a result, cut-off frequency is increased for devices performing at high frequency.

In comparison to previous structures, the buffer leakage can be reduced further due to the compressive strain in the channel produced from the InGaN/GaN interface. Also, the piezoelectric polarisation in InGaN is opposite to the AlGaN layer, increasing the conduction band below the channel. This contributes towards the reduction of short channel effects and buffer leakage, which improves the 2DEG mobility and, hence, device performance.

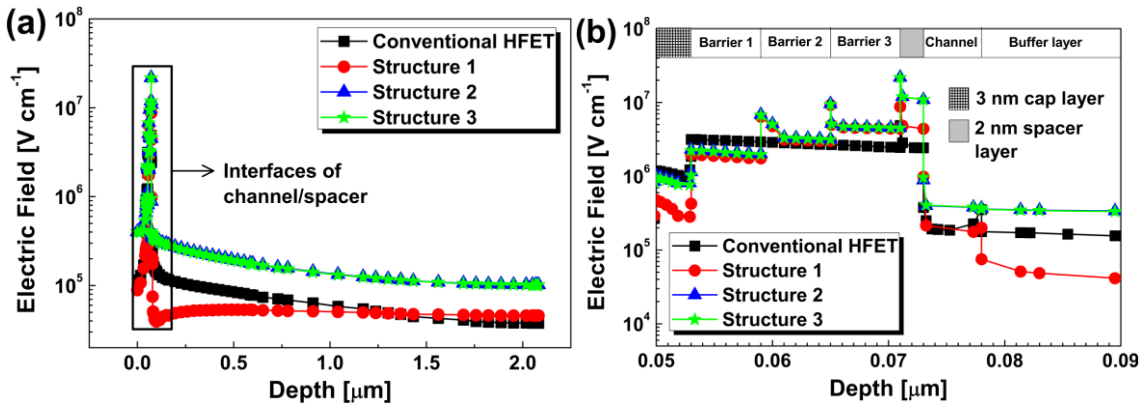

Figure 5.31: (a) Depth profile of electric field for conventional AlGaN/GaN HEMT and Structures 1-3. (b) Closer visual focusing on the field at the interfaces from the depth of 50 nm and 90 nm.

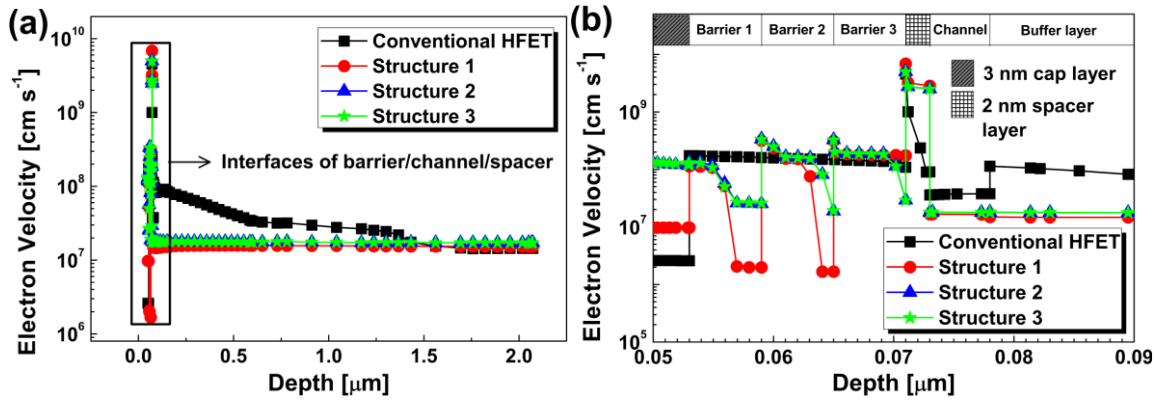

Figure 5.32: (a) Depth profile of electron velocity for conventional AlGaN/GaN HEMT and Structures 1-3. (b) Closer visual focusing on the field at the interfaces from the depth of 50 nm and 90 nm.

5.4.4. Impact of Architectural Geometry on Device Performance

The improved AlGaN/GaN HEMT structure including all enhanced architectural modifications (Structure 3) is studied further by investigating the effects of changing the dimensions of the modifications on device performance. The thicknesses of the step-graded barrier layers (t_{br}), spacer layer (t_{sp}), and buffer layer (t_{bf}) are modified from 6 nm to 9 nm, 2 nm to 5 nm, and 2.0 nm to 3.0 nm, respectively.

The transfer and output characteristics with respect to the thickness of each modification are given for $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ in Figure 5.33(a)-(c) and Figure 5.34(a)-(c), respectively; where each figure shows the transfer and output characteristics for (a) t_{br}, (b) t_{sp}, and (c) t_{bf}. It is shown that an increase in t_{br} , t_{sp} and t_{bf} improves the ON-state performance. However, the threshold voltage (V_{TH}) also increases, which poses as an issue for high frequency applications. With increased V_{TH}, the switching speed of the device is significantly reduced and greater parasitic capacitance would be induced upon switching from OFF-state to ON-state, and vice visa. On the other hand, DC output characteristics are enhanced significantly with

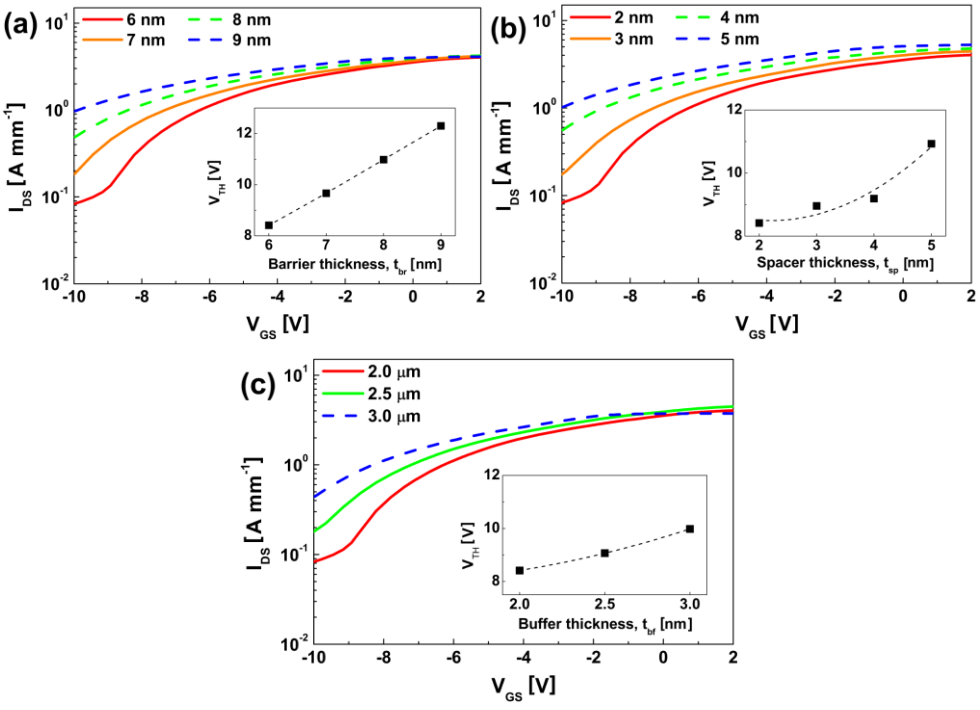

Figure 5.33: Transfer characteristics at V_{DS} = 36 V for various (a) barrier thickness, t_{br}; (b) spacer thickness, t_{sp}; and (c) buffer thickness, t_{bf} of the final structure (Structure 3). Inset: extracted V_{TH} and its trend compared with results of [243] and [244] with respect to t_{br}, t_{sp}, and t_{bf}, respectively.

increased t_{br}, t_{sp}, and t_{bf}, boasting 47 %, 77 %, and 32 % increases in current density, respectively.

Investigating further into the device performance characteristics, the distribution of electron density and mobility are simulated for each modification thickness that is shown in Figure 5.35 and Figure 5.36, respectively. In general, an increase of modification thickness increases the electron density but reduces the electron mobility. The increase in electron density when (i) t_{br}, (ii) t_{sp}, and (iii) t_{bf} is increased is due to (i) the increased surface trap screening and piezoelectric effect, (ii) increased conduction band offset, and (iii) increased carrier confinement and reduced buffer leakage. Reduction in electron mobility with reduced modification thickness stems from lower electric field distribution and surface roughness.

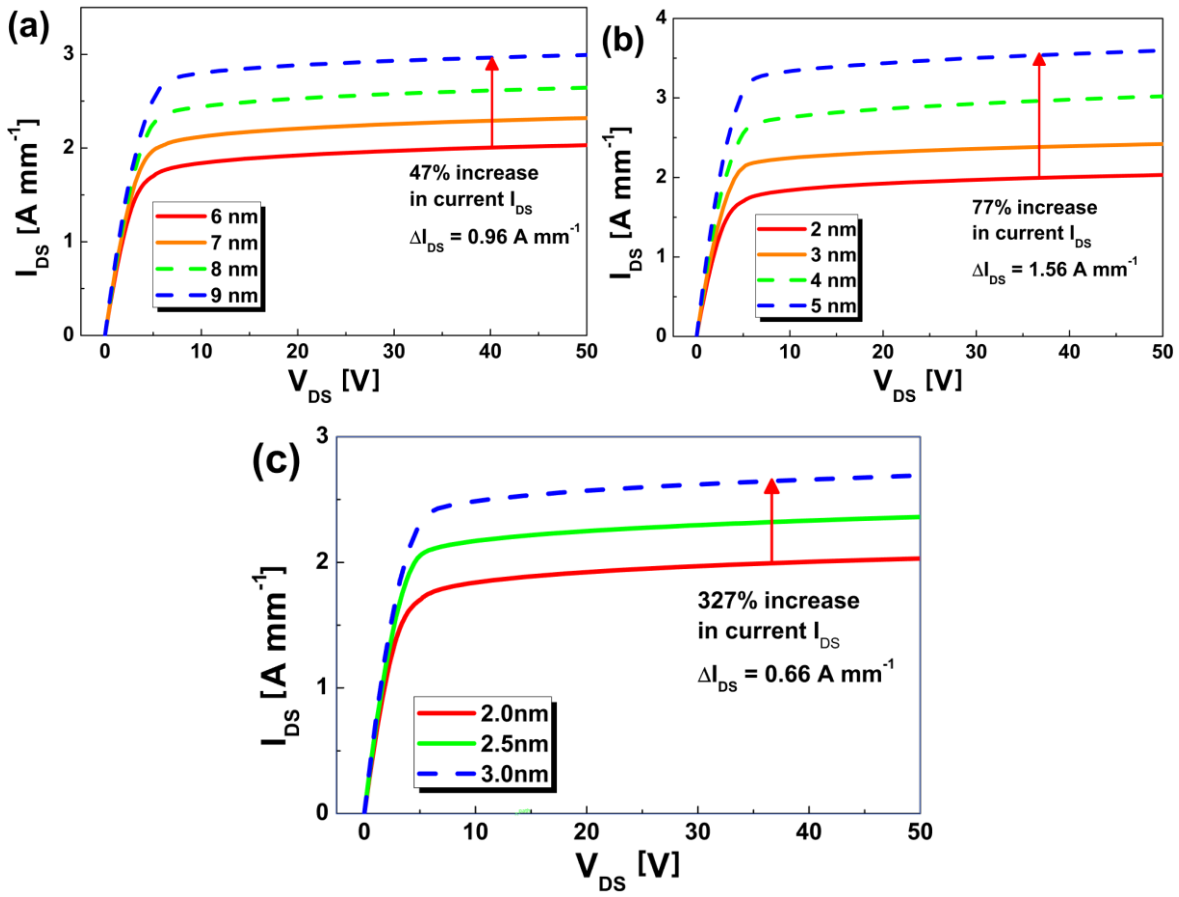

Figure 5.34: Output characteristics at V_{GS} = 2 V for various (a) t_{br}; (b) t_{sp}; and (c) t_{bf} of the final structure (Structure 3).

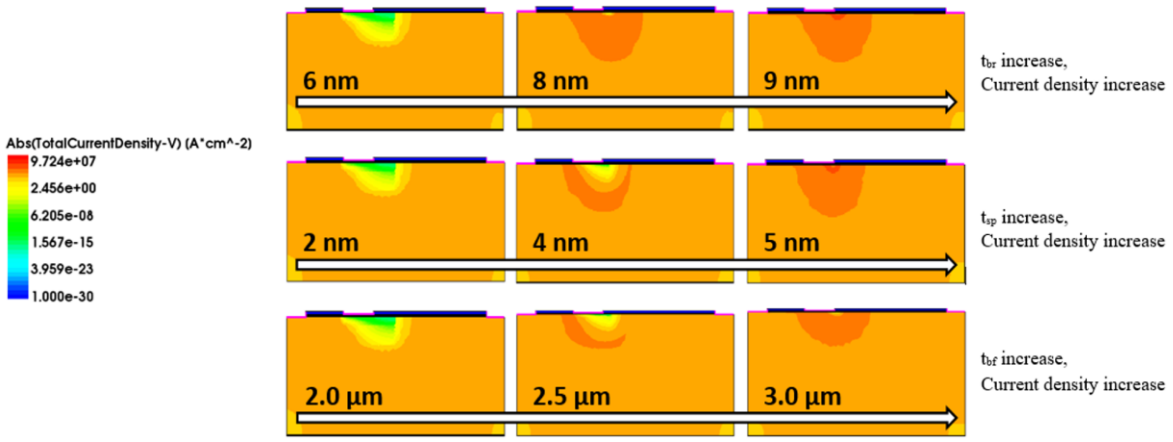

Figure 5.35: Current density distributions at V_{DS} = 36 V for varying t_{br}, t_{sp}, and t_{bf} in Structure 3.

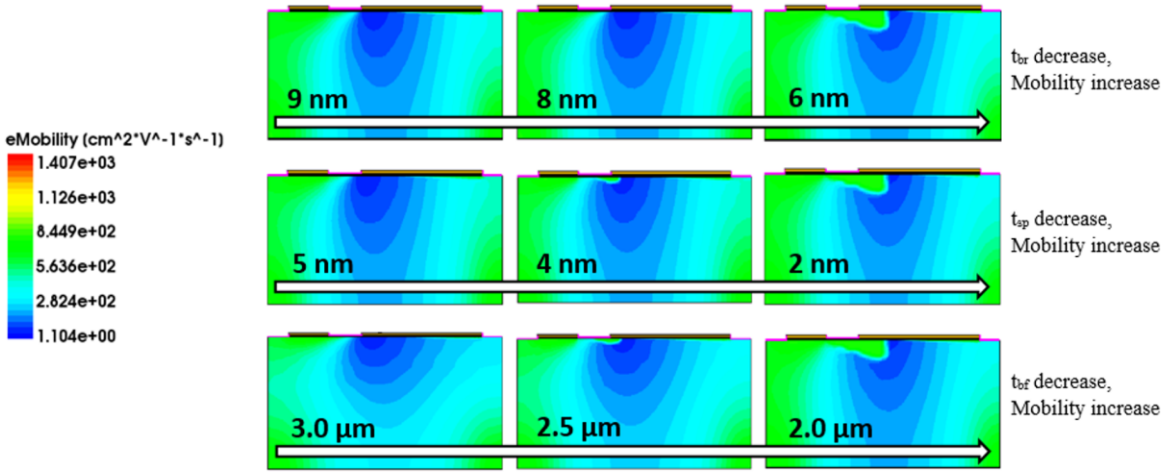

Figure 5.36: Electron mobility distributions at V_{DS} = 36 V for varying t_{br}, t_{sp}, and t_{bf}; Structure 3.

5.5. Summary

In this chapter, we have optimised the fabrication process of the S/D Ohmic contact and gate Schottky contact as well as proposing an upgraded device architecture that enhances device performance.

For S/D contact, an optimised fabrication process of Ohmic contacts is proposed to reduce the access resistance and enhance DC/RF performance of AlGaN/GaN HEMTs. We have experimentally shown that the contact resistance, R_C, of AlGaN/GaN HEMTs with AlN exclusion layer (GaN/$Al_{0.28}Ga_{0.72}N$/AlN) can be significantly reduced from around 1.7 Ω.mm (no etching) to 0.3 Ω.mm (75 % etching). This has been achieved by (i) etching ¾ of the barrier using Ar^+ ion beam dry etching, (ii) using an optimised Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100

nm) multilayer metallisation scheme and (iii) rapid annealing temperature of 850 °C. Despite the possible partial damage of 2DEG due to Ar^+ bombardment during the etching process, the very small distance between the alloy and the 2DEG has led to an overall reduction of R_C. The TLM model extraction combined with 2D drift-diffusion simulations have shown that small R_C leads to a small transfer length, L_T. This could be an issue in terms of thermal management. With the small L_T, a high current density at the inner edges of the contact could results in a large increase in self-heating at this location.

For the gate contact, TiN Schottky processing has been implemented to achieve high Schottky barrier, low leakage current and improved linearity. This process is validated for both optical and electron lithography. A large Schottky barrier of 1.06 eV and low gate leakage of 60 nA mm^{-1} have been obtained after annealing the gate metal at 500 ^oC in an N_2 atmosphere. This optimal Schottky contact is obtained for TiN thicknesses of < 10 nm due to the higher preservation of the strain with reduced TiN thickness. The C – V and I – V characterisations revealed very low trapping density within the optimised device. It has been found that annealing at an optimal temperature (500 ^oC for large gate length and 600 ^oC for sub-micrometer gate length) alters the state of the AlGaN barrier layer. In addition, the conduction band modulation at the TiN/AlGaN interface is also the result of the strain change that creates quasi-p-type doping beneath the Schottky metal.

Finally, the output and transfer characteristics of an optimised design of a GaN-based HEMT has been analysed. The electrical characteristics such as carrier densities, mobility and velocities are extracted. Process and geo-optimisations are applied to the conventional AlGaN/GaN HEMT design, and the final proposed design is studied for the geometrical variation impact. The final proposed structure consists of: (i) step-graded barrier layer of three equal thicknesses; (ii) implementing AlN as the interfacial spacer layer; and (iii) a thin InGaN channel layer. This structure, AlGaN/AlN/InGaN, produces encouraging results in terms of mobility and 2DEG confinements. The threshold voltage obtained for the AlGaN/AlN/InGaN HEMT is 8.4 V. A peak current of 4.04 A mm^{-1} is achieved with the on-state resistance of 2.2 Ω mm^{-1}. The impacts of geometrical variation show that the drive current is improved by increasing the thickness of the barrier and spacer lay, despite having a trade-off to higher buffer leakage. On the contrary, reducing the thickness can lead to mobility enhancement, hence improving both DC and RF performance.

CHAPTER 6

CONCLUSION & FUTURE WORKS

6.1. Conclusion

The aim of this Thesis was to investigate the degradation mechanisms that limit the performance and reliability of AlGaN/GaN-based devices, namely self-heating, on-resistance, current collapse, S/D access resistance, and gate leakage. Through the successful decoupling of self-heating and charge trapping effects, under normal device operation, we acquired vital information on the effect that each degradation mechanism has on AlGaN/GaN-based device performance and reliability. The developed knowledge will contribute towards device failure prevention/prediction and facilitate the device performance/reliability progress, an important step for large-scale deployment can be attained. Our gained expertise was used to assist with propositions of Ohmic and Schottky contacts optimisation and improved AlGaN/GaN-based device architectures. The aforementioned degradation mechanisms were significantly reduced to improve the performance and reliability of AlGaN/GaN-based devices.

Chapter 1 introduced a historical development of GaN technology since its discovery. The primary reasons for why GaN is becoming more used in industry, what applications make use of GaN and how this has effected its market value were summarised. Then, the figure of merits (i.e. JFOM, BHFFOM, and KFOM) of GaN-based devices were compared against other competing semiconductor materials. The current GaN technology issues were outlined, which led towards the rationale of this Thesis. Next, the aim and objectives were then defined and the organisation of the Thesis was presented. Finally, the original contribution of this work towards GaN-based research was recapitulated.

An intensive literature review investigating the physical properties of III-N materials (i.e. crystal structure, material properties and spontaneous/piezoelectric polarisation) was undertaken in Chapter 2. It has been shown that, unlike electron drift-velocity and mobility, very low gain in kinetic energy occurs when a GaN-based device operates at low electric field (< 180 kV cm^{-1}). This is a result of the low effect that elastic scattering mechanisms have on the charge carrier energy. After, the AlGaN/GaN-based device structure, in terms of its 2DEG formation, substrate choice, state-of-the-art and development challenges have been reviewed. An optimal Al concentration in the AlGaN barrier layer was found between 30 and 40 % for typical barrier thickness. It was described that increasing the Al concentration beyond this point causes strain relaxation in the AlGaN barrier and access resistance to increase. Furthermore, the dominant mehcanisms of carrier transport are identified as field emission for Ohmic

contacts and thermionic and thermionic-field emission for Schottky contacts. Finally, self-heating within AlGaN/GaN-based devices is shown to be an extremely fast process, whereby 70 % of its peak operating temperature takes place within the first few microseconds (<2 µm). With this, sufficient knowledge in AlGaN/GaN-based devices has been gained to continue with an investigation into the currently used non-invasive characterisation techniques of degradation mechanisms within such devices. Some of these non-invasive techniques, such as IR, XRD and electrical, have been used for validation throughout this Thesis. Some other invasive techniques, e.g. TEM, SEM and XPS, have been used for post-fabrication verification. The last section outlines the AlGaN/GaN-based device development challenges that are preventing widespread commercial and industrial development. These challenges include (i) self-heating effects, (ii) charge trapping effects, (iii) S/D Ohmic contact resistances, and (iv) Schottky contact gate leakage and barrier height.

In Chapter 3, Infrascope temperature mapping system measurements showed a large increase in temperature at the S/D contacts of AlGaN/GaN-based devices at operating conditions. Temperature coupling of a high conductivity tensile region to the lower conductivity regions was found to be responsible for the temperature rise observed at the inner-edges of the S/D contacts. The thermal coupling also enhanced the peak of temperature at the end of the gate in the AlGaN/GaN HEMTs. In addition, the HR-XRD measurement, supported by DD simulations, revealed that the change of the strain at the vicinity of source and drain Ohmic contacts, due to a difference in expansion coefficients of III-N and source and drain metallisation, was the reason behind this temperature rise. We also studied AlGaN/GaN-based structures with a GaN cap layer grown on a p-type doped HP-Si (111) substrate. Their I – V characteristics from experimental measurements were simulated via a DD transport model using Fermi-Dirac statistics and the SRH recombination model by commercial tool Silvaco Atlas. A thermal model was employed to study the self-heating effects with the thermal conductivity approximated by a power function and calibrated to experimental data. We found that the current became limited by an increase in the lattice temperature with the increase in applied bias up to 13% (the 4 µm structure) and that this limitation occurred sooner in shorter structures. We demonstrated a good agreement of the electro-thermal simulations that predicted a lattice temperature of 374 K against experimental temperature of 399 K at applied bias of 20 V in the largest, 18 µm structure as well as in the smallest, 4 µm structure, a lattice temperature of 434 K against experimental temperature of 453 K at applied bias of 13 V. In addition, we

observed that by applying electrical stress (voltage) on the Ohmic contacts, the total polarisation value in heterostructure reduced when compared to the largest contact distance of 18 µm for 12 µm, 8 µm, and 4 µm by 7 %, 10 %, and 17%, respectively. This decrease in the total polarisation was found to be due to the inverse piezoelectric effect caused by the additional stress induced by the applied electric field on contact. The inverse piezoelectric effect changed the total polarization thus affecting a 2DEG density in the channel.

In Chapter 4, several current degradation misconceptions have led us towards developing a new parametric technique for decoupling self-heating and charge trapping, under normal device operation. In addition, preliminary investigations show that (i) two transient phases of self-heating occur within the device and (ii) the trapped charges have a large impact on the device electrostatic integrity. Using this parametric technique, charge trapping behaviours, with the exclusion of self-heating, were analysed through the use of source and drain transient currents. Two types of degradation mechanisms were identified: (i) fast degradation – less than 1 ms, followed by (ii) slow degradation – greater than 1 ms. Both bulk traps and surface traps contribute towards fast degradation. Through monitoring source and drain transient currents, we observe a difference between I_S and I_D, which is defined as bulk trapping. However, only surface traps contribute towards slow degradation, where $I_S - I_D$ = 0 mA. Through monitoring the diffierence between I_S and I_D, bulk trapping time constant was shown to be independent of V_{DS} and V_{GS}. Although, V_{DS} was found to affect the bulk trap density. Large V_{DS} was found to be a cause of bulk charge trapping during both ON and OFF states of the device. Surface trapping is found to have a much greater impact on slow degradation when compared to self-heating and bulk trapping. This is an important step to understanding the priority of device engineering, whereby the focus should be aimed towards reducing surface trapping accumulation and redistribution in order to minimise current degradation.

In Chapter 5, we had experimentally shown that the contact resistance, R_C, of AlGaN/GaN HEMTs with AlN exclusion layer (GaN/$Al_{0.28}Ga_{0.72}N$/AlN) could be significantly reduced from 1.7 Ω.mm (no etching) to 0.3 Ω.mm. This was achieved by (i) etching ¾ of the barrier using Ar+ ion beam dry etching, (ii) using an optimised Ti/Al/Ni/Au (12 nm/200 nm/40 nm/100 nm) multilayer metallisation scheme and (iii) rapid annealing temperature of 850 °C. Despite the possible partial damage of 2DEG due to Ar^+ bombardment during the etching process, the very small distance between the alloy and the 2DEG led to an overall reduction of R_C. The

TLM model extraction combined with 2D drift-diffusion simulations showed that a small R_C led to a small transfer length, L_T. This was shown to be a potential issue in terms of thermal management. With the small L_T, a high current density at the inner edges of the contact could result in a large increase in self-heating at this location. The Schottky contact of an AlGaN/GaN HEMT was then optimised. TiN Schottky processing has been implemented to achieve high Schottky barrier, low leakage current and improved linearity. A large Schottky barrier of 1.06 eV and low gate leakage of 60 nA mm^{-1} have been obtained after annealing the gate metal at 500 ^oC in an N_2 atmosphere. This optimal Schottky contact is obtained for TiN thicknesses of < 10 nm due to the higher preservation of the strain with reduced TiN thickness. The C – V and I – V characterisations revealed very low trapping density within the optimised device. It has been found that annealing at an optimal temperature (500 ^oC for large gate length and 600 ^oC for sub-micrometer gate length) alters the state of the AlGaN barrier layer. In addition, the conduction band modulation at the TiN/AlGaN interface is also the result of the strain change that creates quasi-p-type doping beneath the Schottky metal. Finally, several modifications to a conventional HEMT was made in order to improve its output and transport characteristics, namely 2DEG density and carrier mobility. We began by comparing the characteristics of a conventional AlGaN/GaN HEMT with a HEMT that has an AlGaN step-graded barrier layer, AlN spacer layer, and InGaN channel layer. A large improvement in output and transfer characteristics were observed. Upon changing the geometric design of some of the modifications, we observed an increase in current density when the barrier, spacer and buffer thickness was increased. However, reducing the thicknesses led to enhancement of carrier mobility. Therefore, with the optimisations for Ohmic and Schottky contacts as well as device structure, the overall performance of AlGaN/GaN-based devices were significantly improved. Overall, our aim of understanding and reducing the degradation mechanisms causing the performance and reliability degradation of AlGaN/GaN-based devices has been achieved.

6.2. Future Works

We have investigated the reliability and performance degradation mechanisms of AlGaN/GaN-based devices. However, there is further research that can be performed to contribute towards better understanding of the kinetics of these degradation mechanisms. An accurate knowledge of the charge trapping characteristics as a function of operating temperature is important because (i) the thermal condition of a device is closely related to its mean time-to-failure and

(ii) help to identify the quantitative impact of the advanced device architecture on self-heating and/or charge trapping.

6.2.1. Decoupling of Bulk Trapping and Self-Heating

Although bulk trapping has been identified to be the different between source current and drain current (Section 4.5.2), it is unclear as to whether it is dominant over self-heating. In order to investigate this, a temperature sensor can be implemented at the surface of the device, near the drain side gate edge, to measure the self-heating characteristic. This self-heating characteristic, which is independent of applied power and bias conditions, can then be compared to the source and drain transient currents, under different precharging conditions, to identify the bulk trapping kinetic. To note, Infrared cannot be used due to its inaccuracy and time resolution and μRaman cannot be used as it requires high power to operate effectively.

In Section 4.5.2.3, we have experimentaly shown that bulk trapping is gate voltage independent. This suggests that bulk traps are caused by hot carrier injections, since the bulk traps are known to be temperature independent [193]. This conclusion need to be verified through Monte Carlo simulations, taking into account the optical phonon scattering.

From Section 4.5.3, it is clear that surface traps degrade the current within our devices due to changes in electrostatic for time constants larger than 1 ms. However, the physics behind the quasi-saturation of the drain current, before 1 ms, is unclear and needs further investigation. We think that the impact of non-distributed surface traps on the electrostatic, and thus the current, is minimal compared to redistributed traps. This investigation can be carried out through drift-diffusion simulations.

6.2.2. Thermal Management of Strain-Induced Self-Heating

In Section 3.2.2, we have shown that strain reduction is the cause of temperature rise that occurs at the inner-ends of the source and drain contacts of MBE grown devices. However, this thermal management issue needs to be verified for MOCVD grown devices, since it is the primary growth technique chosen for commercial devices.

Furthermore, two options can be proposed in order to enhance the S/D thermal management. Firstly, develop a new Ohmic contact metalisation scheme via the optimisation of the metal source target-to-substrate distance. Unlike the process of the gate contact, described in Section 3.2.2.3, the compressive strain of S/D metal contact needs to be minimised to lower strain

compensation at metal/AlGaN interface, and therefore, reduce self-heating. Secondly, simulate the overgrowth layer that is described in Section 5.2.2. to observe the impact that reduced vertical electric field has on transfer length and, therefore, self-heating. This simulaton can be used to optimise the overgrowth layer thickness and angle.

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CHAPTER 7

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APPENDIX A

EXPERIMENTAL INSTRUMENTATION

A.1. Probing Station and Measurement Framework

The following describes the electrical characterisation facilities, Summit 12000-AP probing station used to probe our 2 inch AlGaN/GaN wafer and our Keithley 4200A-SCS parametric analyser which sources voltage and measures the current of the chosen device. An illustration of the described setup is given in Figure A.1.

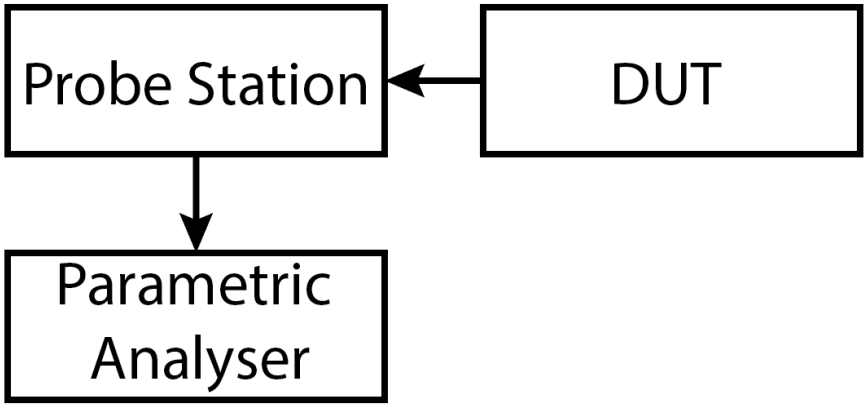

Figure A.1: Setup for electrical characterisation of AlGaN/GaN HEMT. The DUT is placed on the baseplate of the probing station and probed. The probe station is then connected to the parametric analyser which allows for measurement of DUT electrical characteristics.

A.1.1. Summit 12000-AP Probing Station

The Summit 12000-AP probing station, shown in Figure A.2, is used perform our low noise measurements. This particular probing station allows access to the full range of testing instruments for up to 200 mm wafers with the use of its 200 mm gold-plated aluminium chuck. A variety of configurations are easily accessible in order to optimise analysis of the DUT such as (i) wide range of microscope zoom and focus options, (ii) a thermal range of -60 ^{o}C to 300 ^{o}C, and (iii) chuck size, depth and orientation. Wafer navigation, mapping, automation and integration with measurement software is available on-screen through the Velox^{TM} probe station control software. In addition, Cascade DCM-210 3-axis micro-positioners with high positioning accuracy (< 2 µm) and large position range (12.7 mm x, y and z axes range) were magnetically stationed onto the Summit 12000-AP probing station. The magnetic pull from the micro-positioners to the probing station prevented mechanical ambient effects from interfering with the measured signal. Finally, a low resistance Cascade 154-001 radial probing needle was connected to the micro-positioner which probed the DUT. The low resistance minimises the

parasitic capacitance that occurs when bias is increased within a short edge time.

Figure A.2: Summit 12000-AP probing station using the Velox™ control software, Cascade DCM-210 micro-positioners and Cascade 154-001 radial probing needles.

A.1.2. Keithley 4200A-SCS Parametric Analyser

The parametric analyser used for this Thesis is the Keithley 4200A-SCS. The framework includes the Clarius application program in order to allow measurement of semiconductor devices and materials. Several common characterisation techniques can be performed using Clarius such as I – V, C – V, pulsed I – V, and transient I – t characterisation.

The parametric analyser allows source and measurement functions through its eight model 4200 source-measure units (4200-SMUs), typically used for DC measurements. This fundamental instrument module can source and measure either voltage or current in a sweep, step, or constant bias configuration. A sense-LO, sense, force and preamp control (PA CNTRL) terminal is available for each 4200-SMU. For the purposes of our experiments, only the force terminal is used to source and measure voltage and current. The 4200-SMUs available for our parametric analyser are specifically the 4200-SMU model. The module is essentially a voltage/current source in series with a current meter that is connected in parallel with a voltage meter. A detailed block diagram of this module is given in Figure A.3. Here, The voltage, current and power compliance of 210 V, 105 mA and 2.2 W, respectively, is set by voltage limit (V-limit) and current limit (I-limit) circuits.

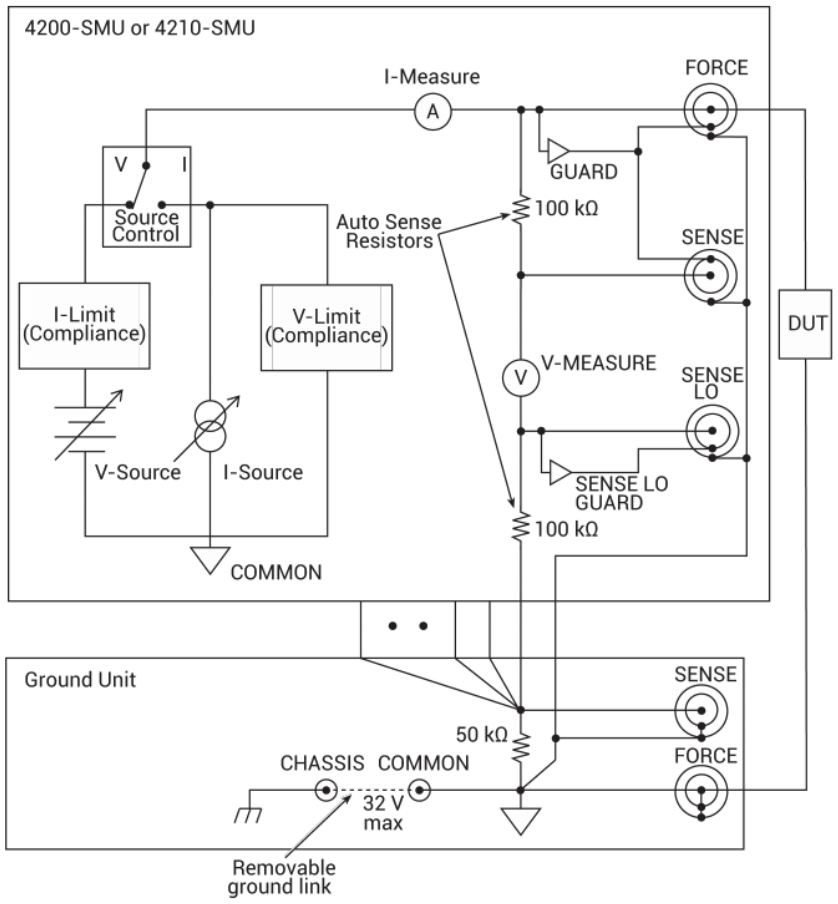

Figure A.3: Basic block diagram of SMU source-measure configuration.

The Keithley 4200A-SCS also has four model 4225 pulse measure units (4225-PMUs) that are used over SMUs for measuring I – V characteristics with minimal self-heating and transient current. These modules provide a broad range of voltage sourcing with voltage and current measurements at very short time intervals. The module is capable of providing multi-level waveforms segments of 20 ns to 40 s with pulse periods of 120 ns to 1 s. Amplitudes of ±40 V with millivolt resolution and measurements at up to 800 mA with < 12 nA resolution can also be achieved from these multi-level waveforms. Three types of ultra-fast I – V tests can be performed as illustrated in Figure A.4:

i. Pulsed I – V – High speed, time-based measurements that provide DC-like results are achieved from a pulsed source. Current and/or voltage measurements are taken as an average of readings within a defined pulse measurement window (i.e. between 120 ns to 1 s). Customisation of duty cycle, rise/fall times, and amplitude can be used with this

setting.

ii. Transient I – V – Pulsed waveforms are captured in a time-based manner for current and/or voltage measurements. Typically, this is a single pulsed waveform that is used to analyse the time-varying electrical characteristics of a device, i.e. transient current degradation. A large number of samples can be captured within a short measurement window using this setting, making it useful for precise time-based measurements.

iii. Pulsed Sourcing – Involves outputting multi-level pulses using the built-in Segment ARB function. This function allows for the creation of any type of waveform within the given compliances and timing limitations of the 4225-PMU. Measurements of AC or DC voltage and current can be performed using this setting, removing the need for additional measurement hardware or complicated programming to capture these measurements.

This complex measurement hardware is built with respect to the block diagram of the 4225-PMU module shown in Figure A.5. The remote pulse measure unit (RPM) is connected between the 4225-PMU and Summit 12000 AP probe station. This module allows inputs of both 4200-SMU and 4225-PMU simultaneously and is used for convenience of switching between DC and pulsed measurements.

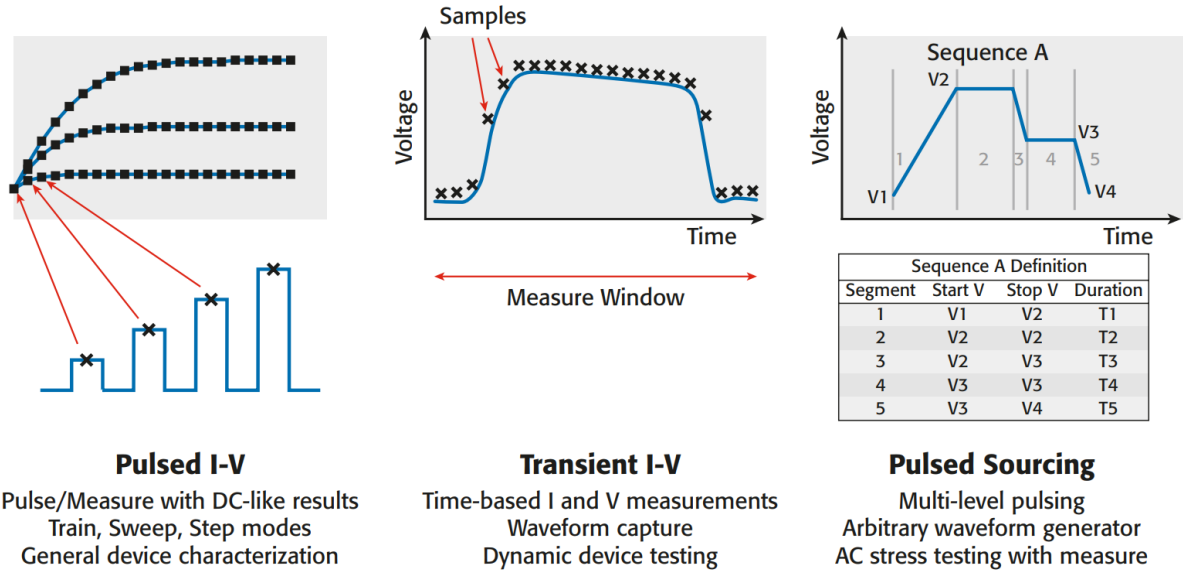

Figure A.4: Settings achievable by the 4225-PMU module and their benefits for (i) Pulsed I – V, (ii) Transient I – V, and (iii) Pulsed Sourcing.

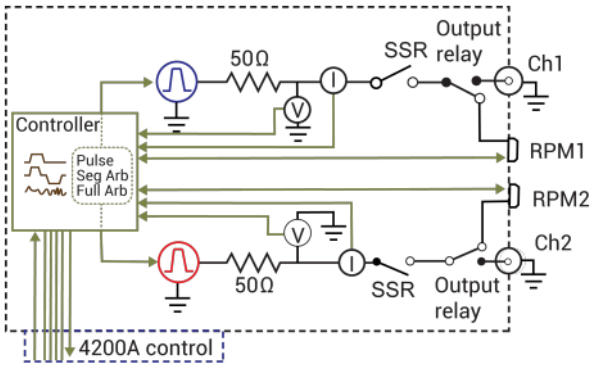

Figure A.5: Block diagram of the 4225-PMU control system showing the connections between the Keithley 4200A-SCS and 4225-RPM.

A.2. Instrument Calibration

Since this is the first time that we are measuring both source and drain transient currents simultaneously, it is very important to identify the difference between I_S and I_D (offset) of these currents. As a result of hardware interfacing, our characterisation facilities, Keithley 4200-SCS framework and Summit 12000-AP probe station, given in Section A.1, needs to be calibrated. In order to do this, a 180 Ω ± 5 % resistor is connected via 4225-PMU of the framework whereby a high voltage pulse waveform of 13 V is applied for 2 s. I_S and I_D are then measured. An I_S, I_D offset (ΔI) of 0.4 mA is clearly visible in Figure A.6 and persists throughout the entirety of the measurement. Therefore, during data processing of any further measurements in this chapter, I_S is required to be set 0.4 mA lower to correlate with I_D.

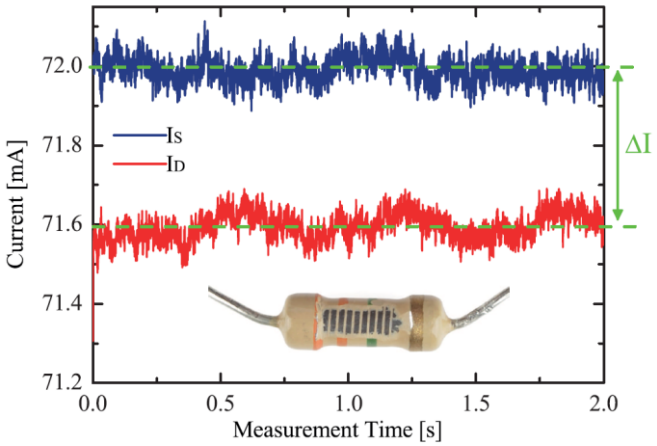

Figure A.6: Transient I_S and I_D of a 180 Ω resistor at 13 V, showing the I_S, I_D offset, ΔI, is persistently 0.4 mA.