

INTERACTION BETWEEN RANDOM TELEGRAPHY NOISE AND HOT CARRIER AGEING

A. B. Manut, J. F. Zhang, Z. Ji, W. Zhang

Department of Electronics and Electrical Engineering, Liverpool John Moores University,
Byrom Street, Liverpool L3 3AF, UK
E-mail: j.f.zhang@ljmu.ac.uk

Abstract

As downscaling reaches nanometer scale, Hot Carrier Ageing (HCA) and Random Telegraphy Noise (RTN) are two important sources of device instability. Early works typically investigate them separately and treat them as independent phenomena. In reality, however, they occur simultaneously in a device and their interaction is not fully understood. In this work, we study the impact of HCA on RTN amplitude. It is found that for devices of average RTN, HCA only has a limited effect on RTN. For devices of abnormally high RTN, however, HCA can substantially reduce the RTN. The underlying physical mechanism is explored.

Introduction

As the downscaling of CMOS nodes continues, Random Telegraphy Noise (RTN) [1-6] and Hot Carrier Ageing (HCA) [7-10] are important sources of device instabilities. RTN causes a fluctuation of device parameters, such as drain current and threshold voltage, around their average value. It is well accepted that charging and discharging traps in gate dielectric are responsible for RTN. When there is a single trap, RTN gives a two level signal. More often, however, there are multiple traps, producing a complex within-a-device fluctuation [4-6].

Unlike RTN, stresses charge traps and cause device parameters shifting in one direction, typically a reduction of drain current and an increase of threshold voltage [11-14]. Although both of RTN and HCA received many attentions in early works [1-10], they were studied as independent phenomena. In a real device, however, they occur concurrently and can interact with each other. This interaction is not well understood, as there is little investigation on it. The objective of this work is to study the impact of HCA on the amplitude of RTN and to explore the underlying physical process.

Devices and Experiments

The devices used were fabricated by a 45 nm CMOS process. The nMOSFETs have a metal gate and a high-k/SiON dielectric stack with an equivalent oxide thickness of 1.45 nm. The channel length is 50 nm and the width is 90 nm.

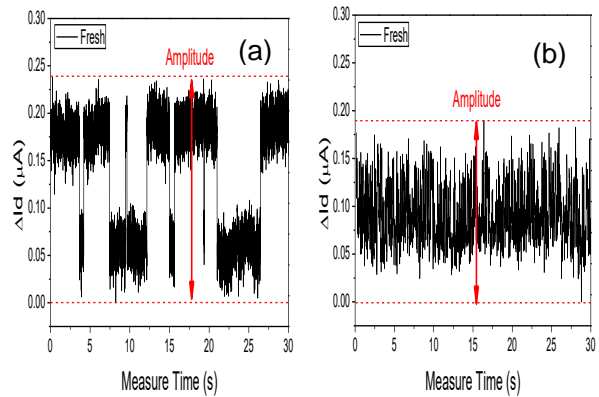


Fig. 1. Typical test results where there is clear RTN signal (a) and there is no clear RTN signal (b).

The RTN measurement was carried out by monitoring I_d under $V_g=1.0$ V and $V_d=0.1$ V. Fig. 1a shows a typical result where RTN signal can be clearly observed, while Fig. 1b shows that multiple traps result in a complex within-a-device fluctuation [4,10]. In this work, we focus on the amplitude of RTN, as defined in Figs. 1a&b.

After RTN measurement, HCA was carried out typically under $V_g=V_d=2.2$ V for 1,000 sec. The RTN was then measured again under the same I_d , so that the surface potential is kept the same for the RTN measurement. The impact of HCA is assessed by comparing the RTN pre- and post-HCA.

Device-to-device variations of RTN

As expected, Fig. 2 shows that there is a large device-to-device variation (DDV) of RTN. Among the 50 devices tested, the DDV is over a factor of 5. This is

caused by the statistical variation of traps, in term of both the number and the location [2,3]. For the same device, the RTN is sensitive to the measurement V_g . For instance, the device of the highest RTN under $V_g=1.0$ V has a RTN below the average under $V_g=0.9$ V. This is because RTN is dominated by traps close to Fermi-level at the dielectric/substrate interface, E_f , and a change of V_g alters the relative position of E_f .

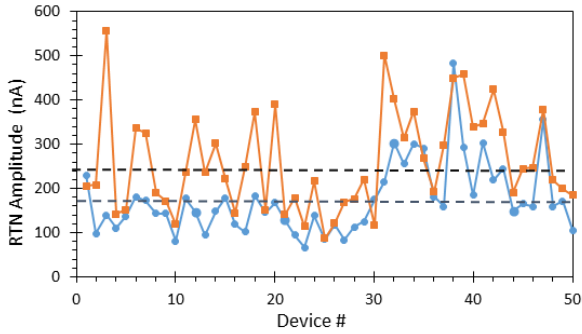


Fig. 2. The device-to-device variations of RTN amplitude measured under $V_g=1$ V (squares) and 0.9 V (circles), respectively. The dashed lines are the averages.

Impact of HCA on devices of average RTN

We first investigate the impact of HCA on devices of average RTN, i.e., those close to the dashed lines in Fig. 2. Fig. 3 gives the typical results. After HCA, RTN can either increase (Figs. 3a&b) or decrease (Figs. 3c&d), but the variation of less than 25% is relatively modest, when compared with the DDV in Fig. 2.

HCA generates new traps in the gate dielectric [8-10], which could be responsible for the increased RTN in Fig. 3b. The defect generation, however, could not explain the decrease of RTN after HCA in Fig. 3d. We will explain this decrease after investigating the impact of HCA on the devices of abnormally high RTN.

Impact of HCA on devices of abnormally high RTN

The devices of abnormally high RTN are those well above the average dashed line in Fig. 2. Fig. 4 shows that the RTN is substantially reduced after HCA. Unlike the average devices where RTN can also increase after HCA, we did not observe such increase here. These devices of abnormally high RTN always have lower RTN after HCA. The underlying physical process will be explored next.

Physical processes

It has been reported that, after HCA, there is little recovery of the degradation under $V_g=0$ V [8,9]. This indicates that the HCA-generated defects have energy levels well below the E_f , when RTN is measured, as

illustrated in Fig. 5. As these traps are always filled during RTN measurement, they will not contribute to RTN through discharging-charging. This, however, does not mean that they cannot affect the RTN, as detailed below.

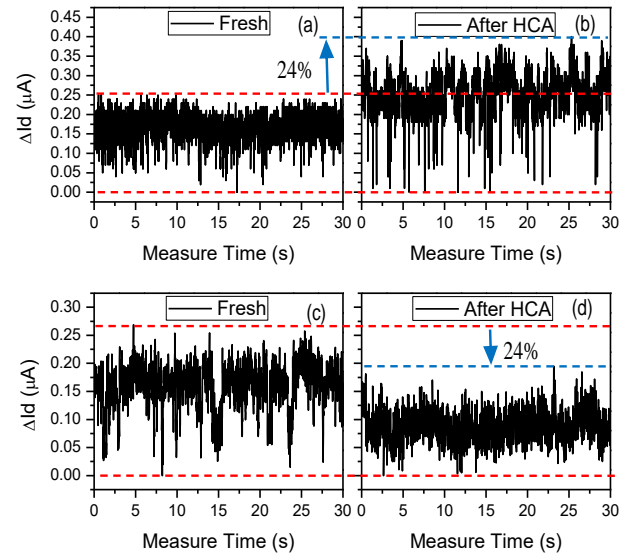


Fig. 3. Impact of HCA on devices of average RTN. RTN can either increase (a and b) or decrease (c and d) modestly after HCA.

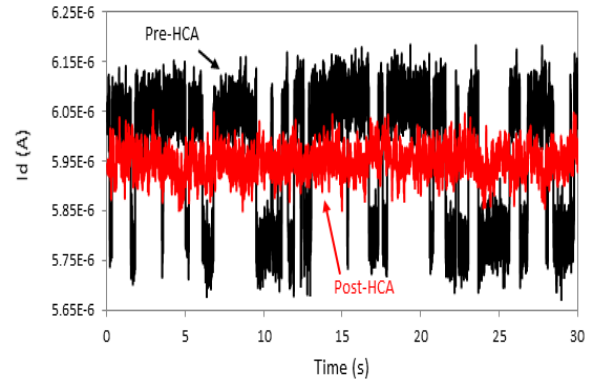


Fig. 4. Impact of HCA on devices of abnormally high RTN. RTN is reduced by more than half after HCA.

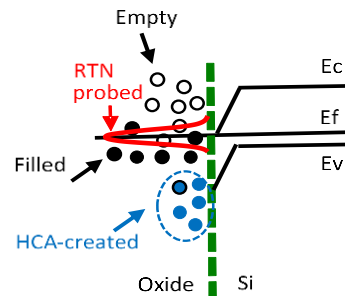


Fig. 5. The HCA-created deep trap does not discharge and will not contribute to RTN measurement directly.

It has been reported that the current flow in a device is not uniform and the impact of a trap on the current depends on its location [2,3]. As schematically illustrated in Fig. 6a, the higher the local current density under a trap, the larger its impact on current will be.

When a device has abnormally high RTN, there is a trap above the bottleneck of current flow, as shown in Fig. 6a. After HCA, the HCA-generated defects can change the current distribution, so that this trap is no longer above the bottleneck, as illustrated in Fig. 6b. This explains the sharp reduction in RTN in Fig. 4. For an average device, there is no trap above the bottleneck of current flow or there is no clear bottleneck in the current flow. A HCA-induced change of current distribution only can either increase or decrease RTN modestly, therefore.

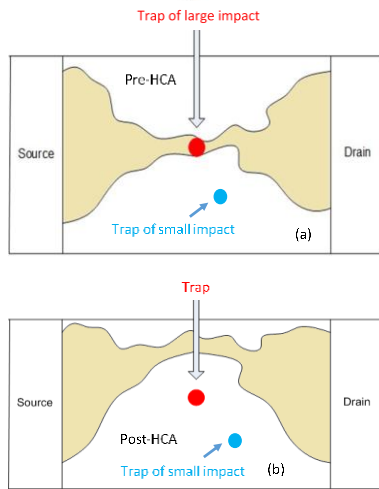


Fig. 6. Pre-HCA, the red trap is above the bottleneck of current flow and produce a large RTN. Post-HCA, current flow distribution changes, so that the red trap is no longer above the bottleneck and the RTN reduces.

Conclusions

In this work, we investigated the impact of HCA on RTN. It is shown that for the device of average RTN, HCA only has a modest impact and RTN can either increase or decrease after HCA. For the devices of abnormally high RTN, HCA reduces the RTN. This is because the abnormally high RTN is caused by the presence of traps just above the current flow bottleneck and HCA alters the current flow to move the bottleneck away from the trap.

Acknowledgements

The authors thank B. Kaczer, D. Linten, and G. Groeseneken of IMEC, Belgium, for supply of test samples used in this work. This work was supported by the EPSRC of UK under the grant no. EP/L010607/1.

References

- [1] J. Zou, R. Wang, N. Gong, R. Huang, X. Xu, J. Ou, C. Liu, J. Wang, J. Liu, J. Wu, S. Yu, P. Ren, H. Wu, S. W. Lee, and Y. Wang, *Proc. Symp. VLSI Technol.*, pp. 139–140, 2012.
- [2] B. Kaczer, T. Grasser, P. J. Roussel, J. Franco, R. Degraeve, L. A. Ragnarsson, E. Simoen, G. Groeseneken, and H. Reisinger, *Proc. IRPS*, pp. 26–32, 2010.
- [3] A. B. Manut, J. F. Zhang, M. Duan, Z. Ji, W. Zhang, B. Kaczer, T. Schram, N. Horiguchi, and G. Groeseneken, *IEEE J. Electron Dev. Soc.*, Vol. 4, pp.15–21, 2016.
- [4] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, B. Kaczer, T. Schram, R. Ritzenthaler, G. Groeseneken, and A. Asenov, *IEEE Trans. Elec. Dev.*, Vol. 60, pp. 2505–2511, 2013.
- [5] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, B. Kaczer, T. Schram, R. Ritzenthaler, A. Thean, G. Groeseneken, and A. Asenov, *Proc of Symp. VLSI Technol.*, pp.74–75, 2014.
- [6] M. Duan, J. F. Zhang, Z. Ji, J. G. Ma, W. Zhang, B. Kaczer, T. Schram, R. Ritzenthaler, G. Groeseneken, and A. Asenov, *Proc. IEDM*, pp. 774–777, 2013.
- [7] C. Hu, S. C. Tam, F. C. Hsu, P. K. Ko, T. Y. Chan, and K. W. Terrill, *IEEE Trans. Elec. Dev.*, Vol. ED-32, pp. 375–385, 1985.
- [8] M. Duan, J. F. Zhang, A. Manut, Z. Ji, W. Zhang, A. Asenov, L. Gerrer, D. Reid, H. Razaidi, D. Vigar, V. Chandra, R. Aitken, B. Kaczer, and G. Groeseneken, *Proc. IEDM*, pp. 547–550, 2015.
- [9] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, D. Vigar, A. Asenov, L. Gerrer, V. Chandra, R. Aitken, and B. Kaczer *IEEE Trans. Elec. Dev.*, Vol. 63, pp. 3642–3648, 2016.
- [10] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, B. Kaczer, and A. Asenov, *IEEE Trans. Elec. Dev.*, Vol. 64, pp.2478–2484, 2017.
- [11] S. F. W. M. Hatta, Z. Ji, J. F. Zhang, M. Duan, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, *IEEE Trans. Elec. Dev.*, Vol. 60, pp. 1745–1753, 2013.
- [12] J. F. Zhang, M. H. Chang, Z. Ji, L. Lin, I. Ferain, G. Groeseneken, L. Pantisano, S. De Gendt, and M. M. Heyns, *IEEE Elec. Dev. Lett.*, Vol. 29, pp.1360–1363, 2008.
- [13] C. Z. Zhao and J. F. Zhang, *J. Appl. Phys.*, Vol. 97, art. no. 073703, 2005.
- [14] J. F. Zhang, Z. Ji, and W. Zhang, *Microelectronics Reliability*, Vol. 80, pp. 109–123, 2018.