Journal of Applied Physics

Comparison of atomic layer deposited Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on the characteristics of GaN-capped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors

Cite as: J. Appl. Phys. **126**, 034102 (2019); https://doi.org/10.1063/1.5049220
Submitted: 20 July 2018 . Accepted: 25 June 2019 . Published Online: 18 July 2019

T. Partida-Manzanera, Z. H. Zaidi, J. W. Roberts, S. B. Dolmanan, K. B. Lee, P. A. Houston, P. R. Chalker, S. Tripathy, and R. J. Potter

Journal of Applied Physics ARTICLE scitation.org/journal/jap

Comparison of atomic layer deposited Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics on the characteristics of GaN-capped AlGaN/GaN metal-oxide-semiconductor high electron mobility transistors

Cite as: J. Appl. Phys. **126**, 034102 (2019); doi: 10.1063/1.5049220
Submitted: 20 July 2018 · Accepted: 25 June 2019 ·
Published Online: 18 July 2019

T. Partida-Manzanera,[1,2,a)] Z. H. Zaidi,[3] J. W. Roberts,[1] S. B. Dolmanan,[2] K. B. Lee,[3] P. A. Houston,[3] P. R. Chalker,[1] S. Tripathy,[2] and R. J. Potter[1]

AFFILIATIONS

[1]Department of Mechanical, Materials and Aerospace Engineering, School of Engineering, University of Liverpool, L69 3GH Liverpool, United Kingdom
[2]Institute of Materials Research and Engineering, A*STAR (Agency for Science, Technology, and Research), Innovis, 2 Fusionopolis Way, 138634 Singapore
[3]Department of Electronic and Electrical Engineering, University of Sheffield, S1 3JD Sheffield, United Kingdom

[a)]**Electronic mail:** t.partidamanzanera@ljmu.ac.uk

ABSTRACT

The current research investigates the potential advantages of replacing Al_2O_3 with $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as a higher dielectric constant (κ) gate dielectric for GaN-based metal-oxide-semiconductor high electron mobility transistors (MOS-HEMTs). The electrical characteristics of GaN-capped AlGaN/GaN MOS-HEMT devices with $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ as the gate dielectric are compared to devices with Al_2O_3 gate dielectric and devices without any gate dielectric (Schottky HEMTs). Compared to the Al_2O_3 MOS-HEMT, the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT achieves a larger capacitance and a smaller absolute threshold voltage, together with a higher two-dimensional electron gas carrier concentration. This results in a superior improvement of the output characteristics with respect to the Schottky HEMT, with higher maximum and saturation drain current values observed from DC current-voltage measurements. Gate transfer measurements also show a higher transconductance for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT. Furthermore, from OFF-state measurements, the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT shows a larger reduction of the gate leakage current in comparison to the Al_2O_3 MOS-HEMT. These results demonstrate that the increase in κ of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ compared with Al_2O_3 leads to enhanced device performance when the ternary phase is used as a gate dielectric in the GaN-based MOS-HEMT.

I. INTRODUCTION

Wide bandgap semiconductors such as GaN have a high breakdown field strength, making them very attractive for high-frequency, high-power, and high-temperature power electronic applications.[1,2] Most commercial GaN-based devices available today are based on high electron mobility transistor (HEMT) structures.[3] These devices provide a highly conductive two-dimensional electron gas (2DEG) formed at the heterojunction between GaN and a wider bandgap material such as AlGaN as a result of spontaneous and piezoelectric polarization effects.[4] AlGaN/GaN HEMTs have attracted much attention in the past few years for power switching applications in the medium voltage market (600–1200 V) and radio frequency (RF) applications due to their higher conversion efficiency and higher switching frequency when compared to conventional Si power devices.[5–7] One of the major issues remaining for AlGaN/GaN HEMTs is the high leakage current through the Schottky gate which

causes device performance and reliability issues, as well as increase device losses in the OFF-state.[8–10] To reduce the gate leakage current, wide bandgap, high dielectric constant (high-κ) oxides such as Al_2O_3,[11–14] HfO_2,[15–17] ZrO_2,[17,18] and Ta_2O_5[19] have been used to produce metal-oxide-semiconductor HEMTs (MOS-HEMTs) structures. Al_2O_3 is currently one of the most widely exploited gate dielectrics for GaN-based MOS-HEMTs due to its large bandgap (6.5 eV),[20] large breakdown electric field (5–10 MV/cm),[21] and good chemical and thermal stability. The main limitation of Al_2O_3 as a gate oxide is its modest permittivity ($\kappa \sim 9$).[22] Traditional high-κ dielectrics such as HfO_2 ($\kappa \sim 18$)[22] and ZrO_2 ($\kappa \sim 20$)[23] have a significantly higher permittivity than Al_2O_3, but this comes at the expense of a smaller bandgap,[23,24] which can increase carrier leakage if the barrier height between the insulator and the semiconductor is too low. Compared to HfO_2 and ZrO_2, Ta_2O_5 has shown some promise as a high-κ ($\kappa \sim 25$)[25] gate dielectric for GaN-based devices, with high breakdown electric field (4.5 MV/cm) and relatively low gate leakage despite its lower bandgap (4.4 eV).[18,19,26] Our previous research has shown that the combination of wide bandgap Al_2O_3 with a higher κ material such as Ta_2O_5 can achieve a higher κ value with respect to Al_2O_3 together with a sufficient conduction band offset (CBO) to the GaN-HEMT (>1 eV) for electron confinement,[27] which could allow a further reduction of the gate leakage while maintaining or enhancing the device gate capacitance. In this paper, the optimum composition selected for the ternary oxide was $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$. This is based on preliminary band alignment studies where the band offsets between $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ ($0 \le x \le 1$) films and GaN-on-Si substrate were analyzed as a function of the x molar fraction (shown in the supplementary material). The aim of the selection process was to maximize the κ value of the oxide by maximizing the Ta_2O_5 molar fraction while also ensuring that the band offsets between the oxide and GaN did not fall below 1 eV. To evaluate how the introduction of this ternary gate oxide affects the performance of GaN-based HEMT devices, this paper presents a comparative study of the electrical characteristics of GaN-capped AlGaN/GaN HEMTs with the standard Schottky gate and MOS-HEMTs with either Al_2O_3 or $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate dielectrics.

II. EXPERIMENTAL DETAILS

Figure 1 shows the schematics of the AlGaN/GaN Schottky gate HEMT and the MOS-HEMT devices used in the present study. The $Al_xGa_{1-x}N$/GaN HEMT stack was grown on a 150 mm diameter (1.0 mm thick) Si(111) substrate using an Aixtron close-coupled showerhead metal organic chemical vapor deposition system. The total thickness of the nitride HEMT stack is about 3.6 μm. It consists of an ∼280 nm thick high-temperature AlN layer, followed by three step-graded $Al_xGa_{1-x}N$ intermediate layers with Al composition tuned from 58% to 20%, followed by an uninterrupted growth of a GaN buffer with a thickness of about 1.3 μm and an undoped GaN channel layer of 500 nm in thickness. The GaN buffer grown is unintentionally C-doped. The top HEMT layers comprise a thin AlN spacer layer ∼1.0 nm thick, an ∼20 nm thick $Al_{0.23}Ga_{0.77}N$ barrier layer, and a thin ∼2 nm GaN cap layer.

The average full width at half maximum (FWHM) of the GaN (002) and (102) rocking curves obtained from high-resolution X-ray diffraction measurements were 518 and 1540 arc sec, respectively, indicative of device grade GaN layers on 150 mm Si(111).[28] Atomic force microscopy showed very smooth surface morphology, with an arithmetic average root mean square roughness of 0.15 nm measured in a $5 \times 5\,\mu m^2$ scan area. From Hall-effect measurements at room temperature, the sheet density of the resultant 2DEG was in the order of $\sim 6.5–7.7 \times 10^{12}\,cm^{-2}$ and the electron mobility was about $\sim 1300–1400\,cm^2/V\,s$.

To fabricate the devices, mesa isolation was performed using inductively coupled plasma (ICP) etching with a Cl_2-based plasma to etch around 350 nm. A Ti/Al/Ni/Au metal stack was thermally evaporated onto the sample and annealed at 830 °C under N_2 ambient to form the source and drain ohmic contacts. The contact resistance extracted from transmission line model measurements[29] was in the range of 0.5–0.9 Ω mm. A SiN_x passivation layer of ∼80 nm was deposited using plasma-enhanced chemical vapor deposition, and 1.5 μm gate windows were opened by etching through the SiN_x layer using ICP etching. For the MOS-HEMT devices, ∼10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides were deposited at 250 °C by atomic layer deposition (ALD) using an Oxford OpAL thermal ALD reactor. Trimethylaluminium (TMA), pentakis(dimethylamino)tantalum (PDMAT), and de-ionized water (H_2O) were used as the aluminum, tantalum, and oxygen sources, respectively. Tantalum doping was achieved using delta doping where every three cycles of TMA and H_2O (20 ms TMA dose/5 s purge/20 ms H_2O dose/5 s purge) were followed by a cycle of PDMAT and H_2O (4 s PDMAT dose/5 s purge/20 ms H_2O dose/5 s purge). The measured growth rates for the Al_2O_3 and Ta_2O_5 ALD processes were about 0.9Å/cycle and 0.76Å/cycle, respectively. The gate oxides were grown using a total of 120 ALD cycles. The samples were then annealed at 600 °C for 60 s under N_2 ambient to improve the interface between the gate dielectric and the semiconductor surface (see Ref. 27 for more details). Following this, T- shape Ni/Au gate metal electrodes with 100 μm gate width were deposited by thermal evaporation. The final devices have a gate-source separation of 2.5 μm, a gate-drain separation of 12 μm, and a gate field plate extension of 1 μm toward both the drain and the source. For the present study, a minimum number of five devices were measured for each structure. The data presented are representative of the typical behaviors observed for each of the three structures.

III. RESULTS AND DISCUSSION

A. Input characteristics

The gate-source capacitance for the Schottky HEMT (C_{GS}^{HEMT}) can be modeled as a series capacitance of the AlN spacer (C_{AlN}), the AlGaN barrier (C_{AlGaN}), and the GaN cap (C_{GaN}) [Fig. 1(a)]. For the MOS-HEMTs, it is assumed that the gate oxide contributes an additional series capacitance to the gate structure [Fig. 1(b)]. The MOS-HEMTs gate-source capacitance ($C_{GS}^{MOS-HEMT}$) can, therefore, be described by

$$1/C_{GS}^{MOS-HEMT} = 1/C_{AlN} + 1/C_{AlGaN} + 1/C_{GaN} + 1/C_{ox}, \quad (1)$$

where $C_{AlN} = \kappa_{AlN} \cdot \varepsilon_0 \cdot A/t_{AlN}$, $C_{AlGaN} = \kappa_{AlGaN} \cdot \varepsilon_0 \cdot A/t_{AlGaN}$, $C_{GaN} = \kappa_{GaN} \cdot \varepsilon_0 \cdot A/t_{GaN}$, and $C_{ox} = \kappa_{ox} \cdot \varepsilon_0 \cdot A/t_{ox}$. κ and t are

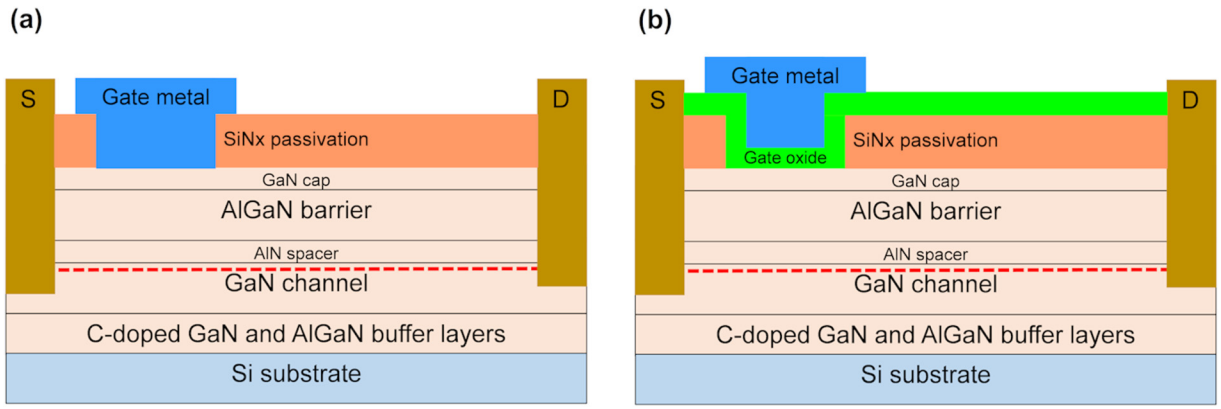

FIG. 1. Schematic of the cross section of the (a) Schottky gate AlGaN/GaN HEMT and (b) AlGaN/GaN MOS-HEMT structures used in the present study.

the relative permittivity and thickness of the layers, ε_0 is the permittivity of free space, and A is the area of the gate.

Figure 2 shows the gate-source capacitance (C_{GS}) of $\sim 100 \times 160\,\mu m^2$ area Schottky and MOS-HEMTs obtained as a function of the gate-source voltage (V_{GS}), using C-V measurements at 10 kHz with V_{GS} swept from −6 V to +1 V. As expected, the accumulation capacitance for the MOS-HEMT devices is significantly less than that of the Schottky HEMT (Fig. 2), which is in agreement with Eq. (1). It can be observed that the capacitance of the Schottky HEMT dramatically increases above 0.5 V. This is attributed to charge overflow from the 2DEG channel,[30] which decreases the effective barrier layer thickness. The accumulation C_{GS} values obtained for the three devices range from 4.3×10^{-3} F/m^2 for the Schottky HEMT to 2.6×10^{-3} F/m^2 for the Al_2O_3 MOS-HEMT and 2.8×10^{-3} F/m^2 for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT. Using the measured C_{GS} values and Eq. (1), the κ values calculated for the ∼10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ layers are 7.2 and 9.8, respectively. The increase in the permittivity of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ with respect to that of the Al_2O_3 is in agreement with our previous study where the permittivity of $(Ta_2O_5)_x(Al_2O_3)_{1-x}$ layers on Si was measured as a function of the Ta_2O_5 molar fraction.[27]

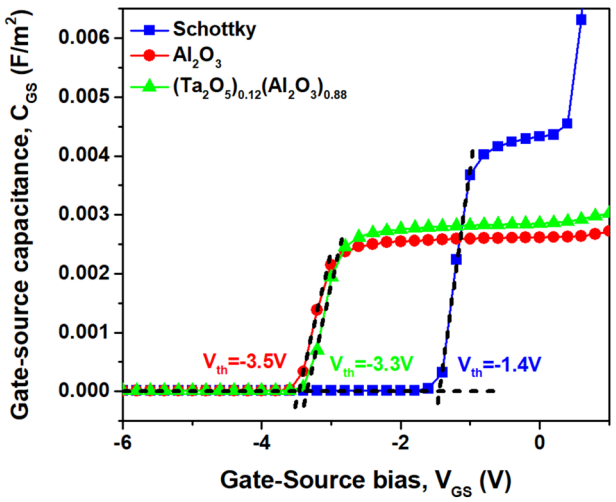

FIG. 2. C-V measurements at 10 kHz for $\sim 100 \times 160\,\mu m^2$ area Schottky gate HEMT and MOS-HEMT structures fabricated with ∼10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides.

The reduction in C_{GS} following the introduction of the gate oxide is equivalent to a reduced ability to deplete the 2DEG channel with a given bias. A higher V_{GS} is, therefore, needed to "pinch-off" the channel in the MOS-HEMTs compared to the Schottky HEMT. This is reflected by a significant increase in the absolute threshold voltage (V_{th}) value[31] extracted from the C-V characteristics (Fig. 2). Assuming the same sheet charge density in the channel for the Schottky HEMT and the MOS-HEMTs at zero gate bias and not taking into account the surface charge at the oxide/GaN interface, the V_{th} absolute value of the MOS-HEMTs ($V_{th}^{MOS-HEMT}$) increases with respect to that of the HEMT (V_{th}^{HEMT}) as follows:[31]

$$Q_S = q\,N_S = C_{GS}^{MOS-HEMT} \times V_{th}^{MOS-HEMT} = C_{GS}^{HEMT} \times V_{th}^{HEMT}, \tag{2}$$

$$V_{th}^{MOS-HEMT} = V_{th}^{HEMT}(C_{GS}^{HEMT}/C_{GS}^{MOS-HEMT}), \tag{3}$$

where Q_S is the charge at the metal/oxide and metal/semiconductor interfaces and N_S is the 2DEG sheet carrier density.

A negative shift in the V_{th} can be observed for the MOS-HEMT devices (Fig. 2), which is in agreement with Eq. (3). The V_{th} decreases from −1.4 V for the Schottky HEMT to −3.5 V and −3.3 V for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs, respectively. The theoretical V_{th} values from Eq. (3) for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs are −2.3 V and −2.1 V, respectively, which are 1.2 eV smaller than the values obtained

experimentally. The difference between the experimental and calculated values is attributed to fixed oxide charges due to oxide/GaN interface states and/or bulk oxide traps.[30–32] The V_{th} shift caused by the interface charge is the same for both the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs. This is attributed to the fact that initial ALD cycles for the growth of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ were Al_2O_3 cycles; hence, the tantalum dopant ions are not directly in contact with the semiconductor. The results show that the smaller V_{th} absolute value obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT in comparison to the Al_2O_3 MOS-HEMT is related to the bigger C_{GS} achieved using a higher κ gate dielectric.

The 2DEG sheet carrier concentration (n_s) of the HEMTs for a given gate bias and low electric fields can be approximated by a simple analytical model by Thayne *et al.*,[33]

$$n_s = [C_{GS}/q] \times [V_{GS} - V_{th}]\ . \tag{4}$$

Figure 3 shows n_s of the three devices as a function of V_{GS}, obtained from the C-V measurements. The results show that n_s is a linear function of V_{GS} for voltages beyond the V_{th} (Fig. 3), which is in accordance with Eq. (4). The exception to this is for the Schottky HEMT at V_{GS} values above 0.5 V, where the slope increases due to the charge overflow from the 2DEG channel[30] discussed earlier. It can be observed that n_s of the MOS-HEMTs is higher than n_s of the Schottky HEMT for voltages $V_{th} < V < 0.5$ V. This experimental increase observed for the n_s in the active region of the MOS-HEMTs is explained by the fact that the reduction of C_{GS} does not exactly correspond to the increase of the V_{th} [Eq. (4)]. The increase in n_s is believed to be caused by either the gate oxide's passivation effect in the gate region, which reduces the number of GaN surface states that can trap electrons leading to less electron depletion in the 2DEG,[34,35] or by the increase in positive charge/reduction in negative charge at the oxide/GaN interface after oxide deposition, which neutralizes the fixed polarization charge.[34] The results indicate that n_s depends on the gate dielectric properties. For a given V_{GS}, n_s of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT is bigger than n_s of the Al_2O_3 MOS-HEMT. In fact, from Eq. (4), the slope of the n_s can be approximated as[32]

$$\frac{\partial n_s}{\partial V_{GS}} = C_{GS}/q. \tag{5}$$

Thus, the decrease in the n_s slope observed for the MOS-HEMTs is due to smaller C_{GS} obtained after the introduction of the gate dielectrics, which is in agreement with the simple HEMT analytical model.

B. ON-state output characteristics

1. Direct-current current-voltage characteristics

The drain current (I_D) of a HEMT can be described as[36]

$$I_D = q \times W_G \times n_s \times v, \tag{6}$$

where W_G is the gate width and v is the 2DEG charge carrier velocity.

Figure 4 shows a comparison of the current-voltage (I-V) characteristics under DC biasing for the three devices, for various V_{GS} values between −4 V and +2 V, in steps of 2 V. The pinch-off voltage is −2 V for the Schottky HEMT and −4 V for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs. In several of the data sets, I_D reaches a maximum and then decreases slightly with a further increase in V_{DS}. This is attributed to self-heating arising from the poor thermal conductivity of the Si substrate.[37]

An increase in the MOS-HEMTs maximum I_D at a positive gate bias is observed (Fig. 4), which is consistent with Eq. (6). When a $V_{GS} = +2$ V is applied, the maximum drain saturation

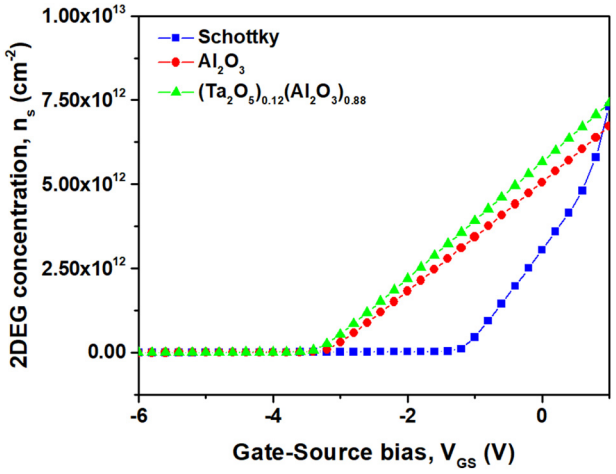

FIG. 3. n_s as a function of the V_{GS} obtained from C-V measurements at 10 kHz for the ~100 × 160 μm^2 area Schottky gate HEMT and MOS-HEMT structures fabricated with ~10 nm thick Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides.

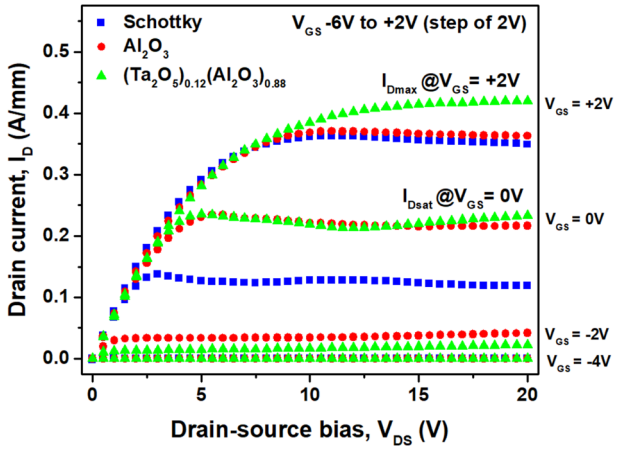

FIG. 4. Output I-V characteristics of the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs showing I_D as a function of V_{DS} for varying V_{GS} between −6 V and +2 V in steps of +2 V.

current ($I_{D,sat}$) measured for the Schottky HEMT is 0.36 A/mm, while for the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs the values are 0.37 A/mm and 0.42 A/mm, respectively. Since the DC saturation current is a key parameter in establishing the maximum RF power output for HEMT devices, the results indicate the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ to increase κ of Al_2O_3 as gate dielectric further improves the MOS-HEMT DC output characteristics.

According to a more advanced model proposed by Das to describe the basic DC characteristics of an ideal HEMT,[38] the decrease in C_{GS} with accompanying increase in V_{th} absolute value after the introduction of the gate oxides results in a higher $I_{D,sat}$ and a significant shift in the drain-source saturation voltage ($V_{DS,sat}$) obtained from the I-V characteristics (Fig. 4). It has been reported that, for zero or small positive V_{GS}, the introduction of a gate dielectric increases the MOS-HEMT $I_{D,sat}$ by a factor of approximately $C_{GS}^{MOS-HEMT}/C_{GS}^{HEMT}$,[39] which is commensurate with the results obtained in this study. Compared to the Schottky HEMT, $I_{D,sat}$ of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs increases from 0.14 A/mm to 0.23 A/mm and 0.24 A/mm at $V_{GS} = 0$ V, respectively. It has also been reported that the MOS-HEMT $V_{DS,sat}$ increases by a value close to the absolute value of the V_{th} shift,[39] which is also observed here. $V_{DS,sat}$ of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs increases from +3 V to +5.5 V and +5 V at $V_{GS} = 0$ V, respectively, indicating that the use of the gate oxides improves the DC saturation characteristics of the MOS-HEMTs by increasing the saturation current and enabling the use of a higher positive gate voltage. $I_{D,sat}$ achieved for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT is bigger than $I_{D,sat}$ of the Al_2O_3 MOS-HEMT. In addition, $V_{DS,sat}$ obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT is smaller than the Al_2O_3 MOS-HEMT $V_{DS,sat}$. This smaller increase in $V_{DS,sat}$ is related to the smaller V_{th} shift toward negative values previously observed for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT in comparison to the Al_2O_3 MOS-HEMT and has the effect of reducing the on-state losses in switching transistors and improved power added efficiency in RF devices.

2. Gate transfer characteristics

The intrinsic transconductance (g_m) of a HEMT can be extracted by differentiating I_D with respect V_{GS}.[38] Using the model proposed by Das, a decrease in the C_{GS} due to the introduction of a dielectric layer results in a decrease of the g_m ($g_m < C_{GS}/L_G \cdot v_{sat}$),

$$g_m = (C_{GS}/L_G) \times \left(1 - (1 + 2 \times ([V_{GS} - V_{th}]/V_{cr}))^{-\frac{1}{2}}\right) \times v_{sat}, \quad (7)$$

where L_G is the gate length, v_{sat} is the 2DEG charge carrier saturation velocity, and V_{cr} is the critical voltage.

Figure 5 shows a comparison of the gate transfer characteristics for the three devices. I_D and g_m are obtained as a function of V_{GS}, sweeping V_{GS} from −6 V to +2 V with V_{DS} kept at 10 V [Fig. 5(a)]. It can be observed that the maximum transconductance ($g_{m,max}$) for the Al_2O_3 MOS-HEMT is less than that of the other two devices, which is consistent with Eq. (7). The g_m curve for the Al_2O_3 MOS-HEMT exhibits a second peak, which is attributed to the presence of a parasitic current path beyond the 2DEG channel which could be avoided with further optimization of the device fabrication process.[40] Unlike the decrease in $g_{m,max}$ obtained for the Al_2O_3 MOS-HEMT, the results show similar $g_{m,max}$ values for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT and the Schottky HEMT. This can be caused by an improvement in the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT intrinsic mobility due to a mobility-dependent carrier depletion effect below the gate.[41] Consequently, $g_{m,max}$ of MOS-HEMTs can be similar or even higher than that of the Schottky HEMT, and the increase of $g_{m,max}$ is more readily obtained for higher κ or thinner insulators,[41] which is consistent with the results here. $g_{m,max}$ obtained for the Schottky HEMT and the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT is 0.13 S/mm, whereas for the Al_2O_3 MOS-HEMT, $g_{m,max}$ decreases to 0.11 S/mm. The gate transconductance ultimately quantifies the ability to control the

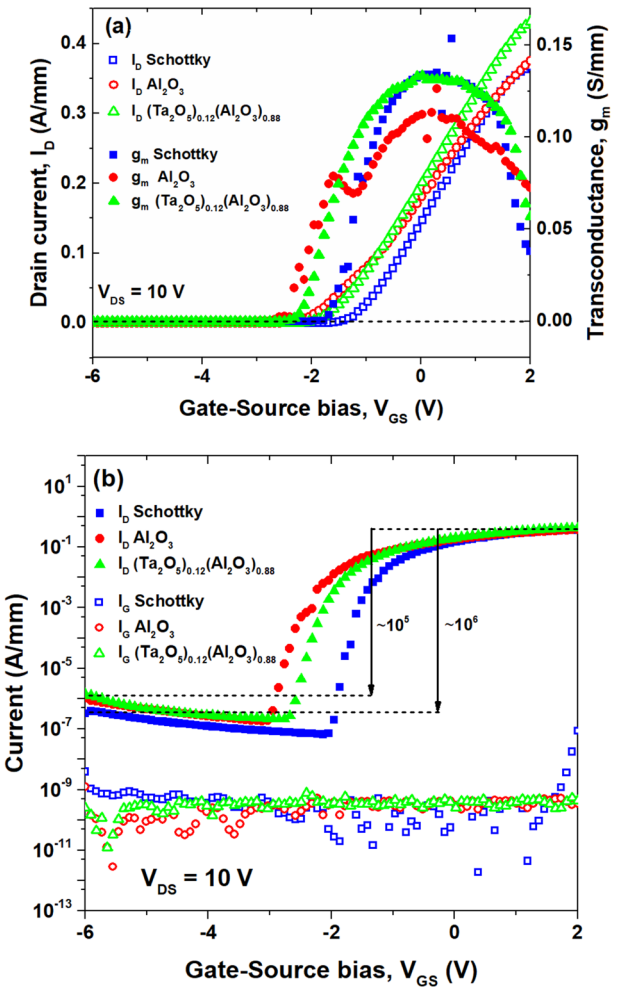

FIG. 5. (a) Output I_D and g_m and (b) I_D and I_G of the Schottky HEMT and the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs with $V_{DS} = +10$ V and V_{GS} sweeps from −6 V to +2 V.

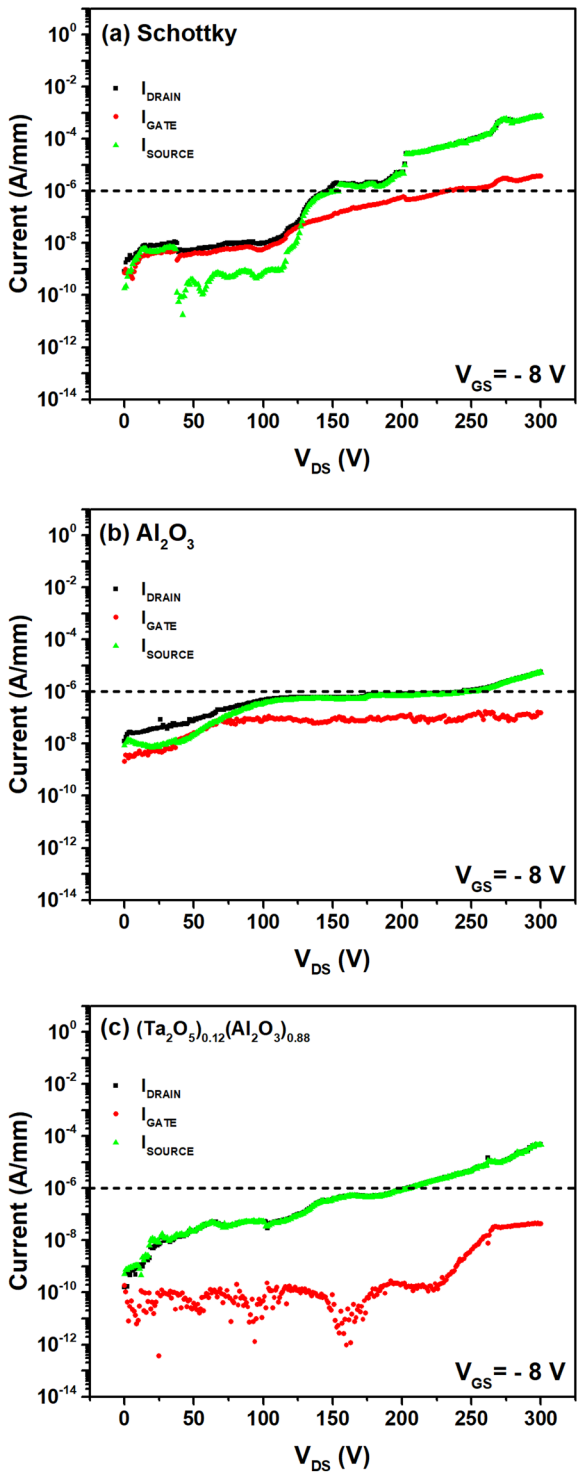

FIG. 6. Three-terminal OFF-state measurements of the (a) Schottky HEMT, (b) Al_2O_3 MOS-HEMT, and (c) $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT with $V_{GS} = -8$ V and V_{DS} swept from −0 V to +300 V.

2DEG channel. Therefore, the bigger g_m obtained for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT in comparison to the Al_2O_3 MOS-HEMT is an indicator of superior channel control.

The devices output I_D and gate current (I_G) are shown in Fig. 5(b), as a function of V_{GS} at $V_{DS} = +10$ V. The I_D ON-OFF ratio of the three devices is limited by the OFF-state drain leakage current likely dominated by horizontal source-drain leakage via buffer[42] rather than I_G. When V_{GS} is −6 V, I_D of the Schottky HEMT is below 4×10^{-7} A/mm, whereas I_D of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs is below 2×10^{-6} A/mm. This results in an I_D ON-OFF ratio of around 10^6 for the Schottky HEMT and 10^5 for the MOS-HEMTs. On the other hand, I_G of the three devices remains reasonably stable below $\sim 10^{-9}$ A/mm for V_{GS} values up to +1 V. The MOS-HEMTs and the Schottky HEMT show similar I_G values due to the measurements minimum current limit at a low voltage regime (<+10 V). However, for V_{GS} values above +1 V, I_G of the Schottky HEMT starts to increase rapidly. This indicates that the substitution of the gate Schottky barrier by a MOS structure can effectively reduce the ON-state gate leakage.[34]

C. OFF-state output characteristics

Figure 6 shows the three-terminal OFF-state I-V characteristics of the three devices, obtained by sweeping V_{DS} from 0 V to 300 V with V_{GS} kept at −8 V. The substrates were not grounded during the measurements. From Fig. 6(a), it can be observed that the gate leakage current (I_{GATE}) of the Schottky gate HEMT structure dominates when V_{DS} is below 130 V, and the leakage between the source and the drain terminals (I_{SOURCE}) overtakes I_{GATE} for voltages above 130 V. I_{GATE} surpasses 1 μA/mm for voltages above 233 V. For the MOS-HEMTs [Figs. 6(b) and 6(c)], I_{GATE} is smaller than I_{SOURCE} up to 300 V. This means that I_{GATE} is not the main source of leakage in the MOS-HEMTs for the range of V_{DS} measured. In addition to this, I_{GATE} remains below 1 μA/mm up to 300 V. Compared to the Schottky HEMT, I_{GATE} of the MOS-HEMTs is significantly less at $V_{DS} = 300$ V. For the Schottky gate device, I_{GATE} at $V_{DS} = 300$ V is found to be below 4×10^{-6} A/mm, whereas I_{GATE} of the Al_2O_3 and $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMTs are under 1.5×10^{-7} A/mm and 4.3×10^{-8} A/mm at $V_{DS} = 300$ V, respectively. Thus, a reduction of the OFF-state gate leakage current is achieved by introducing the gate oxides, with an observed decrease of over one order of magnitude for the Al_2O_3 MOS-HEMT and a higher decrease of over two orders of magnitude for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT.

IV. CONCLUSIONS

The electrical characteristics of a GaN-capped AlGaN/GaN Schottky HEMT and MOS-HEMTs with either Al_2O_3 or $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ gate oxides have been analyzed. The MOS-HEMTs show a smaller gate capacitance and bigger absolute threshold voltages than an equivalent Schottky HEMT device due to the larger gate-to-channel separation and the charge induced at the oxide/GaN interface. However, compared to the Al_2O_3 MOS-HEMT, the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT achieves a bigger capacitance and a smaller absolute threshold voltage, improving the gate modulation efficiency and reducing power consumption during switching. This in turn results in a higher 2DEG

concentration for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT compared with those of the Schottky HEMT and the Al_2O_3 MOS-HEMT, increasing its saturation drain current, which gives superior device power output. The maximum transconductance of the Al_2O_3 MOS-HEMT compared to the Schottky HEMT decreases, whereas the maximum transconductance of the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT remains similar, which indicates better channel control. The MOS-HEMTs also show a significant reduction of the gate leakage current [over one order of magnitude for the Al_2O_3 MOS-HEMT and over two orders of magnitude for the $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ MOS-HEMT, when the drain-source voltage is 300 V]. Hence, as well as larger gate leakage current suppression, the use of $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ increases κ of the gate dielectric, further improving the MOS-HEMT electrical performance.

SUPPLEMENTARY MATERIAL

See the supplementary material for the band offsets between $(Ta_2O_5)_{0.12}(Al_2O_3)_{0.88}$ $(0 \leq x \leq 1)$ films and GaN-on-Si substrate as a function of the x molar fraction.

ACKNOWLEDGMENTS

Z. H. Zaidi, J. W. Roberts, K. B. Lee, P. A. Houston, and P. R. Chalker gratefully acknowledge funding support from the Engineering and Physical Sciences Research Council Programme Grant—Silicon Compatible GaN Power Electronics (No. EP/K014471/1).

REFERENCES

[1]T. Flack, B. Pushpakaran, and S. Bayne, J. Electron. Mater. **45**, 2673 (2016).
[2]M. J. Scott, L. X. Fu, X. Zhang, J. Z. Li, C. C. Yao, M. Sievers, and J. Wang, Semicond. Sci. Technol. **28**, 074013 (2013).
[3]E. A. Jones, F. Wang, and D. Costinett, J. Emerg. Sel. Top. Power Electron. **4**, 707 (2016).
[4]O. Ambacher, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu, M. Murphy, W. J. Schaff, L. F. Eastman, R. Dimitrov, L. Wittmer, M. Stutzmann, W. Rieger, and J. Hilsenbeck, J. Appl. Phys. **85**, 3222 (1999).
[5]K. S. Boutros, R. Chu, and B. Hughes, in *IEEE Energytech* (IEEE, 2012).
[6]B. J. Baliga, Semicond. Sci. Technol. **28**, 074011 (2013).
[7]U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, Proc. IEEE **96**, 287 (2008).
[8]E. Yu, J. Appl. Phys. **99**, 023703 (2006).
[9]L. Xia, A. Hanson, T. Boles, and D. Jin, Appl. Phys. Lett. **102**, 113510 (2013).
[10]J. W. Chung, T. Palacios, J. C. Roberts, and E. L. Piner, IEEE Electron Device Lett. **29**, 1196 (2008).
[11]P. D. Ye, B. Yang, K. K. Ng, J. Bude, G. D. Wilk, S. Halder, and J. C. M. Hwang, Appl. Phys. Lett. **86**, 063501 (2005).
[12]Y. Yue, Y. Hao, Q. Feng, J. Zhang, X. Ma, and J. Ni, Chin. Phys. Lett. **24**, 2419 (2007).
[13]G. Pozzovivo, J. Kuzmik, S. Golka, W. Schrenk, G. Strasser, D. Pogany, K. Čičo, M. Ťapajna, K. Fröhlich, J. F. Carlin, M. Gonschorek, E. Feltin, and N. Grandjean, Appl. Phys. Lett. **91**, 043509 (2007).
[14]F. Medjdoub, E. Kohn, N. Sarazin, M. Tordjman, M. Magis, M. A. Di Forte-Poisson, S. L. Delage, M. Knez, E. Delos, and C. Gaquière, Electron. Lett. **43**, 691 (2007).
[15]Y. Yue, Y. Hao, J. Zhang, J. Ni, W. Mao, Q. Feng, and L. Liu, IEEE Electron Device Lett. **29**, 838 (2008).
[16]Y. C. Chang, W. H. Chang, Y. H. Chang, J. Kwo, Y. S. Lin, S. H. Hsu, J. M. Hong, C. C. Tsai, and M. Hong, Microelectron. Eng. **87**, 2042 (2011).
[17]S. Abermann, G. Pozzovivo, J. Kuzmik, G. Strasser, D. Pogany, J. F. Carlin, N. Grandjean, and E. Bertagnolli, Semicond. Sci. Technol. **22**, 1272 (2007).
[18]G. G. Ye, H. Wang, S. Arulkumaran, G. I. Ng, R. Hofstetter, Y. Li, M. J. Anand, K. S. Ang, Y. K. T. Maung, and S. C. Foo, Appl. Phys. Lett. **103**, 142109 (2013).
[19]D. Deen, D. Storm, D. Meyer, D. S. Katzer, R. Bass, S. Binari, and T. Gougousi, Phys. Status Solidi C **8**, 2420 (2011).
[20]E. Bersch, S. Rangan, R. A. Bartynski, E. Garfunkel, and E. Vescovo, Phys. Rev. B **78**, 085114 (2008).
[21]H. C. Lin, P. D. Ye, and G. D. Wilk, Appl. Phys. Lett. **87**, 182904 (2005).
[22]Y. C. Chang, M. L. Huang, Y. H. Chang, Y. J. Lee, H. C. Chiu, J. Kwo, and M. Hong, Microelectron. Eng. **88**, 1207 (2011).
[23]R. E. Nieh, C. S. Kang, H. J. Cho, K. Onishi, R. Choi, S. Krishnan, J. H. Han, Y. H. Kim, M. S. Akbar, and J. C. Lee, IEEE Trans. Electron. Devices **50**, 333 (2003).
[24]J. Yang, B. S. Eller, C. Zhu, C. England, and R. J. Nemanich, J. Appl. Phys. **112**, 053710 (2012).
[25]C. Adelmann, A. Delabie, B. Schepers, L. N. J. Rodriguez, A. Franquet, T. Conard, K. Opsomer, I. Vaesen, A. Moussa, G. Pourtois, K. Pierloot, M. Caymax, and S. Van Elshocht, Chem. Vap. Depos. **18**, 225 (2012).
[26]A. Paskaleva and E. Atanassova, J. Phys. D **39**, 2950 (2006).
[27]T. Partida-Manzanera, J. W. Roberts, T. N. Bhat, Z. Zhang, H. R. Tan, S. B. Dolmanan, N. Sedghi, S. Tripathy, and R. J. Potter, J. Appl. Phys. **119**, 025303 (2016).
[28]B. Heying, X. H. Wu, S. Keller, Y. Li, D. Kapolnek, B. P. Keller, S. P. Denbaars, and J. S. Speck, Appl. Phys. Lett. **68**, 643 (1996).
[29]H. H. Berger, Solid-State Electron. **15**, 145 (1972).
[30]M. Khan, X. Hu, A. Tarakji, G. Simin, J. Yang, R. Gaska, and M. Shur, Appl. Phys. Lett. **77**, 1339 (2000).
[31]M. A. Khan, G. Simin, J. Yang, J. Zhang, A. Koudymov, M. S. Shur, X. Hu, and A. Tarakji, IEEE Trans. Microwave Theory Tech. **51**, 624 (2003).
[32]A. Pérez-Tomás, M. Placidi, X. Perpiñà, A. Constant, P. Godignon, X. Jordà, P. Brosselard, and J. Millán, J. Appl. Phys. **105**, 114510 (2009).
[33]K. Thayne, I. Elgaid, and G. Ternet, *Devices and Fabrication Technology* (IEEE, London, 2001), pp. 31–81.
[34]M. Marso, G. Heidelberger, K. M. Indlekofer, J. Bernát, A. Fox, P. Kordoš, and H. Lüth, IEEE Trans. Electron Devices **53**, 1517 (2006).
[35]R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, IEEE Trans. Electron Devices **48**, 560 (2001).
[36]X. Cheng, M. Li, and Y. Wang, Solid State Electron. **54**, 42 (2010).
[37]H. I. Fujishiro, N. Mikami, T. Takei, M. Izawa, T. Moku, and K. Ohtuka, in *2003 International Symposium on Compound Semiconductors Post-Conference Proceedings* (IEEE, 2003), pp.152–157.
[38]M. B. Das, *HEMT Device Physics and Models* (Artech House, Norwood, MA, 1991), pp. 11–75.
[39]A. Pérez-Tomás, A. Fontsere, M. R. Jennings, and P. M. Gammon, Mater. Sci. Semicond. Process. **16**, 1336 (2013).
[40]M. K. Tsai, S. W. Tan, Y. W. Wu, W. S. Lou, and Y. J. Yang, Semicond. Sci. Technol. **17**, 15 (2002).
[41]J. Kuzmik, G. Pozzovivo, S. Abermann, J. F. Carlin, M. Gonschorek, E. Feltin, N. Grandjean, E. Bertagnolli, G. Strasser, and D. Pogany, IEEE Trans. Electron. Devices **55**, 937 (2008).
[42]E. Bahat-Treidel, O. Hilt, F. Brunner, J. Würfl, and G. Tränkle, IEEE Trans. Electron Devices **55**, 3354 (2008).