Evaluation of DC-Link Voltage Switching Ripple in Multiphase PWM Voltage Source Inverters

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***Abstract*—This paper presents a generalized approach towards the dc-link voltage switching ripple analysis in two-level multiphase PWM voltage source inverters with balanced load. Since voltage ripple is one of the crucial sizing criteria for dc-link capacitor, simple and practical equation for designing the dc-link capacitor, based on the maximum (peak-to-peak) value of the dc-link voltage ripple, has been proposed for multiphase inverters. The amplitude of the dc-link voltage switching ripple is analytically derived as a function of operating conditions. The effect of the number of phases on the dc-link capacitor size is investigated as well. It is found that considering the same total output current, the dc-link capacitor size is reduced increasing the number of phases up to seven. However, from the point of view of dc-link capacitor size, there are no benefits of further increasing the number of phases. Reference is made to two commonly used modulation strategies – sinusoidal PWM and continuous symmetric centered PWM (i.e., space vector). The mathematical models derived aim to provide precise dc-link capacitor sizing and hence improve the power density of the whole system. Comparison of different phase numbers has been made. Proposed theoretical developments are verified by simulation and experimental tests.**

I. Introduction

Nowadays, highly reliable and efficient power electronics, as well as low operational and maintenance cost, are the major requirements set by the industry. Besides active semiconductor power devices, capacitors are another type of components that fail more frequently than other components in power electronic systems [1, 2]. Therefore, a huge research interest has been recently devoted to the dc-link capacitor optimization. This is particularly important for the applications of multiphase machines such as in electric vehicles, where the volume, fault-tolerance, weight and cost are of crucial importance. Therefore, reduction of dc-link capacitor size (and not increase) is an additional benefit.

The challenges in the design and selection of dc-link capacitors could be considered from different perspectives, such as the trends for reduction of weight and volume, high reliability for exposure to harsh environments (high ambient temperature, high humidity, etc.), the prevention of overheating, the extension of life-time and cost reduction [3]. In order to overcome the above challenges, it is necessary to carry out a detailed analysis of inverter's input variables since the dc-link capacitor is usually sized and selected according to their ripple profiles.

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The presence of high ripple currents on the dc-link side causes the increase of capacitor's core temperature, and thus accelerates the degradation of the capacitor itself. This is why many recent studies have focused on root mean square (RMS) calculations and spectral analysis of the input current. Dominantly, the analysis refers to the two-level three-phase inverters. In [4-6], the RMS value of the dc-link capacitor current is calculated, by using the time domain approach. In [7-9], the dc-link current spectra are described by a double Fourier series. A new PWM strategy, called extended double carrier PWM, for a two-level three-phase inverters has been proposed in [10] aiming at reducing the RMS current flowing through the dc-link capacitors. The RMS values and frequency spectra of the capacitor current in three-phase EV drive systems are analyzed in [11] with respect to three modulation strategies and various operating conditions. A generalized approach for determining the harmonic spectrum of the dc-link capacitor currents in different two- and three-level VSI topologies has been developed in [12]. The calculation of dc-link capacitor RMS current and current spectrum comparison considering AC current ripple has been achieved in [13].

The RMS calculations of the input current has been extended to the two-level multiphase inverters as well. For example, in [14] the impact of classical PWM modulation, with and without common mode injection on the RMS value of the dc-link current has been studied for dual-three phase induction machine. A PWM strategy dedicated to minimization of the RMS of the dc-link current in dual three-phase drive has been compared in [15] with more conventional PWM techniques. It has been shown that PWM strategies have different effect on the RMS of the dc-link current and on the quality of the output current. However, both constraints have to be taken into account for the dc link capacitor sizing. The RMS value of the input current ripple is derived in [16] for a six-phase drive system. As an alternative solution to six-phase drive system, double winding and dual inverter fed ac drive systems are considered and the input current ripple is compared among several modulations. In [17] it has been shown that if a square-wave VSI control is used, the increase of the phase number allows decrease of the RMS value of the dc-link current. Comparison of square-wave and a PWM control through spectral analysis is conducted for a seven-phase drive. The RMS calculations of input current ripple in nine-phase PWM inverter are carried out in [18]. In [19] is shown that the RMS of the input current ripple can be reduced by increasing the phase number from three to five. It also shows that when the phase number is higher than nine no significant reduction of the input current ripple was proven.

Unlike the input current, the input (dc-link) voltage has been analyzed less. The peak-to-peak voltage ripple calculations are useful for sizing the dc-link capacitor precisely, allowing thus, more stringent requirements on the dc-link capacitor size reduction to be met. Apart from this, maximum of the dc-link voltage switching ripple amplitude could have additional specific restrictions to limit switching noise, electromagnetic interferences and voltage stress on the dc bus components. Still, most of the research related to the dc-link voltage has been devoted to the three-phase cases. For example, the peak-to-peak voltage ripple envelope is calculated in [20] as a function of modulation index, output current and output phase angle when space vector modulation is applied. The theoretical developments are further used for the dc-link capacitor design. The effect of unbalanced load conditions on the input current and dc-link voltage, in three-phase VSIs, has been presented in [21]. In [22], the dc-link current and voltage ripple are calculated for inverters and rectifiers in hybrid electric vehicle (HEV) converter/inverter systems, operated by sinusoidal PWM and six-step modulation.

Referring to the multiphase inverters, the input dc-link voltage ripple analysis has been significantly less investigated. Calculation of input current and voltage ripple RMS values, for five-phase inverters has been reported in [23]. Different modulation techniques are considered, and it is shown that the RMS value of the input current ripple is practically independent of it. However, for the dc-link voltage ripple RMS value it is concluded that it is minimal for sinusoidal PWM (which is different to three-phase case). The peak-to-peak (rather than RMS) dc-link voltage ripple amplitude for five-phase VSIs has been preliminary derived in [24] when space vector modulation is applied. Its maximum value has been shown as a function of modulation index for different output phase angles. Simulations are shown but the experimental proofs are not reported. Similarly, the dc-link voltage switching ripple amplitude has been calculated for the seven-phase VSIs in [25]. The analytical developments are supported by simulation results only.

Therefore, most of the analyses of multiphase inverters have been related to the RMS calculations of the input current ripple, and only two preliminary analyses related to the dc-link peak-to-peak voltage ripple analysis in multiphase drives have been performed. Apart from the experimental proofs, a generalization and a fair comparison among the different cases are missing, and hence are performed here.

In this paper, the analysis of the dc-link voltage switching ripple for two-level multiphase PWM voltage source inverters with an odd number of phases, equal or greater than three, has been presented considering balanced load conditions.

The peak-to-peak value of the ripple has been considered. Being an intermediate variable in calculating the dc-link voltage ripple, the inverter input current calculation has been revised in Section II. A short review of applied modulation techniques is provided in what follows. In Section III, the dc-link voltage switching ripple has been evaluated, focusing particularly on the five- and seven-phase case. The peak-to-peak voltage ripple amplitude is analytically determined over the fundamental period as a function of operational conditions for two applied modulation techniques. In Section IV, different diagrams of the normalized peak-to-peak voltage ripple amplitude are shown, and the maximum of the voltage ripple amplitude is numerically determined as a function of modulation index. The comparison of voltage switching ripple in terms of the voltage ripple envelope and its maximum value has been provided considering also higher phase numbers. The effect of applied modulations on the maximum value of the dc-link voltage switching ripple has been analyzed as well.

The capacitor size is designed according to the voltage switching ripple requirements, and the effect of the number of phases on the sizing has been discussed. In Section V numerical simulations and complete set of experimental tests for both, five- and seven-phase inverter topologies are performed in order to verify theoretical developments. Finally, the main results are summarized in the Conclusion.

II. Basic Inverter Equations

A. General remarks

The multiphase (n-phase, n is generally considered here as an odd number) VSI topology supplying a star connected balanced passive- or motor-load is presented in Fig. 1. The inverter is supplied by a dc-link voltage v, supposed to be almost constant ($v \approx V$), determined by a dc voltage source V_{dc} and a series dc impedance Z_{dc}, representing an input filter (i.e. a dc reactor) or a resistive dc supply.

Considering the linear modulation region, the reference inverter phase voltages are sinusoidal and symmetrical, corresponding to:

$$v_k^* = mV\cos\left(\vartheta-(k-1)\frac{2\pi}{n}\right),\ k = 1,2,...n \qquad (1)$$

where $\Theta=\omega t$, $\omega=2\pi/T$ is the fundamental angular frequency, T is the fundamental period and m is the inverter modulation index, defined as the ratio between the amplitude of the desired phase voltage V_0, and V, i.e. $m = V_0/V$.

Considering sinusoidal PWM output voltages (1), for balanced load and neglecting the output current ripple, the corresponding n-phase output currents are sinusoidal and symmetrical as well

$$i_k = I_0\cos\left(\vartheta-(k-1)\frac{2\pi}{n}-\varphi\right),\ k = 1, 2, ...n \qquad (2)$$

where I_0 is the output current amplitude and φ is the output phase angle.

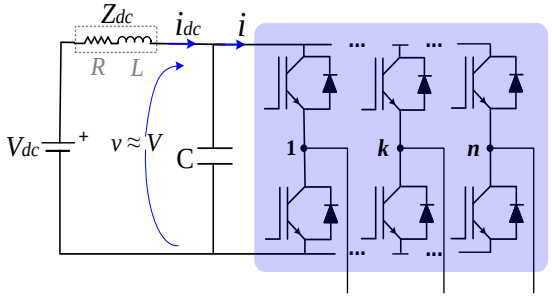

Fig.1. Circuit scheme of n-phase voltage source inverter.

B. A short review of applied modulations

For the dc-link voltage ripple evaluation developed in the next sections, two commonly used modulation techniques, sinusoidal PWM (SPWM) and continuous symmetric centered PWM (CPWM, equivalent to space vector modulation, SVM), are considered. Therefore, a short review of them follows.

The general *n*-phase reference signals are obtained using *n* fundamental sinusoidal signals (1), which are summed with an appropriate common-mode injected signal v_i and expressed as:

$$v_k^* = mV\cos\left(\vartheta-(k-1)\frac{2\pi}{n}\right)+v_i,\quad k=1,2,...n. \tag{3}$$

The injected signal is equal to 0 in case of SPWM. Consequently, the reference signals correspond to sinusoidal voltages given by (1).

In case of CPWM (equivalent to SVM), the centering process is called "min-max" injection, assuming the form:

$$v_i = -\frac{1}{2}\left(v_{\max}+v_{\min}\right), \tag{4}$$

where $v_{\max}=\max\left[v_1^*, v_2^*,..., v_n^*\right]$ and $v_{\min}=\min\left[v_1^*, v_2^*,..., v_n^*\right]$.

Since the timing waveforms have the same pattern in Sector I, as in other sectors as well, the following evaluation can be reduced to the first sector of the SV diagram, or first π/n radians. From the mutual order of the reference signals in the first sector, the application times for five-phase and seven-phase VSIs can be derived for both SPWM and SVM and they are summarized in Table I [26], [27].

The table is identical for SPWM and SVM except for the time sharing of the null configuration between the application times of the two redundant switching states. In case of so called "centered modulation" (CPWM, equivalent to SVM) the total application time of the zero state (t_0+t_n) is equally distributed among two zero space vectors. Therefore, (according to the notation in Table I) $t_0 = t_5$ (five-phase VSIs),

TABLE I
The application times t_k for SPWM determined in the half period T_{sw} /2.

Five-phase VSI (SPWM)	Seven-phase VSI (SPWM)
$t_0=\frac{T_{sw}}{2}(1/2-m\cos(\vartheta))$	$t_0=\frac{T_{sw}}{2}(1/2-m\cos(\vartheta))$
$t_1=mT_{sw}\sin(\pi/5)\sin(\pi/5-\vartheta)$	$t_1=mT_{sw}\sin(\pi/7)\sin(\pi/7-\vartheta)$
$t_2=mT_{sw}\sin(2\pi/5)\sin(\vartheta)$	$t_2=mT_{sw}\sin(5\pi/7)\sin(\vartheta)$
$t_3=mT_{sw}\sin(2\pi/5)\sin(\pi/5-\vartheta)$	$t_3=mT_{sw}\sin(3\pi/7)\sin(\pi/7-\vartheta)$
$t_4=mT_{sw}\sin(\pi/5)\sin(\vartheta)$	$t_4=mT_{sw}\sin(3\pi/7)\sin(\vartheta)$
$t_5=\frac{T_{sw}}{2}(1/2-m\cos(\pi/5-\vartheta))$	$t_5=mT_{sw}\sin(5\pi/7)\sin(\pi/7-\vartheta)$
	$t_6=mT_{sw}\sin(\pi/7)\sin(\vartheta)$
	$t_7=\frac{T_{sw}}{2}(1/2-m\cos(\pi/7-\vartheta))$

TABLE II
Zero vector application times t_k for SVM (CPWM) determined in T_{sw}/2.

Five–phase VSI (SVM)
$t_0=t_5=\frac{T_{sw}}{2}-\left(t_1+t_2+t_3+t_4\right)=$
$=\frac{T_{sw}}{2}\left[1-m\left(1+\cos(\pi/5)\right)\cos\vartheta-m\sin(\pi/5)\sin\vartheta\right]$
Seven–phase VSI (SVM)
$t_0=t_7=\frac{T_{sw}}{2}-\left(t_1+t_2+t_3+t_4+t_5+t_6\right)=$
$=\frac{T_{sw}}{2}\left[\begin{matrix}1-2m\left(\sin(\pi/7)+\sin(3\pi/7)+\sin(5\pi/7)\right)\\ \left(\sin(\pi/7)\cos(\vartheta)+\left(1-\cos(\pi/7)\sin(\vartheta)\right)\right)\end{matrix}\right]$

and $t_0 = t_7$ (seven-phase VSIs). Corresponding application times, t_0 (t_5) and t_0 (t_7), determined in the half period T_{sw} /2, are given in Table II. The limit of the linear modulation range is given according to the generalized expression for *n* phases, (*n* is odd number) $m_{max} = 1 / [2\cos(\pi/2n)]$ [28].

C. Inverter input current analysis

The instantaneous input current $i(t)$ can be generally expressed by three components: dc (average) component $I = I_{dc}$, low-frequency component (hundreds Hz), and high-frequency (switching frequency, 1-20 kHz) component $\Delta i(t)$. Considering balanced load conditions, the low-frequency component is zero and the inverter input current contains only the dc (average) and the high frequency component, written as:

$$i(t) = I_{dc} + \Delta i(t). \tag{5}$$

Under the assumption that inverter power switches are ideal, the input current averaged over the switching period T_{sw} can be obtained on the basis of the input/output power balance. Therefore, the average input current is given by (6):

$$I_{dc} = \frac{m}{2} nI_0\cos\varphi. \tag{6}$$

The input current can be calculated from the switching intervals when the energy is transferred from the input to the output. Therefore, the input current is the sum of *n* inverter leg currents, where each leg current is defined as a product of the binary switching function S_k = [0, 1], k = 1, 2, …, n (where '1'/'0' corresponds to the 'on'/'off' state of the upper switch in particular leg), and corresponding output current. Consequently, the input current can be expressed as:

$$i = \sum_{k=1}^{n} S_k i_k. \tag{7}$$

The switching frequency input current component can be easily calculated utilizing equations (5)–(7) as:

$$\Delta i(t) = i(t) - I_{dc} = \sum_{k=1}^{n} S_k i_k - \frac{m}{2} n I_0\cos\varphi. \tag{8}$$

Due to the symmetry of the inverter input current waveforms, the analysis can be limited to 1/(2*n*) of the fundamental period [*T*/(2*n*)], i.e. the first π/n radians.

III. DC-LINK VOLTAGE RIPPLE EVALUATION

A. Dc-link voltage components

Similar to the inverter input current, the instantaneous dc-link voltage can be expressed by three relevant components: dc (average) component V, low-frequency component, and high-frequency (switching frequency) component Δv. The low-frequency dc-link voltage component is zero in the considered case of balanced load since it results from the corresponding current component. As a consequence, the instantaneous dc-link voltage is expressed as:

$$v(t) = V + \Delta v(t)\,. \tag{9}$$

In case of presence of the series dc supply resistance R_{dc}, the average component V is calculated by subtracting the voltage drop on the dc supply resistance R_{dc} from the dc supply voltage V_{dc}, as (see Fig. 1):

$$V = V_{dc} - R_{dc} I_{dc}\,. \tag{10}$$

The peak-to-peak amplitude of the switching frequency dc-link voltage component, Δv_{pp}, can be defined as the difference between its maximum and minimum value within a switching period:

$$\Delta v_{pp} = \max\left\{\Delta v(t)\right\}_{T_{sw}} - \min\left\{\Delta v(t)\right\}_{T_{sw}}\,. \tag{11}$$

Due to the symmetry among the n-phases in the considered case of sinusoidal balanced output currents, only one phase (the first) is examined in the following analysis.

B. Peak-to-peak voltage ripple evaluation

The peak-to-peak amplitude of the switching frequency dc-link voltage component Δv_{pp} can be evaluated on the basis of the switching frequency current component Δi. An equivalent circuit of the dc-link inverter side at the switching frequency is shown in Fig. 2. In particular, the equivalent dc source impedance Z_{dc} and the reactance $1/(2\pi f_{sw}C)$ of the dc-link capacitor C are connected in parallel. Assuming that the capacitor reactance is much smaller than the equivalent dc source impedance calculated at the switching frequency ($f_{sw}=1/T_{sw}$), the whole switching frequency current ripple component (Δi) can be assumed to circulate only through the dc-link capacitor. In this case, only the capacitance is determining the voltage switching ripple.

In general, any real capacitor can be modelled as a series connection of an ideal capacitor (C), an equivalent series resistor (ESR) and the equivalent series inductor (ESL, or L_s). To understand the effect of ESR and L_s on the dc-link voltage ripple, the total impedance of the capacitor (Z_c) should be

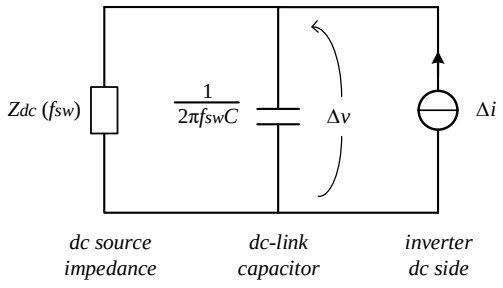

Fig. 2. Dc-link equivalent circuit of the inverter at switching frequency.

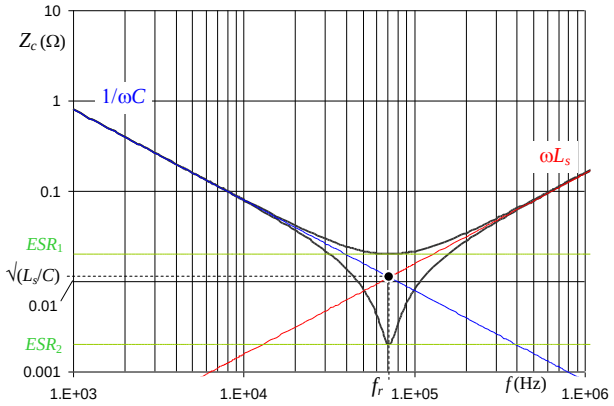

Fig. 3. Impedance vs. frequency characteristic of a real capacitor with the following parameters: C = 200 µF, L_s = 25 nH, ESR_1 = 20 mΩ, ESR_2 = 2 mΩ.

taken into account. Fig. 3 shows the impedance (Z_c) characteristic of the adopted film capacitor for two values of ESR. The impedance Z_c is calculated as:

$$Z_c = \sqrt{ESR^2 + \left(2\pi f\, L_s - \frac{1}{2\pi f\, C}\right)^2}\,. \tag{12}$$

The strong dependency of the dc-link capacitor impedance on the frequency is obvious. A reasonable criterion to establish if L_s should be considered for voltage ripple calculation could be the comparison of switching frequency (f_{sw}) with self-resonance frequency (f_r). Similarly, to establish if ESR has to be considered, a comparison between the ESR and the value of $\sqrt{L_s/C}$, i.e. the intersection depicted in Fig. 3, should be also made. It can be noticed in Fig. 3 that for the switching frequencies well below the self-resonant frequency of the dc-link capacitor, its inductive reactance is negligible comparing to the capacitive reactance, and the same applies to ESR if it has similar or lower value comparing to $\sqrt{L_s/C}$.

In case of inverter-fed drives, the maximum switching frequency is usually 15-20 kHz. If a dc-link film capacitor in the order of few hundred µF is considered, with L_s in order of few tens nH, the resulting self-resonance frequency is always higher than switching frequency. Hence, for the considered cases, the effect of capacitor's parasitic components on the dc-link voltage ripple is negligible at the switching frequency.

On the basis of the previous considerations, only the dc-link capacitance can be considered to determine the dc-link voltage ripple. In particular, the voltage excursion can be calculated within each application time interval t_k (determined in Table I and Table II) based on the equation for the voltage drop over capacitor and by considering the switching current component Δi constant within the considered interval:

$$\Delta v_{pp}^{k} = \frac{1}{C}\Delta i\; t_k\,. \tag{13}$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by combining different Δv_{pp}^{k} and finding the maximum within the switching period, as shown in the following.

Due to the periodicity of the input current $i(t)$ waveform, the evaluation of the voltage ripple can be reduced to the phase angle range $0 \le \vartheta \le \pi/n$ (or the first sector of SV diagram). Within the first sector, depending on the value of I_{dc}, n–1 different case can be distinguished. In Fig. 4, the peak-to-peak dc-link voltage variation Δv_{pp} and an example of possible instantaneous input current $i(t)$ waveform (blue staircase waveform with flat (horizontal) staircase treads) are depicted in one switching period. In general, the instantaneous input current $i(t)$ is calculated by (7). Note that the output current ripple is neglected in the following analysis. As a consequence, the staircase treads shown in Fig. 4 can be considered flat. It will be shown later that the omission of the output current ripple for the dc-link current and voltage ripple analysis was reasonable.

In order to analytically determine the dc-link peak-to-peak voltage ripple amplitude, two different multiphase schemes are further addressed. In particular, five-phase and seven-phase VSI topologies are analyzed next, being the three-phase case already examined in [20].

1) Five-phase case

Regarding the five-phase inverter, the evaluation of the voltage ripple can be reduced to the phase angle range $0 \le \vartheta \le \pi/5$. The following analysis refers to Fig. 4 (left). Depending on the value of I_{dc}, and if SVM is applied (same as CPWM, $t_0 = t_5$), four different cases can be distinguished and corresponding peak-to-peak dc-link voltage variations can be expressed as:

case A: when $i_1 \ge I_{dc}$,

$$\Delta v_{pp}^{A} = \frac{1}{C} I_{dc} 2t_0.$$

case B: when $i_1 \le I_{dc} < i_1+i_2$,

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + \frac{1}{C}(I_{dc} - i_1) 2t_1.$$

case C: when $i_1+i_2 \le I_{dc} < -(i_3+i_4)$,

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + \frac{1}{C}(I_{dc} - i_1 - i_2) 2t_2.$$

case D: when $-(i_3+i_4) \le I_{dc} < -i_4$,

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + \frac{1}{C}(I_{dc} + i_3 + i_4) 2t_3.$$

The global peak-to-peak dc-link voltage ripple amplitude Δv_{pp} is obtained by finding the maximum value of possible cases, i.e., $\max\{\Delta v_{pp}{}^{A} \ldots \Delta v_{pp}{}^{D}\}$, according to Fig. 4 (left).

When sinusoidal PWM is applied there is an additional case*:*

case E: when $i_1 \ge I_{dc}$, since $t_0 \ne t_5$,

$$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + \frac{1}{C} I_{dc}\, 2t_5.$$

The final equations obtained after analytical derivations, for each sub-sector within the first sector, are presented in Table III. Note that for calculation of the final results given in Table III, the values from Tables I and II, as well as (2), (6), and (7), should be used. In order to emphasize the influence of the modulation strategy, the dc-link peak-to-peak voltage ripple amplitude can be normalized introducing r_{pp}, according to:

$$\Delta v_{pp} = \frac{I_o}{f_{sw} C} r_{pp}(m, \vartheta, \varphi). \tag{14}$$

Normalized peak-to-peak voltage ripple amplitudes r_{pp}^{SVM} and r_{pp}^{SPWM} , can be defined by (14) with reference to Δv_{pp}^{SVM} and Δv_{pp}^{SPWM} , for SVM (CPWM) and SPWM, respectively.

2) Seven-phase case

Regarding the seven-phase inverter, the evaluation of the voltage ripple can be reduced to the phase angle range $0 \le \vartheta \le \pi/7$. In Fig. 4 (right) the peak-to-peak dc-link voltage variation Δv_{pp} and the instantaneous input current $i(t)$ (blue staircase line) are depicted in one switching period. Depending on the value of I_{dc}, if SVM is applied (same as CPWM, $t_0 = t_7$), six different cases can be distinguished and corresponding peak-to-peak dc-link voltage variations can be calculated as:

TABLE III
Peak-to-peak dc-link voltage ripple amplitude in each sub-interval within the first sector, considering five-phase VSI and both modulation techniques (SVM and SPWM).

Space vector modulation (SVM, CPWM)	Sinusoidal PWM (SPWM)
$\Delta v_{pp}^{A} = \frac{5}{4}\frac{I_o}{f_{sw}C} m\cos\varphi\left(1 - m\begin{pmatrix}1+\cos(\pi/5)\cos(\vartheta)\\ -m\sin(\pi/5)\sin(\vartheta)\end{pmatrix}\right)$	$\Delta v_{pp}^{A} = \frac{5}{2}\frac{I_o}{f_{sw}C} m\cos\varphi(1/2 - m\cos(\vartheta))$
$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + 2\frac{I_o}{f_{sw}C} m\sin(\pi/5)\sin(\pi/5-\vartheta)\left(\frac{5}{2}m\cos\varphi - \cos(\vartheta-\varphi)\right)$	
$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + 2\frac{I_o}{f_{sw}C} m\sin(3\pi/5)\sin(\vartheta)\left(\frac{5}{2}m\cos\varphi - \cos(\vartheta-\varphi) - \cos(\vartheta-2\pi/5-\varphi)\right)$	
$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + 2\frac{I_o}{f_{sw}C} m\sin(3\pi/5)\sin(\pi/5-\vartheta)\left(\frac{5}{2}m\cos\varphi + \cos(\vartheta-4\pi/5-\varphi) - \cos(\vartheta-6\pi/5-\varphi)\right)$	
	$\Delta v_{pp}^{E} = \frac{5}{2}\frac{I_o}{f_{sw}C} m\cos\varphi(1/2 - m\cos(\pi/5-\vartheta))$

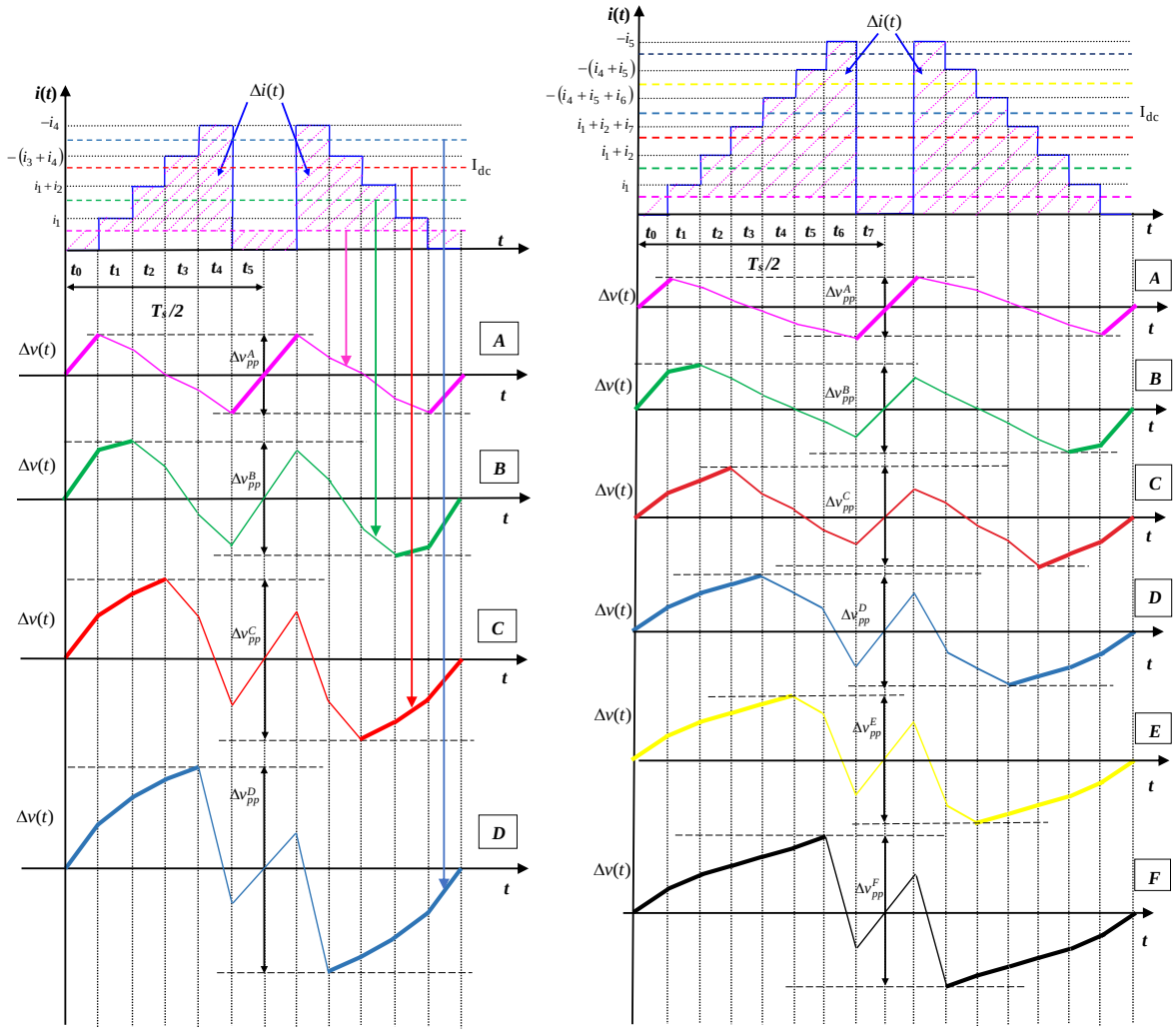

Fig. 4. Dc-link current and voltage ripple in one switching period T_{sw}, for five-phase (left) and seven-phase (right) VSIs.

case A: when $i_1 \geq I_{dc}$,

$$\Delta v_{pp}^{A} = \frac{1}{C} I_{dc} 2t_0.$$

case B: when $i_1 \leq I_{dc} < i_1+i_2$,

$$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + \frac{1}{C}(I_{dc} - i_1) 2t_1.$$

case C: when $i_1+i_2 \leq I_{dc} < i_1+i_2+i_7$,

$$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + \frac{1}{C}(I_{dc} - i_1 - i_2) 2t_2.$$

case D: when $i_1+i_2+i_7 \leq I_{dc} < -(i_4+i_5+i_6)$,

$$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + \frac{1}{C}(I_{dc} - i_1 - i_2 - i_7) 2t_3.$$

case E: when $-(i_4+i_5+i_6) \leq I_{dc} < -(i_4+i_5)$,

$$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + \frac{1}{C}(I_{dc} + i_4 + i_5 + i_6) 2t_4.$$

case F: when $-(i_4+i_5) \leq I_{dc} < -i_5$,

$$\Delta v_{pp}^{F} = \Delta v_{pp}^{E} + \frac{1}{C}(I_{dc} + i_4 + i_5) 2t_5.$$

When sinusoidal PWM is applied there is an additional case:

case G: when $i_1 \geq I_{dc}$, since $t_0 \neq t_7$,

$$\Delta v_{pp}^{G} = \frac{1}{C} I_{dc} 2t_7.$$

According to Fig. 4 (right), the global peak-to-peak dc-link voltage ripple amplitude for SVM and SPWM method (Δv_{pp}^{SVM} and Δv_{pp}^{SPWM}) is again obtained by finding the maximum value of possible cases, i.e., $\max\{\Delta v_{pp}{}^{A} \ldots \Delta v_{pp}{}^{G}\}$. By using (14), the normalized peak-to-peak voltage ripple amplitudes r_{pp}^{SVM} and r_{pp}^{SPWM} are defined as well. The equations obtained after analytical derivations, for each sub-sector within the first sector, are presented in Table IV. Application times t_k for seven-phase system, given in Table I and Table II, as well as (2), (6) and (7) are used for obtaining these analytical values.

IV. DC-LINK VOLTAGE RIPPLE COMPARISON IN MULTIPHASE INVERTERS

A. Peak-to-peak voltage ripple amplitude

For the dc-link capacitor's design and selection purposes, it is of importance to understand behaviour of the peak-to-peak voltage ripple amplitude and to identify its maximum value. In order to predict the ripple behaviour, Fig. 5 shows normalized function of the dc-link voltage ripple amplitude for three-, five- and seven- phase VSIs. For five- and seven- phase cases the evaluation is done on the basis of the analysis presented in the previous sections, whereas for the three-phase case the evaluation is done according to [20], and it is used here for the sake of comparison of different phase numbers.

For all considered topologies, the ripple normalization is given according to (14). Three values of modulation index (m = 1/4, 1/3, and 1/2) and two power phase angles are considered. In particular, φ = 20° and φ = 70° have been chosen to approximately represent the usual phase angle range for an induction motor, corresponding to rated and no-load conditions, respectively. An additional intermediate angle (φ = 45°) will be also consider for further analysis.

The results are shown in Fig. 5 with reference to both SPWM and SVM (solid and dashed lines, respectively). The impact of applied modulation techniques is evident in case of three-phase inverter. Significant reduction in the voltage ripple amplitude can be noted due to the centering performed in the SVM (CPWM), especially for lower power phase angles. It leads to the conclusion that SVM (or CPWM) is preferable modulation for three-phase inverters from the point of view of the dc-link voltage ripple requirements and the dc-link capacitor sizing. However, no significant influence of CPWM on the voltage ripple amplitude is shown in case of five- and seven-phase inverters.

A wide excursion of the normalized voltage ripple is noticeable, generally ranging between 0 and 0.22. Yet, it is evident that by increasing the number of phases the voltage ripple amplitude profile becomes more flat and uniform. Unlike the three-phase case, in five- and seven- phase case increasing the power phase angle the voltage ripple amplitude is significantly reduced. In presented cases, the amplitude is half reduced, and the reduction is better noticeable for higher number of phases.

B. Maximum of the peak-to-peak voltage ripple amplitude

For a fair comparison of inverter topologies with different phase numbers, the same output power should be considered. For this reason, the total output current nI_o is introduced (that is proportional to the apparent power), and a "per-phase" normalization of the dc-link peak-to-peak voltage ripple is defined as

$$\Delta v_{pp} = \frac{nI_o}{f_{sw}C} r_{ppn}, \tag{15}$$

being $r_{ppn} = \frac{r_{pp}}{n}$ and n the number of phases. Maximum of the per phase normalized peak-to-peak voltage ripple amplitude r_{ppn}, as a function of modulation index is obtained numerically and shown in Fig. 6, considering the same phase angles as in Fig. 5 with the additional intermediate point φ = 45° to better cover the considered range. Numerical analysis is extended to higher number of phases in order to provide comparative evaluation of the peak-to-peak voltage ripple amplitude behavior in two-level multiphase inverters and support general conclusions on the dc-link capacitor sizing.

TABLE IV
Peak-to-peak dc-link voltage ripple amplitude in each sub-interval within the first sector, considering seven -phase VSI and both modulation techniques (SVM and SPWM).

Space vector modulation (SVM, CPWM)	Sinusoidal PWM (SPWM)
$\Delta v_{pp}^{A} = \frac{7}{4}\frac{I_o}{f_{sw}C} m\cos\varphi \left[\begin{array}{l} 1-2m\left(\sin(\pi/7)+\sin(3\pi/7)+\sin(5\pi/7)\right) \\ \left(\sin(\pi/7)\cos(\vartheta)+\left(1-\cos(\pi/7)\right)\sin(\vartheta)\right) \end{array}\right]$	$\Delta v_{pp}^{A} = \frac{7}{2}\frac{I_o}{f_{sw}C} m\cos\varphi\left(1/2 - m\cos(\vartheta)\right)$
$\Delta v_{pp}^{B} = \Delta v_{pp}^{A} + 2\frac{I_o}{f_{sw}C} m\sin(\pi/7)\sin(\pi/7-\vartheta)\left[\frac{7}{2}m\cos\varphi - \cos(\vartheta-\varphi)\right]$	
$\Delta v_{pp}^{C} = \Delta v_{pp}^{B} + 2\frac{I_o}{f_{sw}C} m\sin(5\pi/7)\sin(\vartheta)\left[\frac{7}{2}m\cos\varphi - \cos(\vartheta-\varphi) - \cos(\vartheta-2\pi/7-\varphi)\right]$	
$\Delta v_{pp}^{D} = \Delta v_{pp}^{C} + 2\frac{I_o}{f_{sw}C} m\sin(3\pi/7)\sin(\pi/7-\vartheta)\left[\frac{7}{2}m\cos\varphi - \cos(\vartheta-\varphi) - \cos(\vartheta-2\pi/7-\varphi) - \cos(\vartheta-12\pi/7-\varphi)\right]$	
$\Delta v_{pp}^{E} = \Delta v_{pp}^{D} + 2\frac{I_o}{f_{sw}C} m\sin(3\pi/7)\left[\frac{7}{2}m\cos\varphi + \cos(\vartheta-6\pi/7-\varphi) - \cos(\vartheta-8\pi/7-\varphi) + \cos(\vartheta-10\pi/7-\varphi)\right]$	
$\Delta v_{pp}^{F} = \Delta v_{pp}^{E} + 2\frac{I_o}{f_{sw}C} m\sin(5\pi/7)\sin(\pi/7-\vartheta)\left[\frac{7}{2}m\cos\varphi + \cos(\vartheta-6\pi/7-\varphi) + \cos(\vartheta-8\pi/7-\varphi)\right]$	
	$\Delta v_{pp}^{G} = \frac{7}{2}\frac{I_o}{f_{sw}C} m\cos\varphi\left(1/2 + m\cos(\vartheta-8\pi/7)\right)$

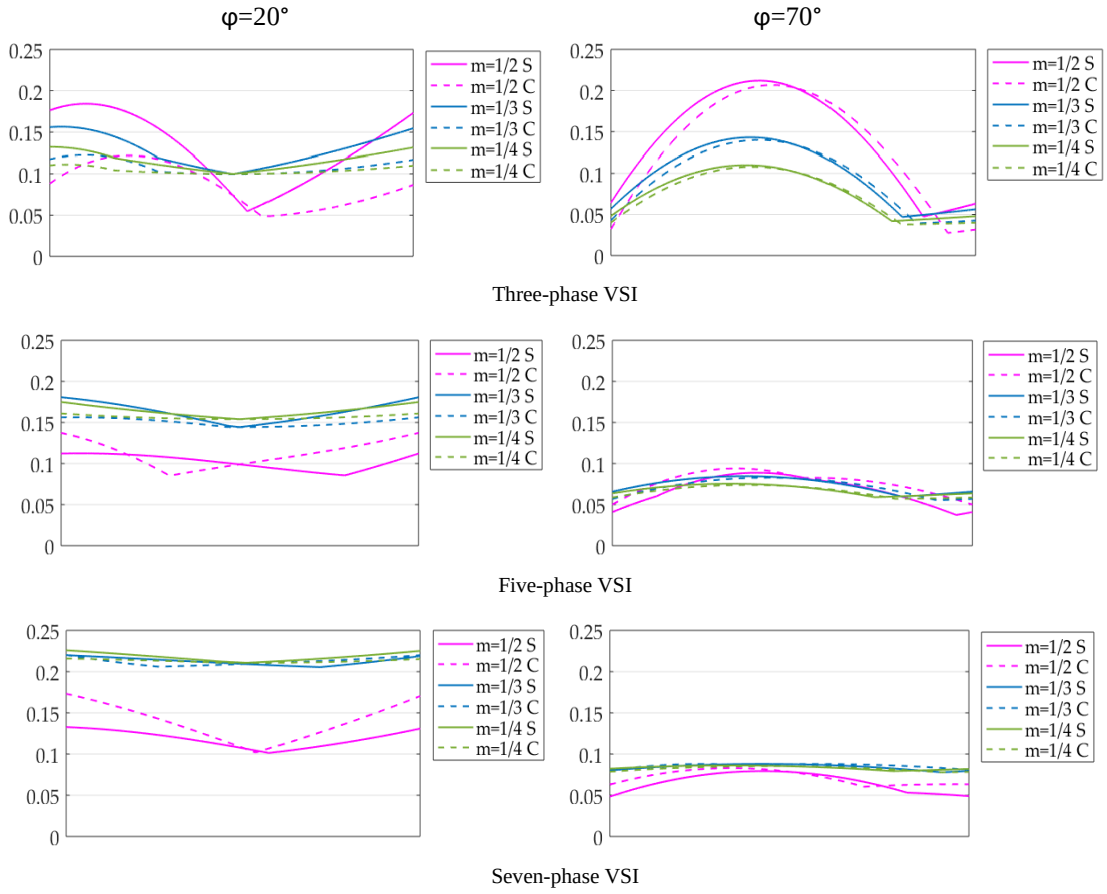

Fig. 5. Normalized peak-to-peak dc-link voltage ripple amplitude $r_{pp}(\vartheta)$ over its period for three-, five-, and seven-phase VSIs, considering three modulation indices, m = 1/4, 1/3, and 1/2, two output phase angles φ = 20° (left column) and φ = 70° (right column), with SPWM and SVM (continuous and dashed lines, respectively).

The following observations are worth noting on the maximum peak-to-peak voltage ripple amplitude (r_{ppn}) displayed in Fig. 6. First, the maximum of dc-link voltage ripple amplitude is decreasing when the number of phases increases. The reduction is significant when the number of phases increases from three to five, and less significant when it increases to seven. Finally, no practical difference in the maximum voltage ripple is obtained for the number of phases higher than seven.

Referring to the three-phase case, the maximum of the normalized peak-to-peak voltage ripple amplitude is almost linear function of modulation index. A slight increase of the maximum value can be noticed when increasing the output phase angle. However, for five- and seven-phase case the global maximum of the voltage ripple amplitude slightly reduces when the phase angle increases. No further reduction of maximum voltage ripple is observed for higher number of phases (n > 7).

These diagrams are particularly useful for the dc-link capacitor design, proposed in the following sub-section.

According to Fig. 6, global maximum $r_{ppn}^{\max}$ for different

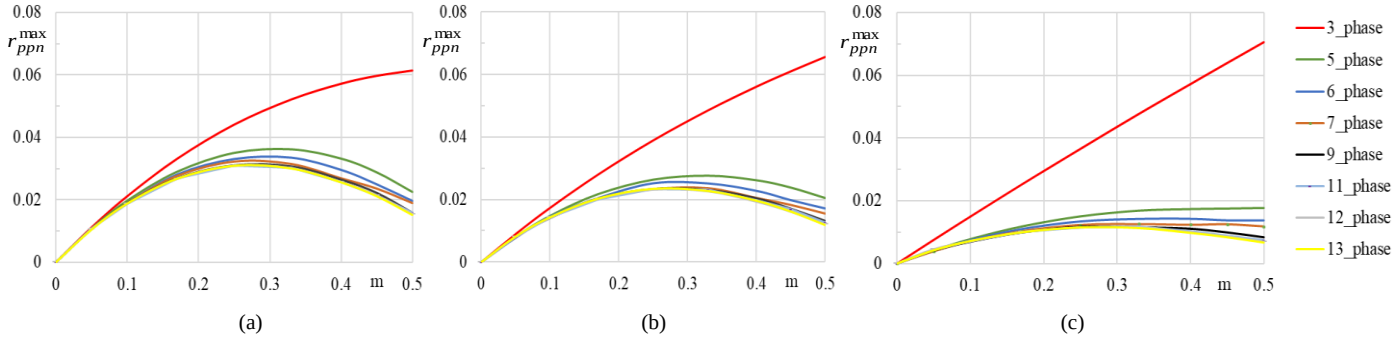

Fig. 6. Maximum of peak-to-peak voltage ripple amplitude in multiphase VSIs, normalized per total output current, $r_{ppn}^{\max}$, as a function of modulation index for output phase angles: (a) φ = 20°, (b) φ = 45°, and (c) φ = 70°.

phase numbers is presented in Table V. It is evident that considering the same total output current (apparent power) the maximum value of the dc voltage ripple amplitude reduces with the increase of the phase number up to seven, but not for higher number of phases.

C. Dc-link capacitor design

In this sub-section, the capacitor size is designed based on the voltage switching ripple requirements Δv_{pp}^{*} by assuming that at given switching frequency (at least in order of kHz), the dc source impedance (Z_{dc}) is much higher than the capacitor reactance ($1/(2\pi f_{sw}C)$). As discussed, under this assumption, dc voltage ripple is determined only by the size of the dc-link capacitor (Fig. 2). By observing Fig. 6, and considering $r_{ppn}^{\max}$ given by Table V, a simple formula for the dc-link capacitor design is obtained on the basis of (15), by specifying the desired Δv_{pp}^{*} as:

$$C \geq \frac{nI_o}{f_{sw}} r_{ppn}^{\max}(\varphi) \frac{1}{\Delta v_{pp}^{*}}. \tag{16}$$

Of course, the worst-case scenario should be considered for final design of capacitor. As an example, five-phase VSIs is analyzed in the following.

According to Table V, the angle $\varphi = 20°$ (motor around the rated power conditions) should be considered because the maximum of the peak-to-peak voltage ripple amplitude (normalized per total output current) $r_{ppn}^{\max}$ reaches then the highest value of 0.0361. If given the values of the output current of an inverter, its switching frequency and the required peak-to-peak voltage switching ripple, the dc-link capacitor can be chosen based on (16) as

$$C \geq 0,0361 \frac{5I_o}{f_{sw}\,\Delta v_{pp}^{*}}. \tag{17}$$

The given example shows that (16) can be used straightforward in case of any multiphase VSI topology where $n \geq 3$.

TABLE V

Global maximum of $r_{ppn}^{\max}$ as a function of number of phases for different phase angles.

Angle	Phase number (n)							
φ	**3**	**5**	**6**	**7**	**9**	**11**	**12**	**13**
20°	0.061	0.036	0.034	0.032	0.031	0.031	0.031	0.031
45°	0.066	0.028	0.025	0.024	0.023	0.023	0.023	0.023
70°	0.071	0.018	0.014	0.013	0.012	0.012	0.012	0.012

V. RESULTS

Theoretical developments shown in previous sections are verified by numerical simulations and experimental tests. Circuit simulations are performed by Matlab/Simulink considering five- and seven-phase inverters with balanced loads. Multiphase passive loads have been preferred to motor load for a better stability of the measured voltage switching ripple profile. However, regardless of whether the load is a passive- or a motor- load, if the output currents are almost sinusoidal and balanced (and the output current ripple is not severe) the proposed analysis of the dc-link input current and voltage is the same. The simulation parameters, summarized in Table VI, are set to match the corresponding experimental setup parameters. The two output phase angles of interest are obtained by using two different sets of passive balanced *R-L* load impedances, having the parameters shown in Table VII.

The hardware set-up consists of custom-made voltage source inverter (VSI), with up to eight-phases. It is based on Infineon FS50R12KE3 (50A, 1200V) IGBT modules. For control implementation dSpace ds1006 real-time platform, directly programmable from Matlab/Simulink, is used. PWM signals are generated using ds5101 board, as a part of the dSpace system. Sampling frequency in all cases is 2 kHz. The inverter dead-time value is 6μs. Dc supply voltage is provided from the external dc source Sorensen SGI 600/25. The Z_{dc} impedance is added between the dc source and the dc-link. Equivalent value of two dc-link film capacitors connected in parallel is 200μF. The experimental setup is shown in Fig. 7.

Tektronix oscilloscope MSO2014 with P5205A differential voltage probe was used for measurement. In order to clean the waveforms and eliminate the switching spikes, the low-pass filter with a cut-off frequency of 1MHz has been applied in post-processing of the experimental data. In addition, to re-

TABLE VI

The experimental setup parameters.

Parameter	**Symbol**	**Value**
Dc voltage supply	V_{dc}	300 V
Dc source resistance	R_{dc}	5.3 Ω
Dc source inductance	L_{dc}	4.5 mH
Dc-link capacitance (2x parallel film caps.)	C	200 μF
Equivalent series resistance	ESR	10 mΩ
Equivalent series inductance	L_s	25 nH
Fundamental frequency	f	50 Hz
Switching frequency	f_{sw}	2 kHz

TABLE VII

Passive R-L load parameters.

5x, 7x	**φ = 20°**	**φ = 70°**
R_L (Ω)	24	24
L_L (mH)	25	204

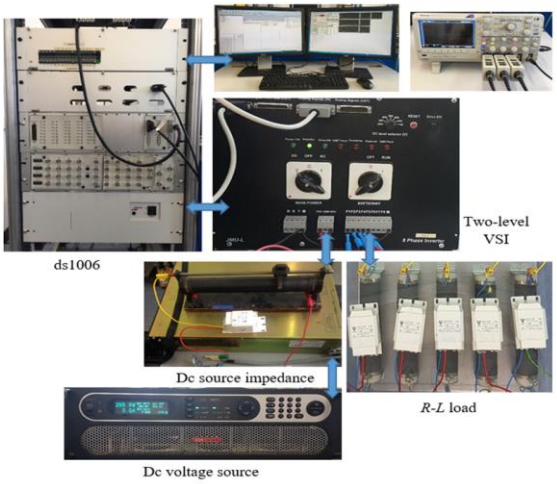

Fig. 7. Experimental setup.

move small low frequency components, FFT was applied. Figs. 8 and 9 show simulations (blue traces) and experimental results (gray traces) together with the analytically calculated voltage ripple envelopes for five-phase inverter when SPWM and SVM are applied, respectively. Two values of modulation index: m = 1/4 and 1/2 are considered for two output phase angles φ = 20° (left column) and φ = 70° (right column). The peak-to-peak envelopes are calculated as shown in Section III, as the half of the peak-to-peak voltage ripple amplitude, $\Delta v_{pp}(t)/2$.

Figs. 10 and 11 show the simulations (blue traces) and the experimental results (gray traces) together with the calculated voltage ripple envelopes for seven-phase inverter when SPWM and SVM are applied, respectively. Again, two values of modulation index: m=1/4 and 1/2 are considered for two output phase angles φ = 20° (left column) and φ = 70° (right column). The instantaneous dc-link voltage switching ripple $\Delta v(t)$ is shown together with the peak-to-peak envelope that is calculated as one half of the peak-to-peak voltage ripple amplitude $\Delta v_{pp}(t)/2$.

In all cases, numerical simulations show perfect matching between dc voltage ripple and theoretically calculated envelope. Experimental results are also in a good agreement with both theoretical and simulation results. Note that an ideal dc-link capacitor has been primarily considered in the simulations. In order to show the effect of the capacitor's parasitic components on the dc-link voltage ripple, the simulations have been also performed considering a real-world capacitor model (a series-connected *RLC* circuit). An equivalent dc circuit of analyzed inverter when a real dc-link capacitor's model is considered is shown in Fig. 12.

Since the two film capacitors connected in parallel have been used in the experiments, having the total capacitance and parasitic components' given in Table VI, the simulation parameters are set to match the corresponding experimental values. The impedance characteristics of the adopted equivalent capacitor has been previously shown in Fig. 3. Simulated dc-voltage ripple is filtered in the same way as the experimental data. Simulation results are shown in Fig. 13 for the five-phase case when m = 1/4 and φ = 70°. It corresponds to the experimental result shown in Fig. 8 (b). Therefore, as com-

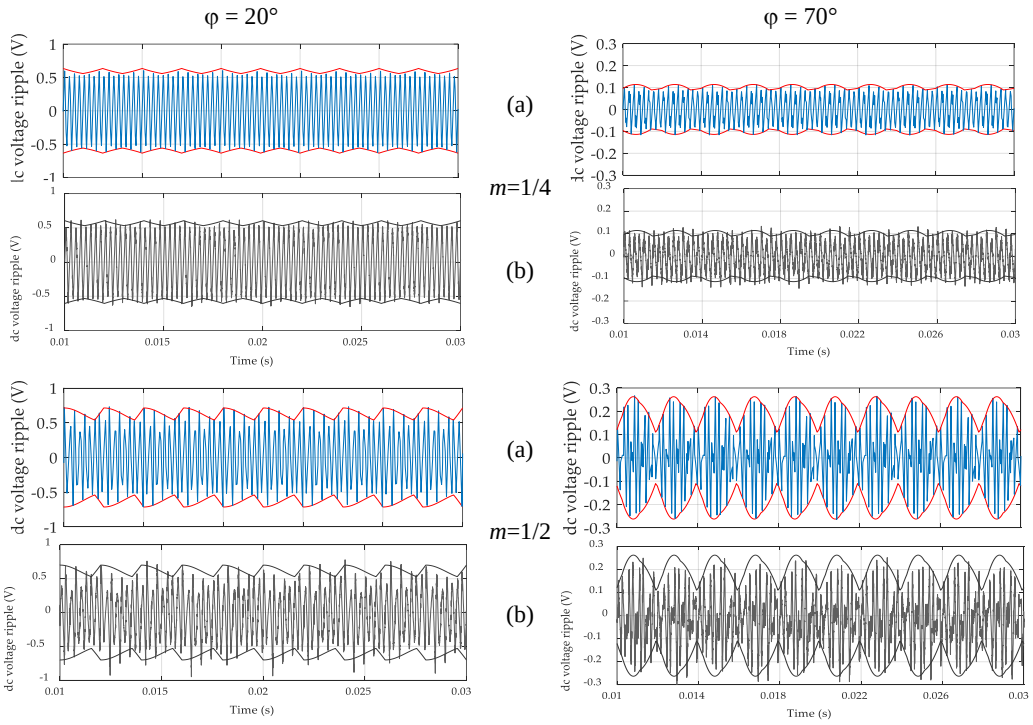

Fig. 8. Dc-link voltage switching ripple in five-phase inverter (SPWM): (a) simulation and (b) experimental results. Calculated peak-to-peak envelope (red trace) for φ = 20° (left) and φ = 70° (right) for m = 1/4 and 1/2.

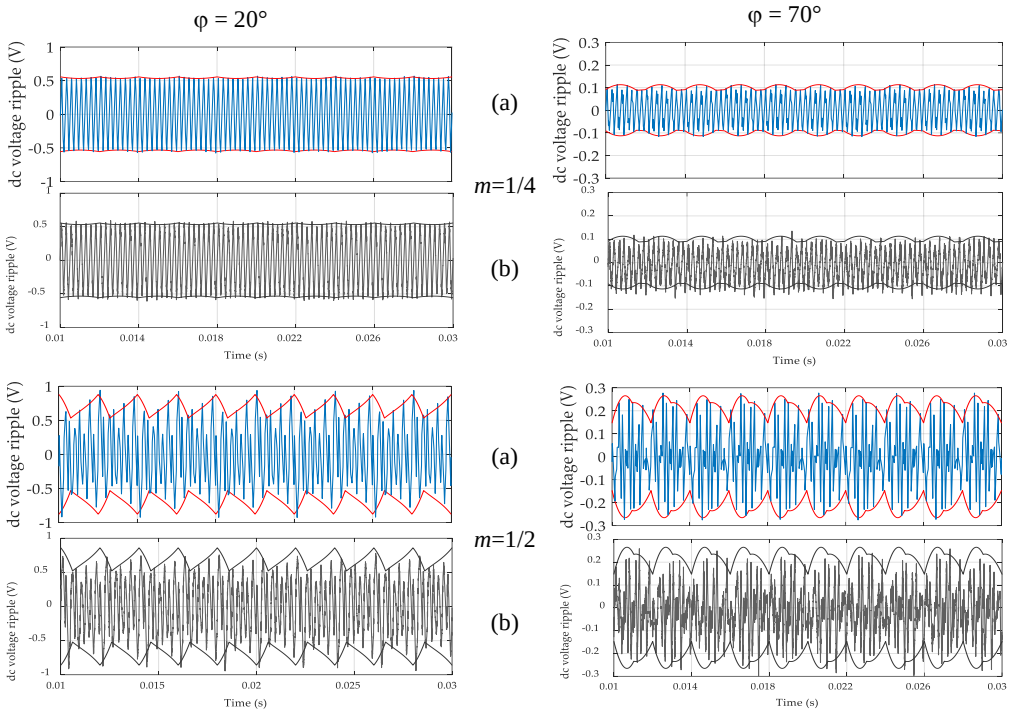

Fig. 9. Dc-link voltage switching ripple in five-phase inverter (SVM): (a) simulation and (b) experimental results.
Calculated peak-to-peak envelope (red trace) for φ = 20° (left) and φ = 70° (right) for m = 1/4 and 1/2.

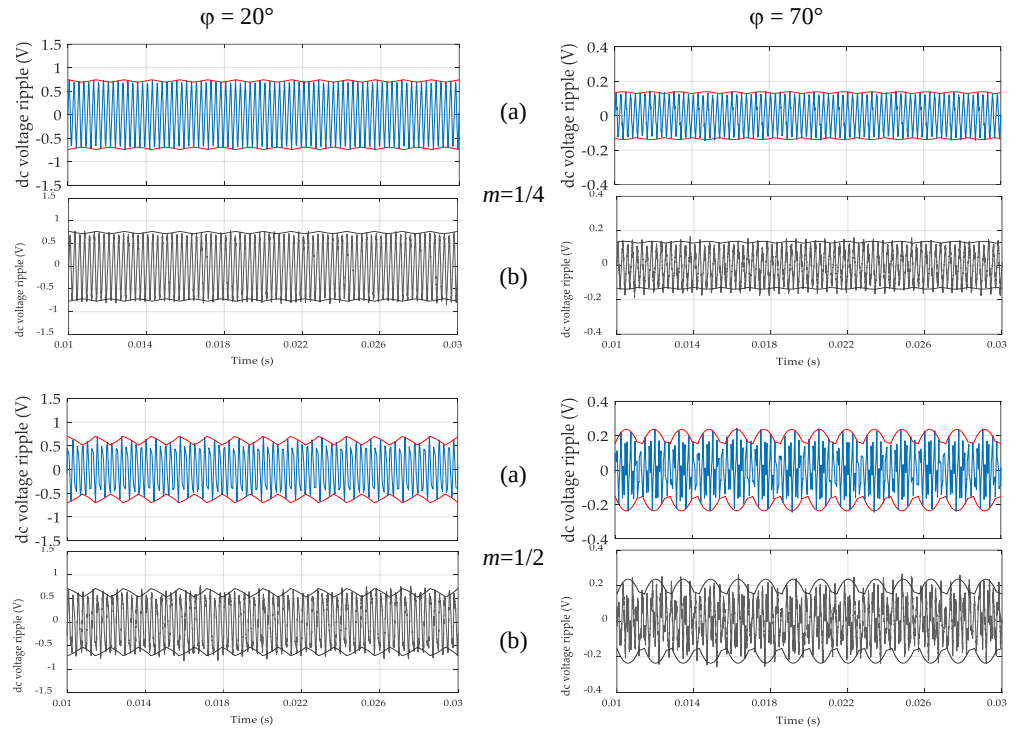

Fig. 10. Dc-link voltage switching ripple in seven-phase inverter (SPWM): (a) simulation and (b) experimental results.
Calculated peak-to-peak envelope (red trace) for φ = 20° (left) and φ = 70° (right) for m = 1/4 and 1/2.

mented before, for the considered case, the effects of the *ESR* and L_s on the dc-link voltage ripple are negligible.

The effect of the capacitor's parasitic components can be severe in case of the switching frequency close to the self-reso-

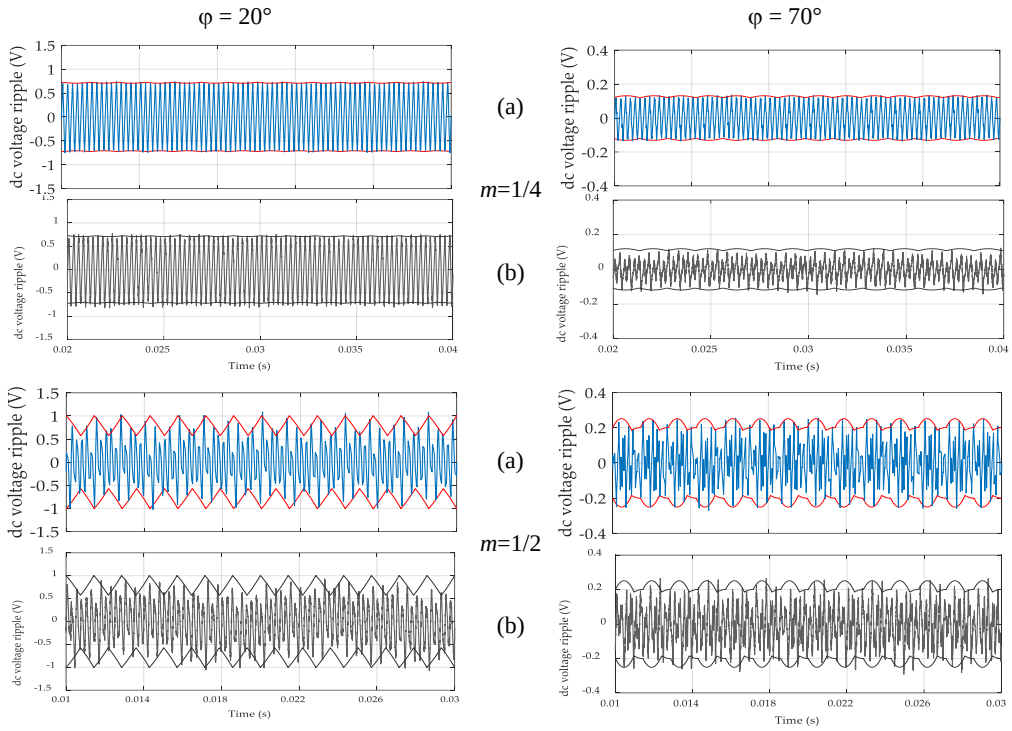

Fig. 11. Dc-link voltage switching ripple in seven-phase inverter (SVM): (a) simulation and (b) experimental results. Calculated peak-to-peak envelope (red trace) for φ = 20° (left) and φ = 70° (right) for *m* = 1/4 and 1/2.

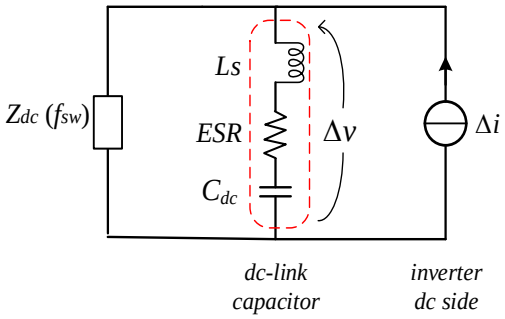

Fig. 12. Dc-link equivalent circuit of the inverter when a real dc-link capacitor model is considered.

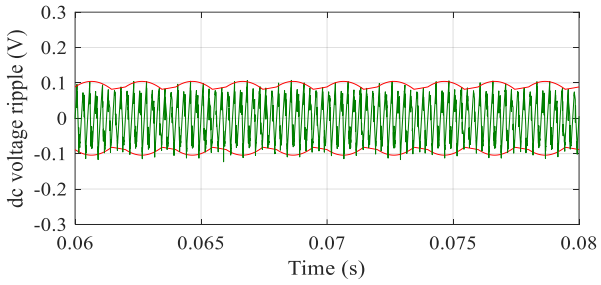

Fig. 13. Dc-link voltage ripple and its envelope in five-phase VSI (*m*=1/4, φ=70°) considering a real dc-link capacitor model with the following parameters: *C*=200 μF, *ESR*=10 mΩ, L_s=25 nH, simulation results.

nant frequency of the dc-link capacitor, as shown in Fig. 3, but the detail analysis of this is beyond the scope of this paper. Moreover, note that the results prove that when going for higher numbers of phases, smaller capacitance can be used, which practically means that instead of large electrolytic capacitors, smaller higher quality capacitors (such as film capacitors) with lower *ESR* can be used.

VI. Conclusion

This paper presents the analysis of dc-link voltage switching ripple in two-level multiphase PWM voltage source inverters with balanced load, focusing on odd phase numbers, equal or greater than three. The peak-to-peak voltage ripple amplitude is determined as a function of modulation index, amplitude of the output current and output phase angle, for five- and seven-phase VSIs. Two popular modulation techniques (SPWM and SVM, i.e. CPWM) are considered and their effect on the voltage ripple amplitude has been discussed. Namely, it is shown that the use of the SVM results in lower voltage ripple amplitude only in case of three-phase inverter, especially for lower output phase angle. However, the centering performed in SVM (CPWM) has no significant influence on the voltage ripple in case of five-, seven- and higher phase numbers.

In order to show characteristics and distribution of the voltage ripple amplitude, the normalized function is introduced, and various diagrams are presented. Comparison is made considering different multiphase VSIs, output phase angles within the typical range for induction motors (from rated-load up to no-load), and full range of modulation index. The maximum value of the peak-to-peak dc-link voltage ripple envelope is derived as a function of modulation index. Finally, the required dc-link capacitor is designed according to the

voltage switching ripple requirements, providing for simple formula on the basis of phase number and output phase current. It is found that considering the same total output current (apparent power), the dc-link capacitor size can be reduced when increasing the number of phases from three up to seven. However, no further size reduction is obtained when increasing the number of phases more than seven. These findings are particularly important for the design of the multiphase power inverters especially when supplied by batteries (e.g. in electric vehicles) where the impedance of the dc source can be extremely variable, and where very careful choice of the dc-link capacitors (size and type, including parasitic properties) have to be made.

Theoretical developments are verified by numerical simulations and experimental tests for two-level five-phase and two-level seven-phase VSIs supplying a balanced load. In all considered cases, a very good agreement is achieved.

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