Multi-Channel Signal Generator ASIC for Acoustic Holograms

Rui Song, Grace Richard, Christopher You-Yee Cheng, Lijun Teng, Yongqiang Qiu, Martin PJ Lavery, Susan Trolier-McKinstry, Sandy Cochran, Ian Underwood

***Abstract*—A CMOS application-specific integrated circuit (ASIC) has been developed to generate arbitrary, dynamic phase patterns for acoustic hologram applications. An experimental prototype has been fabricated to demonstrate phase shaping. It comprises a cascadable 1 × 9 array of identical, independently-controlled signal generators implemented in a 0.35 μm minimum feature size process. It can individually control the phase of a square wave on each of the nine output pads. The footprint of the integrated circuit is 1175 × 88 μm^2. A 128 MHz clock frequency is used to produce outputs at 8 MHz with phase resolution of 16 levels (4-bit) per channel. A 6 × 6 air-coupled matrix array ultrasonic transducer was built and driven by four ASICs, with the help of commercial buffer amplifiers, for the application demonstration. Acoustic pressure mapping and particle manipulation were performed. Additionally, a 2 × 2 array piezoelectric micromachined ultrasonic transducer (PMUT) was connected and driven by four output channels of a single ASIC, demonstrating the flexibility of the ASIC to work with different transducers and the potential for direct integration of CMOS and PMUTs.**

***Index Terms*—Digital integrated circuits, Phased arrays, Scalability, Ultrasonic transducer arrays, Phase control**

I. Introduction

Contactless particle manipulation devices, e.g. optical and acoustic tweezers, are important tools in the biomedical field [1, 2]. While optical tweezers are best suited for manipulating micron-scale particles, acoustic tweezers can manipulate submillimeter-scale particles and agglomerates of micron-scale bioparticles, without impairing their viability [3-5].

Holographic acoustic tweezers are of interest for their capability to perform 3-D manipulation [6, 7]. Marzo et al. demonstrated acoustic holography with a single-sided 8 × 8 element ultrasonic 2-D phased array where each transducer element was directly wired to an external driver and was individually addressable [6]. Melde et al. demonstrated that the information content of the acoustic field depends directly on the number of independently addressed ultrasound elements, named as pixels in the remainder of this paper, with a 2-D phased array; they successfully constructed 15,000 pixels in a 3-D printed hologram [7]. Although this allows higher manipulation precision and resolution, as the printed hologram is fixed, real-time reconfiguration of the acoustic field is not possible.

Subsequently, efforts have been made to increase the number of directly-connected ultrasound transducers in the array to 2,500 [8] to achieve high-precision dynamic manipulation. However, this requires increased electronic complexity and the cost of further scaling is unfavorable. This is because, for a directly-connected (direct-wiring) device with N × M transducer elements, N × M independently configurable drivers and N × M interconnections are required. For example, to achieve the same 500 × 500 addressable pixels found in a spatial light modulator for optical tweezers [9] by acoustic means, 250,000 drivers like FPGA (field programmable gate array) gates would be required.

In order to construct a high pixel-count acoustic tweezer, we propose to integrate acoustic actuators with drive electronics on a single complementary metal oxide semiconductor (CMOS) application-specific integrated circuit (ASIC). Since acoustic tweezers and imaging transceivers present similar challenges in control and wiring complexity, existing ASIC imaging systems merit consideration. Chen et al. [10] developed an integrated lead zirconate titanate (PZT) transducer matrix based on a micro-beamforming method. Although the channel count is reduced by a factor of 9, the use of micro-beamforming, limited the phase pattern that could be generated. Chen et al. [11] and Wygant et al. [12] used passive-matrix addressing techniques which further reduced the port count to N + M. However, the pixels did not actuate simultaneously, preventing the generation of arbitrary phase patterns across all signal outputs. There are also many system-on-chip and handheld ultrasound system implementing ASIC transceivers [13 - 19]. However, none of them maintains full scalability whilst providing the arbitrary phase pattern reconfigurable in real time required for flexible acoustic hologram generation.

We propose a fully scalable 2-D ultrasonic active-matrix signal generator ASIC capable of generating arbitrary, dynamic phase patterns in real time. This signal generator allows each pixel to actively maintain its state while other pixels are being addressed. The pixel control circuit is much simpler than its counterpart reported in [20] and hence more scalable. A prototype 1 × 9 array signal generator was implemented in a 5 V, 0.35 μm CMOS process at Austria Mikro Systeme (AMS). The scalability and phase control of the proposed matrix signal generator have been verified by combining several of these prototypes to generate 2-D phase patterns, with port count reduction compared to conventional direct-wiring devices [6].

II. System-Level Architecture

The system-level architecture of the ASIC is shown in Fig. 1. To maximize scalability, an active-matrix addressing technique was implemented in two stages. The first pair of column-and-row addressing signals are the per-column Column Select (*CS*) signal and the per-row Enable / Disable (*En_Disen*) signal, the latter of which enables and disables the addressed pixel. *CS* is used a second time, together with an

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External Delay (*Ex_D*) signal, to trigger a phase shift in the addressed pixel. In each column, only one *CS* input is required. The implementation of this active-matrix addressing technique changes the interconnection count for a N × M 2-D matrix from N × M to (3 × N) + M with no reduction in phase shaping flexibility.

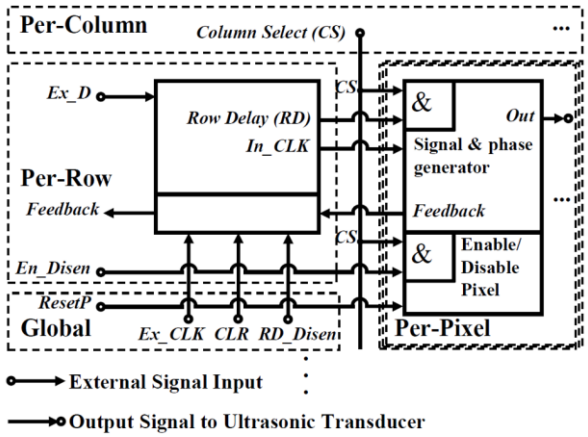

Fig. 1. Outline system-level architecture for 1 × M array (1 row of pixel signal generators) suitable for use in N columns for an N × M 2-D array.

III. Detailed Circuit and Operation

A. Phase Shifting Scheme

Fig. 2 shows an example of the phase-shifting scheme illustrated with a 2-bit counter applied per pixel. The phase shift is implemented in the pixel control circuit; a delay request is sent to the *Ex_D* port and the row-driver circuit responds and transfers the asynchronous request to a synchronous Row Delay (*RD*) signal. The synchronous *RD* signal is sent to the specific pixel in the selected column. The selected pixel control circuit removes one Internal Clock (*In_CLK*) pulse and a step delay is generated at the output. As a result, the phase shift resolution varies proportionally to the counter resolution. The advantage of implementing this scheme is that it can shift the output phase of pixels using an active-matrix technique, which significantly reduces the port count i.e. the external ASIC connection count.

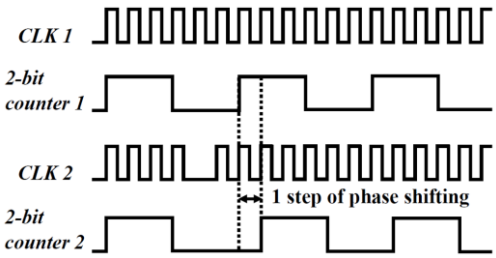

Fig. 2. Signal waveforms illustrating phase shifting

B. Row Drive-circuit and Operation

The row-driver (delay signal generation) circuit is shown in Fig. 3. The function of this circuit is to capture each *Ex_D* request, regardless of arrival time, and transfer the request to a synchronous *RD* signal, as illustrated in Fig. 4 (a). When a delay request is received from the *Ex_D* port, the D-type flip flop 1 (DFF1) saves the request and waits for the next rising edge of the External Clock (*Ex_CLK)* signal; the request is transferred to and saved by DFF2. At the next falling edge, the *RD* output of DFF3 is toggled; meanwhile DFF1 and DFF2 are reset. DFF2 is set up in this manner to remove set-up and hold violations from output DFF3, preventing additional phase shifts. The operation cycle ends at the next falling edge with the *RD* output toggled back to low and the *RD* high pulse covering one *In_CLK* high pulse.

In this scheme, *RD_Disen* holds the output at logic low; it does not clear the saved data in DFF1 and DFF2, and This is achieved by *CLR*. High capacity buffers are needed for the clock and delay signals. If the pixel count in a row increases beyond 9 in future designs, it will be preferable to use a buffer tree structure.

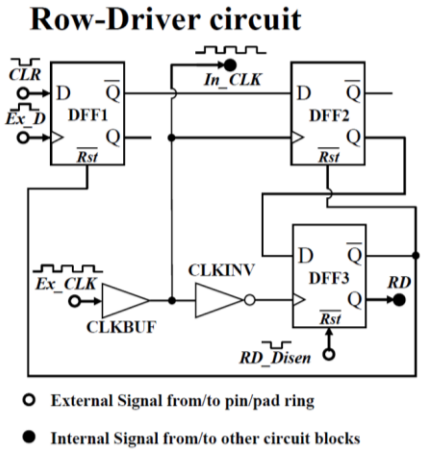

Fig. 3. Row-driver circuit for delay signal generation

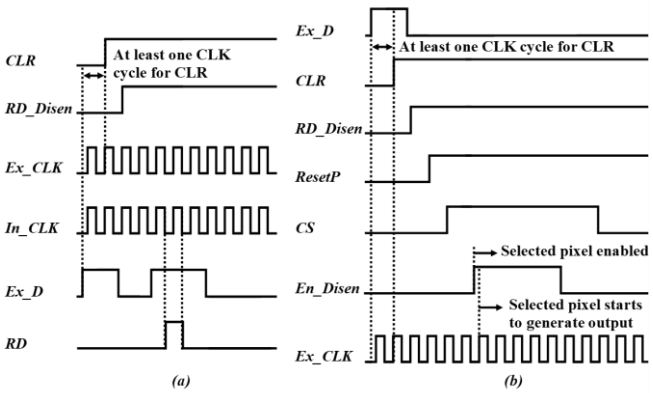

Fig. 4. (a) Signal waveforms illustrating functioning of the row-driver circuit; *In_CLK* is the buffered *Ex_CLK*; it contains propagation delays caused by buffers set in the ASIC. (b) System-level operation set-up and timing

C. Pixel Circuit and Operation

In Fig. 5, active-matrix addressing for the pixel HIGH / LOW state is realized through a 2-input AND gate (AND2) and phase shifting is implemented by a D-latch (Latch1). Once *CS* is enabled by logic high, another logic high at the *En_Disen* port triggers a toggle at DFF4, addressing the pixel with the HIGH state so that it outputs a signal. On the other hand, provided that the pixel is in a HIGH state and *CS* is enabled at logic HIGH, whenever there is an incoming signal at *RD*, it is inverted at Latch1 and removes one *In_CLK* pulse by disabling the AND1. This is possible because the *RD* rising edge is half of the *In_CLK* time period before the *In_CLK* signal's rising edge, and the falling edge of *RD* is inherently one propagation delay after the falling edge of the *In_CLK*

pulse. That is to say, the 3-input AND gate removes the second *In_CLK* pulse after the system reading a rising edge of the *Ex_D* signal. The 4-bit counter was chosen for this design because it provides 4-bit phase resolution at the outputs which has been demonstrated to give satisfactory results in trapping strength [21]. In future iterations, the 4-bit counter can be replaced by a higher bit count counter or a programmable counter to achieve more flexibility. The *CS* signal also controls the '*Feedback*' output to send out feedback from the selected pixel in a row to be monitored, as only the transmission gate in the pixel addressed by *CS* is enabled to transmit a signal.

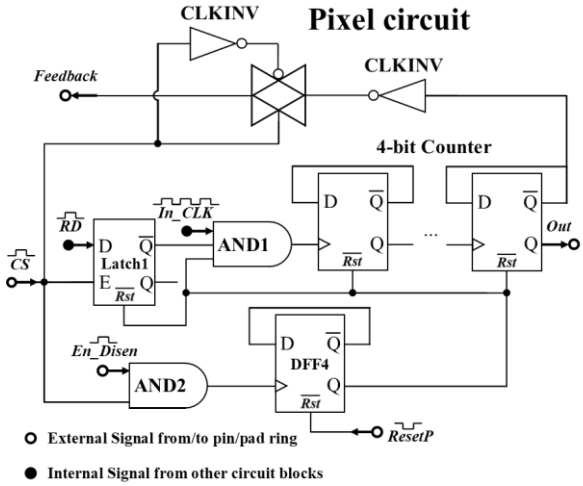

Fig. 5. Schematic diagram of the pixel control circuit

IV. Simulation Results

A. System-level Operation Set-up and Timing Diagram

To remove all unknown states in the circuit before operation, the *CLR* signal is reset to logic 0 (LOW), working with a rising edge of *Ex_D* to clear the row-driver. In the next sequence, *RD_Disen* and *ResetP* must be set to logic LOW before being enabled by logic HIGH as illustrated in Fig. 4 (b). Then *CS* and *En_Disen* will enable a specific pixel to generate a square wave with frequency f_{Ex_CLK} / 16. If multiple driving signals with the same phase are required by ultrasound transducer elements, *Ex_CLK* should be set only after enabling all pixels when the ASIC starts.

B. Simulated Results

Cadence [22] was used to simulate a 1 × 9 pixel signal generator array clocked at 128 MHz, and the phase shift performance is shown in Fig. 6.

After applying the set-up sequence shown in Fig. 4 (b), another LOW-to-HIGH pulse is sent to *Ex_D*, so a row delay symbol is generated at *RD*. As Column Select 9 (*CS9)* is set when the delay signal is sent out from the row-driver circuit, the 4-bit counter in *CS9* receives one less clock pulse than the Column Select 1 (*CS1)* signal and a 22.5° phase-shift, which is the smallest phase-shift step that can be provided by this design, is generated. Fig. 6 shows the various signal pulses and their timings. The key signals for phase shifting at *Output9* are illustrated with red waveforms and the blue traces are for *CS1* and *Output1* in column 1 and system start-up. This confirms that *CS9* has an additional pulse compared to *CS1*, and *Output9* is hence delayed by 22.5° compared to *Output1*. Note that the misalignment between *Ex_CLK* and each of the output signals is caused by propagation delays within the ASIC.

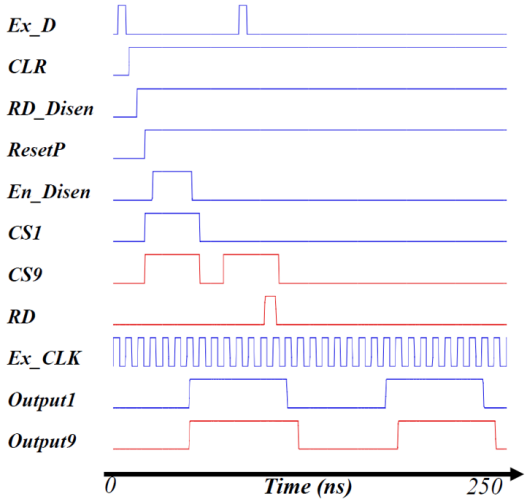

Fig. 6. Phase shifting performance in simulation.

V. Experimental Setup and Test Results

A. Electrical testing of the ASIC

The prototype ASIC was implemented with an Austria Mikro System (AMS, ams.com) fabrication process with 0.35 µm minimum feature size. For validation, test points and additional buffers were set around the design, with the 1175 × 88 µm^2 structure at the center of the chip forming the 1 × 9 array, Fig. 7 (a). Fig. 7 (b - d) show the fabricated 1 × 9 signal generator array at different levels of magnification.

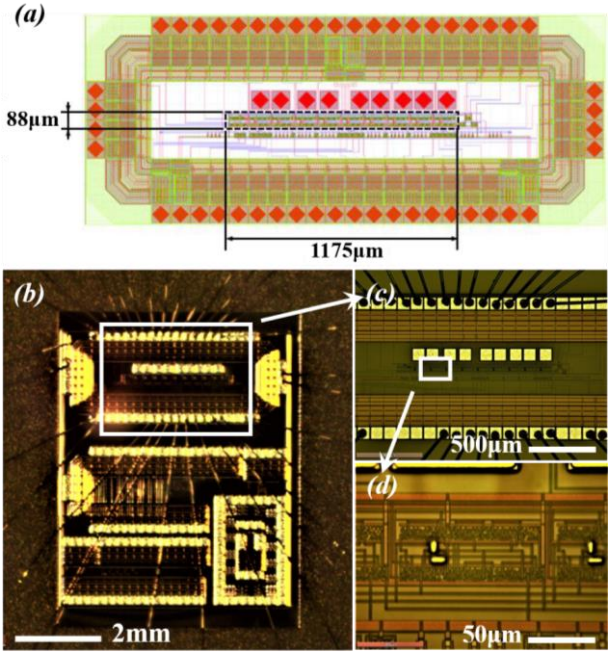

Fig. 7. (a) Full design layout of 1 × 9 test structure. (b) Photomicrograph of the full chip. (c) Photomicrograph of the 1 × 9 test structure. (d) Photomicrograph of circuitry for a single pixel

The output buffer set on chip allows the ASIC to provide 5 V square waves with 1 mA drive current and ~5 pF as output capacitance. The power rating of the ASIC was designed to be

35 mW, which meets the requirements of the buffers and core circuits set on-chip. For future on-chip integration with transducers, custom-designed drivers / buffers are suggested to be implemented to optimize the performance of transducers, and the power rating should be adjusted accordingly.

To allow direct comparison, the experiment and simulation were designed to have the same start-up sequence. Single-pole double-throw switches (SPDT, MCTI series, Farnell, Leeds, UK) were implemented with switch de-bouncing circuits to generate control signals. The measured 1 - 4 steps of the phase shift are shown in Fig. 8. All pixels on chip function as expected and phase-shifts of 22.5°, 45°, 67.5° and 90° can be clearly observed.

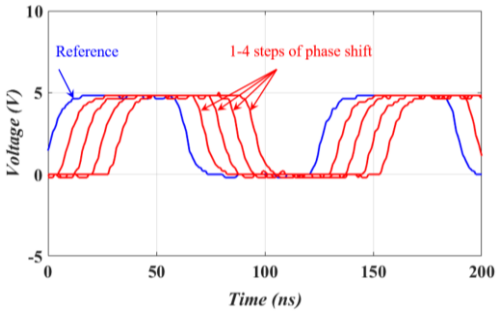

Fig. 8. Experimentally observed phase shifts of 22.5°, 45°, 67.5° and 90° at 8 MHz output frequency.

B. Ultrasonic Testing System Setup

To prove that the circuitry is scalable and demonstrate its phase shaping capability acoustically, we designed a system to demonstrate its programmable phase shifting capabilities. A schematic outline of the electrical system is shown in Fig. 9. Four ASIC prototypes were integrated onto a printed circuit board (PCB) with patch support to provide control for a total of 36 pixels. Although the ASICs represent four 1 × 9 control arrays, they are shown here controlled a 6 × 6 array. The PCB acts as the main board to relay the appropriate phase to the transducer matrix. A separate PCB was designed for a 6 × 6 air-coupled 2-D transducer matrix array, connected to the main board with ribbon cables for transducer activation.

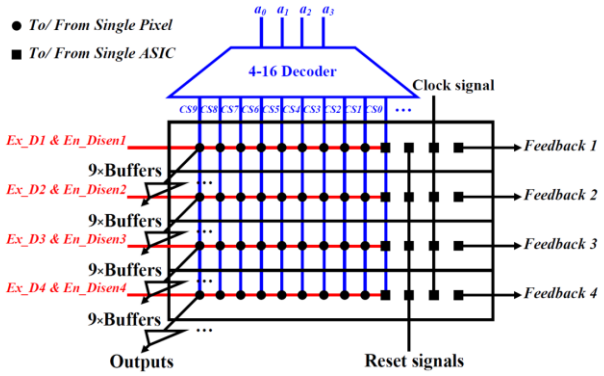

Fig. 9. Schematic outline of the complete electrical system

The main control board of the system also demonstrates scalability and buffering of ASIC outputs. As shown in Fig. 9, a decoder is added to reduce the number of *CS* input connections. Likewise, taking advantage of the ASIC design, two additional decoders could be implemented to reduce the number of per-row *En_Disen* signals and per-row *RD* signals. However, as there are only four of each signal type in the present system, the yield is limited and the idea was not adopted. 5 V buffers are added to protect the ASIC outputs and improve the driving flexibility of the system, to support later experiments.

C. Calibration

As a demonstration, commercial 40 kHz air-coupled ultrasound transducers (Prowave 400ST100, Farnell, Leeds, UK) were implemented in a 6 × 6 2-D array. As the transducers are low cost items, it was anticipated that the array would be nonuniform due to electrical impedance mismatching causing undesired delays to the acoustic outputs. To improve performance, a microphone system [23] was used to calibrate the system by positioning it under each transducer and comparing the measured signal against a reference signal. During calibration, the amplitude of the measured signal is normalized and the phase difference between reference and measured signal gives a phase offset that is then introduced as an additional phase shift for array control. The calibration phase pattern for the system is shown in Fig. 10 (a). The calibration phase pattern depends on the measurement setup; in the present case, it is valid for a vertical distance of 60 mm between microphone and transducer matrix.

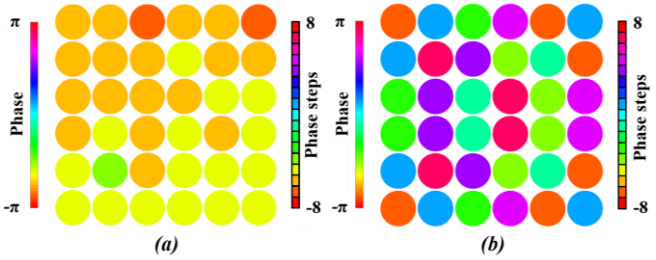

Fig. 10. (a) Experimental phase calibration pattern. This pattern only valid for a vertical distance of 60 mm between microphone and transducer matrix. (b) Trapping phase pattern

The calibration precision is determined by the phase shift resolution. For the presented case, as the system has 4-bit phase resolution, the maximum phase error is reduced to π/8. For further improvement, careful impedance matching would need to be carried out between every buffer output and the ultrasound transducer input connected to it. However, since the purpose of the present system is to demonstrate functioning of the phase control ASIC, no further adjustment was performed.

D. Calibrated System and Programmable Phase Control

To initially demonstrate the calibration outcome and system phase control, two simple patterns were produced by the system and measured with the microphone setup [23]. Fig. 11 (a) shows the acoustic field generated by a single excited transducer element with 0° phase shift applied. The driving signal was fixed at 5 V_{pp}, and the relative intensity was measured across a 50 × 50 mm^2 area. From the phase map, it is clear that the phase of the wavefront at a vertical distance of 60 mm is approximately zero at the centre position of the operating transducer, as expected.

A π/8 (22.5°) phase change was then applied to the system, which is the minimum phase change the integrated circuit can provide, and the acoustic field formed is shown in Fig. 11 (b).

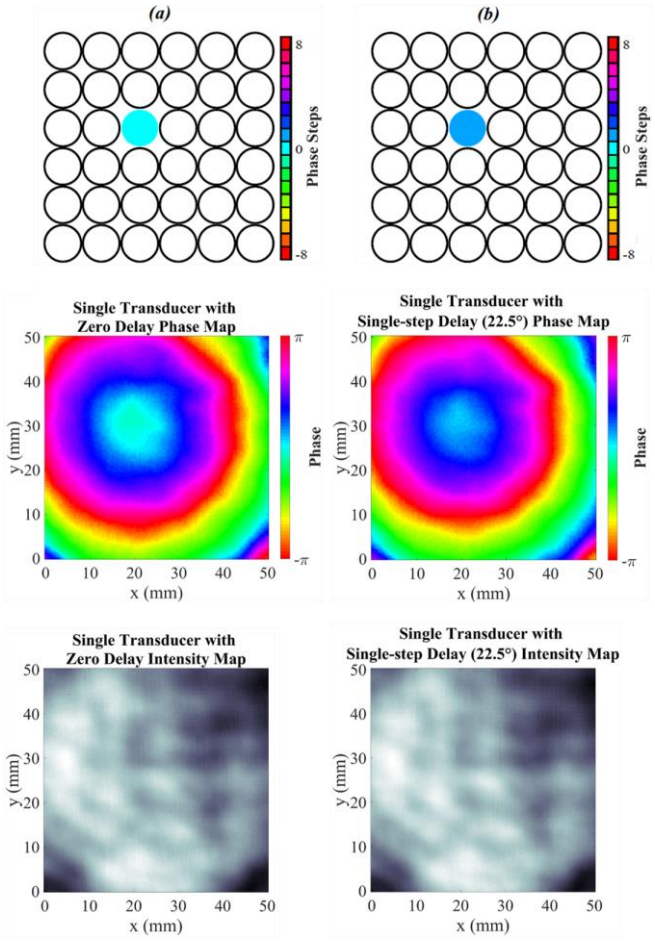

Fig. 11. (a) Phase and relative intensity of the acoustic field generated by stimulating a single transducer element with a non-delayed square wave (b) Phase and relative intensity of the acoustic field generated by stimulating a single transducer element with one step-delay (22.5°) square wave. The measurement was taken 60 mm above the transducers.

By subtracting the results shown in Fig. 11 (a) and averaging the difference, the phase difference between the two patterns was found to be 23.9°. This gives a 1.4° error from the expected 22.5° phase change. Thus, the ASIC is shown to be capable of delivering 4-bit resolution phase control.

E. Orbital Angular Moment Pattern

In order to demonstrate the programmability of the phase of the system, an azimuthal phase pattern was set up. This is similar to patterns used for the generation of structured wavefronts that carry orbital angular momentum (OAM) [24] and have been used to rotate particles [8] without continuous updating of the amplitude of the acoustic signal [6]. To achieve suitable spatial resolution, all 36 transducer elements were activated. The transducers are mapped with the appropriate phase profile, expressed by $\psi(\varphi) = exp(i\ell\varphi)$, where ℓ is the topological charge and is an unbounded integer, while φ is the azimuthal angular coordinate. Fig. 12 (b) is a representation of the phase profile for $\ell = 1$ for 36 transducers, Fig. 12 (a). By applying this profile onto the transducer array, the intensity and phase maps in Figs. 12 (c) and (d), respectively, were produced.

An example of an OAM mode can be found in [23]. Comparing the results in Figs. 12 (c) and (d) to that mode, it is clear that there are some undesired interface effects at the center of the measurement in this work. These are attributed to phase aberrations arising from electrical impedance mismatches, errors in the spatial locations of the transducers, and grating lobes caused by the transducer spacing being larger than the wavelength of sound. Performance could be improved by particularly by reducing the spacing between transducer elements to at most 4.3 mm to eliminate grating lobes and generate a coherent wavefront, as shown in [23].

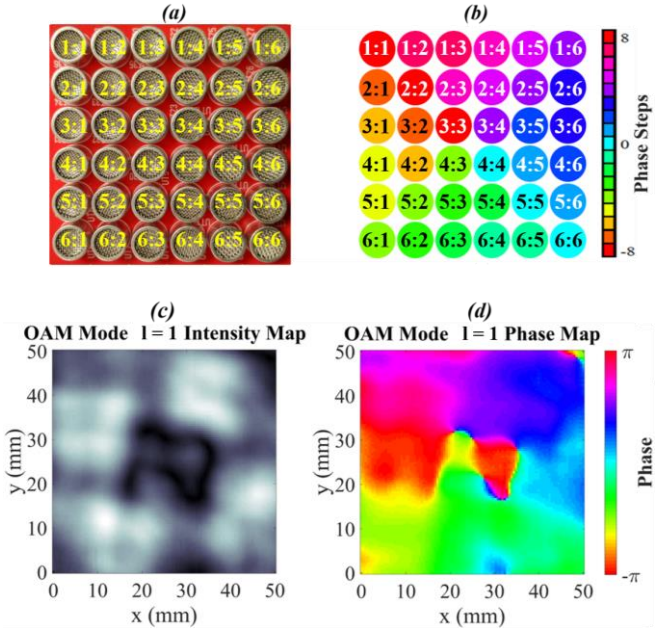

Fig. 12. (a) Image of the transducer array used to generate spatially structured acoustic beams. Small variations in position of the transducers can be seen. (b) The azimuthally varying phase applied to the transducer array. (c) Intensity and (d), phase of the acoustic field generated by applying the pattern in (b) and showing aberrations from arising impendence errors and interference. The measurement was taken 60 mm above the transducers.

F. In-air Particle Trapping and Vertical Manipulation

To further demonstrate the system capabilities and flexibility, one of the holographic acoustic framework phase patterns presented in [6] was adopted, as shown in Fig. 10 (b). To provide a field strong enough to levitate a physical object in air, four 1 × 9 voltage-level translator / adaptor electronic arrays were built. Fig. 13 shows the circuitry of one of the adaptors. The potentiometer is set to allow the output amplitude to be adjusted between 0 and $(V^+ - V^-)$; with a value ×10, the gain of the amplifying circuitry is set to be large enough to ensure the output amplitude can reach $(V^+ - V^-)$ in an ideal case. By connecting these adaptors into the system, we were able to generate 25 V_{pp} continuous square waves to stimulate the 40 kHz transducer elements. With the phase pattern and calibration set, the system was able to levitate and trap a 5 mm diameter expanded polystyrene particle, as seen in Fig. 14 (a).

To prove that the system is capable of generating real-time dynamic acoustic fields, simple vertical real-time manipulation was performed. The trapping patterns for object manipulation can be decomposed into two patterns, one with the required phases for trapping and manipulation and the other one a phase pattern used for focusing holographic lenses [6]. To realize real-time vertical manipulation, delays are continually added to the transducer elements in the outer ring, changing the focal point of the "lens", thus changing the vertical trapping position. As a result, the expanded polystyrene particle moves up and down with reference to the trapping point. This vertical manipulation is shown in

Figs. 14 (b) and (c); the maximum vertical distance is ~5 mm with minimum step ~0.3 mm and a total of 16 steps.

These results are a qualitative demonstration of the acoustic field shaping and flexibility of the system. Compared with a direct-wiring system, the speed of dynamic phase control will be slightly reduced for large-scale arrays due to the trade-off made when implementing the active-matrix addressing methodology. For example, if a 640 kHz clock is implemented to drive a 500 pixel × 500 pixel system, the worst-case whole-matrix phase pattern update time can be estimated to be ~0.59 s. However, this time may be reduced by optimizing the dynamic programmable phase algorithm or by constraining in ways allowed by a given application.

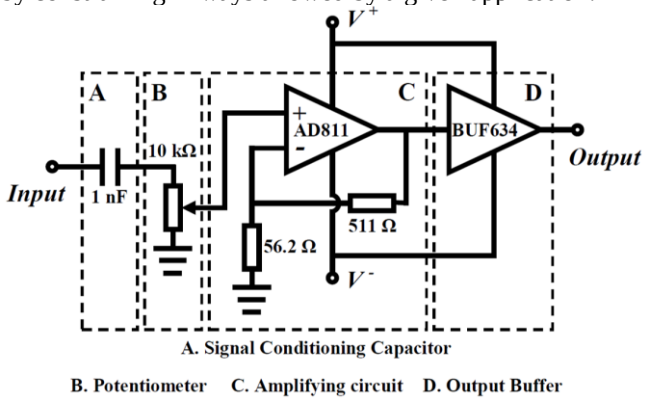

Fig. 13. Single adaptor structure of the 1 × 9 adaptor / driver array

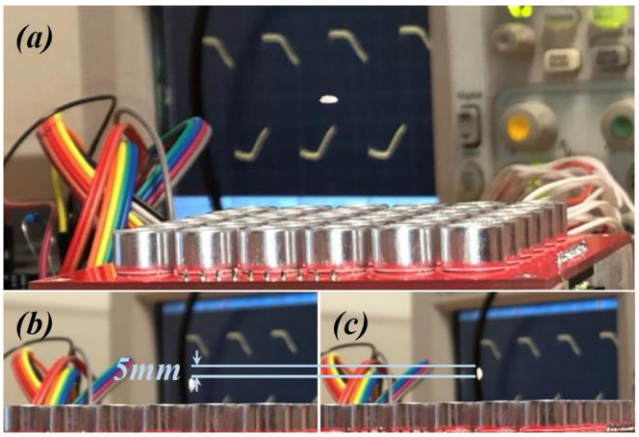

Fig. 14. (a) In-air particle trapping: (b) start of vertical manipulation, (c) end of vertical manipulation. The particle is levitated to ~5 mm above the transducer surface and the height can be varied by approximately the same amount in 16 steps.

G. *Towards Integrated Tweezers with Micromachined Ultrasonic Transducers*

An attractive physical configuration of the ASIC that has been described is in an integration system with a piezoelectric micromachined ultrasonic transducer (PMUT) array. To demonstrate the potential of integration and control, an experimental prototype PMUT matrix was driven by one of the ASICs integrated on the main control PCB in the system shown in Fig. 9.

The PMUT matrix consists of a 2 × 2 arrangement of elements, and each element contains nine (i.e. 3 × 3) diaphragms operating at 8 MHz. Four synchronized 8 MHz, 5 V_{pp} unipolar square waves were generated from the ASIC to drive the four PMUT arrays. To demonstrate the phase control performance, four square waves were set with 0°, 90°, 180° and 270° phase shifts and the vibration of the PMUT matrix was recorded with a laser Doppler vibrometer, Fig. 15.

Because the electrical connections between the CMOS matrix signal generator and the PMUT elements were made through external cables, the deflection of the PMUTs was inevitably degraded due to the impedance mismatch. Impedance mismatch reduces the energy transfer from the ASIC outputs to the transducer and hence results in reduced deflection amplitude. This degradation is recorded as an intensity map in Fig. 15 (c), which shows an average deflection amplitude of several nm. By properly matching the impedance between the matrix signal generator and PMUTs in future on-chip integrations, an improved average deflection is expected.

Although the propagation delay and RC time delay cause undesired phase shifts in the acoustic outputs, these shifts are expected to be uniform as they are generated by identical cables of the same length when the circuitry is connected to the PMUTs. Further study of the phase differences among acoustic outputs to demonstrate acoustic field shaping is warranted. Nevertheless, as shown in Fig. 15 (d), the four phase quadrants can be observed clearly. There is an approximately 50° phase difference between the phase pattern set in the program, which is shown in Fig. 15 (b), and the measurement shown in Fig. 15 (d). It is observed that this difference is uniform across all diaphragm locations, hence our conclusion that the cause is some combination of propagation delay and resistor-capacitor time delay. Importantly, however, the relative phase between transducer elements is as expected, which is sufficient to demonstrate acoustic field shaping.

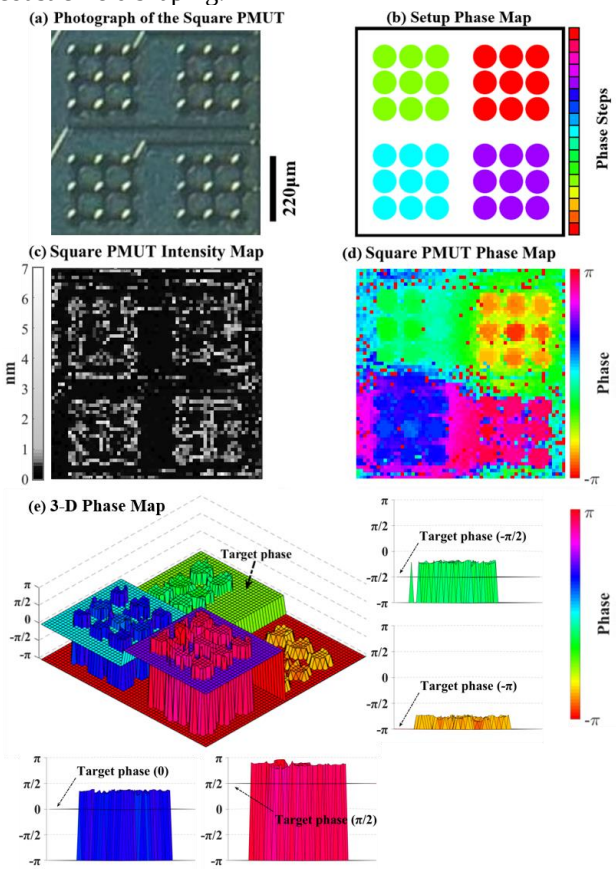

Fig. 15. Vibration phase and intensity captured by laser vibrometer

VI. Conclusions

This paper has described a digital active-matrix ASIC solution to output excitation signals for an array of PZT transducers to generate acoustic holograms. For an N × M channel matrix with arbitrary phase pattern generation capability, the port count is (3 × N) + M. This compares very favorably with the N × M port count for conventional direct-wiring devices. The scalability of this design opens the potential for its use in a wide range of applications. For the intended ultrasound application, practical acoustic hologram resolution can be significantly improved by the port count reduction we have achieved. Direct comparison of simulation and experimental results has proved the functionality of the ASIC. The functional potential of piezoelectric and CMOS integration has been demonstrated not only with bulk transducers but with micromachined ultrasonic transducers, through acoustic experiments and measurement and potential detailed improvements have been outlined where relevant.

Acknowledgment

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