Energy Distribution of Positive Charges in Al_2O_3/GeO_2/Ge pMOSFETs

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***Abstract*— The high hole mobility of Ge makes it a strong candidate for end of roadmap pMOSFETs and low interface states have been achieved for the Al_2O_3/GeO_2/Ge gate-stack. This structure, however, suffers from significant negative bias temperature instability (NBTI), dominated by positive charge (PC) in Al_2O_3/GeO_2. An in-depth understanding of the PCs will assist in the minimization of NBTI and the defect energy distribution will provide valuable information. The energy distribution also provides the effective charge density at a given surface potential, a key parameter required for simulating the impact of NBTI on device and circuit performance. For the first time, this letter reports the energy distribution of the PC in Al_2O_3/GeO_2 on Ge. It is found that the energy density of the PC has a clear peak near Ge Ec at the interface and a relatively low level between Ec and Ev. Below Ev at the interface, it increases rapidly and screens 20% of the Vg rise.**

***Index Terms*— Positive charges, energy distribution, Al_2O_3/GeO_2, Ge pMOSFETs, NBTI, aging, reliability.**

I. Introduction

GERMANIUM has attracted much attention for end of roadmap CMOS application, especially the pMOSFET because of its high hole mobility [1]–[5]. Ge MOSFETs used to suffer from the lack of a good native oxide and a high level of interface states, but significant progress has been made recently [1]–[5]. It has been reported that the interface state density at the GeO_2/Ge interface can be comparable with that at SiO_2/Si, if the interaction between GeO_2 and Ge and GeO evaporation can be controlled [3], [4]. Al_2O_3 has been used to effectively suppress the GeO evaporation and Ge MOSFETs with promising performance have been demonstrated with an Al_2O_3/GeO_2 gate stack [3], [4].

After achieving good initial performance, attention should be paid to its reliability. The lifetime of Si pMOSFETs is limited by negative bias temperature instability (NBTI) [6]–[11] and the Ge pMOSFET with Al_2O_3/GeO_2 also suffers from substantial NBTI. NBTI has two sources: generated interface states and positive charges formed in the gate dielectric by hole trapping, referred to as positive charge ('PC') hereafter [6], [7], [9]. The PCs in Si MOSFETs have a complex behavior and caused much confusion since 1970s [6], [12]–[15]. There is little information on the PCs in Al_2O_3/GeO_2/Ge and to assist understanding, it is desirable to know their energy distribution. This distribution also provides the PC density at a given surface potential needed for simulating the NBTI impact on devices and circuits.

The objective of this letter is to report the energy distribution of PCs in the Al_2O_3/GeO_2/Ge system. We have recently developed a technique that can probe the energy distribution of PCs for Si MOSFETs [16] and it is adapted here for Ge MOSFETs. The results show that the energy density of PCs has a clear peak near the Ge Ec at the interface and is substantially lower between Ec and Ev. Once below Ev at the interface, however, it rises rapidly.

II. Device and Experiments

A 700 nm Ge layer was prepared on a Si wafer, followed by oxidation at 150 °C in atomic oxygen to form 1.2 nm of GeO_2. A 4 nm Al_2O_3 layer was then deposited and the SiO_2 equivalent oxide thickness is 2.35 nm. After the gate metallization with a 10 nm PVD TiN layer, the pMOSFETs were annealed in forming gas at 350 °C for 20 min. The channel length and width is 1 μm and 50 μm, respectively.

The test started with recording the reference Is–Vg at Vd = −100 mV from a gate pulse edge of 5 μs and trapping during this measurement is negligible [17], [18]. The reference threshold voltage, i.e. Vtho, was extracted by extrapolating from the maximum transconductance.

After stressing and charging at Vgst, |Vg| was reduced from |Vgst| to a base level of |Vdischarge,1| for discharge by using the waveform in Fig. 1(a). During discharge, the device was pulsed from |Vdischarge,1| to monitor the Vth shift, i.e. ΔVth, at a constant Is = 100 × W/L nA. Once Discharge,1 completes, Vg was stepped to |Vdischarge,2| and the same procedure was applied. This allows the extraction of oxide charges as a function of the base discharge voltage. A pulse edge time of 5 μs was fast enough to freeze discharging [19]. The effective density of positive charges, ΔNox, defined in section III, versus discharging time is given in Fig. 1(b). Fig. 1(b) shows that the discharge mainly occurs within 1 sec, so that a discharge time of 1 sec will be used for each Vdischarge hereafter. Fig. 1(c) gives the ΔVth at 1 sec of discharge versus Vdischarge. The variation of ΔVth with Vdischarge is significant.

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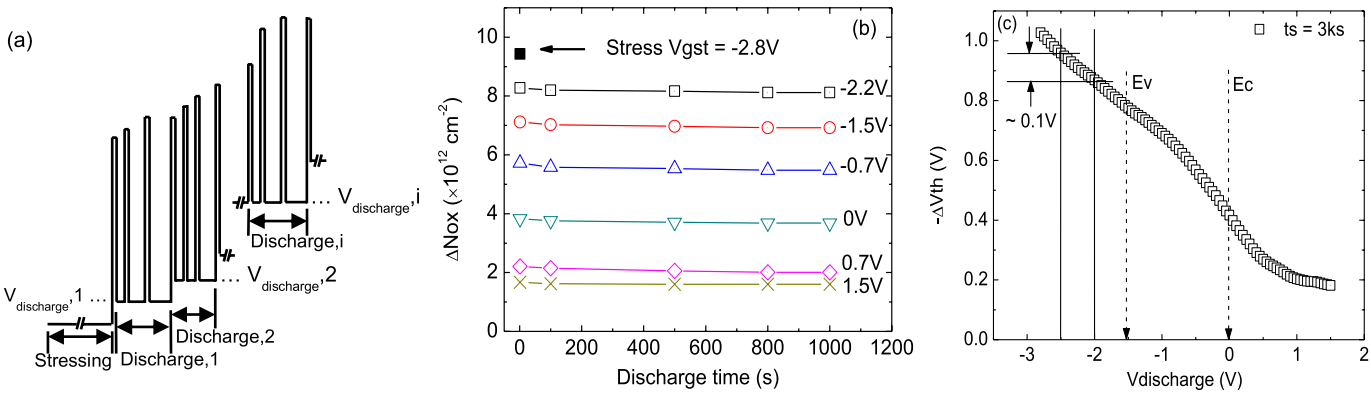

Fig. 1. (a) The Vg waveform; (b) The discharging against time under each Vdischarge; and (c) The ΔVth at the end of each discharge period against Vdischarge. The device was stressed at Vgst = −2.8 V, 20 °C, for 3000 sec.

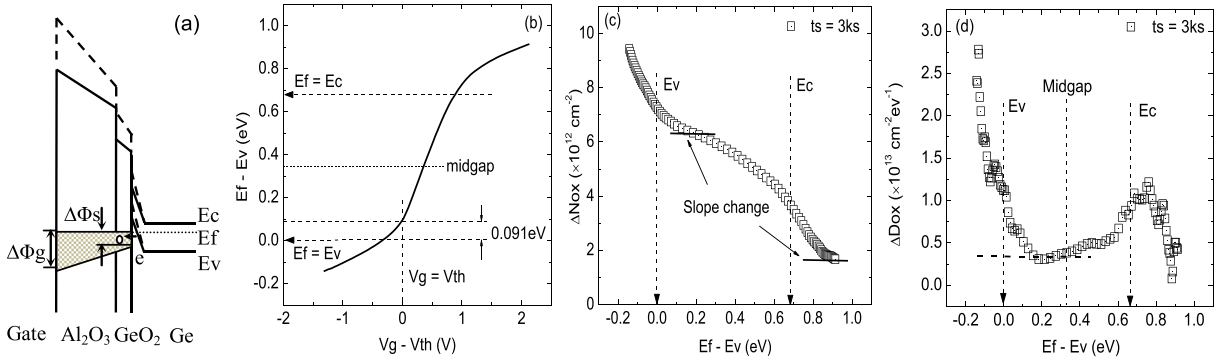

Fig. 2. (a) A schematic energy diagram before (dashed lines) and after (Solid lines) Vdischarge stepping towards positive. After the stepping, the PCs in the shaped region is below Ef and will be discharged. (b) The Ef-Ev against Vg−Vth for converting each Vdischarge to an Ef-Ev. (c) The typical energy distribution of PCs per unit area, ΔNox. (d) The corresponding energy density, ΔDox. The device was stressed at Vgst = −2.8 V, 20 °C, for 3000 sec.

III. Results and Discussion

The principle of the probing technique is illustrated in Fig. 2(a). When Vdischarge was stepped towards positive, the PCs in the shaded area fell below Ef and discharged [16], [20]. By varying Vdischarge over a large range, Ef can be swept from below Ev to above Ec at the interface. It should be pointed out that the quantization effect leads to a deviation of ground state energy levels from the Ec and Ev at the interface in Fig. 2(a). The 'Ec' and 'Ev' were used here to represent band bending, following common practice [21].

To obtain the energy distribution, Vdischarge should be converted to Ef-Ev at the interface. This relationship was obtained from a 1D Schrödinger-Poisson simulator [22] and the result is given in Fig. 2(b). It should be noted that the horizontal axis of Fig. 2(b) is Vg−Vth and Vth = Vtho+ΔVth varies during discharging.

Fig. 2(c) plots the effective density of PCs, i.e. ΔNox, versus Ef-Ev, evaluated from $\Delta Nox = Cox \times \Delta Vth/q - \Delta Nit$, where ΔNit is the number of generated interface states charged at Is = 100 × W/L nA [16]. For a given stress level, ΔNit does not change with Vdischarge, since ΔVth was always measured at the same source current for all Vdischarge. The interface states were measured by the charge pumping method at 1 MHz, a rise/fall time of 20 ns, and an amplitude of 1.0 V. Their density pre- and post-stress is 6.12×10^{11} cm^{-2}, 1.08×10^{12} cm^{-2} and the generated ones are 4.68×10^{11} cm^{-2}, one order of magnitude less than the ΔNox in Fig. 2(c), so that the NBTI of $Al_2O_3/GeO_2/Ge$ is dominated by PCs. Their effect has been taken into account in evaluating the energy distribution of PCs [16].

The energy density of PCs is evaluated from $\Delta Dox = -d(\Delta Nox)/d(Ef\text{-}Ev)$ and a typical result is given in Fig. 2(d). As Ef-Ev at the interface increases, Fig. 2(c) shows that ΔNox initially decreases rapidly, resulting in a high ΔDox in the order of 10^{13} cm^{-2}eV^{-1}. As Ef approaches Ev, however, the declining rate of ΔNox reduces sharply. To assess how the PCs below Ev affect device operation, Fig. 1(c) shows that Ef = Ev occurs at Vg = −1.55 V. As a result, the hole traps below Ev are neutral and have no effect on devices with an operational |Vg|<1.55 V. For higher operation |Vg| however, some PCs will be positively charged, reducing the driving |Vg−Vth|. For example, if |Vg| increases from 2 to 2.5 V, Fig. 1(c) shows that 0.1 V. i.e. 20% of the |Vg| -increase, will be used to compensate the PCs.

When Ef moves above Ev, Fig. 2(c) shows a slope change, leading to a low level of ΔDox between Ev and Ec. As Ef approaches Ec, however, the declining rate of ΔNox picks up again, before the second slope change above Ec. This creates a clear peak of ∼10^{13} cm^{-2}eV^{-1} in ΔDox near Ec. The PCs near Ec will be charged under an operation Vg and cause significant NBTI for $Al_2O_3/GeO_2/Ge$ pMOSFETs.

To explore the relation between the PCs below Ev and those above Ev, Fig. 3 shows a comparison of their dependence on stress time. It is clear that, at short time (the symbol '•'), PCs are negligible above Ev, but substantial below Ev. As stress time increases, the PCs above Ev increase, but they do not shift up in parallel. To show that the PCs below Ev are insensitive to stress time, the top-dashed curve is used as an eye-guide for the top data-set with a stress time of 10 ksec. It is then shifted downward in parallel, showing good agreement with the data-set at 5 ms. It means that the

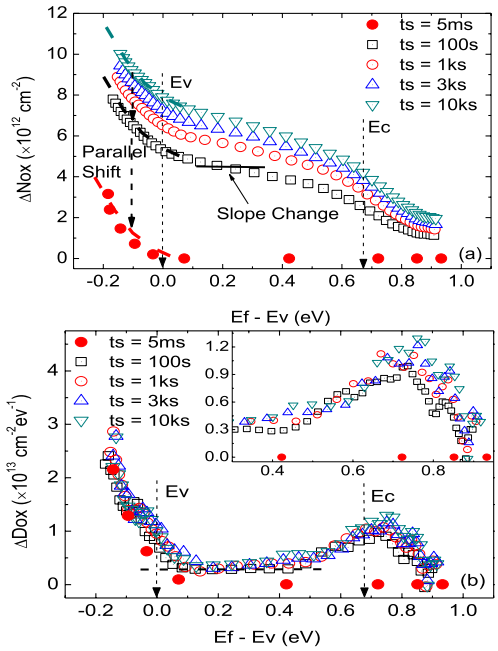

Fig. 3. A comparison of ΔNox (a) and ΔDox (b) after different stress time under Vgst = −2.8V at 20 °C. The top dashed curve is an eye-guide for the top data-set at ts = 10 ks. The other two dashed curves were a parallel downward shift of the top dashed curve. The symbols • were obtained on a fresh device with a time for each point of 5 ms to minimize generation. The Vg was swept from positive to negative direction for this dataset.

below-Ev PCs were already fully charged after only 5 ms. The ΔDox near Ec, however, increases substantially after stress. The different stress-time dependence of defects below Ev and around Ec indicates that they could originate from different defects, although the electrical measurements reported here do not give direct information on their microscopic structure. For SiO_2/Si, it is reported that oxygen vacancy is a hole trap [23], [24] and some hydrogen-related defects can form different types of hole traps [9], [24], [25]. One may speculate that oxygen vacancy and hydrogenous defects also exist in the present Al_2O_3/GeO_2/Ge sample, which awaits further investigation [26].

IV. Conclusion

In this letter, the energy distribution of PCs in the Al_2O_3/GeO_2/Ge gate stack was characterized. The results show that ΔVth can vary significantly when Ef was swept from below Ev to above Ec at the Ge interface. The energy density distribution has three features: a rapid rise when moving below Ev at the interface, relatively low between Ev and Ec, and a peak near Ec. The below- and above-Ev PCs have different dependences on stress time: the charging of below-Ev PCs is rapid and saturates, while it is slower and does not saturate for the above-Ev PCs. The density can reach 10^{13} $cm^{-2}eV^{-1}$ below Ev and 20% of |Vg|-increases can be screened by these PCs.

References

[1] C. Le Royer, "Interfaces and performance: What future for nanoscale Ge and SiGe based CMOS? (invited)," *Microelectron. Eng.*, vol. 88, no. 7, pp. 1541–1548, Jul. 2011.

[2] P. C. McIntyre, Y. Oshima, E. Kim, *et al.*, "Interface studies of ALD-grown metal oxide insulators on Ge and III–V semiconductors (invited paper)," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1536–1539, Jul./Sep. 2009.

[3] A. Toriumi, T. Tabata, C. H. Lee, *et al.*, "Opportunities and challenges for Ge CMOS—Control of interfacing field on Ge is a key (invited paper)," *Microelectron. Eng.*, vol. 86, nos. 7–9, pp. 1571–1576, Jul./Sep. 2009.

[4] R. Zhang, T. Iwasaki, N. Taoka, *et al.*, "High-mobility Ge pMOSFET with 1-nm EOT Al_2O_3/GeO_x/Ge gate stack fabricated by plasma post oxidation," *IEEE Trans. Electron Devices*, vol. 59, no. 2, pp. 335–341, Feb. 2012.

[5] B. Benbakhti, J. F. Zhang, Z. Ji, *et al.*, "Characterization of electron traps in Si-capped Ge MOSFETs with HfO_2/SiO_2 gate stack," *IEEE Electron Device Lett.*, vol. 33, no. 12, pp. 1681–1683, Dec. 2012.

[6] J. F. Zhang, "Defects and instabilities in Hf-dielectric/SiON stacks (invited paper)," *Microelectron. Eng.*, vol. 86, nos. 7-9, pp. 1883–1887, Jul./Sep. 2009.

[7] M.-F. Li, D. M. Huang, W. J. Liu, *et al.*, "New insights of BTI degradation in MOSFETs with SiON gate dielectrics," *ECS Trans.*, vol. 19, no. 2, pp. 301–318, 2009.

[8] Z. Q. Teo, D. S. Ang, and K. S. See, "Can the reaction-diffusion model explain generation and recovery of interface states contributing to NBTI," in *Proc. IEEE IEDM*, Dec. 2009, pp. 1–4.

[9] V. Huard, F. Monsieur, G. Ribes, *et al.*, "Evidence for hydrogen-related defects during NBTl stress in p-MOSFETs," in *Proc. 41st Annu. IEEE IRPS*, Mar./Apr. 2003, pp. 178–182.

[10] T. Grasser, B. Kaczer, W. Goes, *et al.*, "The paradigm shift in understanding the bias temperature instability: From reaction-diffusion to switching oxide traps," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3652–3666, Nov. 2011.

[11] H. Reisinger, T. Grasser, W. Gustin, *et al.*, "The statistical analysis of individual defects constituting NBTI and its implications for modeling DC- and AC-stress," in *Proc. IEEE IRPS*, May 2010, pp. 7–15.

[12] D. R. Young, E. A. Irene, D. J. Dimaria, *et al.*, "Electron trapping in SiO_2 at 295 and 77 degree-K," *J. Appl. Phys.*, vol. 50, no. 10, pp. 6366–6372, 1979.

[13] J. F. Zhang, M. H. Chang, Z. Ji, *et al.*, "Dominant layer for stress-induced positive charges in Hf-based gate stacks," *IEEE Electron Device Lett.*, vol. 29, no. 12, pp. 1360–1363, Dec. 2008.

[14] M. H. Chang and J. F. Zhang, "On positive charge formed under negative bias temperature stress," *J. Appl. Phys.*, vol. 101, no. 2, pp. 024516-1–024516-7, Jan. 2007.

[15] J. F. Zhang, M. H. Chang, and G. Groeseneken, "Effects of measurement temperature on NBTI," *IEEE Electron Device Lett.*, vol. 28, no. 4, pp. 298–300, Apr. 2007.

[16] S. W. M. Hatta, Z. Ji, J. F. Zhang, *et al.*, "Energy distribution of positive charges in gate dielectric: Probing technique and impacts of different defects," *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1745–1753, May 2013.

[17] Z. Ji, L. Lin, J. F. Zhang, *et al.*, "NBTI lifetime prediction and kinetics at operation bias based on ultrafast pulse measurement," *IEEE Trans. Electron Devices*, vol. 57, no. 1, pp. 228–237, Jan. 2010.

[18] Z. Ji, J. F. Zhang, M. H. Chang, *et al.*, "An analysis of the NBTI-induced threshold voltage shift evaluated by different techniques," *IEEE Trans. Electron Devices*, vol. 56, no. 5, pp. 1086–1093, May 2009.

[19] C. Shen, M. F. Li, X. P. Wang, *et al.*, "A fast measurement technique of MOSFET I-d-V-g characteristics," *IEEE Electron Device Lett.*, vol. 27, no. 1, pp. 55–57, Jan. 2006.

[20] T. Aichinger, M. Nelhiebel, S. Einspieler, *et al.*, "Observing two stage recovery of gate oxide damage created under negative bias temperature stress," *J. Appl. Phys.*, vol. 107, no. 2, pp. 024508-1–024508-8, Jan. 2010.

[21] Y. T. Hou, M. F. Li, Y. Jin, *et al.*, "Direct tunneling hole currents through ultrathin gate oxides in metal-oxide-semiconductor devices," *J. Appl. Phys.*, vol. 91, no. 1, pp. 258–264, 2002.

[22] G. L. Snider. (2013, Feb. 23). *1D Poisson Schrödinger*, University of Notre Dame, Notre Dame, IN, USA [Online]. Available: http://www3.nd.edu/~gsnider/

[23] P. M. Lenahan and J. F. Conley, "A physically based predictive model of Si/SiO_2 interface trap generation resulting from the presence of holes in the SiO_2," *Appl. Phys. Lett.*, vol. 71, no. 21, pp. 3126–3128, Nov. 1997.

[24] C. Z. Zhao and J. F. Zhang, "Effects of hydrogen on positive charges in gate oxides," *J. Appl. Phys.*, vol. 97, no. 7, pp. 073703-1–073703-8, Apr. 2005.

[25] C. Z. Zhao, J. F. Zhang, M. H. Chang, *et al.*, "Stress-induced positive charge in Hf-based gate dielectrics: Impact on device performance and a framework for the defect," *IEEE Trans. Electron Device*, vol. 55, no. 7, pp. 1647–1656, Jul. 2008.

[26] L. Lin, K. Xiong, and J. Robertson, "Atomic structure, electronic structure, and band offsets at Ge:GeO:GeO_2 interfaces," *Appl. Phys. Lett.*, vol. 97, no. 24, pp. 242902-1–242903-3, Dec. 2010.