A Parametric Technique for Traps Characterization in AlGaN/GaN HEMTs

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***Abstract*— A new parametric and cost-effective technique is developed to decouple the mechanisms behind current degradation in AlGaN/GaN HEMTs under a normal device operation: self-heating and charge trapping. Our unique approach investigates charge trapping using both source (I_S) and drain (I_D) transient currents for the first time. Two types of charge trapping mechanisms are identified: (i) bulk charge trapping occurring on a time scale of less than 1 ms, followed by (ii) surface charge trapping with a time constant larger than a millisecond. Through monitoring the difference between I_S and I_D, a bulk charge trapping time constant is found to be independent of both drain (V_{DS}) and gate (V_{GS}) biases. Surface charge trapping is found to have a much greater impact on a slow degradation when compared to bulk trapping and self-heating. At a short timescale (< 1 ms), the RF performance is mainly restricted by both bulk charge trapping and self-heating effects. However, at a longer time (> 1 ms), the dynamic ON resistance degradation is predominantly limited by surface charge trapping.**

***Index Terms*— AlGaN/GaN HEMTs; Transient Currents; Charge Trapping; Self-Heating Effects.**

I. Introduction

GAN based High Electron Mobility Transistors (HEMTs) are predicted to significantly improve efficiency and to dominate power RF applications required to deliver a high-power at a very-fast switching rate in ultra-wide-band communication, ultra-scaled radars, wireless sensors, etc. The transistor efficiency comes from wide-bandgap of III-nitrides, which have high electron saturation velocity and good thermal conductivity [1]. In recent years, these devices were steadily improving and new record performances were reported each year [2], [3]. However, their reliability issues persist due to the strong coupling of charge trapping and self-heating mechanisms [4]–[8].

Several studies investigating the current degradation in AlGaN/GaN HEMTs resulted in different conclusions [6], [9], [10]. Some studies of transient drain current suggest that the current degradation, at different time constants, are caused by both bulk and surface charge trapping [6], [9]. Other investigations suggest that the current degradation trends are proportional to self-heating effects that occur at different times [10]. However, a recent wide agreement is that the transient current degradation involves both device charge trapping and self-heating [11]–[14] at different times. Therefore, the time constants of the transient current need to be investigated since they are of critical consequence to device reliability and RF performance [15]. Consequently, the charge trapping is essential effect entering a design space of circuits [16] because a circuit dynamic operation affects a device operation as accounted for in an MIT virtual source GaN HEMT model [17].

This work reports the development of a parametric technique for bulk and surface charge trapping characterization in AlGaN/GaN HEMTs. The parametric technique is a new, cost-effective and practical technique to acquire essential information about trap dynamics in GaN HEMTs [15], [18]. We show that a careful analysis of both the source and the drain current trends and their differences can distinguish between self-heating effects and trapping mechanisms, and determine short-

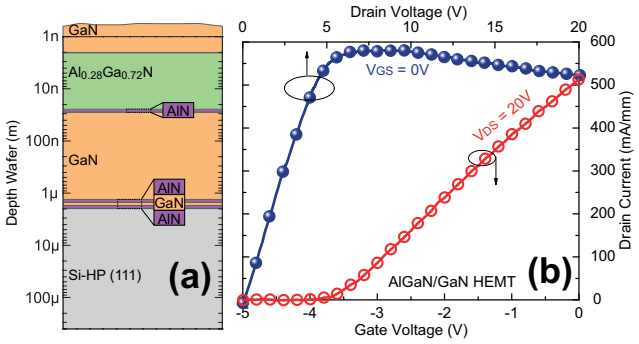

Fig. 1. (a) Schematic cross-section of the device epi-structure grown on a Si-HP (111) substrate. The source-to-drain distance and the gate width are 5 μm and 100 μm, respectively. (b) I_{DS}-V_{DS} and I_{DS}-V_{GS} characteristics at $V_{GS} = 0$ V and $V_{DS} = 20$ V obtained from the $Al_{0.28}Ga_{0.72}N$/GaN HEMT. The threshold voltage (V_{th}) is -3.5 V.

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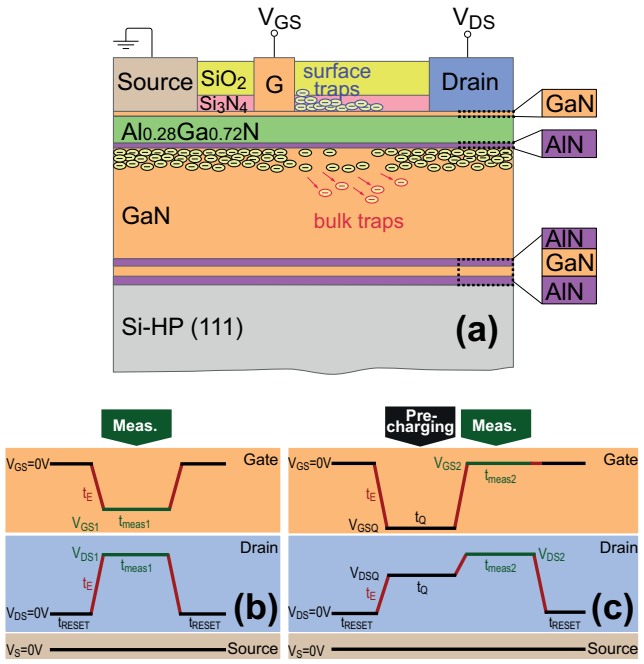

Fig. 2. (a) Illustration of bulk and surface charge trapping mechanisms in the investigated AlGaN/GaN HEMT in a semi-ON state. Pulse waveforms used for measurements of transient source and drain currents, I_S and I_D, are: (b) without traps pre-charging and (c) with traps pre-charging phase. The used refresh/reset time, t_{RESET}, is 10 s and all rising/falling time edges are set to time $t_E = 200$ ns.

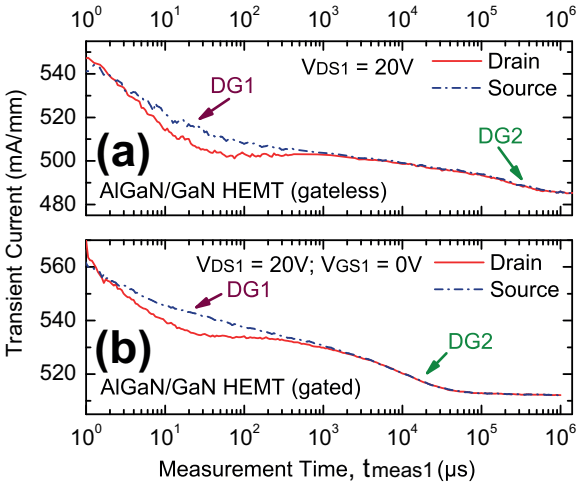

Fig. 3. Transient source and drain currents, I_S and I_D, of (a) a gateless AlGaN/GaN HEMT and (b) a gated AlGaN/GaN HEMT. Very similar degradation mechanisms, one fast (DG1) and one slow (DG2), are observed in both devices. The experimental conditions and the used pulse waveforms are summarized in Fig. 2(b).

time and long-time trapping processes. Specifically, we inspect the degradation of both source and drain transient currents with the exclusion of self-heating and under normal device operation. Section II overviews the used device and experimental procedure. A unique approach that involves both source (I_S) and drain (I_D) currents to investigate the mechanisms behind transient current degradation is presented in Section III. In addition to our previously published results in [7], Section III includes (i) validation of the proposed technique for different AlGaN/GaN device architectures (gated or gateless), (ii) physical interpretations of the experimental observations through drift-diffusion simulations of the used AlGaN/GaN HEMT, and (iii) a comparison between the surface charge trapping and device self-heating effects. Conclusions are drawn in Section IV.

II. Device and Experimental Procedure

A. Device Structure and Fabrication

The epi-structure of the investigated AlGaN/GaN HEMT has been grown by molecular beam epitaxy on high-purity and high-resistivity (2000 Ω.cm) HP-Si (111) substrate. As shown in Fig. 1(a), this epi-structure consists, from the substrate to the top, of low-temperature AlN(40 nm)/GaN(250 nm)/AlN(250 nm) nucleation layers, a 1.1 μm GaN buffer layer, a 1 nm AlN exclusion layer to reduce alloy scattering and to improve the carrier confinement of the 2-dimensional electron gas (2DEG), a 25 nm undoped $Al_{0.28}Ga_{0.72}N$ barrier and, finally, a 1 nm undoped GaN cap layer. The source-to-gate and the gate-to-drain spacers of the HEMT are 1 μm and 3.5 μm, respectively, and the gate length is 0.5 μm. Room temperature Hall measurement yields a sheet resistance of 340 Ω/□, an electron sheet density of 1.25×10^{13} cm^{-2}, an electron mobility of 1480 cm V^{-1}s^{-1}, and a dislocation density of $\sim5\times10^{9}$ cm^{-2}. The gate metallization scheme is Ni(5 nm)/Pt(25 nm)/Ti(25 nm)/Mo(30 nm)/Au(250 nm), where Ti(10 nm)/Al(200 nm)/Ni(40 nm)/Au(100 nm) multilayers have been used for the source/drain terminal. The ohmic contact resistance and specific resistivity are 0.39 Ω.mm and 3.8×10^{-6}Ω·cm^2, respectively. To reduce charge trapping effects and dispersion, the surface of the device is N_2O pre-treated for 2 min followed by SiO_2(100 nm)/Si_3N_4(50 nm) bi-layer passivation. The fabrication process is similar to that described in Ref. [19]. I_{DS}-V_{GS} characteristics of the AlGaN/GaN HEMT at $V_{DS} = 20$ V and I_{DS}-V_{DS} characteristics at $V_{GS} = 0$ V are given in Fig. 1(b). These electrical characteristics are performed at DC and dark conditions using Agilent B1500A framework [7].

B. Experimental Methodology

For the first time, both source and drain transient currents are measured in two experiments to investigate charge trapping in AlGaN/GaN HEMTs under normal device operation as illustrated in Fig. 2(a). The pulse waveforms of the first experiment, schematically shown in Fig. 2(b), are used to characterize the transient current degradation mechanism. Here, the drain voltage $V_{DS} = 0$ V and $V_{GS} = 0$ V are pulsed to V_{DS1} and V_{GS1}, respectively, for a measurement time of $t_{meas1} = 1$ s. The pulse waveforms of the second experiment, illustrated in Fig. 2(c), are similar to the first experiment but involve a pre-charging phase at quiescent biasing conditions, V_{DSQ} and V_{GSQ}, before pulsing to $V_{DS2} = 10$ V and $V_{GS2} = 0$ V, respectively, for a time $t_{meas2} = 1$ s. The corresponding results of these two experiments for particularly used V_{DS1} and V_{GS1} are presented and analyzed in Section III.

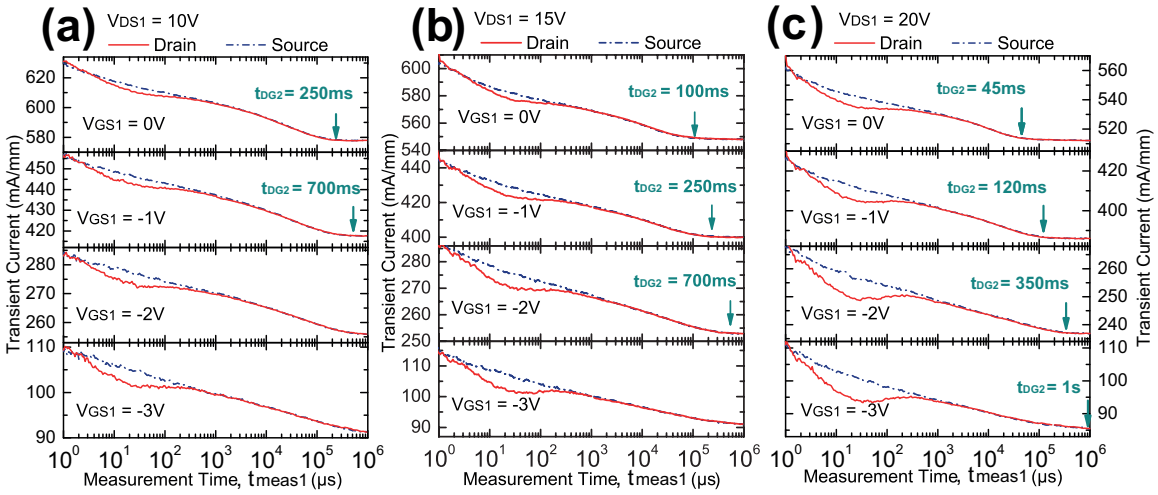

Fig. 4. Transient behaviour of the drain, I_D, and the source, I_S, currents versus the measurement time, t_{meas1}, on log scale using the pulse waveforms given in Fig. 2(b) at V_{GS1} =0 V to -3 V with (a) V_{DS1} = 10 V, (b) V_{DS1} = 15 V, and (c) V_{DS1} = 20 V.

In all experiment, the time to refresh/reset the device is set to $t_{RESET} = 10$ s to recover the device from trapped charges and self-heating that would affect further measurements. All rising/falling time edges are fixed to $t_E = 200$ ns. The trace of the transient current is reproducible revealing that no permanent degradation of the current occurs from the experiment, only recoverable degradation, i.e., charge trapping and self-heating (not shown).

III. Transient Current Degradation

Using the experimental methodology of Fig. 2(b), transient currents at the source (I_S) and at the drain (I_D) are measured on both gated and gateless AlGaN/GaN structures as shown in Figs. 3(a) and 3(b), respectively. Similar trends of degradation phenomena persist regardless of the device architecture, gated or gateless. The transient behaviour of I_S and I_D can be broadly split into two phases, a fast degradation (DG1) for time window shorter than a millisecond, and a slow degradation (DG2) for a longer time (> 1 ms). For the time shorter than 1 ms, the current difference I_S-I_D is always positive in the both gateless and gated devices. This indicates that a difference between I_S and I_D is not caused by the gate terminal. Therefore, the later described analysis of these current transients is not only limited to AlGaN/GaN HEMTs.

In the following subsections, we investigate the mechanisms of DG1 and DG2 under various biasing conditions. Using the same pulse waveforms given in Fig. 2(b), we apply $V_{DS1} =$ 10 V, 15 V and 20 V, and $V_{GS1} = 0$ V to -3 V (step -1 V) to the AlGaN/GaN HEMT. These conditions place the device in a semi−ON state. The transient currents for each gate biasing condition are shown in Fig. 4(a) for $V_{DS1} = 10$ V, and in Fig. 4(b) for $V_{DS1} = 20$ V.

A. Fast Current Degradation - DG1

During the fast current degradation phase, DG1, a significant magnitude of I_S-I_D is observed. Electrons that are injected from the source terminal and get trapped within the bulk, e.g. the GaN buffer, are not collected by the drain terminal, resulting in a difference between I_S and I_D (I_S-$I_D > 0$ mA mm^{-1}). This stems from the applied electric field that provides enough energy for charge carriers to be trapped within the bulk [9]. This fast degradation saturates within the first 100 μs. The self-heating and trapped surface charges do not influence this difference, I_S-I_D, as they degrade both I_S and I_D proportionally [5], [20]. The mechanism behind this fast current degradation has to contribute to the bulk charge trapping and self-heating.

Due to applied electric field between the gate and the drain, charge carriers can be trapped at the surface of the device where dangling bonds create surface states, as illustrated in Fig. 2(a). As the surface charge trapping occurs within a short period, typically within the first microsecond [21], its contribution towards the DG1 is difficult to distinguish from self-heating.

To analyse the dependence of the bulk charge trapping on drain and gate voltages, Fig. 5(a) shows the current difference of I_S-I_D values with respect to the measurement time. From these measurements, one can deduce that the time constant, t_{DG1}, of the DG1 is independent of biasing conditions. This suggests that the rate/speed of bulk charge trapping does not change as this is dependent of the density of threading dislocations and defects [9].

The magnitude of the current drop due to trapped bulk charges, I_S-I_D value, taken from Fig. 5(a) at measurement time ($t_{meas1} \approx 35$ μs), is plotted against each drain and gate biasing condition in Fig. 5(b). We observe an increase of bulk charge trapping with respect to the drain voltage, V_{DS1}. Increasing the drain bias, V_{DS1}, provides more kinetic energy to carriers to reach deeper traps in the access region that results in an increase of the bulk trapping. The gate bias V_{GS1} has, however, insignificant impact on the bulk charge trapping. Further experiments are given in Section III-C to investigate the relationship between the bias conditions and the bulk charge trapping.

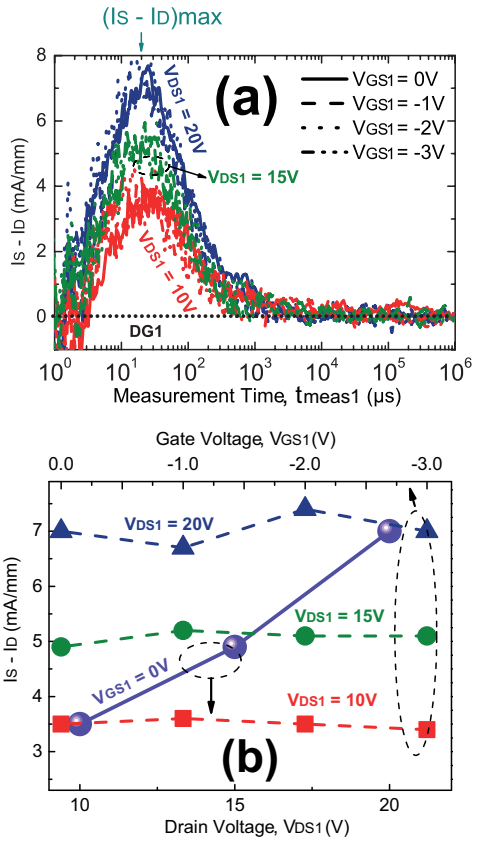

Fig. 5. (a) I_S and I_D difference (I_S-I_D) versus the measurement time, t_{meas1}, at V_{DS1} = **10** V, **15** V and **20** V for different gate voltages (V_{GS1} = **−3** V to **0** V); indicating the bulk charge trapping process (DG1). The DG1 time constant is independent of both drain and gate biases. (b) The impact of drain voltage, V_{DS1}, and gate voltage, V_{GS1}, on I_S-I_D showing a dependence of the bulk trapped charge density and V_{DS1}. Unlike V_{DS1}, V_{GS1} has a negligible impact on bulk trapping characteristics.

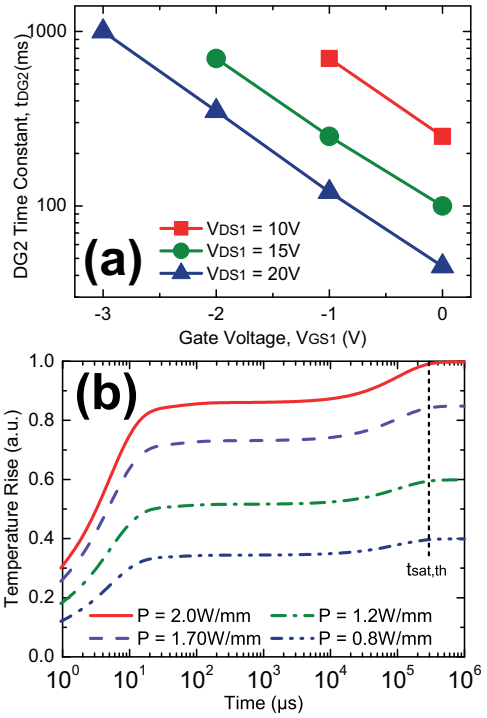

Fig. 6. (a) Time constant of DG2, t_{DG2}, at V_{DS1} = **10** V, **15** V, and **20** V and V_{GS1} = **−3** V to **0** V; revealing the dependence of t_{DG2} on both drain and gate voltages. (b) Transient heating characteristics at various power densities (P) using the RC thermal model [10], [25]. Note that $t_{sat,th}$ is temperature independent.

B. Slow Current Degradation - DG2

Throughout the slow current degradation phase, DG2, current begins to diminish a second time, after the saturation of DG1 and the first phase of self-heating. A negligible I_S-I_D magnitude is observed indicating an insignificant bulk charge trapping in this phase of the DG2. Unlike bulk charge trapping, where I_S-$I_D > 0$ mA mm^{-1}, the surface charge trapping and self-heating alter the electrostatic integrity and channel resistance in the device. As a result, both source and drain currents degrade proportionally (I_S-$I_D = 0$ mA mm^{-1}).

We extracted the time constant of DG2 (t_{DG2}) from Fig. 4 and presented it in Fig. 6(a) with respect to both drain and gate biasing conditions. The increase of V_{GS1} induces a greater surface trapping density, leading to a larger time for the surface charges to redistribute between gate and drain terminals. However, the required time to redistribute the trapped charges at the surface and to extend the 'virtual gate' towards the drain side reduces with increased V_{DS1}. A larger drain voltage induces a higher electric field and, therefore, distributes surface charges more quickly [22]. The extracted t_{DG2} corresponds with that of other works [23], [24].

In contrast to the time constant of DG1, t_{DG2} is both drain and gate bias dependent. The slow degradation of DG2 can also be coupled with a possible second phase of self-heating. Evidence of this second phase of self-heating comes from the RC thermal model shown in Fig. 6(b) [10], [25]. We observe that the time constant of this second transient heating ($t_{sat,th}$) is independent of the applied power. Therefore, the surface trapping is the cause of t_{DG2} variation.

The pulse waveforms given in Fig. 2(c) are used to investigate the dominant degradation mechanism of the DG2. Pre-charging quiescent conditions, V_{DSQ} =10 V and V_{GSQ} = −10 V, −8 V, −5 V, −3 V, and −1 V, are set at pre-charging times t_Q = 1 μs, 10 ms, and 1 s. After the device is pre-charged, the transient current measurements are taken at V_{DS2} =10 V and V_{GS2} =0 V for a time of $t_{meas,2}$ from 1 μs to 1 s. The corresponding results of this experiment are shown in Fig. 7.

During the pre-charging phase, surface charge trapping and distribution occur and are controlled by V_{GSQ} and V_{DSQ}. No device self-heating effects can take place when the device is OFF ($V_{GSQ} < V_{th}$). However, when the device is in a semi−ON state ($V_{GSQ} > V_{th}$), a self-heating will occur in addition to the bulk charge trapping due to a high V_{DSQ} of 10 V.

Through the measurement phase, the trapped surface charges begin to re-distribute in the opposite manner to the pre-charging conditions and surface trapping density reduces. This is the consequence of the decreased magnitude of gate voltage from the quiescent to the measurement condition. Self-heating increases as the device is switched from the OFF/semi−ON state to the ON−state. For all quiescent bias conditions where

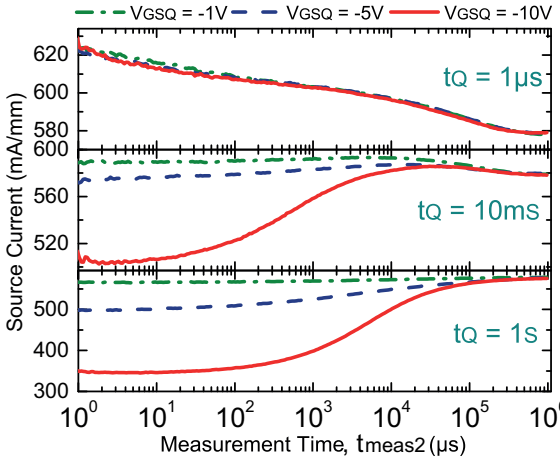

Fig. 7. Transient behaviour of the source current, I_S, versus the measurement time, t_{meas2}, using the pulse waveforms given in Fig. 2(c) with V_{DSQ} =V_{DS2} =10 V, V_{GSQ} =-1 V, -5 V, and -10 V, and V_{GS2} =0 V. The effect of current recovery is shown to increase with greater $|V_{GSQ}|$ and t_Q due to a greater surface trapping density and re-distribution.

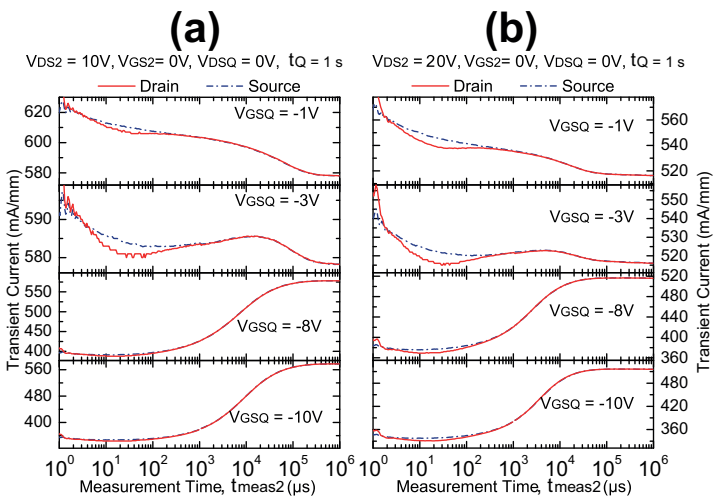

Fig. 8. Transient behaviour of the drain, I_D, and the source, I_S, currents, versus the measurement time, t_{meas2}, on log scale using the pulse waveforms given in Fig. 2(c) at different pre-charging conditions (V_{DSQ} =0 V; V_{GSQ} = -1 V, -3 V, -8 V, and -10 V; t_Q = 1 s) with (a) V_{DS2} = 10 V; V_{GS2} = 0 V and (b) V_{DS2} = 20 V; V_{GS2} =0 V. The bulk trapping has a minimal impact on the recovery of current degradation when pre-charging conditions set the device to the OFF-state; $|V_{GSQ}| > V_{th}$.

$t_Q > 1$ ms, bulk charge trapping is saturated during the pre-charging phase at the same amount as found in Section III.A and no further bulk trapping takes place in the measurement phase. The behaviour of transient current is analyzed for each pre-charging condition:

- $t_Q = 1$ μs - For all V_{GSQ}, negligible surface/bulk charge trapping and self-heating are induced during the pre-charging condition because of short pre-charging time. As a result, no recovery of surface trapping occurs during the measurement. Instead, bulk trapping, self-heating, and surface trapping degrade the current. Therefore, the transient current behaviour is similar to that of Fig. 4(a) at V_{GS1} =0 V.
- t_Q = 10 ms - During the pre-charging phase, surface charge trapping/distribution and complete bulk charge trapping occur. No self-heating is induced during the pre-charging for V_{GSQ} =-5 V and -10 V. As a result, the primary cause of the degraded current at $t_{meas,2}$ =1 μs is the surface and bulk charge trapping. This initial degradation increases with larger $|V_{GSQ}|$ as a larger surface charge density is trapped/distributed. A recovery of the current is then observed during measurement from $\sim$ 10 μs to $\sim$ 40 ms at V_{GSQ} =-1 V to -10 V, respectively. This shows that the surface trapping recovery has a greater impact on current behaviour than the degradation of the current due to self-heating. Since the time t_Q = 10 ms is not sufficiently long to complete the surface trapping process during the pre-charging phase, as observed in Fig. 4(a), the surface trapping recovery ends before the current degradation is complete during the measurement phase. Hence, a degradation of the current is observed beyond $\sim$ 40 ms as the result of self-heating effects.
- t_Q = 1 s - Pre-charging of surface traps is complete and at a larger magnitude. The current recovers throughout the entire measurement window. A large recovery of the current is observed due to the dominance of a recovery from the surface traps over a recovery from self-heating.

Fig. 7 illustrates that, at $t_Q \geq 10$ ms, two mechanisms of transient current develop when reducing the gate voltage from $|V_{GSQ}|$ to $|V_{GS2}|$: (i) a recovery of surface trapping redistribution whereby a 'virtual gate' length is reduced, lowering the channel resistance and recovering the current, and (ii) a self-heating that increases the channel resistance and degrades the current.

C. Bulk charge trapping versus bias conditions

In this subsection, we investigate the relationship between the bulk charge trapping and the bias conditions. Contrary to the previous experiment of Fig. 7, the bulk charge trapping is excluded from the pre-charging phase whilst maintaining the surface trapping throughout the pre-charging. To achieve this, V_{DSQ} =0 V is used (Fig. 2(c)). The other pre-charging

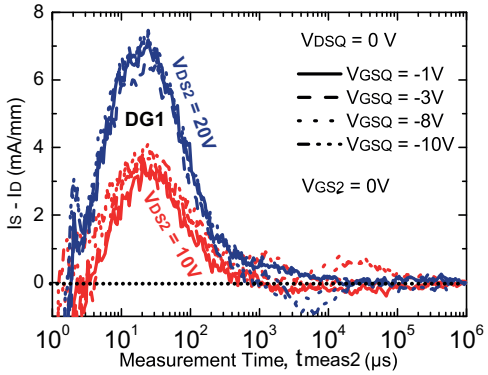

Fig. 9. I_S and I_D difference (I_S-I_D) versus the measurement time at a gate voltage V_{GS2} = -1 V and two drain voltages (V_{DS2} = 10 V and 20 V) showing that charge carrier trapping in the bulk is negligible during pre-charging phase when compared with Fig. 5(a).

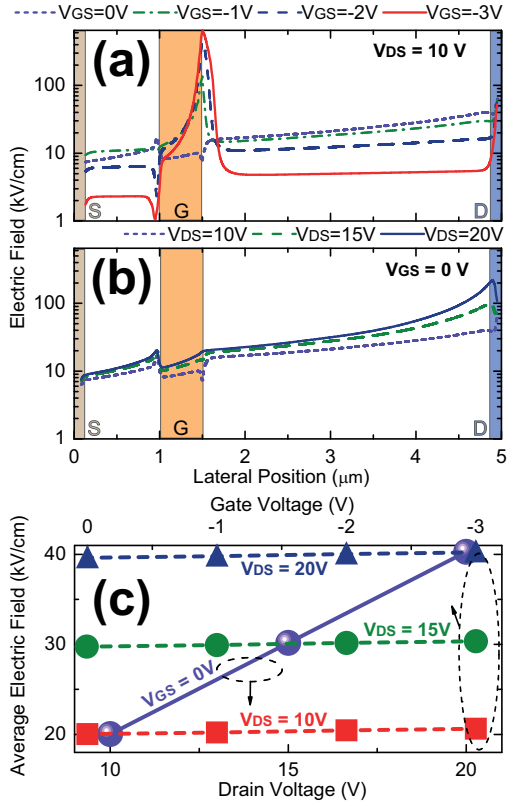

Fig. 10. Drift-diffusion simulation of electric field distributions in the channel of the AlGaN/GaN HEMT: (a) at $V_{DS} = 10$ V and different V_{GS} and (b) at $V_{GS} = 0$ V and different V_{DS}. (c) Comparison of the average overall electric field along the channel at different bias conditions showing a negligible impact of the gate voltage on the average overall electric field.

conditions are V_{GSQ} =-1 V, -3 V, -8 V and -10 V for t_Q =1 s. The measurement settings are V_{GS2} =0 V and $t_{meas,2}$ =1 s with different drain voltages of V_{DS2} =10 V and 20 V, as shown in Fig. 8(a) and Fig. 8(b), respectively. The difference between I_S and I_D is extracted from Fig. 8 and presented in Fig. 9 showing near identical characteristics to those in Fig. 5(a). These nearly identical characteristics confirm that (i) no bulk trapping had taken place during the pre-charging at V_{DSQ} =0 V and (ii) bulk trapping rate is not affected by the gate bias during the ON and OFF states of the devices, only by the drain voltage.

The electric field distribution along the channel is extracted from drift-diffusion simulations at the AlN/GaN interface of the device, described in Section II.A, at different V_{GS} and V_{DS} bias conditions. At a constant V_{DS}, the increase of the electric field with V_{GS} at the drain edge of the gate is related to a drop of the field in the access region as shown in Fig. 10(a) while, at a constant V_{GS}, the electric field increases with V_{DS} in the whole channel (Fig. 10(b)). The distribution of the electric field presented in Fig. 10(a) indicates that more charge trapping occurs at the drain side of the gate edge at $V_{GS} = -3$ V comparing to $V_{GS} = -1$ V. This is because the electric field is larger at more negative gate voltages. However, away from the gate edge towards the drain side, the electric field is different. At $V_{GS} = -1$ V, the electric is higher than at $V_{GS} = -3$ V. Therefore, to relate the increase in the difference between the source and the drain currents with the increase of drain bias shown in Fig. 5(b), and thus to assess the effect of the overall trapping processes along the whole channel, not just in a particular area of the device, we have calculated the overall electric field for all bias conditions by averaging the electric field along the transistor channel as shown in Fig. 10(c). The figure illustrates that the increase in V_{DS} at a fixed V_{GS} increases the average overall electric field linearly (the bottom scale of Fig. 10(c)), while the decrease in V_{GS} at a fixed V_{DS} keeps the overall electric field practically constant (the top scale of Fig. 10(c)) [26]. The dependence of the average overall electric field on the drain and gate biases presented in Fig. 10(c) is thus in a good correlation with the dependence of experimental data in Fig. 5(b).

The details of the used device simulation technique can be found in [4], [5], [27]–[30]. In the past, this simulation technique has been successfully used to predict performance of AlGaN/GaN HEMTs grown on various substrates (i.e., Si, 4H-SiC, diamond, sapphire). The transport parameters such as electron drift velocity, energy relaxation time, and electron effective mass are obtained from Monte Carlo simulations at different lattice temperatures [30]. Both simulated I-V characteristics and calculated temperatures have been compared to experimental I-V characteristics and temperature measurements, demonstrating a good agreement [5], [27]–[29]. This simulation technique has been adapted for both gated and gateless AlGaN/GaN HEMTs.

IV. Conclusions

A new source and drain transient currents (I_S and I_D) technique for a charge trapping characterization in AlGaN/GaN HEMTs, under normal device operation, has been developed. This proposed technique takes into account the device operating temperature variation during the transient measurements, a cost-effective complement to the temperature-dependent current-transient based techniques [6], [9], [23], [31]–[34]. It can be easily implemented to decouple the slow bulk charge traps and the surface traps from self-heating effects without turning to device simulations or to more complicated measurements. Using this technique, charge trapping behaviour with the exclusion of self-heating has been analyzed. Two types of charge trapping mechanisms have been identified: (i) a bulk charge trapping occurring on a time scale of less than 1 ms, followed by (ii) a surface charge trapping and distribution beyond 1 ms. The bulk trapping and the surface trapping corresponds to the primary fast and slow current degradation mechanisms, respectively.

Through monitoring the difference between I_S and I_D, the bulk charge trapping time constant is shown to be independent of both V_{DS} and V_{GS}, although, V_{DS} is found to affect the bulk trap density. Large V_{DS} is found to be a cause of the bulk charge trapping during both the ON and the semi-ON states of the device. The surface trapping is found to have a much larger impact on the slow degradation of the current when compared to the self-heating and the bulk charge trapping in the investigated device structures. This is an important step to

understand the priority of the device engineering, whereby the focus should be aimed towards reducing the surface trapping in order to improve an RF performance and a dynamic ON resistance [8].

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