Defect loss and its physical processes

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Abstract
Defects in MOSFETs generally have adverse effects on device performance: they increase the threshold voltage, reduce the driving current, and in turn, lower the operation speed. Early works focus on the charging and discharging of defects and their impact on device lifetime. There is little information on the stability of defects themselves, i.e., whether a defect can be lost. The objective of this work is to demonstrate that defects indeed can be lost and to investigate which type of defects are lost and the physical processes for the defect loss. It is found that the losses originate from the generated interface states and anti-neutralization positive charges. The loss is a thermally activated process and it is speculated that the depletion of hydrogen species from the device could lead to the loss.

1. Introduction
Instability of MOSFETs is a key issue for CMOS technologies and it originates from defects either in gate dielectric or at the dielectric/substrate interface [1-6]. There are two classes of defects: As-grown traps and Generated defects [7,8]. The number of as-grown traps are fixed in a device and they impact device operation through charging and discharging [7,8]. The number of generated defects increase with stress time by following a power law and eventually leads to devices reaching their lifetime [7,8]. Although the impact of defects on devices is general harmful, recent works also make a good use of it in systems such as True Random Number Generators [9].

Early works [1-9] focused on either the charging-discharging of as-grown traps or the physical process of generating new traps. The question is whether defect themselves are stable or some of them can be lost [10,11]. As there is little information on the potential defect loss, this work researches into it. We will first demonstrate the defect loss and distinguish it from the well-known recovery phenomenon. We will then explore which types of defects are responsible for the loss. Finally, the physical processes of defect loss are investigated.

2. Defect losses
Fig. 1 shows a typical result of negative bias temperature instability. When a pMOSFET is under a negative gate bias at elevated temperature, positive charges build up and increase the magnitude of threshold voltage. Once the stress gate bias is removed, the degradation partially recovers. This recovery is caused by the re-neutralization/discharge of defects, rather than defect losses. When the stress is resumed, the neutralized defects are recharged and the degradation at the end of the second stress is higher than that at the end of the first stress, as shown in Fig. 1.

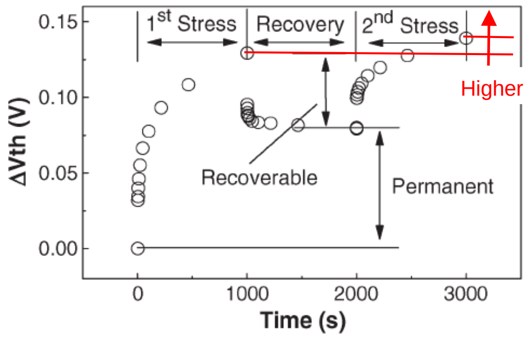

Fig. 1. Typical NBTI results under Vg=-2.5V. The recovery was under Vg=0. Without defect losses, the degradation at the end of second stress is higher than that at the end of 1st stress. [10].

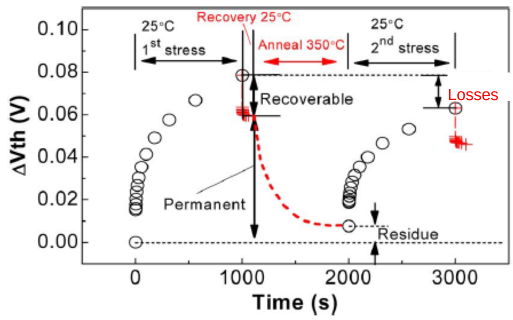

Fig. 2. After the first stress and a short recovery at 25°C, the device was subjected to 350°C (dashed curves) before resuming the stress. The lower of degradation at the end of second stress is caused by defect losses. [11].

In Fig. 2, after the first stress and a short recovery under 25 °C, the temperature was raised to 350 °C with gate floating. It is clearly that higher temperature accelerates the recovery process. What should be emphasized is that, when the stress is resumed, the degradation at the end of second stress becomes lower than that at the end of first stress, which is in contrast with the increase at the end of second stress. As the threshold voltage of fresh device is used as the reference throughout the test, a lower degradation at the end of second stress is caused by defect losses.

In Fig. 2, the time for the second stress is the same as that for the first stress. The question is whether the lost defects can be reactivated by increasing stress time. To test this, we increase the stress time in Fig. 3a. One device was stressed continuously for a long time and the other was subjected to short stress-250ºC cycles a number of time before the long time stress. Fig. 3b compares the two long time stresses with and without the 250ºC steps. Although the ΔVth with the high temperature step is higher initially due to the residual degradation at the end of the high temperature step, the two curves cross over as stress time increases. Fig. 3c shows that the difference between the two curves in Fig. 3b saturates for long stress time. This result confirms that, once a defect is lost, it cannot be reactivated even by using long stresses, so that the loss is real.

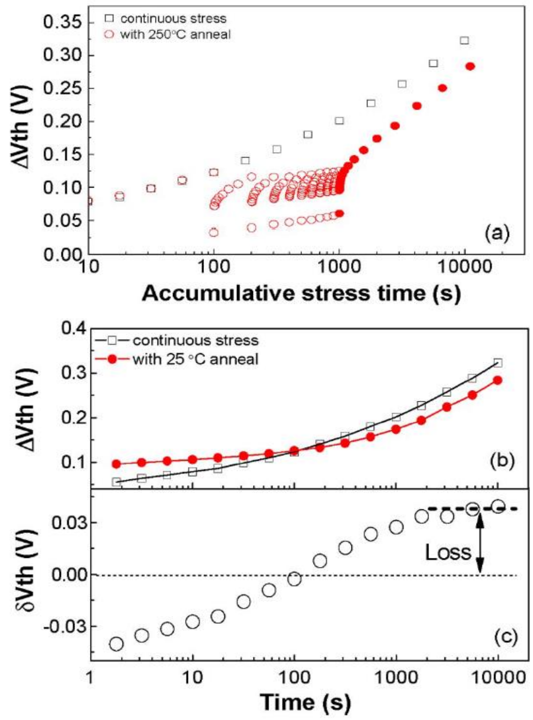

Fig. 3. A comparison of long term degradation with and without defect losses. The '□' is the results of continuous stress without the high temperature step. The '•' is the results by cycling the stress-250ºC many times before the long stress. In (a), the time under 250ºC was removed and accumulative stress time was used. In (b), the time was reset to zero at the start of the long stress. (c) is the difference between the two curves in (b). [11].

3. Defects responsible for the loss

According to the As-grown-Generation (AG) model, defects in MOSFETs can be divided into As-grown traps and Generated defects (GD) [12,13]. As-grown hole traps (AHT) have energy levels below the top edge of Si valance band, Ev, as shown in Fig. 4a. Fig. 4b shows that they can be easily neutralized and contribute to the recoverable components of NBTI. Some of the generated defects are within the Si bandgap and they can be repeatedly charged and discharged by alternating the gate bias polarity. They are referred to Cyclic positive charges (CPC), as marked out in Fig. 4b. CPC also contributes to the recoverable component of NBTI. Some of the generated defect are difficult to neutralize and remain charged at the end of Vg>0 discharge period, because they have highly energy levels. They are called as anti-neutralization positive charges (ANPC).

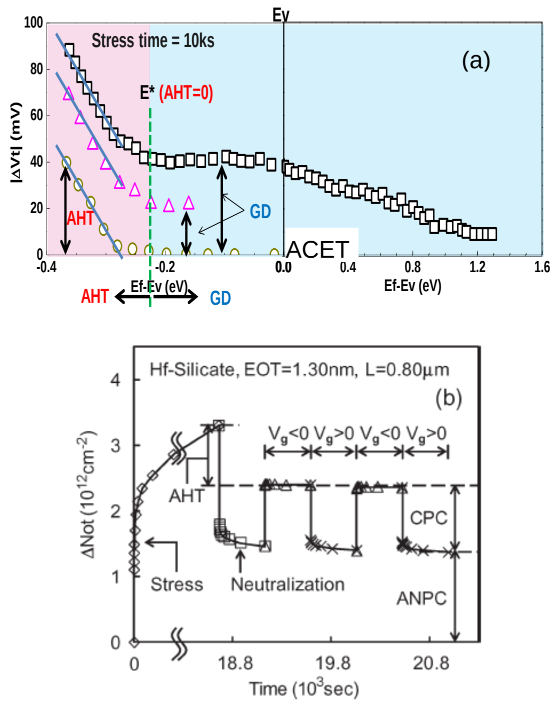

Fig. 4. (a) The energy profile of the as-grown hole traps (AHT) and generated defects (GD). (b) The charging-discharging characteristics of AHT, cyclic positive charge (CPC) and Anti-Neutralization positive charges (ANPC). Both CPC and ANPC are the generated defects. [12,13].

Fig. 2 shows that before and after the defect loss, the recoverable component changes little. Fig. 5a confirms that the As-grown hole traps and the CPC contributes little to the losses. The ANPC, on the other hand, clearly reduces after the loss. This reduction of ANPC are partially responsible for the loss, therefore.

The ANPC is the positive charges in the gate dielectric. In addition to it, positive charges can also come from the generated interface states. Fig. 5b clearly shows that the loss of generated interface states.

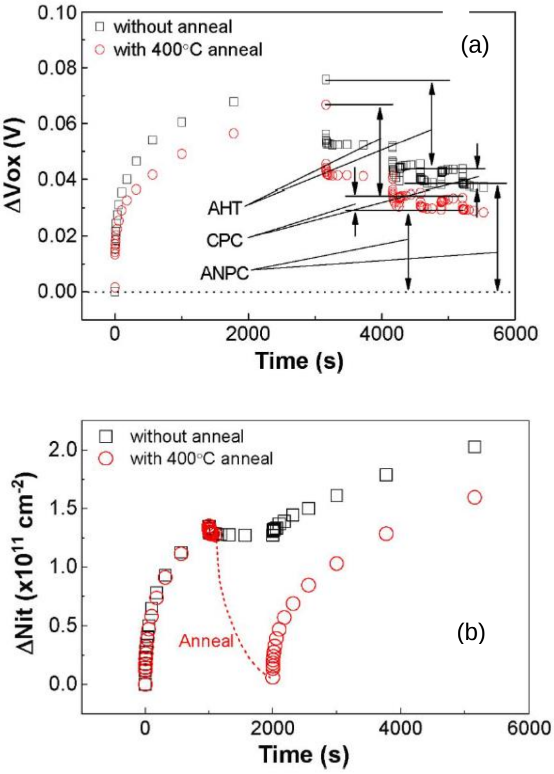

Fig. 5. (a) The AHT and CPC change little after defect losses, but ANPC reduces clearly after defect losses. (b) The generated interface states clearly reduces after defect losses. [11]. The interface states were measured by charge pumping technique.

4. Physical processes responsible for the loss

The first question to be answered is whether the defect loss depends on the charge status of the defect. A defect can be either neutral or charged. To explore if defects can be lost when they are neutral, we exposed a fresh device to 350ºC, as defects are neutral in a fresh device. Fig. 6 compares the defect losses with or without such a pre-stress 350ºC exposure. It is clear that such an exposure does not affect the loss. As a result, exposing neutral defects to 350ºC does not lead to losses. Defects must be charged first before the loss can occur.

The effect of temperature on the loss is further investigated. Fig. 7 compares the losses after different temperature exposure. The loss increases for higher temperature, so that the loss is a thermally activated process.

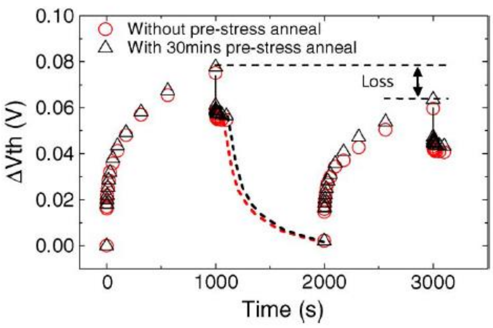

Fig. 6. A comparison of defect losses with and without exposing the fresh devices to 350ºC pre-stress. [10].

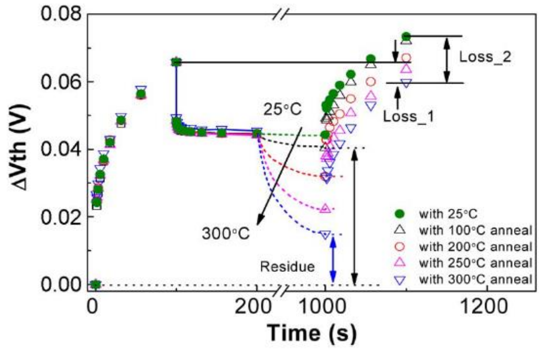

Fig. 7. The thermal activation of defect losses. [11].

It is well known that hydrogenous species plays a key role in device instability [14-17] and it is possible that it also play a role in defect loss. As a speculation, the defect may have a hydrogen bond and its charging process can be shown in the reaction (1):

$$\text{D-H} + \text{hole} \rightarrow \text{D-H}^+. \qquad (1)$$

After charging, the hydrogen bond can be weakened. Under elevated temperature, the hydrogen bond can be broken and the hydrogenous species can be driven out of the device, as shown in the reaction (2). This results in the loss.

$$\text{D-H}^+ \overset{\text{High Temp.}}{\rightleftharpoons} \text{D} + \text{H}^+. \qquad (2)$$

To support the above speculation, we compare the devices exposed to H_2 and N_2 after stresses. In Fig. 8, the devices were first charged and then exposed to 400ºC. This charge-exposure sequence were cycled several times. When the exposure was in H_2, there were no losses. The losses can be clearly seen, however, when the exposure was in N_2. Once the hydrogenous species in the reaction (2) is lost, it can be supplied in H_2, but not in N_2.

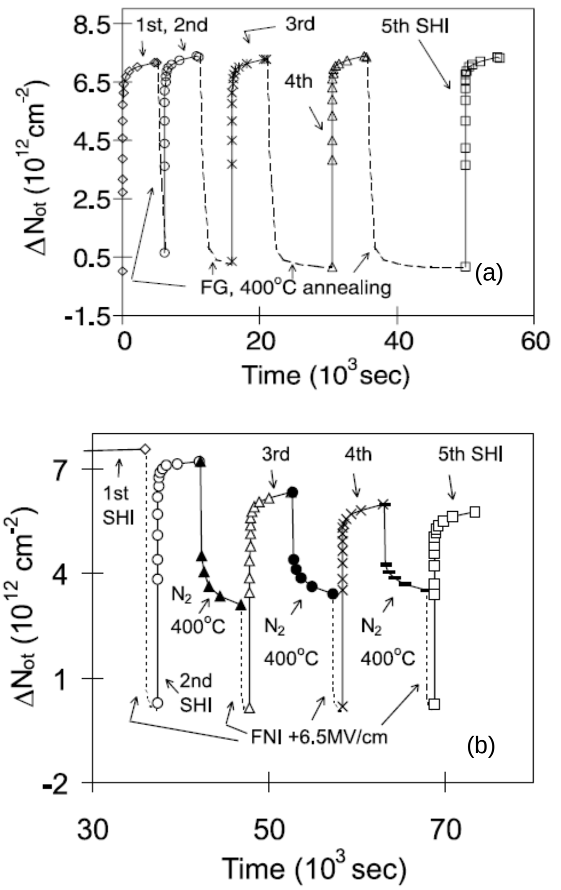

Fig. 8. Impact of cycling stress-400^{o}C exposure on defect losses. The exposure is in forming gas (5% H_2) (a) and in N_2 (b). [14].

5. Summary

The defects in MOSFETs are not permanent and this work investigates their losses. Unlike the neutralization-induced recovery where the same defects can be recharged, once a defect is lost, it will not contribute to device degradation in the subsequent stress. The loss only occurs after the defect is charged and it is a thermally activated process. It originates from the generated interface states and anti-neutralization positive charges, while as-grown hole traps and cyclic positive charges contribute little to it. It is speculated that the loss is caused by the depletion of hydrogenous species from the device.

Acknowledgments

The authors would like to thank IMEC for supplying the test samples. This work is supported by the EPSRC of UK under the grant no. EP/L010607/1.

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