Giant Ferroelectric Resistance Switching Controlled by a Modulatory Terminal for Low-Power Neuromorphic In-Memory Computing

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Ferroelectrics have been demonstrated as excellent building blocks for high-performance nonvolatile memories, including memristors, which play critical roles in the hardware implementation of artificial synapses and in-memory computing. Here, it is reported that the emerging van der Waals ferroelectric α-In$_2$Se$_3$ can be used to successfully implement heterosynaptic plasticity (a fundamental but rarely emulated synaptic form) and achieve a resistance-switching ratio of heterosynaptic memristors above 10^3, which is two orders of magnitude larger than that in other similar devices. The polarization change of ferroelectric α-In$_2$Se$_3$ channel is responsible for the resistance switching at various paired terminals. The third terminal of α-In$_2$Se$_3$ memristors exhibits nonvolatile control over channel current at a picoampere level, endowing the devices with picojoule read-energy consumption to emulate the associative heterosynaptic learning. The simulation proves that both supervised and unsupervised learning manners can be implemented in α-In$_2$Se$_3$ neutral networks with high image recognition accuracy. Moreover, these heterosynaptic devices can naturally realize Boolean logic without an additional circuit component. The results suggest that van der Waals ferroelectrics hold great potential for applications in complex, energy-efficient, brain-inspired computing systems and logic-in-memory computers.

1. Introduction

Device scaling in Si-based integrated circuits has slowed due to the approaching physical limit, leading to difficulties in the extension of Moore's Law.[1] Neuromorphic computing, a brain-inspired model for mimicking the neurobiological architecture, could not only help to significantly extend Moore's law, but also overcome the limitation of the data transfer rate between the storage unit and the processing unit in modern von Neumann computers.[2] Toward this aim, researchers have conducted significant efforts to develop solid-state devices, including nonvolatile memristors, to emulate biological synaptic behaviors.[2–9]

Synaptic plasticity, i.e., the ability of a synapse to adapt its connection strength upon neural stimuli, is believed to actually possess two basic forms: homosynaptic (associated with two neuron terminals) and heterosynaptic plasticity (featuring

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three neuron terminals).[10] Most previous studies have focused on emulating homosynaptic plasticity.[2–9,11] However, the development of electronic heterosynaptic plasticity can not only promote the compact design of memristor monolithic integration, but also greatly optimize the learning scheme of integrated neural network.[7] At present, only a few reports have attempted to implement heterosynaptic functionality in solid-state devices. Nevertheless, tuning the synaptic conductance via the modulatory terminal has produced an on/off ratio of just ≈10 in the current state-of-the-art heterosynaptic device,[12] which is too small to satisfy the requirements of multilevel brain-inspired computing. Therefore, the enhancement of the on/off performance of such devices is critically important for the development of this field.

A nonvolatile heterosynaptic device with multiple terminal inputs could also be combined with in-memory computing, which conceptually unites data storage and processing in a single nonvolatile device. In-memory computing is also a promising route for tackling the bottleneck of von Neumann computers and enabling Moore's law to proceed.[13] This logic-in-memory concept was first demonstrated in parallel-connected memristors based on a TiO_2 thin film.[14] Unfortunately, the Boolean logic of this design, such as the universal NAND gate, is typically synthesized through two logic cycles/steps (besides the initialization process), which inevitably sacrifices logic operation efficiency. Integrating in-memory computing with the multiterminal design of heterosynaptic devices could be one approach to realize the Boolean logic with a single logic cycle.

Toward this aim, ferroelectric materials are considered excellent building blocks for nonvolatile resistance switching memories that could be adopted for neuromorphic in-memory computing systems. Ferroelectric materials can retain electrically aligned polarization states and achieve continuous resistance switching through an applied electric field.[15] However, the most widely used ceramic ferroelectrics feature low conductivity and are commonly configured in a vertically sandwiched two-terminal memory design to enhance the device conductivity via the tunneling effect,[15,16] which limits complex computation requiring three or more terminals. Fortunately, van der Waals ferroelectrics,[17–20] which offer a 2D planar geometry without dangling bonds across the surface, can facilitate a multiterminal design. Among these ferroelectrics, the layered α-In_2Se_3 semiconductor, which can hold stable ferroelectricity down to the monolayer limit as well as excellent conductivity, has received considerable interest.[17,19,20]

Here, we report an approach (i.e., ferroelectric switching) to increase the on/off ratio of heterosynaptic devices to over 10^3 by using the van der Waals semiconducting ferroelectric α-In_2Se_3. Our approach enables heterosynaptic devices with low operation energy consumption, excellent endurance, and long-term retention (see Table S1 in the Supporting Information for comparison). Using α-In_2Se_3 devices, convolutional neural

network (CNN) and spiking neural network can be simulated to fulfill supervised and unsupervised learning, respectively. Our multiterminal heterosynaptic devices can achieve the 3D integration with much simpler control strategy and circuit topology. Additionally, the demonstrated logic operations for OR and NOR gates in the α-In_2Se_3 memristors only require a single logic cycle, providing a route for devising high-efficient neuromorphic in-memory devices.

2. Device Architecture and Current Switching

We exfoliated hexagonal α-In_2Se_3 nanoflakes (see Figure S1 in the Supporting Information for the Raman spectrum) onto silicon wafers with a 300 nm thick oxide layer to fabricate the multiterminal memristors (**Figure 1**a). Because of the unique in-plane (IP) and out-of-plane (OOP) structural asymmetries,[20] ferroelectric polarization in the α-In_2Se_3 nanoflakes can be toggled by an electric field along any direction, which provides a degree of freedom for the flexible design of the planar position of the memristor electrodes. The bottom-left panel in Figure 1a shows an atomic force microscopy (AFM) image of a typical six-terminal memristor with an α-In_2Se_3 thickness of 36 nm. The fabricated terminals were labeled as T1, T2, T3, T4, T5, and T6. In order to confirm the ferroelectricity in the α-In_2Se_3 nanoflake, Figure 1b presents the OOP single-point piezoelectric force microscopy (PFM) spectroscopy, which demonstrates a large piezoresponse switching loop—a signature of ferroelectrics.[17]

In Figure 1c–e and Figure S2a in the Supporting Information, we plot the pinched hysteresis loops from various terminals, with the black arrows showing the switching direction. Upon increasing the maximum sweep voltage, the hysteric window incrementally expands, resulting in increased current switching. The evolution of the hysteric window from a closed state for the ±0.5 V sweep (Figure S2b,c, Supporting Information) to an open state for the ±2.0 V sweep (Figure 1c,d) indicates there is a threshold voltage for opening the memristive phenomena in the α-In_2Se_3 device. In principle, this threshold located in the range of 0.5 to 2.0 V should correspond to the IP ferroelectric coercive voltage. When the sweep voltage is over 4.0 V, the ferroelectric polarization in the device channel can be fully reversed, which is evidenced from the saturation effect of the ±5.0 V sweep in Figure 1c and Figure S2a in the Supporting Information. The asymmetric I–V curves in Figure 1c–e likely arise from the differences in contact area between the electrode Au/Ti and semiconductor α-In_2Se_3, and in residues at their interfaces during device fabrication. The 8-shaped switching under 2 and 4 V sweep in Figure 1d is attributed to the residue charges that make the current-state transition occur beyond the coordinate origin. Moreover, based on Kolmogorov–Avrami–Ishibashi (KAI) theory, we established a ferroelectric memristor model for our α-In_2Se_3 devices (see the Experimental Section). To examine this model, the smooth switching loops in Figure 1d were chosen and simulated as shown in gray in Figure 1d and Figure S3 in the Supporting Information. The perfect overlap verifies that the domain propagation intrinsically dominates resistance switching in α-In_2Se_3 devices (see Figure 3 for more details). Additionally, the reproducibility of pinched hysteresis loops is also demonstrated in Figure S4 in the Supporting Information, suggesting the

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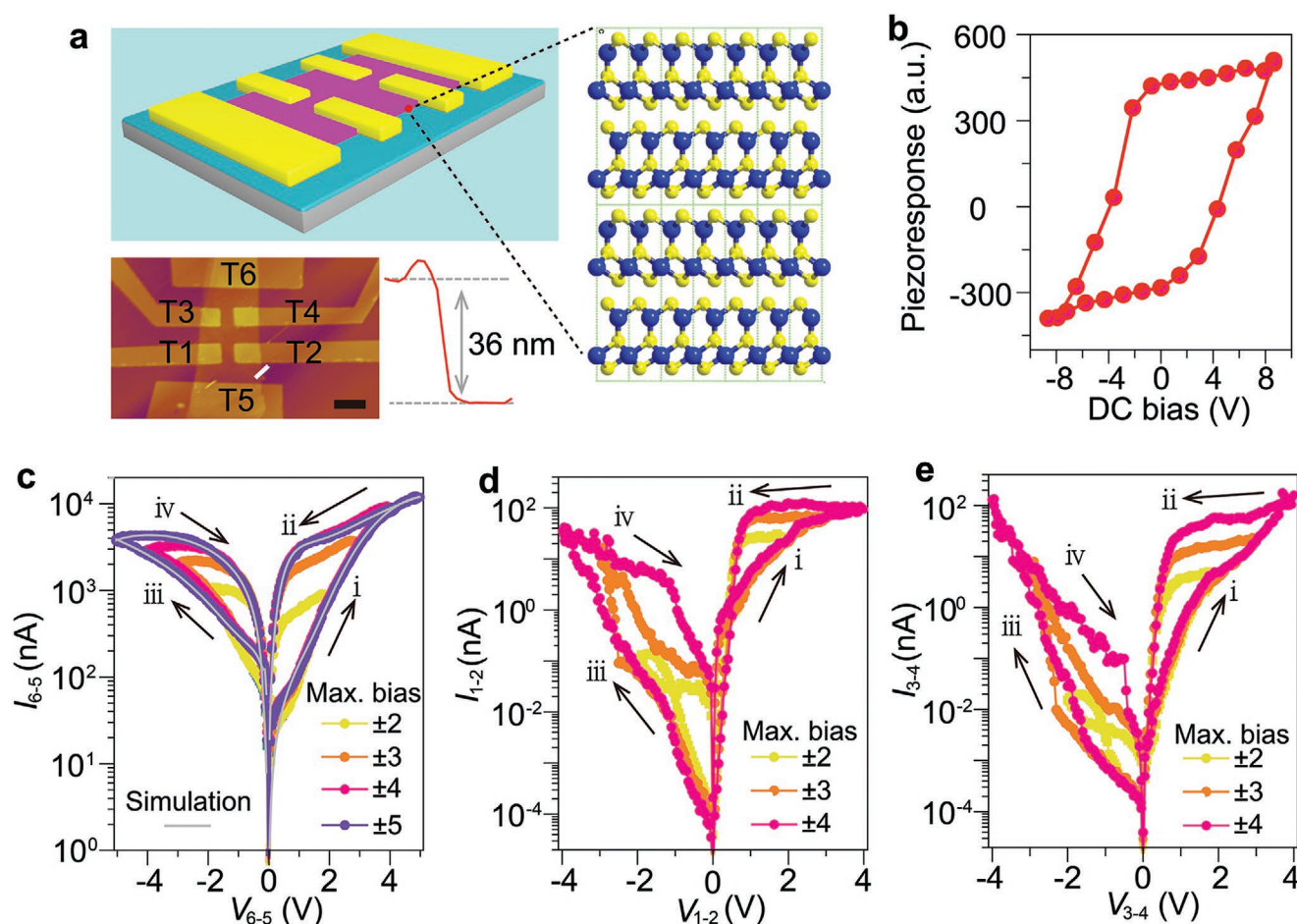Kowloon, Hong Kong, China

Figure 1. Architecture of the van der Waals ferroelectric memristor and hysteresis loops. a) The schematic (left-top panel) and AFM topography image (left-bottom panel) of a typical α-In$_2$Se$_3$ ferroelectric memristor used in this work. The crystal structure of α-In$_2$Se$_3$ is shown in the right panel, where the yellow and blue balls represent Se and In atoms, respectively. The six-terminal electrodes of the memristor are labeled as T1, T2, T3, T4, T5, and T6, as shown in the AFM image. The channel α-In$_2$Se$_3$ thickness (collected from the white solid line shown in the AFM image) was ≈36 nm. Scale bar: 2 μm. b) Single-point PFM spectroscopy of an α-In$_2$Se$_3$ channel in (a). c–e) Pinched hysteresis loops obtained from different electrode pairs in (a), including c) T6-5, d) T1-2, and e) T3-4, under different maximum sweep biases. The switching sequences are highlighted by the black arrows and the simulated IV curves are indicated by the gray in (c) using our established ferroelectric memristor model (see the Experimental Section for more details).

ferroelectric memristive behavior in the α-In$_2$Se$_3$ device is robust at ambient conditions for at least 25 days.

As shown in **Figure 2**a–c and Figure S5 in the Supporting Information, the multiterminal planar memristor exhibits distinct switching characteristics, in which the read current can be modulated by programming pulses applied at various terminal pairs, greatly expanding the degree of freedom for controlling the channel current. For example, the read current I_{1-2} between T1 and T2 can be significantly tuned not only by the programming pulses at T6-5, T1-5, and T1-6, but also by a remote terminal pair such as T3-4. These multiterminal modulating behaviors, dramatically different from reported single-layer MoS$_2$ memristors,[12] are attributed to the ferroelectric polarization reversal that is induced by both T1-2 and their neighboring terminals. If not specified, the widths for all the mentioned pulses were fixed at 2 s, which is sufficient to pole the planner α-In$_2$Se$_3$ device with a micrometer-sized channel length.[21] After applying ±4.0 V programming pulses at T6-5, the resistance switching ratio between T1 and T2 at −0.3 V read

bias is as large as 10^3 (Figure 2b), which is a record value for the modulating effect by a third terminal in a memristor.[7,12] A large resistance switching ratio is extremely appealing for complex brain emulation and in-memory computing. It should be emphasized that the switched resistance (or current) by a modulatory terminal in this work is nonvolatile, distinct from the volatile responses in reported multiterminal memristors.[6,7,22]

Note that a positive pulse at T1-2 makes the channel current I_{1-2} switch to a low current state (Figure 2a) but a negative one results in I_{1-2} switching to a high-current state, which coincides with the electrical transport curves shown in Figure 1d and Figure S6 in the Supporting Information. Conversely, a positive poling pulse at either T6-5 or T3-4 produces the high current switching of I_{1-2}, whereas a negative one leads to the low current switching of I_{1-2} (Figure 2b,c). Note that upon applying poling pulses to T1-2 and T6-5 their opposite switching trend is ascribed to the opposite modulations of ferroelectric polarization charges on electrical transport. This can be inferred from PFM mapping versus poling
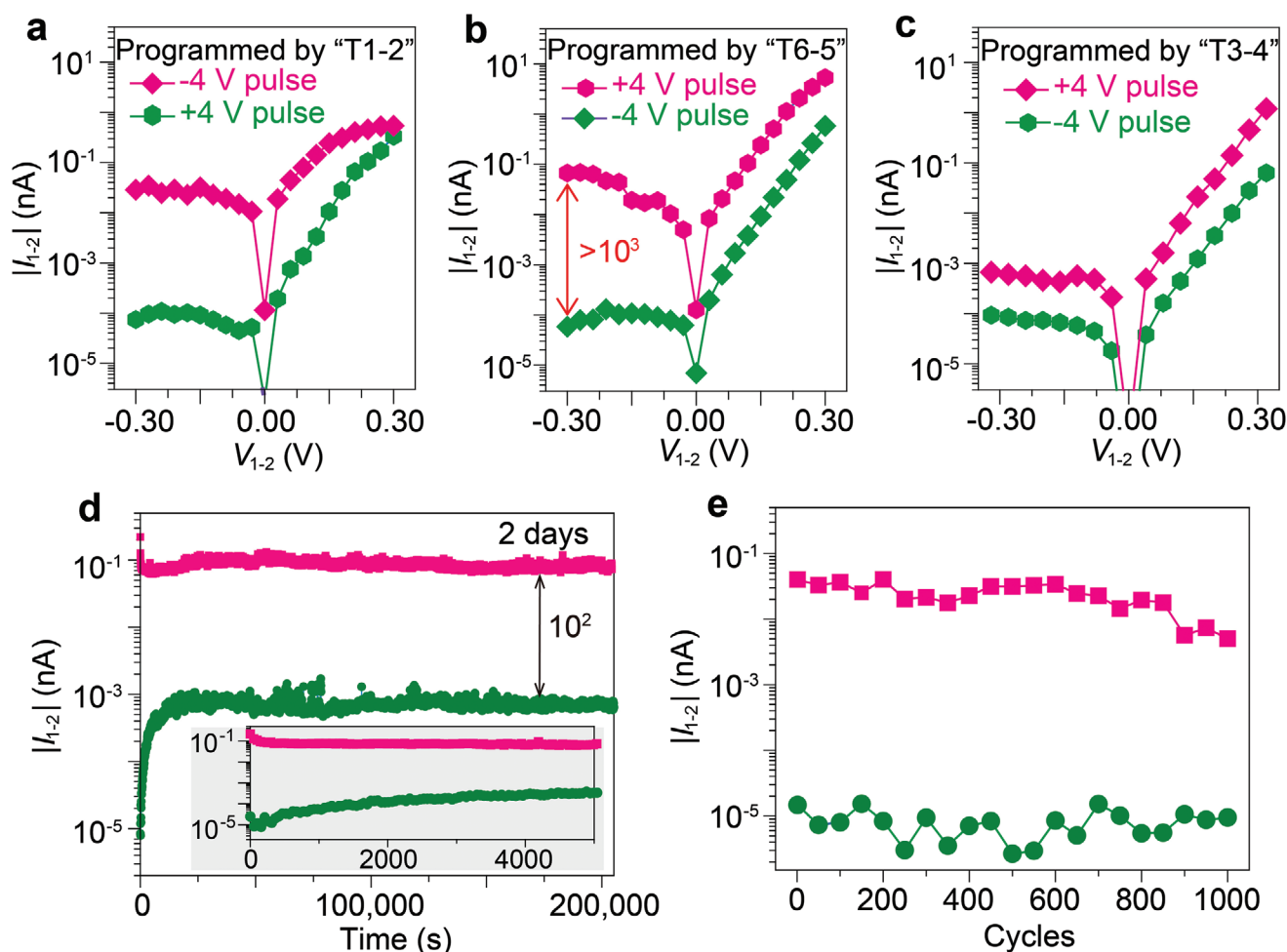
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Figure 2. Current (resistance) switching upon pulse programming. The current change in terminals T1-2 after poling α-In$_2$Se$_3$ at various paired electrodes: a) T1-2, b) T6-5, and c) T3-4. The pulse amplitude and width were set to 4 V and 2 s, respectively. d) Retention after +4 V poling for the high-current state (pink) and −4 V poling for the low-current state (green). The inset shows retention property at the first 5000 s. e) Endurance of the high-current state (pink) and low current state (green). The read voltage in (d) and (e) is −0.3 V.

at different terminals: the polarization induced by +4 V pulse at T1-2 (corresponds to −4 V poling at T2-1 in Figure S7 in the Supporting Information) resembles that poled by −4 V pulse at T6-5 (**Figure 3**a). Due to the partial polarization reversal of the ferroelectric α-In$_2$Se$_3$ channel bridging T1 and T2, it is reasonable for the ratio of the I_{1-2} current switching triggered by the T3-4 pulse (Figure 2c) to be much smaller than that programmed by the T1-2 or T6-5 pulse (Figure 2a,b). Additionally, to demonstrate the long-term stability of the memristor device, we collected the retention properties as shown in Figure 2d, suggesting that the switching ratio above 10^2 can last for up to 2 days. Besides, we conducted an endurance test collected at ±4.0 V for 1000 full-sweep cycles at T1-2 (Figure 2e), in which we note the gradually decreasing trend for the high current state reduces the current switching ratio from 10^3 to 10^2. The performance decay in Figure 2d,e is attributed to the domain backing switching and the screening on polarization charges. It is worth mentioning that our multiterminal ferroelectric memristors can operate at picoampere-range current, less than 4 V poling bias, and femtojoule read-energy consumption,

which is promising for energy-efficient neuromorphic in-memory computing systems.[23]

3. Switching Mechanism

The interlocked IP and OOP dipoles in the ferroelectric α-In$_2$Se$_3$ can be simultaneously reversed by applying an IP or OOP electric field.[17,20,21] For unveiling the device working mechanism, we used OOP PFM mapping to visualize the switching of the polarization upon different programming pulses to T6 (Figure 3a; T5 grounded) and T1 (Figure S7, Supporting Information; T2 grounded). As evidenced by the first image shown in Figure 3a, the −4.0 V pulse applied on T6 through the PFM probe not only fully reverses the IP polarization in the ferroelectric α-In$_2$Se$_3$ to point toward T6 (as the black arrow shows), but also aligns the OOP polarization to face outward (as the circle with the dot shows; see Note S1 in the Supporting Information for more details). As we varied the applied negative pulse to T6 from −4.0 to −2.0 V in 1.0 V steps, the PFM amplitude mapping
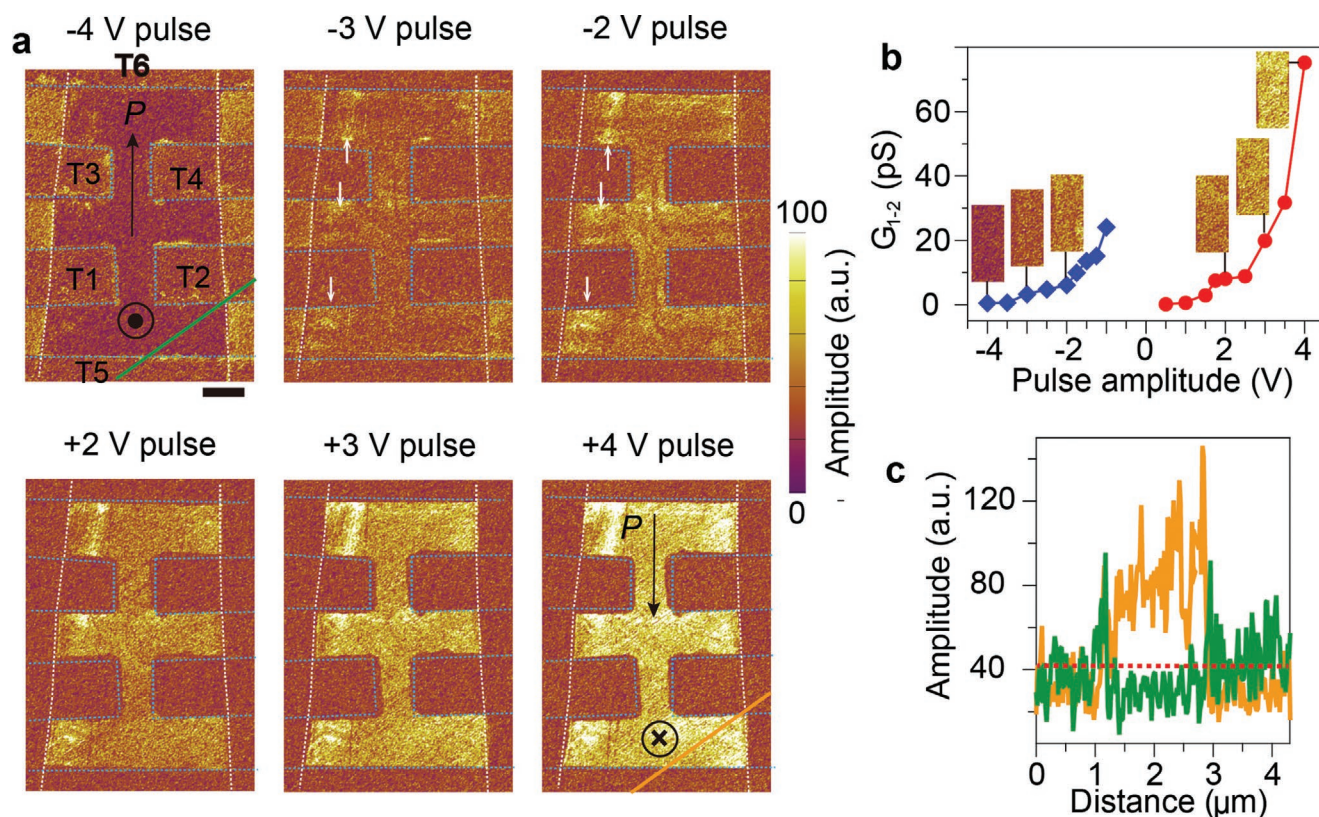
Figure 3. Visualization of the ferroelectric switching dynamic in the ferroelectric α-In$_2$Se$_3$ memristor. a) OOP PFM amplitude mapping after applying various poling pulses (2 s width) on T6 with T5 grounded. The area enclosed by the white dashed lines is the α-In$_2$Se$_3$ flake while the patterns highlighted by the blue dashed lines are the metal electrodes (terminals T1, T2, T3, T4, T5, and T6). The directions of the switched ferroelectric dipoles are depicted by the black arrows, $\odot$ (outward) and $\otimes$ (inward). The typical pre-existing nucleation centers are marked by the white arrows. Scale bar: 1 µm. b) Evolution of the conductance at T1-2 (G_{1-2}) after the application of poling pulses to T6. The channel images of the PFM amplitude between T1 and T2 shown in the insets are derived from (a). c) Quantitative PFM amplitude profiles in the cases of −4 and +4 V poling along the green and yellow solid lines in (a).

becomes much brighter (i.e., a positive piezoresponse is generated), particularly in some specific areas of the channel, as shown by the white arrows, which indicates the increased proportion of IP polarization pointing opposite of T6 (see Note S1 in the Supporting Information for more details). In this scenario, two types of polarized IP domains orientating toward and opposite T6 coexist, contributing to the increased conductance (compared with the conductance at −4.0 V poling), as shown in Figure 3b. When large positive pulses, such as +2.0 and +3.0 V, are subsequently applied on T6, the amplitude of the positive piezoresponse is significantly intensified, suggesting the expansion of the IP domain facing opposite T6. Note that in the case of the +4.0 V pulse programming, the IP polarization is fully switched to face opposite T6, accompanied by the OOP polarization flipping from the outward to inward direction, as the black arrow and circle symbol show in the bottom-right image in Figure 3a. In order to obtain the electric field distribution for easily understanding polarization orientation we performed COMSOL simulation as shown in Figure S8 in the Supporting Information. Meanwhile, we also conducted IP PFM mapping of an α-In$_2$Se$_3$ memristor to confirm the ferroelectric polarization switching effect (Figure S9, Supporting Information). Figure 3c shows the extracted amplitudes of the negative (green

curve) and positive (yellow curve) piezoresponses, implying that the IP ferroelectric domains are dramatically toggled upon switching the polarity by a 4 V programming pulse (see Note S1 in the Supporting Information for details). The asymmetric amplitudes as highlighted by the yellow and green are also caused by the pre-existing dipole that points inward, consequently reducing the whole contraction amplitude to a level like the green curves.

Remarkably, the polarization switching of the α-In$_2$Se$_3$ channel from −2.0 to −4.0 V (or 2.0 to 4.0 V) in Figure 3a is predominantly governed by the growth of existing inhomogeneous nucleation centers (see the nanodomains indicated by white arrows for reference). The presence of large fractions of positive piezoresponse area across the whole channel after applying a pulse of −2.0 V to T6 is possibly due to pre-existing defect-induced dipoles,[15] favoring domain nucleation and switching opposite T6. Even though both IP and OOP polarization can electrostatically induce bound charges over the interface of Au and α-In$_2$Se$_3$, we argue that the IP polarization charges play a dominant role in the channel conductance (see Note S2 and Figure S10 in the Supporting Information). Moreover, to link the carrier transport with the IP polarization switching in the ferroelectric α-In$_2$Se$_3$, we measured the conductance change

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across T1-2 and extracted the corresponding PFM amplitude mapping (Figure 3b). Along with the electrically controlled polarization switching, the channel conductance can be continuously tuned, which is favorable for demonstrating heterosynaptic plasticity.

4. Neuromorphic In-Memory Computing

The capability to toggle the channel polarization and thus continuously modulate the device conductance through different planar terminals endows ferroelectric α-In$_2$Se$_3$ memristors with the potential for successful implementation of heterosynaptic learning. **Figure 4**a illustrates the schematic of typical heterosynaptic plasticity realized in a multiterminal memristor. The T1 and grounded T2 terminals respectively serve as the presynaptic and postsynaptic neurons of an electronic synapse, while the T6 terminal acts as a modulatory interneuron. The applied voltage pulses can be considered as input spikes and the postsynaptic current I_{1-2} is used to monitor the change in the synaptic weight (i.e., the channel conductance). To investigate the control of synaptic potentiation (PO) and depression (DE) by a modulatory interneuron, the current spikes were only delivered to T6, which agrees with virtual synaptic activities.[10] Figure 4b shows the long-term PO and DE as a function of the pulse number for mimicking excitatory and inhibitory synapses. With the accumulation of PO pulses (each pulse has a width of 0.2 s), the postsynaptic current I_{1-2} is evidently set to a much higher current state; then subsequently applying DE pulses, the I_{1-2} evolves to a much lower current state. In Figure 4b, we observe that multiple current states, analogous to various synaptic connection states,[8] can be obtained as the spikes fire.

An important learning rule in biological synapses, so-called spike timing-dependent plasticity (STDP),[5] is also emulated in our multiterminal α-In$_2$Se$_3$ memristor (Figure 4c). If a modulatory spike from T6 precedes a postsynaptic spike from T2, as illustrated in the left inset of Figure 4c, their superposition is equivalent to the spike completely inputted at T6. As a result, the synapse is distinctly weakened (i.e., decrease in conductance). Meanwhile a short time interval (Δt) generates a larger synaptic weakening. As a modulatory T6 spike lags behind a postsynaptic T2 spike, the synapse is significantly strengthened and a short Δt results in a larger synaptic strengthening.

Additionally, the synaptic plasticity is determined not only by the spike time, but also by the spike amplitude.[24] Figure 4d shows the modulatory-spike amplitude dependent postsynaptic current I_{1-2}. As we regularly varied the 0.5 s width spike potential at a step of 1.0 V, the electronic synapse can exhibit either the PO (right panel of Figure 4d) or DE process (left panel of Figure 4d). Interestingly, the postsynaptic current I_{1-2} features an approximately linear relationship with the spike potential. Such linearity is enormously desired and critical for future artificial realistic synapses.[25] Asymmetric pulse stimulation in Figure 4d, such as a −8.0 V pulse, can completely enable low-current switching, but a +20.0 V pulse is needed for high-current switching, which we attribute to the pre-existence of interfacial IP dipoles. In addition, we tested the reproducibility of the modulatory tunability by conducting 50 cycles of PO and

DE by T6 spikes, in which the current switching ratio remained greater than 10^2 (Figure 4e).

To demonstrate the synergistic bioactivities between the modulatory interneuron and presynaptic neuron, Figure 4f explores the cooperation and competition from T6 and T1, in which the left panel shows the schematic of the firing scheme with pulses delivered to T6 and T1 for measurements. In response to the simultaneous inputs of a +4.0 V pulse on T6 and −4.0 V pulse on T1, the presynaptic current I_{1-2} markedly increases to 20 pA, which is clearly larger than their respective fired responses (the middle panel of Figure 4f), demonstrating a good cooperative relationship. Moreover, as shown in the right panel of Figure 4f, we demonstrate the competitive relationship between the modulatory T6 and presynaptic T1 terminals by alternatively firing a −4.0 V pulse to T1 (PO) and a +4.0 V pulse to T6 (DE). We note that the 2D geometry of the α-In$_2$Se$_3$ ferroelectric semiconductor may enable the realization of more complicated biological activities using multiple terminals rather than limited to just the six terminals demonstrated in this work.

Having systematically demonstrated the associative learning of heterosynaptic plasticity in a single solid-state device, we now turn to implement neural network circuits using α-In$_2$Se$_3$ device arrays. In practice, many tasks, including pattern recognition[26] and enhancement,[27] can be performed in a network array, such as a CNN, which can potentially be accelerated with ultralow power consumption using memristor-emulated artificial synapses in the crossbar array. However, the limited resistance levels of the synaptic memristors together with the device variability is a critical factor affecting the accuracy of such neural networks. To examine the offline learning accuracy of α-In$_2$Se$_3$ devices, we constructed a standard AlexNET for numerical simulation and trained with a MNIST handwritten digit database[28] (**Figure 5**a). Taking into account the limited-level-induced quantized weight and the device variability using experimental results from the α-In$_2$Se$_3$ memristors (Figure S11, Supporting Information), the pattern recognition accuracy can reach 98% (Figure 5b). Compared with the ideal case, there is only ≈1% drop, which is mainly ascribed to the quantized levels rather than the device variation, suggesting good variability resilience of our α-In$_2$Se$_3$ CNN for practical use. In addition, we also conducted the numerical simulation using other CNN topologies, such as a LeNET and a multilayer perceptron network (MLP). The comparison of pattern recognition accuracy of MLP, LeNET, and AlexNET is plotted in Figure 5c. We observe that the simulation accuracy of AlexNET is the highest, wherein, although the quantization effect varies with the different networks, the impact of device variation is negligible.

We have shown the supervised learning with our α-In$_2$Se$_3$ memristors in Figure 5a–c. This machine learning manner always needs past information to process present data for labeling and comparing, which consequently exhibits a high accuracy of image recognition[29] like our demonstrated results in Figure 5c. However, the supervised learning is not suitable for classifying big data while unsupervised learning with no input of past information can effectively address it. For the unsupervised learning, we constructed a spiking neural network that essentially operates with the learning rule of STDP. Using our established physical model and fits of experimental data (see the Experimental Section and Figure S12 in the Supporting
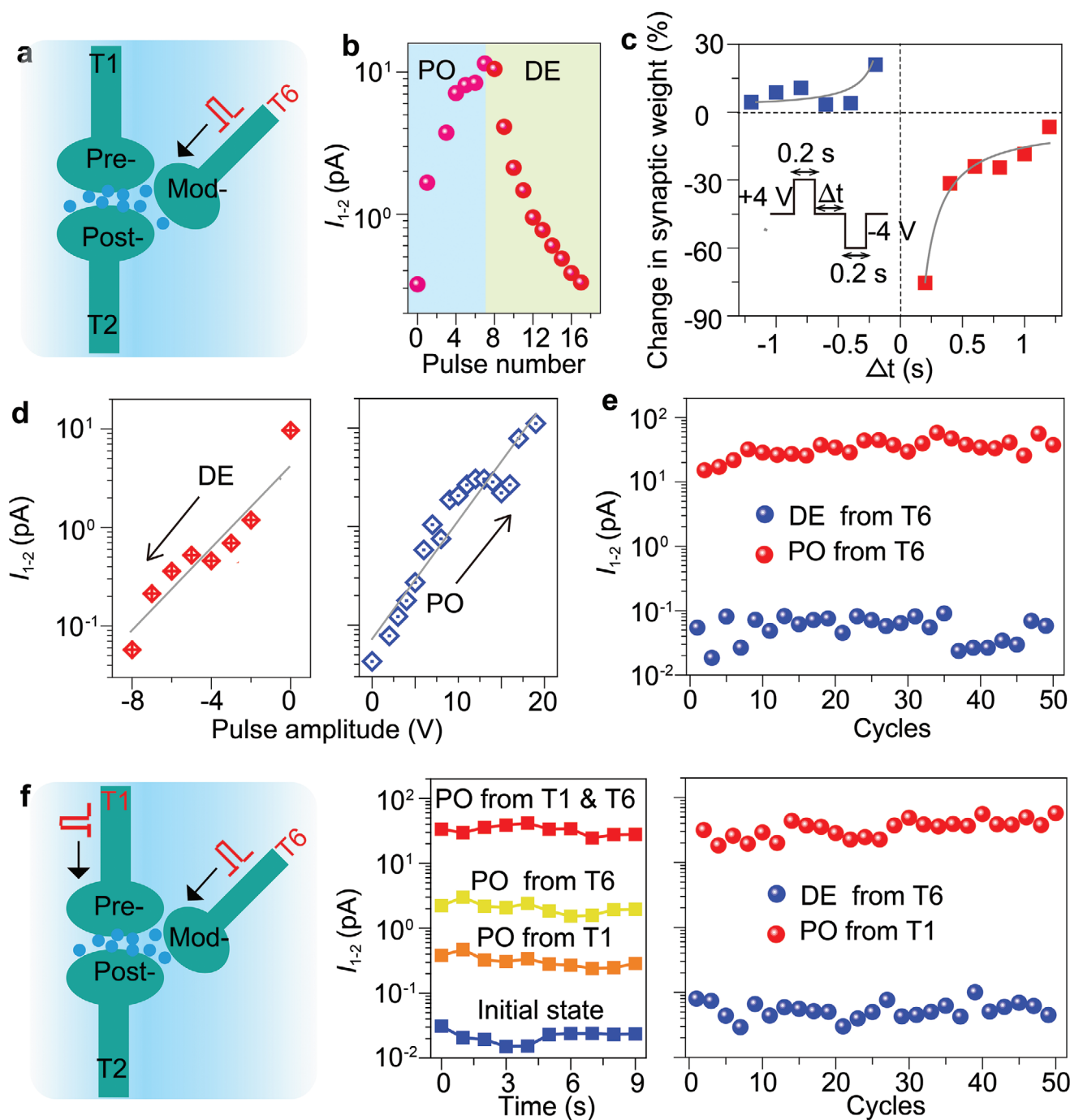
Figure 4. Heterosynaptic learning. a) Schematic showing the operation of heterosynaptic plasticity. T1-2 in the α-In$_2$Se$_3$ memristors mimic homosynaptic plasticity, including a preneuron (Pre-) and a postneuron (Post-), whose synaptic activities can be fully controlled by the third modulatory T6 terminal (Mod-), enabling heterosynaptic plasticity. Note that the results in (b)–(e) are solely collected from T1-2 by the stimulation of modulatory T6. b) Postsynaptic current I_{12} as a function of the pulse number. Positive and negative pulses are respectively employed to achieve synaptic potentiation (PO) and depression (DE). c) The time interval (Δt) dependence of the measured change in the synaptic weight (normalized to the T1-2 maximum weight). The timing scheme and exponential fittings are shown in the inset. d) Postsynaptic current I_{12} with respect to the amplitudes of modulatory voltage spikes with a fixed pulse width of 0.5 s. e) Modulatory stimulated reproducible PO and DE. f) Synaptic cooperation and competition between the preneuron (T1) and modulatory (T6) spikes. The middle panel shows the current responses (PO processes) after the T1, T6, and T1 and T6 successive stimulations; the right panel demonstrates the periodic PO and DE triggered by the alternating −4 V pulses at T1 and +4 V pulses at T6. The pulse amplitude in (b), (c), (e), and (f) are fixed at 4 V while the width for (b) is 0.2 s, but that for (e) and (f) is 2 s. Read bias: −0.3 V.

Information), the STDP curves can be theoretically predicted as shown in Figure 5d,e. It is observed from Figure 5d that the

simulated learning curve matches well with our actual results in Figure 4c, further confirming our ferroelectric model. Moreover,
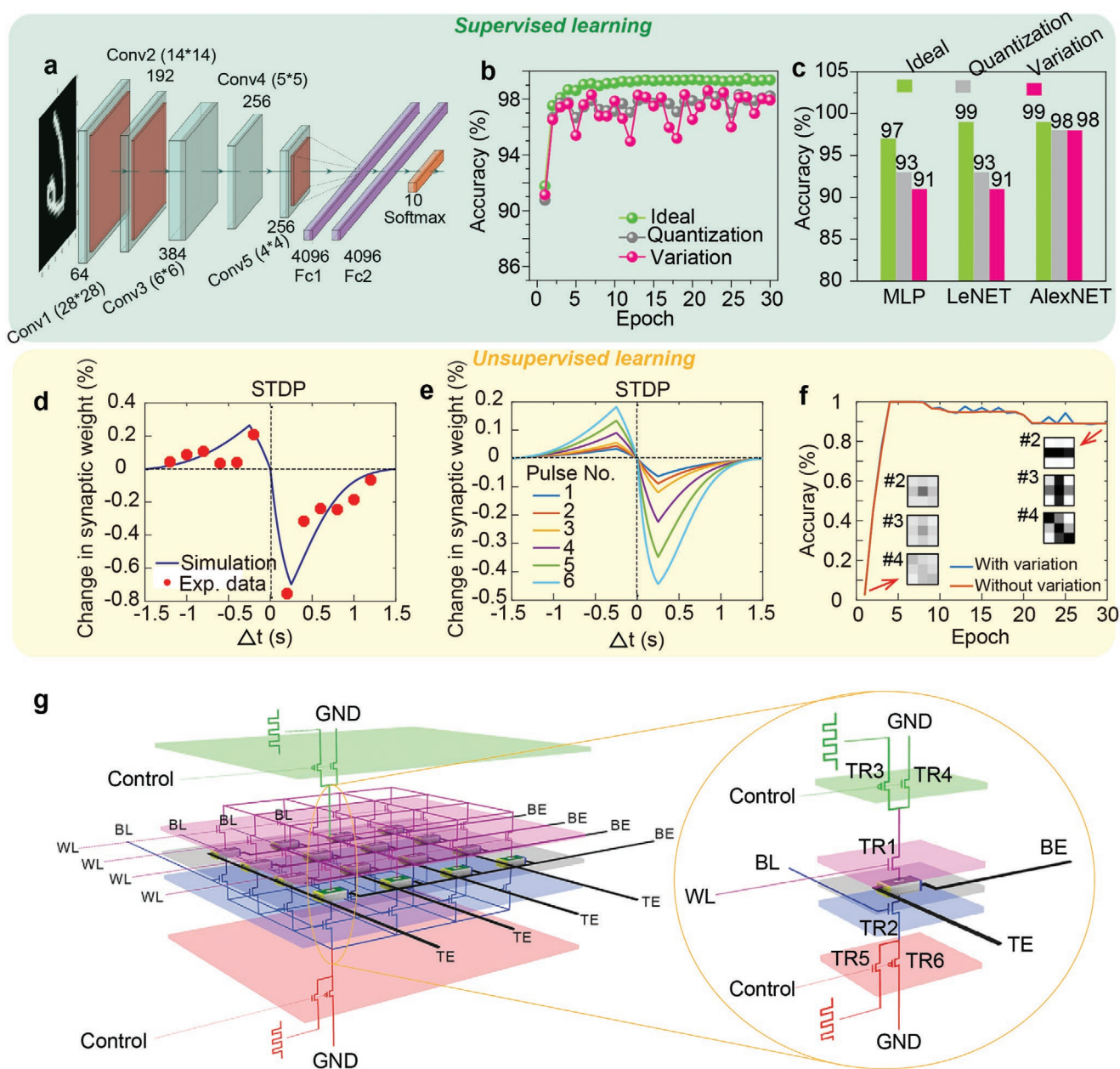
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Figure 5. Neural network simulation and monolithic integration of multiterminal devices. a–c) Implementation of convolutional neural networks with supervised learning. a) Schematic of the AlexNET neural network. b) The image recognition accuracy as a function of training epochs for an ideal device and an α-In$_2$Se$_3$ device with weight quantization and device-to-device variation. Six mean values were utilized for quantization to reduce the computation demand (for more details see the Experimental Section). c) Comparison of the simulation results using different networks (multilayer perceptron network: MLP, LeNET, and AlexNET). d–f) Implementation of spiking neural networks with unsupervised learning. d) Predicted STDP with experimental data (Figure 4c) presented for comparison. e) Predicted STDP as a function of different pulse amplitudes. The pulses marked by nos. 1, 2, 3, 4, 5, and 6 correspond to negative amplitude of −1.8, −1.9, 2.0, −2.25, and −2.75 V. f) The image recognition accuracy with respect to training epochs. g) The four-terminal α-In$_2$Se$_3$ device with its circuitry and monolithic integration. Wherein, the two terminals (TE and BE) are connected laterally as the standard crossbar structure and the other two terminals are integrated vertically for connecting either the pulse unit or the ground. The WL and BL are used for the cell selection. The complimentary gating structure connecting to the control unit guarantee either the positive or the negative pulse to be applied for potentiation and depression.

when varying the amplitude of input pulses (Figure 5e), the STDP curves changes accordingly, which is consistent with biological brain. On the basis of these demonstrated results, we also examine the image recognition accuracy of the constructed spiking neutral network (Figure 5f). After 30 cycles training, the accuracy is finally stabilized at 89%, which is a little smaller than that in convolutional networks as shown in Figure 5c but is normal for the unsupervised learning.[30]

Additionally, with respect to the integration of neural circuits, our α-In$_2$Se$_3$ heterosynaptic devices with flexible design

of multiterminal electrodes do have the advantages. The integrated circuit can be designed vertically in which the control for the resistance adjustment and the sensing for the matrix–vector multiplication get stacked up through 3D integration (Figure 5g). In this highly integrated network circuit, the notorious issue of device-to-device variation[4] could be largely suppressed through slight adjustment of the cell selection terminal (WL and BL). Moreover, this integration approach presents much simpler control strategy and circuit topology. We note that more details related to the neural network simulation and device integration can be found in Note S3 in the Supporting Information.

Apart from neuromorphic computing, in-memory computing is also exceedingly useful for overcoming the bottleneck of von Neumann computers.[7,13] The closely dependent current switching with T1 and T6 programming pulses enables the implementation of in-memory Boolean logic using the multiterminal α-In$_2$Se$_3$ memristor. **Figure 6**a illustrates the schematic

of logic variables p, q, and output s in the device. We designated the voltage state inputted to T1 or T6 as p or q, respectively, whereas the state of the current output across T1-2 represented s. In order to perform an OR logic gate, a −4.0 V pulse signal and a +4.0 V pulse signal were used to execute the logic "1" for p and q, respectively; while the high current condition at T1-2 was assigned to logic "1" for s. Figure 6b shows the experimental demonstrations of the universal OR gate operation and its truth table. Before any OR gate operation, the multiterminal memristor is always reconfigured to a low current state to erase the previous state, which is common for logic operations.[7] Likewise, as shown in Figure 6c,d, the multiterminal α-In$_2$Se$_3$ memristor can also be used to implement NOT and NOR gates. Contrary to the definitions of the OR gate, the logic "1" for p and q were respectively defined as a +4.0 V input and a −4.0 V input, respectively, while the logic "1" for s was defined as the high current state at T1–T2. We note the memristor needs to be initialized to a high current state upon performing any NOT or
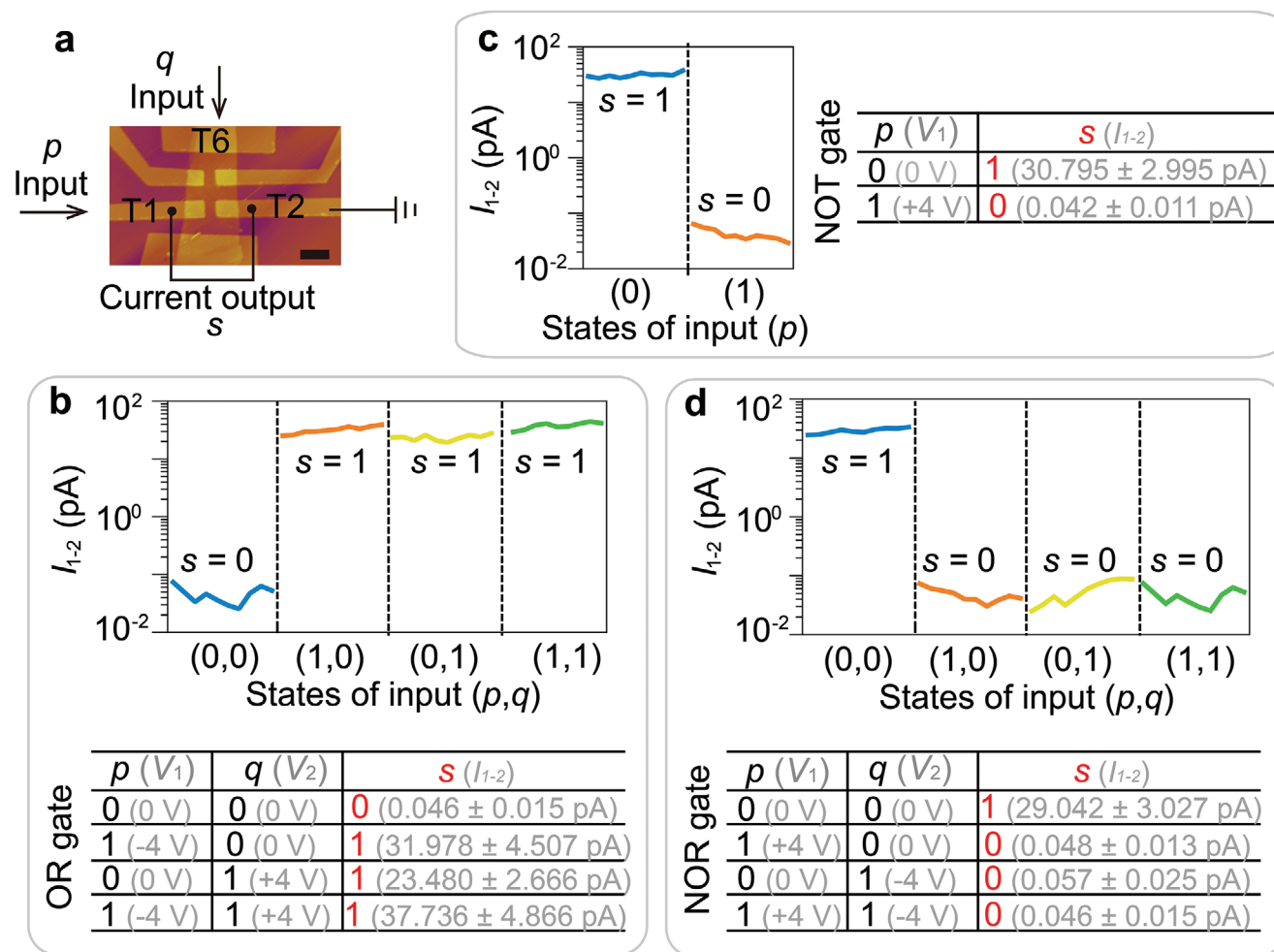

Figure 6. Demonstration of in-memory Boolean logic. a) AFM image of the memristor showing the variables (p and q) and output (s) of the logic gates. Scale bar: 2 µm. b) Output currents under different input states for the OR gate and its truth table. To implement the OR gate, the initial output is reset to the low current state; the "1" truth value for input p is designated as the −4 V signal and that for input q was defined as +4 V. Output currents with different input states for c) NOT gate and d) NOR gate and their truth tables. To demonstrate the NOT and NOR gates, the initial outputs are reset to the high current state; the "1" truth value for input p is designated as the +4 V signal and that for input q is assigned to the −4 V signal. The read voltage applied on T1-2 for the data in (b)–(d) is −0.3 V. The average current of output s and its standard deviation are given in the truth tables.

NOT gate

p (V_1)	s ($I_{1\text{-}2}$)
0 (0 V)	1 (30.795 ± 2.995 pA)
1 (+4 V)	0 (0.042 ± 0.011 pA)

OR gate

p (V_1)	q (V_2)	s ($I_{1\text{-}2}$)
0 (0 V)	0 (0 V)	0 (0.046 ± 0.015 pA)
1 (-4 V)	0 (0 V)	1 (31.978 ± 4.507 pA)
0 (0 V)	1 (+4 V)	1 (23.480 ± 2.666 pA)
1 (-4 V)	1 (+4 V)	1 (37.736 ± 4.866 pA)

NOR gate

p (V_1)	q (V_2)	s ($I_{1\text{-}2}$)
0 (0 V)	0 (0 V)	1 (29.042 ± 3.027 pA)
1 (+4 V)	0 (0 V)	0 (0.048 ± 0.013 pA)
0 (0 V)	1 (-4 V)	0 (0.057 ± 0.025 pA)
1 (+4 V)	1 (-4 V)	0 (0.046 ± 0.015 pA)

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NOR operation. Unlike multicycle logic operations in reported oxide in-memory devices,[14] this ferroelectric memristor only requires one logic step to fulfill the logic gates (thus improving the operation efficiency) due to the flexible ability to flip the channel polarization through various terminals.

5. Conclusion

We have demonstrated ferroelectric switching in van der Waals ferroelectric α-In$_2$Se$_3$ for achieving a record high ratio (>10^3) of nonvolatile resistance switching for heterosynaptic devices. For deep learning, our simulated convolutional neural network and spiking neural network show that α-In$_2$Se$_3$ memristors can realize high pattern recognition accuracy with the supervised and unsupervised learning, respectively. For in-memory computing, Boolean logics can also be fulfilled in these heterosynaptic devices with an ultralow operation current. The multiple terminals of our α-In$_2$Se$_3$ memristors could replace the functionalities of selectors and peripheral circuits as in conventional memristor array, which is, to some extent, favorable for memristor 3D monolithic integration. Our experimental results suggest a significant opportunity for the development of complex brain-inspired systems and low-power logic-in-memory computer by using low-dimensional materials. Toward this goal, experimentally achieving these memristor array is crucial and future work can be done along the following lines: improving retention and endurance properties through reducing the interfacial effect on polarization charges; reducing device-to-device variation in the array by adopting wafer-scale α-In$_2$Se$_3$ film.

6. Experimental Section

Devices and Measurements: The bulk α-In$_2$Se$_3$ crystal was purchased from 2D semiconductors, Inc. E-beam lithography was used to pattern the memristor terminals, which was metalized by two layers of Ti/Au (10 nm/50 nm) using e-beam deposition. All electrical measurements were carried out in the dark (to avoid the interference of the photoelectric effect) at room temperature using a Keithley 4200 Parameter Analyzer, which was also the pulse generation source. The *I–V* curves were collected at a quite sweep mode of Keithley 4200. All single-point current values in the main text correspond to the average value collected from ten points of current sampling. The PFM measurement was performed in a MFP-3D AFM using a 2 N m^{-1} probe and the dual AC resonance mode. The PFM mapping in Figure 3 and Figure S6 in the Supporting Information was acquired with a +0.5 V AC bias applied on the probe. Raman measurement was carried out on WITec alpha 300 with a 532 nm laser.

Modeling the Memristor: From the PFM characterization, it was observed that the propagation of α-In$_2$Se$_3$ ferroelectric nanodomain walls dominates the resistance switching in the channel where two types of domains pointing toward and against T6 coexist and therefore result in the conductance change. The total resistance (*R*) between two terminals can be expressed as[15,31]

$$\frac{1}{R} = \frac{s}{R_{\text{on}}} + \frac{1-s}{R_{\text{off}}} \tag{1}$$

in which R_{on} and R_{off} respectively dictate the low resistance of the channel where the domain fully orientates toward T6, and the high resistance of the channel where the domain entirely faces against T6; *s* represents the fraction of channel polarization pointing against T6. In Equation (1),

the switching dynamic of α-In$_2$Se$_3$ ferroelectric polarization determinates the measured resistance *R*. Up to now, two main models have been proposed to describe this polarization switching dynamic:[15,31] the KAI model applies to the propagation-dominated polarization switching process, while the nucleation-limited-switching model describes the nucleation-controlled polarization switching system. Obviously, the experimental results in Figure 3a support the adoption of KAI model for α-In$_2$Se$_3$ memristors.

For simplifying the KAI model, it was assumed that the whole α-In$_2$Se$_3$ fake is dominated by a single KAI area. Inside this area, all the nucleation sites shared the same nucleation time (τ_N) and propagation time (τ_P), both of which depend on the applied voltage (*V*) according to Merz's Law. Based on these assumptions, the fraction of switched domain (*s*) can be given by

$$\tau_{\text{N,P}}(V) = \tau_{\text{N0,P0}} \times \exp\left(\frac{E_{\text{Na,Pa}}}{E}\right) = \tau_{\text{N0,P0}} \times \exp\left(\frac{U_{\text{N,P}}}{K_B T} \times \frac{E_0}{V} \times d\right) \tag{2}$$

$$s = h(t - \tau_N) \times \left\{1 - \exp\left[-\left(\frac{t - \tau_N}{\tau_P}\right)^2\right]\right\} \tag{3}$$

where $\frac{E_{\text{Na,Pa}}}{E} = \frac{U_{\text{N,P}}}{K_B T} \times E_0$ and $h(t)$ are the activation field and the Heaviside step function, respectively, and *d* is the channel length, and $\tau_{\text{N0,P0}}$ is the initial value.

For a ferroelectric memristor, the read values of R_{on} and R_{off} at small biases are not constant due to the Schottky barrier change induced by the ferroelectric bound charges at the interface of metal and semiconductor. Generally, the R_{on} and R_{off} are derived from the corresponding on-current (I_{on}) and off-current (I_{off}). Following the previous work, the current (*I*) across the α-In$_2$Se$_3$ memristor at a small read voltage (in this case, the applied read voltage does not induce the polarization reversal) can be described as

$$I = BA^{**}T^2 \times \exp\left(-\frac{\varnothing_r}{kT}\right) \times \exp\left(\frac{q\sqrt{q\xi / 4\pi k_s}}{kT}\right) \tag{4}$$

$$\xi = \sqrt{\frac{2qN_D}{k_s}\left(V + V_{\text{bi}} - \frac{kT}{q}\right)} \tag{5}$$

in which *B* represents the area of the Schottky barrier, A^{**} depicts the effective Richardson constant, *k* is the Boltzmann constant, $\varnothing_r$ is the reverse-biased barrier, N_D depicts the donor impurity density, V_{bi} indicates the built-in potential at the barrier, and k_s is the permittivity. To reduce the complexity, the impact of V_{bi} on *I* was ignored, the linear relationship between $\varnothing_r$ and *V* was supposed, and then Equations (4) and (5) were simplified as follows

$$I = H \times \exp\left(-\frac{\varnothing_r}{kT}\right) \times \exp\left(V^{0.25}\right) = G \times \exp\left(V^n\right) \tag{6}$$

in which *H* and *G* are the rectifying constants associated with the constants in Equations (4) and (5), and *n* is the index number of *V*. Consequently, the R_{on} and R_{off} can be estimated from *V/I*.

Referring to the literatures,[12,31] a voltage-controlled ideal memristive device can be defined as

$$V = R(w, V) \times I \tag{7}$$

$$\frac{\partial W}{\partial t} = f(t, V) \tag{8}$$

where *V* and *I* are the input voltage and output current of the memristor respectively, *t* is the time, *w* depicts a variable, and *f* is a continuous *n*-dimensional vector function.

As for the device, the state variable w can be designated to the fraction of switched domain. Combining with Equations (1)–(3), the model of the α-In$_2$Se$_3$ ferroelectric memristor is established as follows

$$V(t) = R(s,V) \times I(t) = \frac{1}{s/R_{\text{on}} + (1-s)/R_{\text{off}}} \times I(t) \tag{9}$$

$$\frac{\partial s}{\partial t} = (1-s) \times \frac{2}{\tau_P} \times \sqrt{\ln\left(\frac{1}{1-s}\right)} \tag{10}$$

Such a model matches well with the hysteretic I–V curves as shown in Figure 1c and Figure S3 in the Supporting Information.

The continuous resistance switching of the α-In$_2$Se$_3$ memristor is ruled by the ferroelectric polarization reversal through two ways: one is the intrinsic resistance difference arising from differently oriented domains; the other is the resistance change resulting from the ferroelectric-bound-charge modulated Schottky barrier height (SBH) at the interface. After large positive and negative voltages subsequently pole the device, their resulted resistance switching read at a small bias (Figure 2a–c) is solely ascribed to the change of SBH because the small bias is below the coercive field of α-In$_2$Se$_3$ and the polarization flipping can be reasonably ignored. Based on previous works,[21,32] the change of SBH can be roughly estimated from the simplified Equation (4)

$$\ln\left[I(P)/I(N)\right] \sim -\Delta\varnothing_r/kT \tag{11}$$

in which $I(P)$ and $I(N)$ respectively are the currents flowing across the α-In$_2$Se$_3$ memristor upon applying positive and negative poling biases.

Neural Network Simulation: Both the CNN (including AlexNet and LeNet) and the multilayer perceptron neural network were constructed in the Pytorch environment. These networks consist of various stacked layers, either convolutional layers or fully connected layers, to generate excitatory signals for positive samples and inhibitory signals for negative samples. Here, the convolutional layer refers to groups of convolutional operators, which identify salient local spatial features by tuning the syntactical weights to support the final classification, while the fully connected layer connects all pairs of neurons across two layers.

In the experiments, the configurations of these neutral network were defined as follows. The MLP was composed of three fully connected layers and the neuron number for these layers were 786, 300, and 10, respectively. The LeNet had two convolutional layers and two fully connected layers, where the first convolutional layer contained 20 kernels, the second convolutional layer contained 50 kernels, and the two fully connected layers had 500 and 10 neurons, respectively. The AlexNet was composed of 5 convolutional layers and three fully connected layers, where the kernel number for each convolutional layer was 64, 192, 384, 256, and 256, respectively, and the neuron number for the fully connected layers were 4096, 4096, and 10. After each convolutional layer, a max-pooling layer was added to subsample the response map while keeping the largest local spatial response values. In addition, the rectified linear unit (ReLU) was used as the activation function after each convolutional or fully connected layers. The networks were trained with the gradient descent backpropagation under the fixed learning rate of 0.001 with the MNIST handwritten digit database. This database is designed for training automatic digit handwriting recognition. It contains 60 000 training images and 10 000 testing images, whose size is 28 by 28 pixels. The well-trained weights in each layer are mapped to two RRAM arrays, which handles the positive and negative weights separately. For weight quantization, six mean values of the conductance levels that were extracted from the measured data were used to reduce the computation demand. Nearest neighbor method was used during the weight mapping. To further take the device variation into account, the lognormal distribution for the six conductance levels extracted from measured data were used to simulate random weights in the arrays. During the inference, the test images were used to evaluate the recognition accuracy of the network.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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