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### Article

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# A Comparative Study of AC Positive Bias Temperature Instability of Germanium nMOSFETs with GeO<sub>2</sub>/Ge and Si-cap/Ge Gate Stack

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This work was supported by the Applied Fundamental Research of Guangzhou City under Grant 202002030299 and the Key Area R&D Program of Guangdong Province under Grant 2019B010145001.

**ABSTRACT** AC positive bias temperature instability (PBTI) of germanium nMOSFETs with GeO<sub>2</sub>/Ge and Si-cap/Ge gate stack was investigated in this brief. AC-DC-AC alternating PBTI stress tests were conducted on both types of devices, the experiment data shows the inserted DC stress phase has little impact on the following AC stress kinetics on GeO<sub>2</sub>/Ge nMOSFETs but introduce a significant “additional DC generation” on Si-cap/Ge devices. The “additional DC generation” is ascribed to the existence of energy alternating defects (EAD) according to previous studies. Energy distribution under DC and AC stress further demonstrate that EAD is significant on Si-cap/Ge but negligible on GeO<sub>2</sub>/Ge devices. Effective lifetime prediction is carried out and compared under DC stress after discharge (with a purposely introduced measurement delay) and AC stress on both GeO<sub>2</sub>/Ge and Si-cap nMOSFETs. The results show GeO<sub>2</sub>/Ge nMOSFETs’ effective lifetime exhibits no difference under two stress modes, while Si-cap/Ge nMOSFETs’ effective lifetime is underestimated using DC stress after discharge approximation without considering the EAD-induced “additional DC generation”. An extra 0.14V 10-year V<sub>dd</sub> design margin can be obtained for Si-cap/Ge nMOSFETs to gain higher performance by taking “additional DC generation” into account. The conclusion is beneficial for process optimization and PBTI reliability improvement of Ge nMOSFETs.

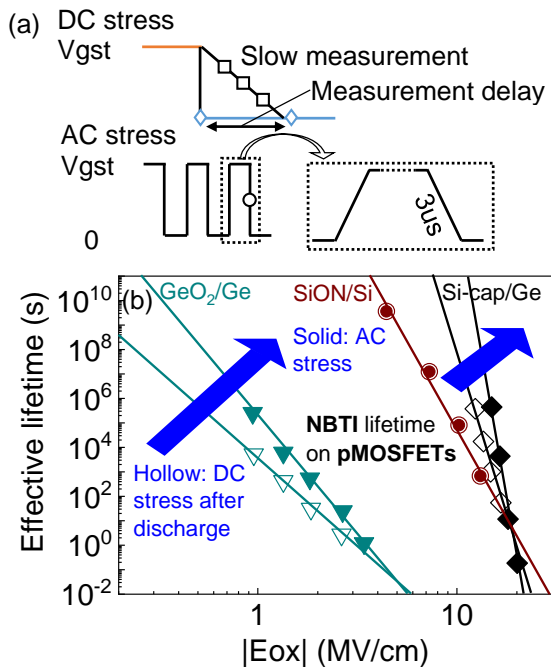
**INDEX TERMS** AC PBTI, Germanium nMOSFETs, GeO<sub>2</sub>/Ge, Si-cap/Ge, Energy Alternating Defects

## I. INTRODUCTION

Owing to the higher bulk mobility of both hole and electron, germanium (Ge) possesses great potential to replace silicon (Si) in the channel of CMOS to enhance the carrier transport and consequently to achieve higher drive currents and switching speeds [1]. Ge MOSFETs used to suffer from the lack of a good native oxide which results in massive interface states, but significant progress has been made recently [2-9]. After good initial performance was achieved, attention has been paid to device reliability to pave the way for the debut of Ge CMOS. Bias temperature instability (BTI) of Ge MOSFETs, as the simplest and most common degradation mechanism, attracts massive attention [10-16].

The improvement of Ge MOSFETs was usually achieved through two routes: GeO<sub>2</sub> directly on Ge [2, 4, 7, 9] or using a Si capping layer [3, 8]. Previous studies reveal that GeO<sub>2</sub>/Ge devices offer higher mobility for both p and n MOSFETs but suffer from poor reliability [16-18], while Si-capped devices exhibit a better NBTI reliability compared to Si counterpart [16]. The bulk of previous studies on Ge BTI adopted DC stress [10-15], and industry usually predicts AC BTI lifetime from DC stress after introducing a measurement delay either purposely [19] or unintentionally by using a measurement time of 10-100ms [20], as shown in Fig. 1a. The underlying justification is the hypothesis that degradation kinetics under effective AC stress time (stress time \* duty factor) is the same

as DC stress kinetics after a delay-induced discharge. We have recently reported that this hypothesis is valid on SiON pMOSFETs but not applicable on GeO<sub>2</sub>/Ge and Si-cap/Ge pMOSFETs subject to NBTI stress. The reason is that GeO<sub>2</sub>/Ge and Si-cap/Ge pMOSFETs contain a lot of Energy Alternating Defects (EAD) [16] which result in a significant “additional DC generation” phenomenon and eventually lead to a significant AC effective lifetime underestimation, as shown in Fig. 1b (data from [16]). EAD were also observed on Si-cap/Ge nMOSFETs [12]. However, whether EAD also exists on GeO<sub>2</sub>/Ge nMOSFETs, and how they impact the AC PBTI lifetime of Ge nMOSFETs, have not been studied yet.



**FIGURE 1.** (a) Waveforms of DC stress after discharge (with measurement delay or slow measurement) and AC stress used for BTI lifetime prediction. (b) A replot of figure from [16], which shows the comparison of NBTI lifetime prediction on SiON, GeO<sub>2</sub> and Si-cap/Ge pMOSFETs. The blue arrows show the underestimation of AC effective lifetime due to “additional DC generation” compared to DC stress after discharge approximation.

In this work, a comparative study of AC PBTI of germanium nMOSFETs with GeO<sub>2</sub>/Ge and Si-cap/Ge gate stack was carried out. AC-DC-AC alternating PBTI stress tests and energy distribution results clearly reveal that: GeO<sub>2</sub>/Ge nMOSFETs have negligible EAD and EAD-induced “additional DC generation”, while Si-cap nMOSFETs have significant EAD and exhibit clear “additional DC generation” phenomenon under DC stress after discharge stress compared to AC stress, resulting in an underestimation of AC effective lifetime if using conventional industry-adopted DC stress after discharge approximation.

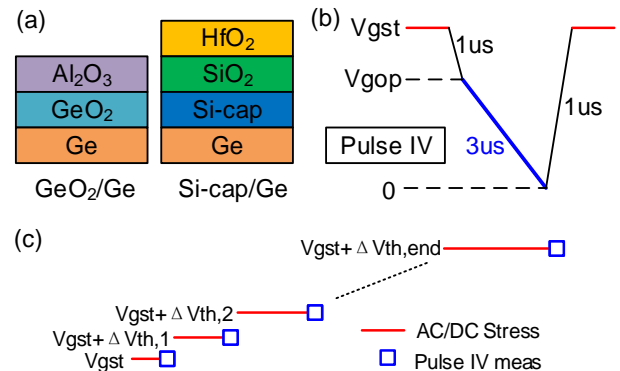
## II. DEVICES AND EXPERIMENTS

The schematic cross section of the two Ge nMOSFETs’ gate stacks is shown in Fig. 2a. The fabrication process of the two types of nMOSFETs are as follows:

1) As for the GeO<sub>2</sub>/Ge nMOSFET, a 700 nm Ge layer was prepared on a Si wafer, followed by oxidation at 150 °C in atomic oxygen to form 1.2 nm of GeO<sub>2</sub>. A 4 nm Al<sub>2</sub>O<sub>3</sub> layer was then deposited and the SiO<sub>2</sub> equivalent oxide thickness (EOT) is 2.35 nm. After the gate metallization with a 10 nm PVD TiN layer, the nMOSFETs were annealed in forming gas at 350 °C for 20 min [18].

2) In terms of the Si-cap/Ge nMOSFET, Si-passivated Ge nMOSFETs were fabricated using a replacement metal gate high-k last process with the gate stack. After dummy gate removal and pre-cleaning, the thin Si layer was epitaxially grown on the Ge channel, followed by laser annealing at 750 °C. The EOT of Si-cap/Ge nMOSFET is 1.40 nm [12].

Using Keysight B1530, arbitrary pulse waveform can be generated to achieve ultrafast pulse measurement. In this work, we employ a three microseconds pulse IV measured from the edge starting at the operating voltage (V<sub>gop</sub>) and stopping at zero to monitor the degradation of threshold voltage (V<sub>th</sub>), as shown in Fig. 2b. Due to the huge PBTI degradation on GeO<sub>2</sub>/Ge nMOSFETs, constant overdrive stress voltage (V<sub>gst\_ov</sub>) was adopted to achieve a constant oxide electric field [21, 22] throughout all stress experiments, as illustrated in Fig. 2c. Unless specified, all the tests are carried out under 125 °C and the AC stress frequency was 10 kHz with a duty factor of 0.5.

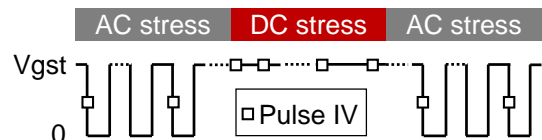


**FIGURE 2.** (a) Schematic cross section of the gate stacks of two types of Ge nMOSFET tested in this work. (b) Pulse IV from a 3us pulse edge was adopted to monitor the V<sub>th</sub>. (c) Constant overdrive stress voltage (V<sub>gst\_ov</sub>) was adopted to achieve a constant oxide electric field throughout the stress tests.

## III. RESULTS AND DISCUSSION

### A. AC-DC-AC ALTERNATING STRESS KINETICS

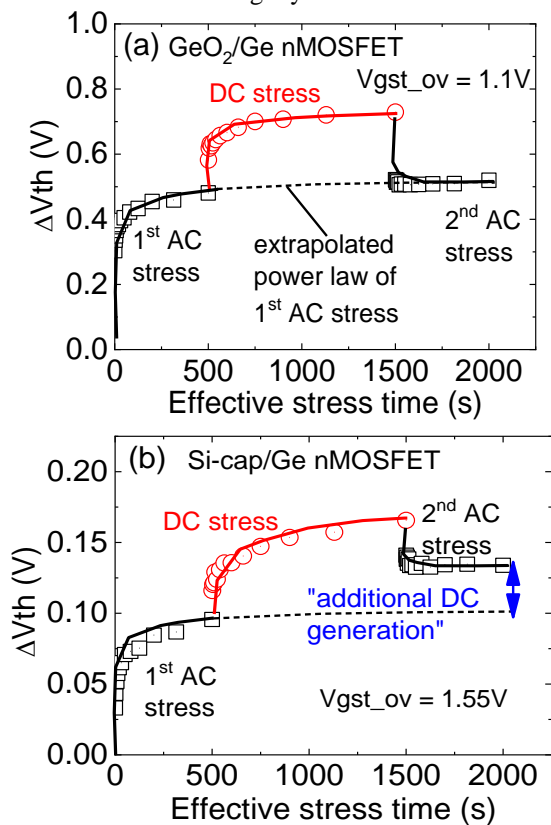
A straight-forward way to evaluate the difference between DC and AC stress is monitoring the AC-DC-AC alternating stress kinetics on a single device, as shown in Fig. 3. Note for simplicity, constant V<sub>gst\_ov</sub> stress was adopted here but not



**FIGURE 3.** Illustration of AC-DC-AC alternating stress waveform. Constant V<sub>gst\_ov</sub> correction is not drawn for simplicity.

drawn in Fig. 3. Pulse IV measurements were taken at the end of ON stage during AC stress to capture the worst degradation. The whole experiment was accomplished within a single arbitrary waveform generated by B1530, without any test delay in the switch between AC and DC stress.

A typical test result of waveform in Fig. 3 on GeO<sub>2</sub>/Ge nMOSFET was shown in Fig. 4a. Note due to the poor reliability of GeO<sub>2</sub>/Ge nMOSFETs, the constant Vg<sub>st\_ov</sub> correction could enhance the applied Vg<sub>st</sub> significantly as stress time evolves, hence Vg<sub>st\_ov</sub> on GeO<sub>2</sub>/Ge nMOSFETs cannot be set too high. Vg<sub>st\_ov</sub>=1.1V AC stress was firstly applied and the degradation can be well fitted by a power law against effective stress time. After the 1<sup>st</sup> AC stress, a DC stress phase with the same Vg<sub>st\_ov</sub>=1.1V was introduced, instantly enhanced  $\Delta V_{th}$  due to the trapping of recoverable defects which have a relatively long capture time thus cannot be charged during the 1<sup>st</sup> AC stress phase. After 1ks DC stress, the stress mode switched back to AC stress, resulting in an abrupt drop of  $\Delta V_{th}$  due to the detrapping of extra charged recoverable defects during DC stress. Most of the extra charged recoverable defects are discharged within 100s, as shown by the ceasing of slight  $\Delta V_{th}$  decrease in the 2<sup>nd</sup> AC stress kinetics. After that, AC stress induced degradation starts to take control and  $\Delta V_{th}$  slightly increases.

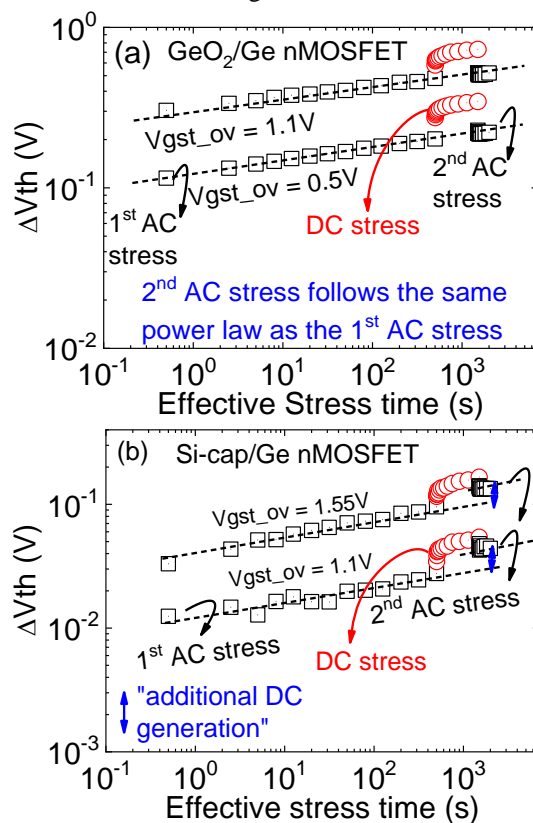


**FIGURE 4.** (a) On GeO<sub>2</sub>/Ge device, the 2<sup>nd</sup> AC stress can fully recover DC-enhanced charging. (b) On Si-cap/Ge device, the 2<sup>nd</sup> AC stress cannot fully recover the additional defects generated from DC stress.

By extrapolating the power law of 1<sup>st</sup> AC stress, we observed that  $\Delta V_{th}$  in the latter half of 2<sup>nd</sup> AC stress can be well fitted by exactly the same power law of the 1<sup>st</sup> AC stress,

implying the inserted DC stress has little impact on the subsequent AC stress on GeO<sub>2</sub>/Ge nMOSFETs. A log-log plot is given in Fig. 5a to show this more clearly. Another AC-DC-AC stress kinetics subject to a lower Vg<sub>st\_ov</sub>=0.5V was given to further confirm the observation.

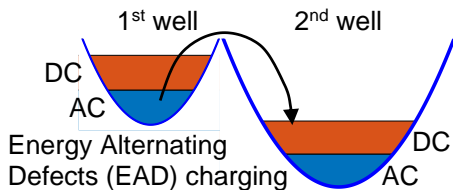
The same test procedure was then performed on Si-cap/Ge nMOSFET, and the results were shown in Fig. 4b. Note due to Si-cap/Ge nMOSFETs possess much better reliability compared to GeO<sub>2</sub>/Ge nMOSFETs, Vg<sub>st\_ov</sub> adopted on Si-cap/Ge nMOSFETs is much higher than GeO<sub>2</sub>/Ge nMOSFETs in order to induce enough  $\Delta V_{th}$  for clearer observation. In contrast to GeO<sub>2</sub>/Ge nMOSFETs, the degradation in the latter half of 2<sup>nd</sup> AC stress is much higher than the extrapolated value from the 1<sup>st</sup> AC stress phase, as shown in Fig. 4b, indicating the DC stress phase had introduced an "additional DC generation" in the following AC stress phase. Another AC-DC-AC test results under Vg<sub>st\_ov</sub>=1.1V are also given in Fig. 5b, further confirming the existence of "additional DC generation".



**FIGURE 5.** (a) On GeO<sub>2</sub>/Ge device, the 2<sup>nd</sup> AC stress phase induced  $\Delta V_{th}$  in AC-DC-AC stress pattern follows the same generation kinetics as the 1<sup>st</sup> AC stress phase, suggesting no "additional DC generation" by the inserted DC stress phase. (b) On Si-cap/Ge device, the 2<sup>nd</sup> AC stress phase induced  $\Delta V_{th}$  in AC-DC-AC stress pattern is much higher than the extrapolated value from 1<sup>st</sup> AC stress phase, exhibiting an "additional DC generation" by the inserted DC stress phase.

The "additional DC generation" phenomenon and the difference between GeO<sub>2</sub>/Ge and Si-cap/Ge nMOSFETs can be explained using the "As-grown Generation (A-G)" model [16, 23]. It has been reported that defects on Ge MOSFETs

can be categorized into three types: Generated Defects (GD), As-grown Traps (AT), and Energy Alternating Defects (EAD) [11, 12, 16, 24]. GD cannot discharge under 0V and follow the same generation kinetics against effective stress time under DC/AC stress [25], thus can be excluded from the origin of “additional DC generation”. AT’s trapping/detrapping is an elastic tunneling process, resulting in a memoryless charging/discharging kinetics hence should also be irrelevant to the “additional DC generation”. In terms of EAD, according to the first-principles calculations, the basic mechanism of EAD is that, following charging, the defect will go through a lattice relaxation that leads to a lowering of the energy of the charged state so that it becomes more stable [26, 27]. The charging process of EAD can be elucidated using a double-well model [28], as shown in Fig. 6. EAD trapping is a two-step process, electrons must firstly overcome the 1<sup>st</sup> barrier, and then proceed to overcome the 2<sup>nd</sup> barrier by a field-enhanced relaxation process and reach the deep well [28]. The EAD trapped in the 2<sup>nd</sup> well is thus proportional to the charge density in the 1<sup>st</sup> well. The shallow level of the 1<sup>st</sup> well makes the charge density in the 1<sup>st</sup> well dynamic: it is much less under AC stress because of the short charging time and discharge at  $V_g=0V$ , eventually leads to less EAD in the 2<sup>nd</sup> well. In addition, AC ON time can be too short to complete the relaxation responsible for the EAD generation. This explains the missing “additional DC generation” on Si-cap/Ge nMOSFETs under AC stress. For  $GeO_2/Ge$  nMOSFETs, EAD is negligible compared to AT, thus manifest no difference between DC and AC stress. This also agree with the report in [12] that EAD in Si-cap/Ge nMOSFETs locate at  $SiO_2$  layer close to the channel, which is missing in  $GeO_2/Ge$  structure nMOSFETs.

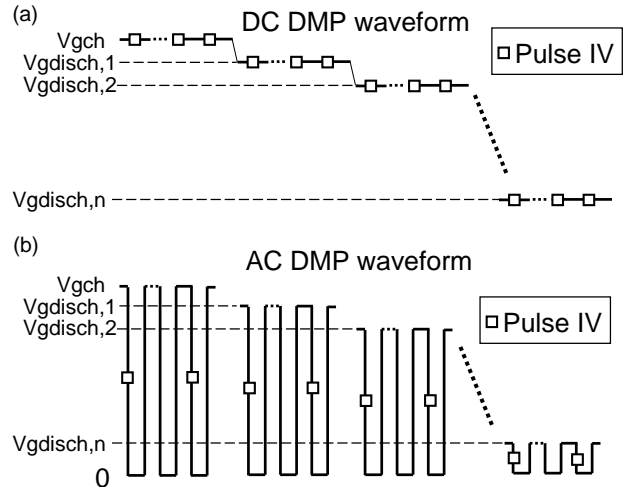


**FIGURE 6.** EAD charging process: EAD trapping in the 2<sup>nd</sup> well requires electrons in the 1<sup>st</sup> well to overcome the 2<sup>nd</sup> barrier, through a field-enhance relaxation process.

### B. ENERGY DISTRIBUTION UNDER DC AND AC STRESS

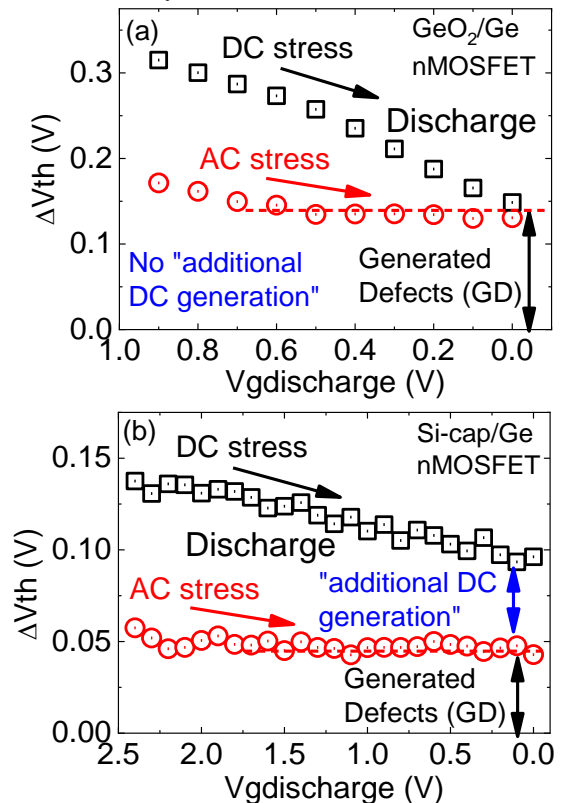
The existence of EAD and EAD-induced “additional DC generation” on Si-cap/Ge nMOSFETs but not on  $GeO_2/Ge$  nMOSFETs could also be observed through the comparison of energy distribution of  $\Delta V_{th}$  under DC and AC stress. Based on the test-proven “Discharging-based Multiple Pulses (DMP)” technique [29, 30], we can extract the energy distribution of  $\Delta V_{th}$  on  $GeO_2/Ge$  and Si-cap/Ge nMOSFETs subject to DC stress. By replacing each DC charging and discharging phases with AC counterparts, the energy distribution of  $\Delta V_{th}$  subject to AC stress can then be obtained, as shown in Fig. 7. Note the charging/discharging time for AC is twice as the values in DC

to keep the same effective charging/discharging time for a fair comparison.



**FIGURE 7.** Illustration of the test waveform of DC and AC “Discharging-based Multiple Pulses (DMP)” technique to extract  $\Delta V_{th}$  energy distribution.

A typical result of DC and AC energy distribution is shown in Fig. 8. Again we see on  $GeO_2/Ge$  nMOSFETs, DC and AC stress generate the same amount of GD with equivalent effective stress time, exhibits “no additional DC generation”, while on Si-cap/Ge nMOSFETs, a significant “additional DC generation” is clearly observed.



**FIGURE 8.** Comparisons of  $\Delta V_{th}$  energy distribution subject to DC and AC stress on (a)  $GeO_2/Ge$  nMOSFETs and (b) Si-cap/Ge nMOSFETs.

### C. LIFETIME ANALYSIS

Due to the existence of EAD and EAD-induced “additional DC generation”, Si-cap/Ge nMOSFETs’ lifetime cannot be estimated from industry adopted DC stress after discharge approximation method. A comparison of lifetime prediction under AC stress and DC stress after discharge (by purposely insert a 1s measurement delay at 0V) was carried out on GeO<sub>2</sub>/Ge and Si-cap/Ge nMOSFETs, as shown in Fig. 9-11. Note constant Vg<sub>st\_ov</sub> stress was adopted for both stress modes, each Vg<sub>st\_ov</sub> curve was obtained by averaging the stress kinetics on 3 devices to rule out the device variation.

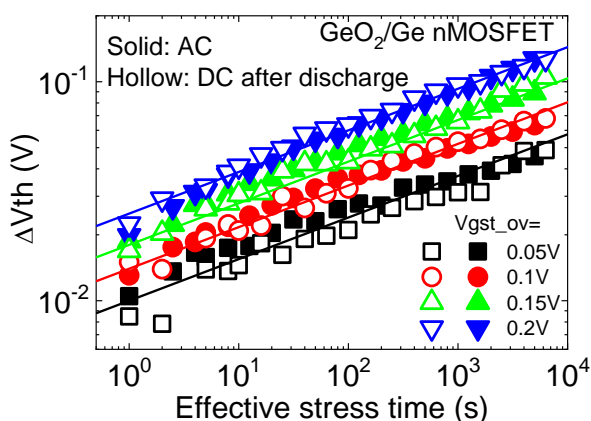
Fig. 9 shows the degradation kinetics under DC stress after discharge and AC stress against effective stress time on GeO<sub>2</sub>/Ge nMOSFETs. Clearly the two different stress modes exhibit exactly the same stress kinetics which can be well fitted by the traditional power law for BTI:

$$\Delta V_{th} = A \cdot V_{gst\_ov}^m \cdot t^n \quad (1)$$

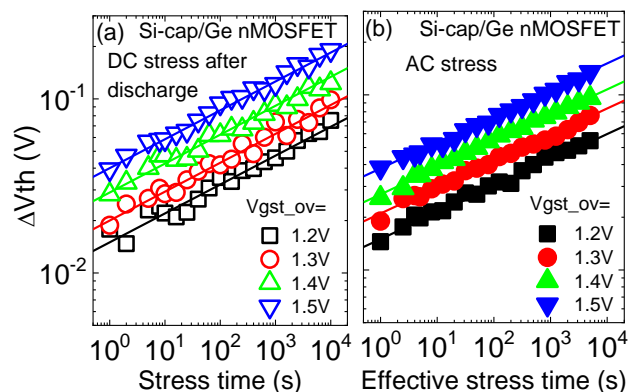
Note the extra small Vg<sub>st\_ov</sub> in Fig. 9 is in order to make the first  $\Delta V_{th}$  value (effective stress time = 1 s in Fig. 9) smaller than 100 mV, which is the typical failure criteria industry adopts for PBTI, to achieve an effective lifetime within the measurement window.

In contrast to GeO<sub>2</sub>/Ge nMOSFETs, Si-cap/Ge nMOSFETs have the “additional DC generation” phenomenon thus DC stress after discharge stress kinetics (Fig. 10a) is higher compared to the AC stress counterpart (Fig. 10b) with the same Vg<sub>st\_ov</sub>.

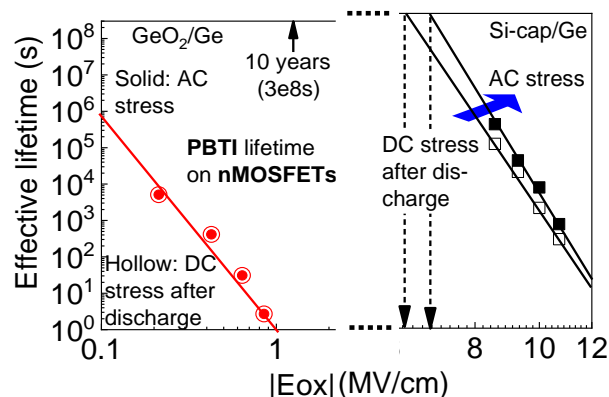
A comparison of effective lifetime prediction under DC stress after discharge and AC stress for GeO<sub>2</sub>/Ge and Si-cap/Ge nMOSFETs at the failure criteria of  $\Delta V_{th}=100\text{mV}$  was shown in Fig. 10. Note the x-axis is discontinuous in the middle to show both effective lifetime clearly. To obtain an effective lifetime of 10 years, the maximum Eox projected by DC stress after discharge and AC stress is 6.26 MV/cm and 6.86 MV/cm, respectively. The corresponding 10-year overdrive V<sub>dd</sub> is 1.47V and 1.61V. By considering the EAD-induced “additional DC generation”, an extra 0.14V 10-year V<sub>dd</sub> design margin is obtained for Si-cap/Ge nMOSFETs to gain higher performance.



**FIGURE 9.**  $\Delta V_{th}$  under DC stress after discharge exhibits the same kinetics as AC stress on GeO<sub>2</sub>/Ge nMOSFETs.



**FIGURE 10.**  $\Delta V_{th}$  under (a) DC stress after discharge is higher compared to (b) AC stress on Si-cap/Ge nMOSFETs.



**FIGURE 11.** Comparisons of GeO<sub>2</sub>/Ge and Si-cap/Ge nMOSFETs’ predicted lifetime subject to DC stress after discharge and AC stress at the failure criteria of  $\Delta V_{th}=100\text{mV}$ . The x-axis is discontinuous in the middle for better view.

## VI. CONCLUSION

A comparative investigation of AC PBTI of GeO<sub>2</sub>/Ge and Si-cap/Ge nMOSFETs was conducted in this work. Our experiment results showed the major difference between GeO<sub>2</sub>/Ge and Si-cap/Ge nMOSFETs’ PBTI is Si-cap/Ge devices contain significant amount of EAD while GeO<sub>2</sub>/Ge devices do not. The difference is speculated to be ascribed to the missing SiO<sub>2</sub> layer in GeO<sub>2</sub>/Ge nMOSFETs according to previous studies. EAD’s two-step charging process of EAD leads to an “additional DC generation” on Si-cap/Ge nMOSFETs, resulting in an underestimation of effective lifetime if conventional DC stress after discharge approximation method is adopted. The conclusion can be of great use for process optimization and PBTI reliability improvement of Ge nMOSFETs.

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