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Electrical and Mechanical Analysis of Different TSV Geometries

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Abstract: Through-silicon via (TSV) is an important component for implementing 3-D packages and 3-D integrated circuits as the TSV technology allows stacked silicon chips to interconnect through direct contact to help facilitate high-speed signal processing. By facilitating the stacking of silicon chips, the TSV technology also helps to meet the increasing demand for high density and high performance miniaturized electronic products. Our review of the literature shows that very few studies have reported on the impact of TSV bump geometry on the electrical and mechanical characteristics of the TSV. This paper reports on the investigation of different TSV geometries with the focus on identifying the ideal shapes for improved electrical signal transmission as well as for improved mechanical reliability. The cylindrical, quadrangular (square), elliptical, and triangular shapes were investigated in our study and our results showed that the quadrangular shape had the best electrical performance due to good characteristic impedance. Our results also showed that the quadrangular and cylindrical shapes provided improved mechanical reliability as these two shapes lead to high Cu protrusion of TSV after the annealing process.

Keywords: TSV; electrical analysis; mechanical analysis; simulation

1. Introduction

The increasing demand for lower cost, miniaturized, and multi-functional electronic devices with lower power consumption has given rise to a number of new manufacturing challenges. To meet these challenges, the electronics packaging R&D industry has worked hard in recent years to develop novel interconnection materials, process techniques, and packaging technologies such as the through-silicon via (TSV) technologies [1,2].

TSV is becoming a promising solution that can offer the shortest interconnection, minimum chip-to-chip bonding pad sizes and spacing, and can greatly improve the density of integration and performance. Additionally, it can provide novel packaging applications for delivering the highest level of silicon integration and space efficiency at the lowest cost [3–5].

The TSV manufacturing process includes via formation, filling, annealing, and wafer thinning. In general, Cu (copper) is the most widely used material for filling the TSV, and forms the electrical connection between the active side to the backside of the silicon die. High conductivity, low cost, and good compatibility with the multilayer interconnects process are the main merits of using copper as the filler material in the TSV [6].

Although the use of TSV can provide several benefits in implementing 3D packaging and 3D integrated circuits, the TSV fabrication and manufacturing processes have been associated with a number of electrical and mechanical reliability issues and challenges [7].

One of the main electrical reliability issues that have been linked with TSV fabrication and manufacturing processes is the signal degradation due to crosstalk and other switch noises. As TSVs are mostly used for signal and power transmission, TSVs used in high frequency applications tend to be affected by crosstalk signal distortion. Equally, the main mechanical reliability challenge is the formation of Cu protrusion caused by the TSV manufacturing process, which is known to induce high stress levels in the wafer [7–9]. Indeed, because of the large coefficient of thermal expansion (CTE) mismatch between Cu (l6.7 ppm/°C) and silicon (2.3 ppm/°C), the material surrounding the TSV (silicon) can experience several reliability issues such as chip or wafer warpage, interfacial delamination, and cracking. This paper reports on the investigation of different TSV geometries with the focus on identifying the ideal shapes for improved electrical signal transmission as well as for improved mechanical reliability.

2. Electrical Investigation of Through-Silicon Via (TSV) Structures

2.1. Through-Silicon Via (TSV) Structure and Manufacturing Process

The main steps used in TSV fabrication are via-drilling, dielectric barrier deposition, seed layer deposition, Cu-filling by electroplating, and chemical-mechanical polishing (CMP) [10]. The deep reactive ion etching (DRIE) process is used for via-drilling, and the process conditions used are 300 sccm SF_6, 200 sccm, C_4F_8, 400 mtorr pressure, and 250 W RF power. For dielectric barrier deposition, the plasma enhanced chemical vapor deposition (PECVD) is used to make a SiO_2 dielectric barrier to isolate Cu and Si. For seed layer deposition, a high density plasma chemical vapor deposition (HDP CVD) is used to form 0.3 µm Ti and 0.5 µm Cu layers, and they are deposited as seed layers on the dielectric barrier. The electroplating solution for Cu filling is prepared from 100 g $CuSO_4$, 30 mL/L H_2SO_4, and small doses of additive. Plating is performed by applying a periodic pulse reverse (PPR) current. Finally, the Cu-filled silicon wafer is thinned to 60 µm using CMP. The steps described above were used for preparing a 4-inch wafer, consisting of 192 TSVs with 30 µm diameter, and 60 µm height that was used for testing (see Figure 1).

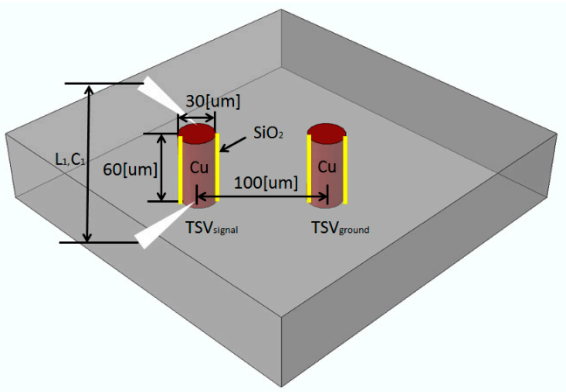

Figure 1. Schematic view of the through-silicon via (TSV) sample.

Electrical parameters such as inductance, L_1, and capacitance, C_1 were measured by a commercial tester of the Agilent Precision LRC meter (model: E4980A, Keysight Technologies Inc., Santa Rosa, CA, USA) in the frequency range of 1 Hz to 1 MHz before implementing the thermal shock test. The thermal shock test was performed to simulate the thermo-mechanical response according to the MIL-STD-833A standard. The temperature range was considered to be between −65 °C and 150 °C (with the dwell and ramp times set to 60 s). Samples were taken at 0, 500, and 1000 cycles. After the thermal shock test, the TSV cross-sections were analyzed by field emission-scanning electron microscopy (FE-SEM).

2.2. Electrical Simulation

The Advanced Design System (ADS), a commercial software, was used for the electrical simulation, and the adaptive sampling frequency (ASF) method was used for the analysis. To simplify the calculation, the dielectric load was ignored due to its small values. For more accurate simulation, the number of mesh and the curved angle were considered as 52 and 45°, respectively. TVS is a very small structure and needs very expensive processing to make the various TVS features. Thus, after manufacturing a single TSV, the characteristic values of the manufactured TSV and the simulated TSV were compared and analyzed. Based on this, various structures of TSVs were analyzed using only the simulation. At low-bandwidth frequencies (1~100 MHz, see Figure 2), the measurements and simulations were performed and compared; at high-bandwidth frequencies (1~10 GHz, see Figure 3 and Figure 5), only simulations were performed because the measurement is difficult.

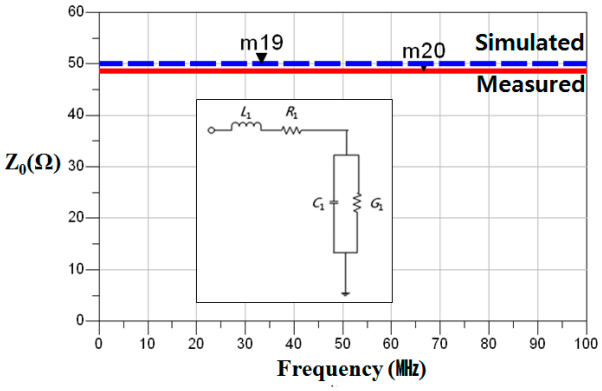

Figure 2. Z_0 and equivalent circuit of Cu filled TSV.

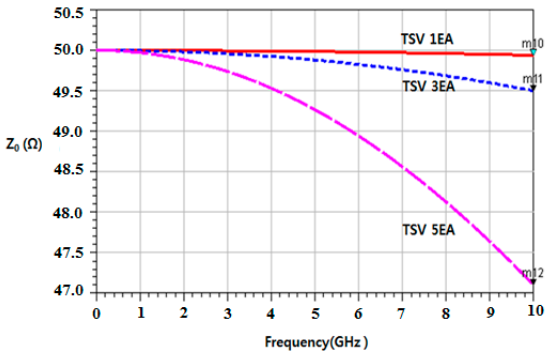

Figure 3. 1EA, 3EA, and 5EA multilayer Z_0 of Cu filled TSV.

Characteristic impedance (Z_0), which is the ratio of the amplitudes of voltage and current of a single wave propagating along the line, is a measure of how effectively the signal is delivered through a transmission line. Z_0 can be expressed by Equation (1), where R is resistance, L is inductance, G is conductance, C is capacitance, j is imaginary unit, and ω is the angular frequency.

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \tag{1}$$

Figure 2 shows that for frequencies in range of 1~100 MHz, Z_0 was measured at 48.5 Ω, whilst the Z_0 value from the ADS simulator was 50.0 Ω (there was a difference of 3% between the measured and simulation values). This difference is due to the fact that the Cu material is assumed as a perfect conductor for the simulation and does not consider the errors that are associated with the TSV manufacturing process, whilst the real Cu material in the fabrication process may have some defects such as micro cracks caused by CMP process after Cu-filling.

The equivalent circuit for the TSV is composed of series inductance (L_1), resistance (R_1), shunt capacitance (C_1), and conductance (G_1). To calculate the electrical parameters, the measured S parameters are converted to the Z parameters by using Equation (2) and then the electrical parameters can be calculated from Equation (3) [11]. The Z parameter is a factor by which input voltage and current, and output voltage and current of the two-port network are related. For any two-port network, input voltage V_1 and output voltage V_2 can be expressed in terms of input current I_1 and output current I_2. Therefore, the Z parameter is defined as $Z_{11} = V_1/I_1(I_2 = 0)$, $Z_{21} = V_2/I_1(I_2 = 0)$, $Z_{12} = V_1/I_2(I_1 = 0)$, $Z_{22} = V_2/I_2(I_1 = 0)$ [11]. Here, the measured result for L_1 and C_1 were 0.052 nH and 0.022 pF, respectively. In addition, from the simulated S parameters, the calculated values of L_1 and C_1 were 0.063 nH and 0.030 pF, respectively.

$$\begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} = \begin{bmatrix} Z_0\frac{(1+S_{11})(1-S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} & Z_0\frac{2S_{12}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \\ Z_0\frac{2S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} & Z_0\frac{(1-S_{11})(1+S_{22})+S_{12}S_{21}}{(1-S_{11})(1-S_{22})-S_{12}S_{21}} \end{bmatrix} \quad (2)$$

$$L_1 = \frac{\mathrm{Imag}(Z_{11} - (Z_{12} + Z_{21}))}{2\pi f}, \quad C_1 = \frac{\mathrm{Imag}(\frac{2}{Z_{12}+Z_{21}})}{2\pi f} \quad (3)$$

2.3. Characteristic Impedance of Multilayer TSV

TSVs are increasingly used in 3D packaging applications as they have the capacity to significantly speed up communication between layered chips, when compared to a planar layout. In this study, we considered the simulation of the characteristic impedance (Z_0) of 1EA, 3EA, and 5EA multilayers in the frequency range of 1~10 GHz. Figure 3 shows the Z_0 for different TSV layers (same Cu filled geometry in each layer) and it was assumed that Z_0 for all multilayers was 50 Ω.

As can be seen, more multiple layers give higher Z_0 values, because the increase in the total TSV length results in more parasitic inductance, which affects signal attenuation and increases the characteristic impedance.

2.4. Characteristic Impedance for Different TSV Shapes

Figure 4 shows the cylindrical, quadrangular, elliptical, and triangular TSV shapes that were considered for the investigation of the characteristic impedance for different TSV shapes.

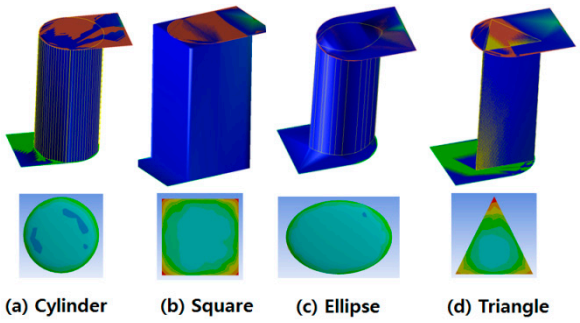

Figure 4. Different TSV shapes considered in the simulation.

Equations (4) and (5) show that the skin effect (δ) is decreased by increasing the frequency; however, this leads to an increase in the effective resistance. This means that the AC current density (J) in a conductor decreases exponentially from its value at the surface (J_S), according to the depth (d) from the surface, where ρ is resistivity, ω is angular frequency, μ is permeability, and ε is permittivity [12–14]. It should also be realized that the effective resistance causes a reduction in Z_0.

$$J = J_S e^{-(1+j)d/\delta} \quad (4)$$

$$\delta = \sqrt{\frac{2\rho}{\omega\mu}}\sqrt{\sqrt{1+(\rho\omega\epsilon)^2}+\rho\omega\epsilon} \quad (5)$$

Figure 5 shows the characteristic Impedance for single TSV layers with different shapes in the frequency range between 1 and 10 GHz. As can be noted, in the low frequency (LF), there is no difference in Z_0 for different TSV shapes, however, in high frequency (HF), the quadrangular (square) TSV shape had better electrical performance compared to the other shapes. This is because the quadrangular TSV shape has a higher insulating layer due to its large outer area and hence protects the signal more than other shapes. It should be noted that in case of multilayer TSVs, the effect of signal attenuation will further deteriorate the characteristic impedance (will lead to more reduction).

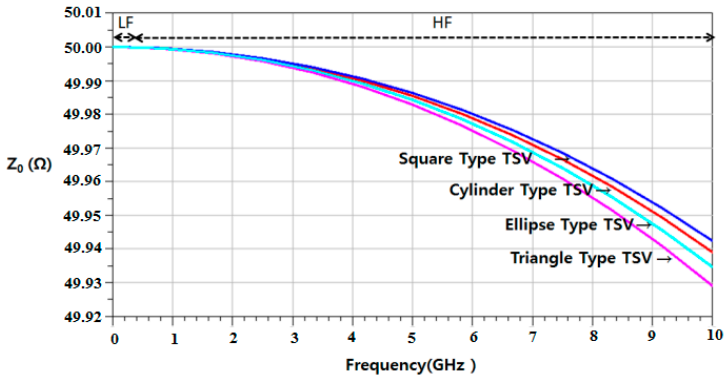

Figure 5. Characteristic impedance (Z_0) for different TSV shapes.

3. Mechanical Investigation of TSV Structures

One of the main reliability issues associated with the TSV fabrication process is the protrusion of Cu due to the Cu–Si CTE mismatch. Figure 6 shows the cross section of the Cu-filled TSV after 500 and 1000 cycles of the thermal shock test. After 1000 cycles, voids and cracks due to electro migration and protrusion (resulting from stresses induced by CTE mismatch) were found on the opening side and the wall side of the TSV. To reduce the effect of protrusion and improve the mechanical reliability of TSV, the annealing process is an effective approach that can be done in the fabrication process.

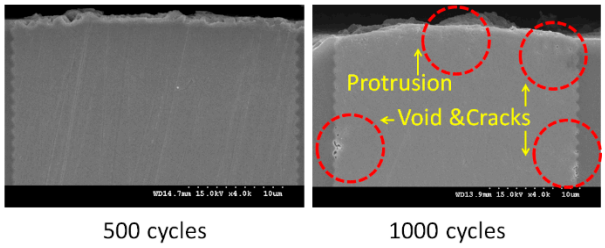

Figure 6. Thermal shock test (500 and 1000 cycles) of Cu filled TSV.

3.1. Finite Element Simulation (FEM)

ABAQUS 6.14 software was used for investigating the Cu protrusion of TSV that results during the annealing process for each of the TSV geometries. This finite element simulation (FEM) software was selected for its features in accurately investigating the nonlinearities in the geometry and material properties. Two symmetrical boundary conditions were applied to the FE models (only one symmetric plane in case of triangular shape). Three-dimensional continuum elements "C3D8R" with a fine mesh density in the Cu region were used to provide enough convergence in the results. As maximum protrusion appears at the maximum temperature, which is independent of the dwell time, therefore, dwell time was not taken into account. In addition, cooling time was not considered because of reduced protrusion during cooling. The annealing temperature used in the simulation was between 250 °C and

450 °C, while the temperature ramp rate was 5 °C/min [15]. Additionally, the temperature and time dependency of the materials (such as creep behavior) were not considered in this work. However, to find the Cu protrusion, plastic behavior (non-reversible deformation) was considered during rising temperatures. Table 1 shows the mechanical properties of the used materials in the simulation (Cu and Si) [15].

Table 1. Mechanical properties of the materials in the simulation.

Mat.	Poisson's Ratio	CTE (ppm/k)	Young Modulus (GPa)	Plastic Curve, Stress (MPa) vs. Strain
Cu	0.34	17.3	121	121@0.001 186@0.004 217@0.01 234@0.02 248@0.04
Si	ν_{yz} = 0.36 ν_{zx} = 0.28 ν_{xy} = 0.064	2.8	Ex = Ey = 169 Ez = 130 Gyz = Gzx = 79.6 Gxy = 50.9	Fully elastic

3.2. Protrusion on Single Layer TSV

Figure 7 displays the vertical deformation of the mid cross section of the cylindrical Cu filled TSV for temperatures between 250 °C and 450 °C. This FEM result showed that a greater annealing temperature induces further thermal expansion on the TSV.

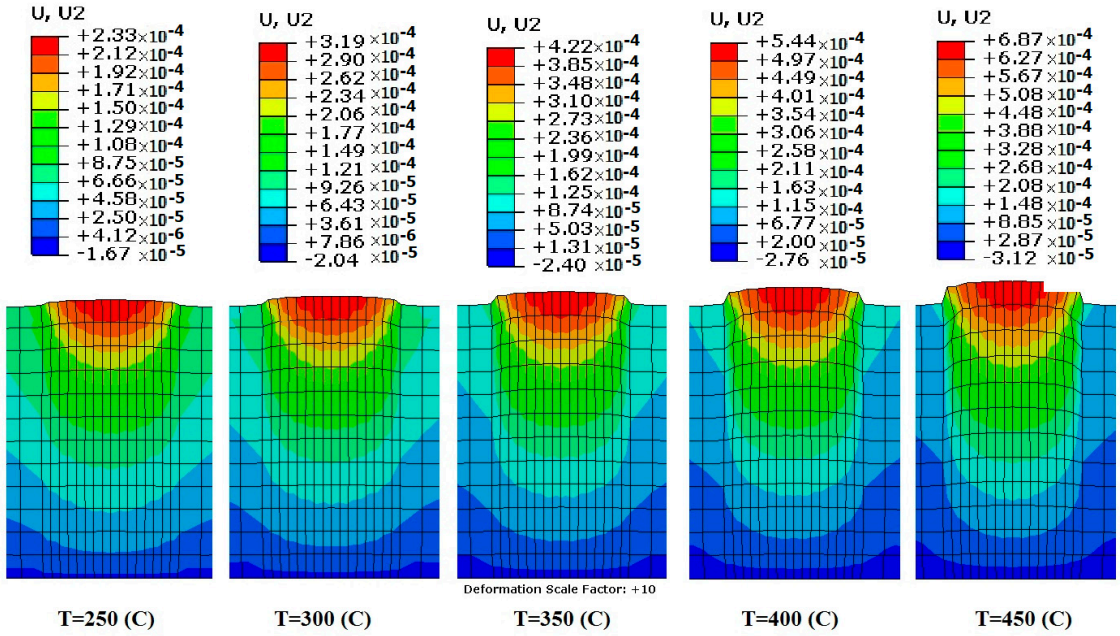

Figure 7. Vertical deformation of the cylindrical TSV shape (in mm).

3.3. Protrusion on Multilayer TSVs

Figure 8 shows the Cu protrusion for the 1EA, 3EA, and 5EA multilayer TSV under annealing temperatures from simulation. The diameter and height of each TSV layer were considered as 30 µm and 60 µm, respectively. From the results, the protrusion height of 1EA (single layer), 3EA, and 5EA were found to be 0.47 µm, 0.36 µm, and 0.35 µm, respectively, at 450 °C. For multilayer TSVs, the protrusion height was saturated because the top layers tended to expand in two sides of the vertical direction and the bottom surface of each layer compressed the top surface of bottom layer. Indeed, in the bottom

layers, the upward thermal expansion was limited by downward expansion of its top layer. However, in the single layer, the top surface was completely free to expand, and hence the protrusion was higher than that of the multi-layer. The results showed that multilayer TSVs have less reliability as they have less Cu protrusion, and they also have a higher probability for cracks due to high stress level induced by the interaction between multilayers that are in contact.

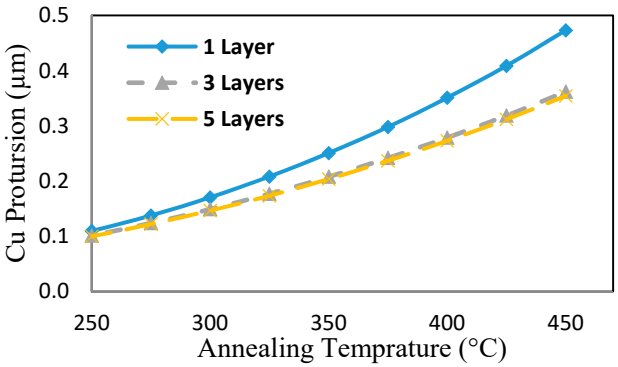

Figure 8. Cu protrusions of multilayer TSVs via annealing temperature.

3.4. Effect of TSV Height on the Protrusion

The results for Cu protrusion of different cylindrical TSV height (from 60 μm to 600 μm) with a 30 μm diameter are shown in Figure 9. This figure shows that at 450 °C annealing, the protrusion height of 60 μm TSV was 0.47 μm, but decreased to about 0.33 μm for TSVs taller than 120 μm. During the high temperature annealing process, the Cu surface goes into plastic phase and plastic behavior can directly affect the expansion of Cu. As can be noted in Figure 9, by increasing the height of the TSV from 60 μm to values higher than 120 μm, the magnitude and height of the plastic region decrease from 45 μm to 40 μm. Indeed, the plastic height of TSV determines the extent of protrusion (plastic height of TSV is more important TSV height; higher plastic height leads to higher protrusion).

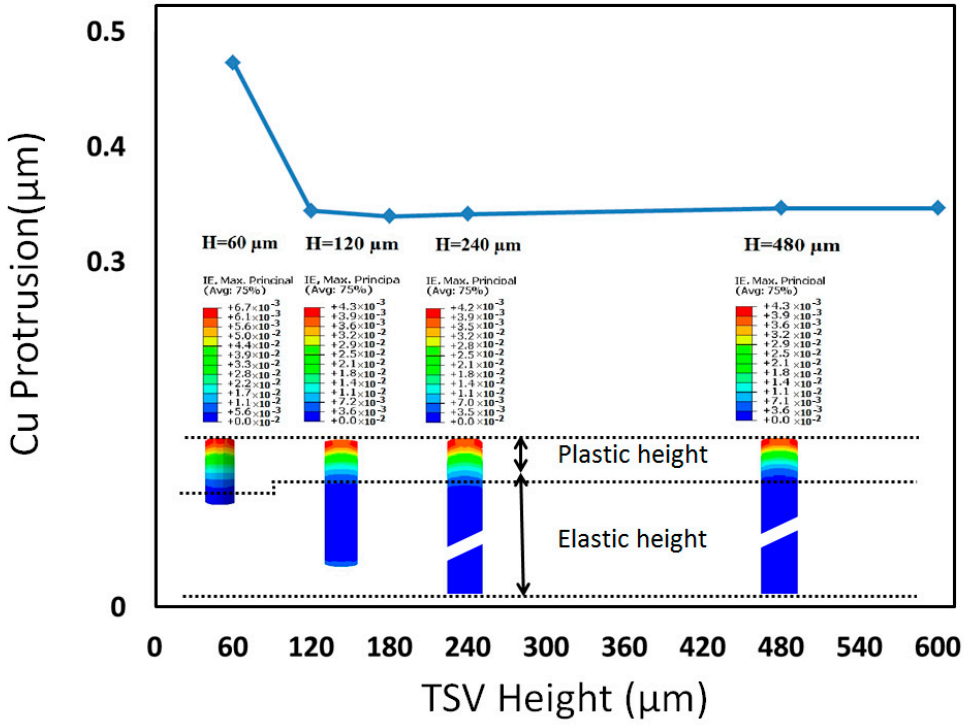

Figure 9. Cu protrusion of cylindrical TSV with different heights (maximum principal plastic strain distribution is also shown).

3.5. The Protrusion and Stress Analysis for Different TSV Shapes

Figure 10 displays the Von-Mises stress distribution in Si material for different TSV shapes at the 450 °C annealing temperature. For all TSV shapes, the maximum Von-Mises stress was concentrated on the bottom of the TSV and as can be noted, they had almost the same magnitude and distribution of stress (the maximum stress range was between 1.07 GPa and 1.24 GPa).

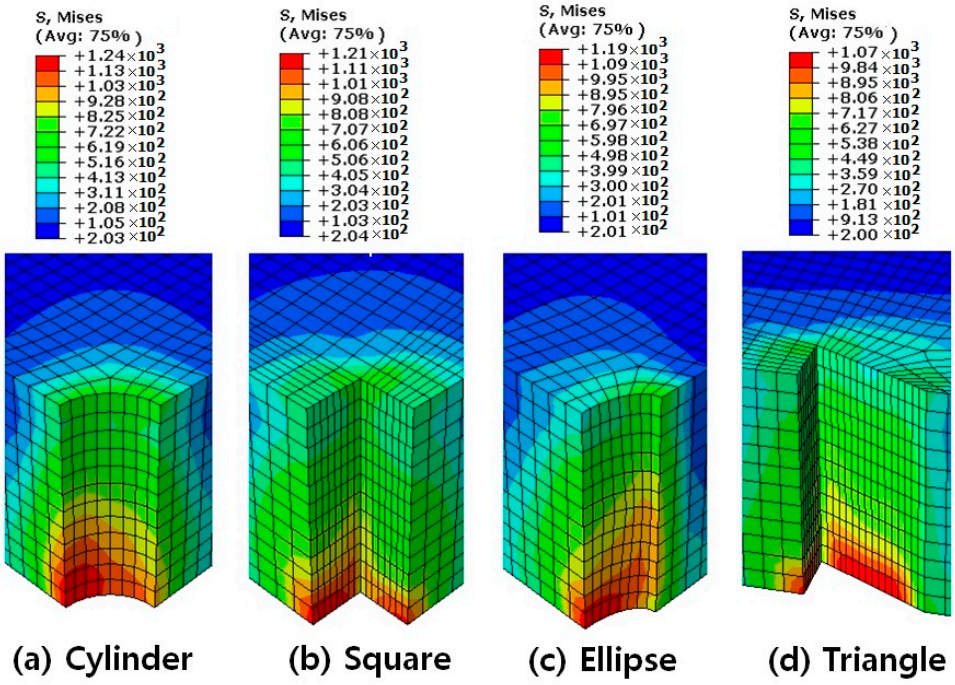

Figure 10. Von-Mises stress distribution in different TSV shapes at 450 °C.

Figure 11 compares the Cu protrusion and maximum Von-Mises stress in Si for different TSV shapes after the 450 °C annealing process. As can be seen, the Cu protrusion of cylindrical, quadrangular, elliptical, and triangular shapes was 0.47 µm, 0.44 µm, 0.25 µm, and 0.17 µm, respectively. If we assume no differences in silicon stress levels for the different TSV shapes, then the cylindrical and quadrangular TSV shapes are more mechanically reliable due to reaching a higher Cu protrusion. It follows that the annealing process releases the internal stresses and causes Cu protrusion at the entrance of the TSV. The high Cu protrusion means that the internal stresses of the TSV have been released more and can suggest more reliability. The final TSV produced by the annealing process followed by the CMP process used for removing the CU protrusion led to a lower internal stress level.

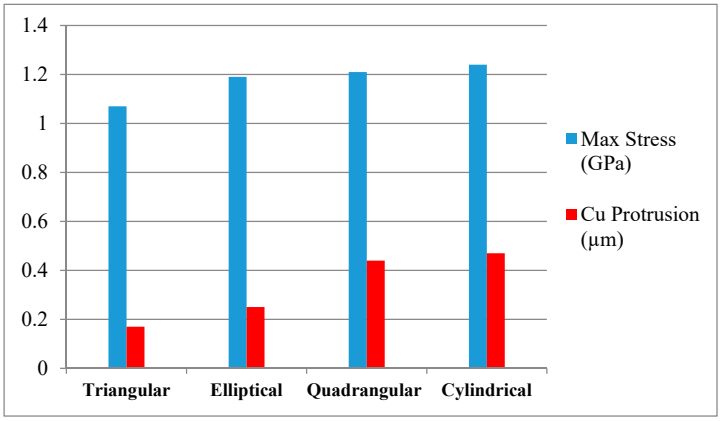

Figure 11. Cu protrusions and max induced stress in Si for different TSV shapes at 450 °C.

4. Conclusions

This paper reports on the investigation of different TSV geometries with the focus on identifying the ideal shapes for improved electrical signal transmission and improved mechanical reliability. The cylindrical, quadrangular (square), elliptical, and triangular shapes were investigated in our study and our results showed that the characteristic impedance (Z_0) for all multilayers investigated were about the same. The single layer TSV showed a higher Cu protrusion (due to reaching higher plastic height); increasing the number of layers did not lead to any significant change in the Cu protrusion height. However, the TSV Cu protrusion decreased for 60 µm to a 120 µm TSV height, and then remained constant for taller TSVs. In terms of TSV shape, the cylindrical and quadrangular TSV shapes showed improved mechanical reliability when compared with the elliptical and triangular shapes. Our results also showed that in low frequencies (less than 1 GHz), Z_0 is constant for different TSV shapes, but in high frequencies, the quadrangular TSV shape showed improved electrical performance (due to having a higher insulating layer and better protecting the signal).

Author Contributions: I.H.J., performed the experiments, measurements and developed the first draft of the paper. A.E.M. undertook FEM simulations and results. J.P.J. and N.N.E. supervised the work and contributed to developing the outline of the paper. All co-authors contributed to the response of reviewers' comments and have read and agreed to the final published version of the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflicts of interest.

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