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Investigation on the Implementation of Stateful Minority Logic for Future In-Memory Computing

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ABSTRACT In-memory computing is one of the best ways to solve the delay and power consumption issues of traditional von Neumann structures in the current Internet of Things and big data era. The realization of in-memory computing based on memristors is being widely studied because of its simple structure, high integration, and compatibility with CMOS technology. Minority logic is considered as the most suitable to realize computation function, and the basic cell based on memristors to implementing minority logic has also been proposed. However, from our analysis, it has requirements on device electrical character. After fabricating resistance random access memory (RRAM) devices that meet basic requirements, demonstration still cannot achieve. Through theoretical derivation and simulation, resistance variation is the main reason for wrong results. Moreover, high variation devices with existing technology can be challenging to demonstrate the basic logic cell.

INDEX TERMS In-memory computing, minority logic, memristor, resistance variation, low power computation.

I. INTRODUCTION

Traditional von-Neumann architecture faces significant challenges on the power consumption caused by the separation between the memory and CPU. Exploring in-memory computing (IMC) using beyond-CMOS devices has been considered a promising pathway towards low-power computation. Wherein, IMC based on RRAM [1], [2] has raised great interest because of the simple structure, high density, good scalability, and CMOS compatibility. Besides, RRAM based IMC can be divided into two types, stateful logic and memristor-transistor logic. There have been several stateful logic methods to realize logic function and further the logic circuit in the memory array, e.g., material implication (IMPLY) [3], memristor aided logic (MAGIC) [4]. In 2008, the lab of HP proposed the IMPLY structure and they first used the resistance state of RRAM as logical variables. However, the problem of IMPLY and its variance [5] is that additional and stable resistors are required. Besides, long time operation is necessary to form complex logic functions, and the output will cover the input after operation. In 2012, the MAGIC structure was proposed to solve the problem of external resistance and coverage. The design practices of logic circuits based on MAGIC NOR gate were studied and effective synthesis methods were reported [6]. However, the issue that requiring long operation steps to realize complex logic functions still exists because the NOR function has low flexibility. Besides, the stringent requirement for V_{SET}/V_{RESET}, which most RRAM devices cannot satisfy, is also a severe challenge [7]. Due to the limitation that more peripheral circuits are needed to realize logic operation in the memory array [8], stateful logic usually suffers more latency and power consumption.

Memristor-transistor logic (MTL) is also one promising technology, likened to conventional CMOS logic [9]. The CMOS-like gates have similar structure to their CMOS counterparts. The RRAM devices are used with threshold voltages, instead of NMOS/PMOS. Voltages represent both the logic input and logic output variables. Besides, it has the advantage of being more suitable to use the existing EDA tools to optimize the circuit design. However, the disadvantage is the extremely slow speed compared with CMOS.

Recent research [10]–[13] has confirmed that majority logic can implement arithmetic-intensive circuits with fewer gates, and it has been proved that Majority-based logic can

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achieve up to 33% reduction in logical depth compared to And-based logic [13]. For example, when comparing with IMPLY, the computation efficiency of the mathematical addition doubles with the majority logic, which is one particular case of the threshold logic [14]. Various realizations of the majority logic have been demonstrated on RRAM arrays, either using the voltage/resistance [15] or resistance/voltage [16] as input/output state variables.

The key challenges are 1) they are non-stateful logic where the conversion between voltage and resistance is required, which complicated both the operation procedure and the circuit design; 2) Majority logic is functionally incomplete and the logic NOT is needed, making it impossible for homogenous implementation with simple design.

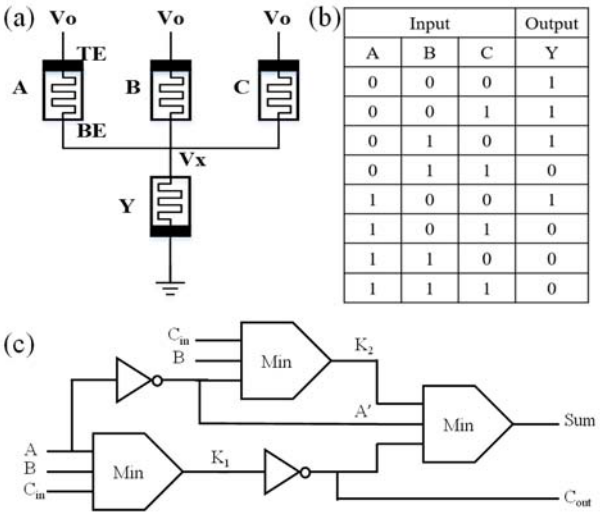
The minority logic, which is the inverted majority logic, is function completeness and therefore can be an ideal alternative. Quantum-dot cellular automata (QCA)-based minority logic gate has been fabricated, and circuit modules designed based on the minority logic, such as 2to4 decoder and multiplexer, are also designed and simulated. Recently, the theoretical design for the stateful minority logic using RRAM, the so-called fast and energy-efficient logic-in-memory (FELIX), was proposed by S. Gupta et al [17]. The aforementioned challenges can be tackled if FELIX is realized with practical RRAM technologies. In this paper, we derived the requirements of RRAM on asymmetric I-V curve in the implementation of FELIX. The Cu/ZnO/Pt structure devices that can meet the requirements are fabricated according to the specific process. By testing the basic circuit cell with different input patterns and checking the logic output, we found that the output of one case is different from the theoretical value. Based on the analysis, we first show that the realization of FELIX is difficult to achieve due to the unavoidable intrinsic variation.

II. BASIC LOGIC CELL

The resistance state of RRAM is used as logical variable, and here we define the high resistance state (HRS) and low resistance state (LRS) of the memristor as logic 0 and logic 1, respectively. By using Ohm's law and Kirchhoff's law, which are both resistance-based laws, data storage and logic computing can be realized in memory arrays, which can solve the ''storage wall problem'' as mentioned above.

The structure of minority basic logic cell is shown in Fig. 1(a), in which the initial resistance states of RRAM A, B, C are logical inputs, while the final resistance state of Y after operation is logical output. The operation consists of two steps, and the first step is initializing the Y to LRS. The second step is applying V_o at the top terminal of A, B, and C, and grounding the top terminal of Y.

After applying corresponding voltage, the voltage at the node of bottom electrode V_x is determined by the resistance states of input RRAMs. All possible inputs can be divided into four categories: LLL, LLH, LHH, and HHH. Wherein each character denotes the state of one input RRAM. For different inputs, the voltage V_x can be different, which in turn



Input			Output
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

FIGURE 1. (a) The circuit structure of proposed basic logic cell. There are four RRAMs in one row, consisting of three inputs A, B, and C, and the output result is stored in Y. (b) Truth table for eight combinations of three inputs and corresponding outputs. (c) Structure of 1-bit addition based on Minority and NOT gate.

affects the switching behaviour of Y. Since mature RRAMs have large resistance ratio, RRAMs with HRS can be considered as open circuit when they are in parallel to other RRAMs of LRS. Thus, V_x is only controlled by the LRS. The requirement for the switching voltage is elaborated below:

- Inputs with more than one RRAM in LRS (LLH or LLL): the total resistance for input RRAMs is smaller than the value of Y. More than half of V_o will fall on the RRAM Y. For example, $V_x = 3/4V_o$ under LLL and $V_x = 2/3V_o$ under LLH. Y must be RESET to HRS for both cases.
- Inputs with more than one RRAM in HRS (LHH or HHH): the total resistance for input RRAMs is larger than the value of Y. V_x is lower than half of V_o. For example, $V_x = 1/2V_o$ under LHH and $V_x = 0$ under HHH. In either case, no RESET should happen, and Y keeps its initial state.

According to the analysis above, the truth table for this basic cell is shown in Fig. 1(b), and the logic function derived is written as Eq. (1). Besides, it can be converted to another version on the next line by a simple derivation, from which we can see that if we preset C as logic 1 (write LRS to memory cell), NOR gate is formed; if we preset C as logic 0 (write HRS to memory cell), NAND gate is formed. Besides, when both B and C are preset into 1 and 0 respectively, NOT gate for input A is formed.

$$\begin{aligned} Y &= \overline{AB + BC + AC} \\ &= \overline{C(A + B) + \overline{C}(AB)} \end{aligned} \tag{2-1}$$

Because both the NAND gate and NOR gate are logical completely, all kinds of digital circuits can be realized by this basic logic function, thereby realizing logic operations in the memory structure is feasible. Compared to other logic

TABLE 1. Expression of 1-bit full adder based on minority logic gate.

Output	Expression
K_1	minority (A, B, C_{in})
$K_1'(C_{out})$	minority (K_1, 0, 1)
A′	minority (A, 0, 1)
K_2	minority (A′, B, C_{in})
Sum	minority (A′, K_1', K_2)

cells realized by existing in-memory computing architecture, this logic function has more degree of freedom, so it may help when realizing complex digital circuits. For example, it is worth mentioning that the logic function result of this proposed structure and the output signal C_{out} of the full adder, which equals $AB + BC_{in} + AC_{in}$, are a pair of opposite signals.

The expression and operating steps of 1-bit adder are derived in Table 1, and the proposed circuit structure is shown in Fig. 1(c), which consists of three minority logic gates. In a ripple-carry adder, the generation and propagation of C_{out} are critical path, which determines the speed and power consumption, so the realization of the N-bit adder can be accelerated and the power consumption is lower compared with other in-memory computing methods.

However, the circuit raised some requirements to RRAM electrical characteristic. On one hand, when input RRAMs are dominated by LRS, the minority logic requires that the output RRAM, Y, resets to HRS when $V_x = 2/3V_o$ and remains at LRS when $V_x = 1/2V_o$. Therefore, the reset voltage, V_{RESET}, must lie in between. As a result, operation voltage V_o should be set to satisfy:

$$1.5 \times |V_{RESET}| < V_o < 2 \times |V_{RESET}| \tag{2-2}$$

On the other hand, when input RRAMs are dominated by HRS, V_x is either $1/2V_o$ or 0, both of which will not trigger the RESET process. However, in such a situation, the input RRAMs are positively biased at the voltage level of more than $1/2V_o$, leading to undesirable SET operation. Therefore, the set voltage, V_{SET}, should lie above its maximum possible value, occurring as V_o under HHH condition. Requirements of V_{SET} can be written as:

$$V_o < V_{SET} \tag{2-3}$$

The relationship between V_{SET}, V_{RESET} and V_o is shown in Fig. 2. According to (2-2) and (2-3), not only a range of V_o is restricted, but also a requirement for device character is needed, as written in (2-4).

$$V_{SET} > 1.5 \times |V_{RESET}| \tag{2-4}$$

The range $\Delta V = 2/3V_o - 1/2V_o$ is an approximation when HRS $\gg$ LRS, so in general cases, this range should be analyzed clearly. By defining the ratio of HRS and LRS as m, then this range is a function of m, which can be written as:

$$\Delta V = \frac{2m+1}{3m+1} \cdot V_o - \frac{m+2}{2m+2} \cdot V_o \tag{2-5}$$

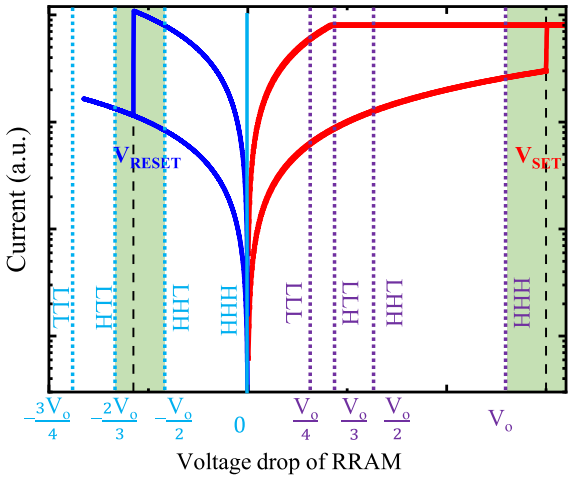


FIGURE 2. The voltage drops between TE and BE of output (blue) and input (purple) RRAM. For output RRAM, voltage drop equals -V_x, while for input RRAM, voltage drop equals (V_o-V_x). The requirement for the V_{SET} and V_{RESET} of minority logic is marked in green.

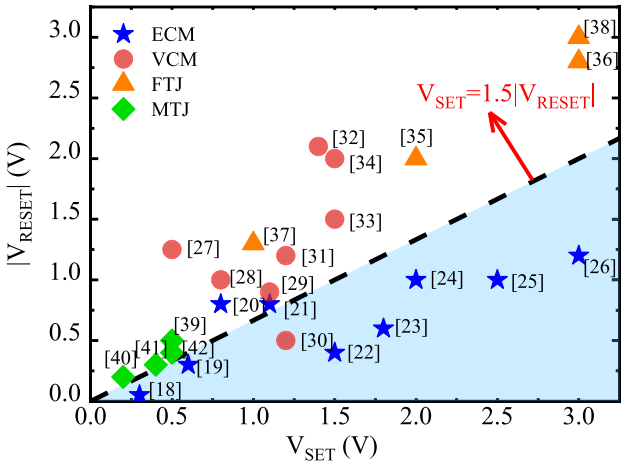


FIGURE 3. A statistic of SET and RESET voltage of ECM RRAM, VCM RRAM, FTJ and MTJ.

Besides, when m > 20, this range almost reaches the maximum value. Due to the variation of the resistance of the device, its high resistance and low resistance have upper and lower limitations, defined as RH_max, RH_min, RL_max, RL_min. Considering the worst case, it is necessary to ensure that each basic cell works normally with RH_min > m * RL_max.

By far, researchers have found that electrochemical conduction mechanism (ECM) RRAM has an asymmetric I-V curve compared with other memristor types. As shown in Fig. 3, a statistic of V_{SET} and V_{RESET} of ECM RRAM [18]–[26], vacancy conduction mechanism (VCM) RRAM [20], [27]–[33], ferroelectric tunneling junction (FTJ) [34]–[37] and magnetic tunneling junction (MTJ) [38]–[41], means that due to different conductive mechanism, using Cu or Ag as electrodes leads to more asymmetric I-V curve.

III. DEVICE FABRICATION

Here, we fabricated a Pt/ZnO/Cu structure devices as shown in the inset of Fig. 4, which is supposed to serve as ECM

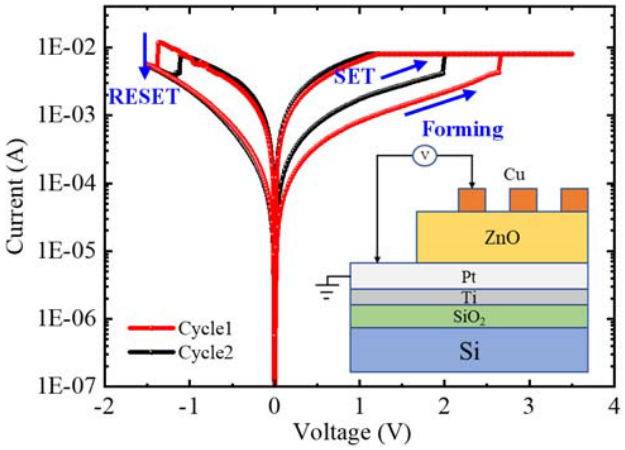


FIGURE 4. The typical I-V curve of devices used in this work, the red line is forming process, with lower initial resistance and higher set and reset voltage. The inset is device structure of fabricated RRAM, Cu/ZnO/Pt, and substrates on a Ti layer.

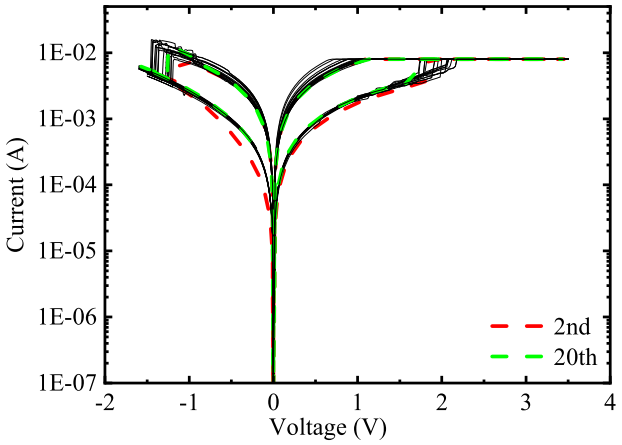


FIGURE 5. The typical I-V curve of 20th SET-RESET cycles, while the red dash line represents the 2nd cycle and the green dash line represents the 20th cycle.

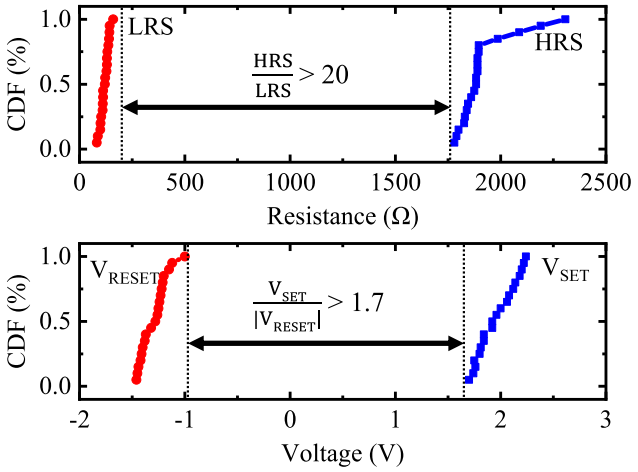


FIGURE 6. Cumulative distribution of V_{SET} and V_{RESET} and cumulative distribution of LRS and HRS.

device. 100nm Cu was deposited on a commercial SiO_2/Si substrate by rf magnetron sputtering at room temperature. 80nm ZnO film was deposited by plasma-enhanced atomic layer deposition (PEALD), using H_2O and Diethyl zinc as precursors, and the deposition rate was about 0.2nm each cycle. As top contacts, sputter-deposited platinum was used with a diameter of 50 μm$\sim$300um, patterned by a shadow mask, using a commercial sputter-coater. After these films are fabricated, wet etch process is used to expose the Cu bottom electrode for electrical testing. The current-voltage (I-V) characteristics of the Pt/ZnO/Cu/SiO_2/Si devices were measured at room temperature in air using a Keithley 4200A-SCS semiconductor parameter analyzer connected to a Kelvin ST-500 probe station. The bias was applied to the top electrode.

The typical I-V curve is shown in Fig. 4. As shown, the I-V curve is asymmetric under positive and negative voltage sweep, due to the different set and reset process mechanisms. By applying a positive voltage to the Cu TE, Cu atoms dissolute and migrate into ZnO film under the applied electric field. The migration of Cu ions eventually leads to a reduction at Pt BE and Cu atoms conductive filament (CF) formed from BE to TE. As a result, a large current flowing through this filament immediately reaches the compliance current (Icc), and the voltage is V_{SET}. Once the bias polarity is reversed and compliance current removed, Cu atoms filament is broken either by reduction or Joule heating so that low current can flow, corresponding to high resistance state, and the voltage is V_{RESET}. The red line shows forming process, the initial resistance of free device is 4KΩ, and it switches to LRS = 70Ω at $V_{FORM} = 2.64$V with compliance current Icc = 8mA, which means conductive filament of Cu first formed due to oxidation of Cu ions originating from top electrode.

Device switches to HRS = 1.5KΩ at $V_{RESET} = -1.3$V, which means the CF ruptured partially with a gap remaining between undissolved CF and Cu electrode. As a result, CF is much easier to form in the next process of positive voltage sweeping, corresponding to a lower switching voltage at $V_{SET} = 2$V. After applying negative voltage, the CF ruptured by reduction of Cu atoms again, which means the device switches to HRS, with resistance ratio >20. These experimental results imply that the device has $|V_{SET}/V_{RESET}| > 1.7$ and HRS/LRS >20, which can satisfy the requirements of basic logic cell mentioned before. In Fig. 5, sweep results of 20 cycles on one fresh RRAM device are tested, and the variation character is summarized. As shown in the upper part of Fig. 6, the V_{SET} varies from 1.8V to 2.4V while V_{RESET} varies from -0.8V to -1.2V, and this range still satisfies the requests mentioned in Eq. (4). The resistance variation is shown in lower part of Fig. 6, and it also satisfies the requests of resistance ratio over 20 with $\sigma_R = 0.3$.

We considered the simulation results of basic logic through Cadence Spectre based on VTEAM model. As shown in Fig. 7, a Cadence Verilog-A model is designed to fit the experimental data. The simulation result of logic output is shown in Fig. 8. In each cycle, inputs change and after operating, the

TABLE 2. Power consumption.

Input Pattern	Average Power Consumption
LLL	24.6pJ
LLH	24.4pJ
LHH	169pJ
HHH	7pJ

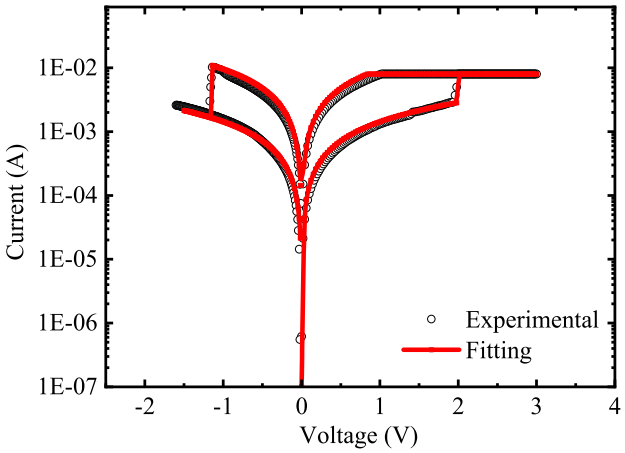


FIGURE 7. I-V curve of Experimental data (points) and Fitting data (line).

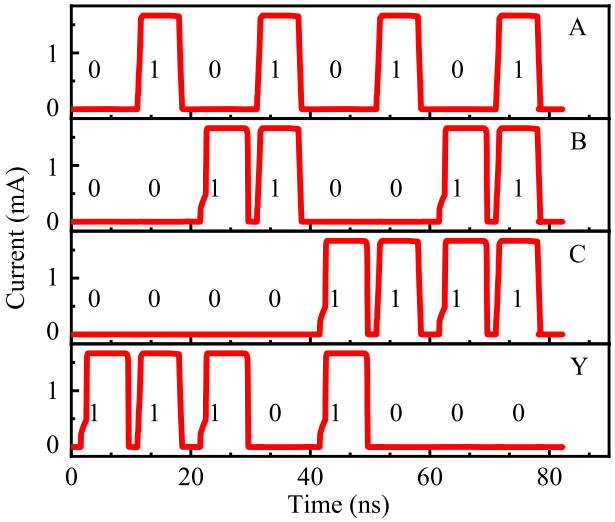


FIGURE 8. Simulation result of eight combinations of input cases, corresponding to the truth table.

results are saved as resistance state of RRAM Y, corresponds to the truth table from top to down. Besides, the simulation result of power consumption for different input patterns are shown in Table 2.

IV. VARIATION ANALYSIS

In order to demonstrate the functional correction of basic logic cell with fabricated devices in this work, we test the basic cell with four probes on the TE of RRAMs and one at the intermediate node and the results are shown below.

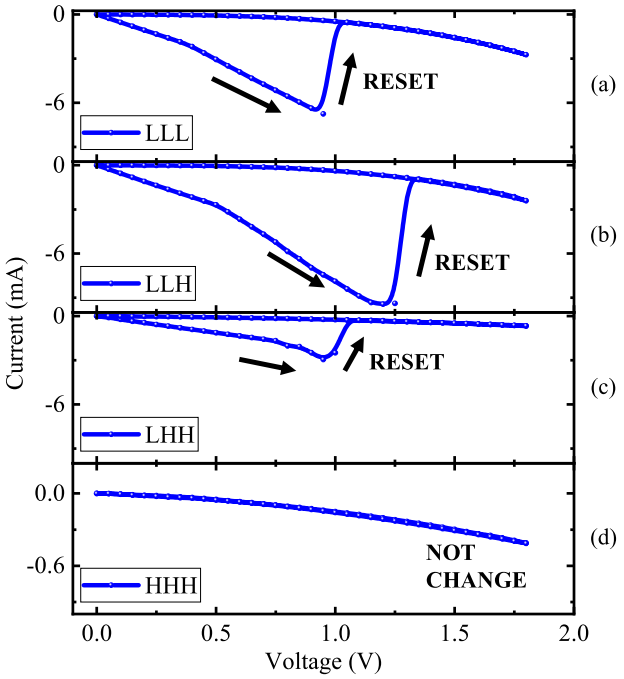


FIGURE 9. Current change of RRAM Y with input cases (a) LLL. (b) LLH. (c) LHH. (d) HHH.

We choose 4 RRAM cells from the sample to apply triangular waveform on TE of input RRAMs and grounding output RRAM. With another probe on ZnO film to record the current flowing through output RRAM Y.

When inputs are LLL or LLH, the output RRAM Y should finally reset to HRS due to V_x larger than $|V_{RESET}|$, as shown in Fig. 9(a) and Fig. 9(b). When inputs are LHH or HHH, the output RRAM Y should finally maintain LRS due to V_x smaller than $|V_{RESET}|$. However, from the result of Fig. 9(c), while input LLH, RRAM Y outputs HRS instead of the correct state of LRS. The output of HHH is correct, as shown in Fig. 9(d).

Here we discuss the reason for the wrong results of case LLH by analyzing resistance and switch voltage variation. For simplicity, we firstly only consider that V_{RESET} has variations. Assuming the average value and the variation of V_{RESET} is μ_{VRESET} and σ_{VRESET}, the following two requirements must be met to guarantee the circuit design with a target yield of three sigma:

- For LLH, the maximum allowable $|V_{RESET}| = (1 + 3\sigma_{VRESET}/\mu_{VRESET}) \cdot \mu_{VRESET}$, should not exceed $L/(L/2 + L) \cdot V_o = 2/3V_o$.
- For LHH, the minimum allowable $|V_{RESET}| = (1 - 3\sigma_{VRESET}/\mu_{VRESET}) \cdot \mu_{VRESET}$, should be higher than $L/(L + L) \cdot V_o = 1/2V_o$.

The maximum allowable σ_{VRESET} occurs when μ_{VRESET} is in the middle of the window, as shown in Fig. 10(a). This gives:

$$\mu_{VRESET} = 0.5 \cdot (2/3 + 1/2) \cdot V_o = 7/12 \cdot V_o \quad (4\text{-}1)$$

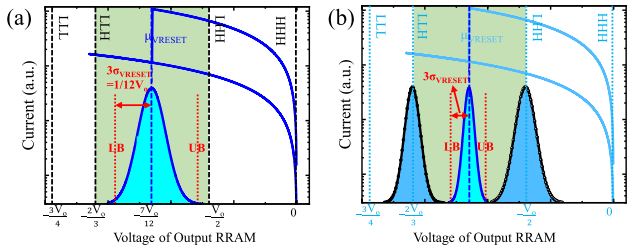


FIGURE 10. (a) Negative sweep for RRAM with V_{RESET} variation and voltage levels for different input cases. (b) Boundary change after considering resistance variation σ_L/μ_L and corresponding change of $\sigma_{VRESET}/\mu_{VRESET}$.

$$\sigma_{\mathrm{VRESET}} = 2/3 \cdot \mathrm{V_o} - \mu_{\mathrm{VRESET}} = 1/12 \cdot \mathrm{V_o} \quad (4\text{-}2)$$

$$\max(\sigma_{\mathrm{VRESET}}/\mu_{\mathrm{VRESET}}) = 1/21 \quad (4\text{-}3)$$

As we can see, in this simplified condition, the maximum normalized variation, $\sigma_{\mathrm{VRESET}}/\mu_{\mathrm{VRESET}}$, is a constant.

Then, if we further consider the resistance variation, it is expected that the tolerance becomes even lower, as shown in Fig. 10(b).

When input case is LLH, the right boundary of voltage level is determined by the maximum pull-up resistance, which changes from $\mu_L/2$ to $(1 + 3\sigma_L/\mu_L) \cdot (\mu_L/2)$, and the minimum pull-down resistance, which changes from μ_L to $(1\text{-}3\sigma_L/\mu_L)\cdot\mu_L$. Due to the requirement that the left boundary of V_x should be lower than the LB of $|V_{RESET}|$, a conjoint relationship between σ_L and σ_{VRESET} is derived in (4-4).

$$\frac{\left(1 - 3\cdot\frac{\sigma_L}{\mu_L}\right)\cdot\mu_L}{\left(1 + 3\cdot\frac{\sigma_L}{\mu_L}\right)\cdot\frac{\mu_L}{2} + \left(1 - 3\cdot\frac{\sigma_L}{\mu_L}\right)\cdot\mu_L}\cdot \mathrm{V_o} > \left(1 + 3\frac{\sigma_{\mathrm{VRESET}}}{\mu_{\mathrm{VRESET}}}\right)\cdot\mu_{\mathrm{VRESET}} \quad (4\text{-}4)$$

When input case is LHH, the left boundary of voltage level is determined by the minimum pull-up resistance, which changes from μ_L to $(1\text{-}3\sigma_L/\mu_L)\cdot\mu_L$, and the maximum pull-down resistance, which changes from μ_L to $(1 + 3\sigma_L/\mu_L)\cdot\mu_L$. Due to the requirement that the right boundary of V_x should be larger than the UB of $|V_{RESET}|$, the corresponding expression is shown in (4-5).

$$\frac{\left(1 + 3\cdot\frac{\sigma_L}{\mu_L}\right)\cdot\mu_L}{\left(1 - 3\cdot\frac{\sigma_L}{\mu_L}\right)\cdot\mu_L + \left(1 + 3\cdot\frac{\sigma_L}{\mu_L}\right)\cdot\mu_L}\cdot \mathrm{V_o} < \left(1 - 3\frac{\sigma_{\mathrm{VRESET}}}{\mu_{\mathrm{VRESET}}}\right)\cdot\mu_{\mathrm{VRESET}} \quad (4\text{-}5)$$

From (4-4) & (4-5), a relationship between σ_L/μ_L and $\sigma_{VRESET}/\mu_{VRESET}$ can be estimated, as shown in Fig. 11(a). The area below both curves means σ_L/μ_L and $\sigma_{VRESET}/\mu_{VRESET}$ that can satisfy the two equations and can implement the logic correctly. Besides, we found that the curve from (4-4) is higher than that from (4-5). It is because when input case is LLH, the variation is lower due to parallel connection of two RRAMs, and as a result, the range of

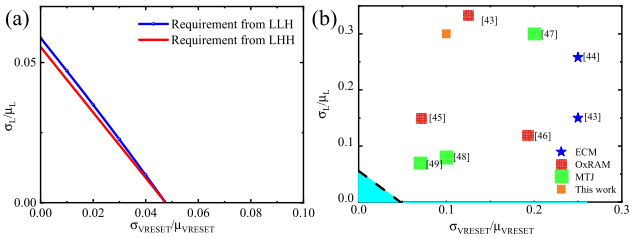


FIGURE 11. (a) Requirement from case LLH and LHH. (b) Relationship between $\sigma_{VRESET}/\mu_{VRESET}$ and σ_L/μ_L.

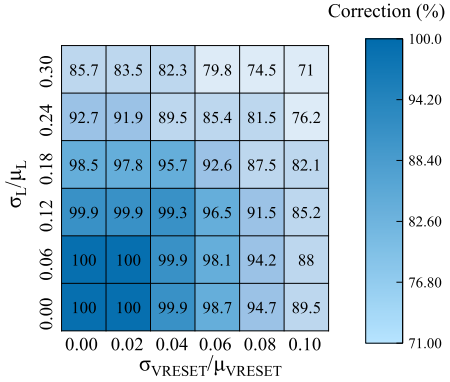


FIGURE 12. Correction changes with different σ_L/μ_L and $\sigma_{VRESET}/\mu_{VRESET}$.

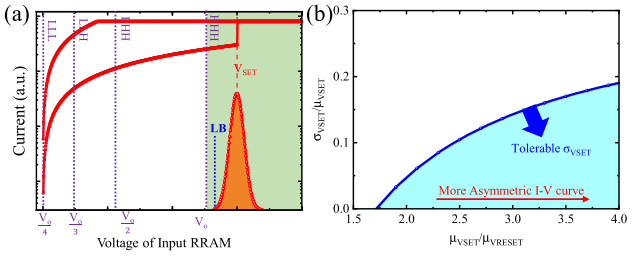


FIGURE 13. (a) Positive sweep for RRAM and voltage levels for different input cases. (b) Relationship between the ratio of μ_{VSET}/μ_{VRESET} and σ_{VSET}/μ_{VSET}.

voltage level is lower than that of LHH, which makes (4-4) easier to be satisfied.

The points marked inside Fig. 11(b) are other categories of devices from references [43]–[49], and as a result, it is hard to realize FELIX with existing devices. In order to show the changing trend, we simulate the correction with different device parameters σ_L/μ_L and $\sigma_{VRESET}/\mu_{VRESET}$, as shown in Fig. 12. From the gradual change of color, the correction decreases from 100% to 70% by degree.

Similarly, for the input RRAMs, the voltage difference between TE and BE is $(V_o\text{-}V_x)$, while for HHH case, this value comes to its maximum value V_o, since V_x is 0. As a result, the requirement is that V_o should not exceed the minimum value of V_{SET} so that the resistance state of input RRAMs can be maintained, as shown in Fig. 13(a). Since the ideal value of μ_{VRESET} is $7/12V_o$, the value of μ_{VSET} can be defined by the ratio of μ_{VSET}/μ_{VRESET}, marked as r, which

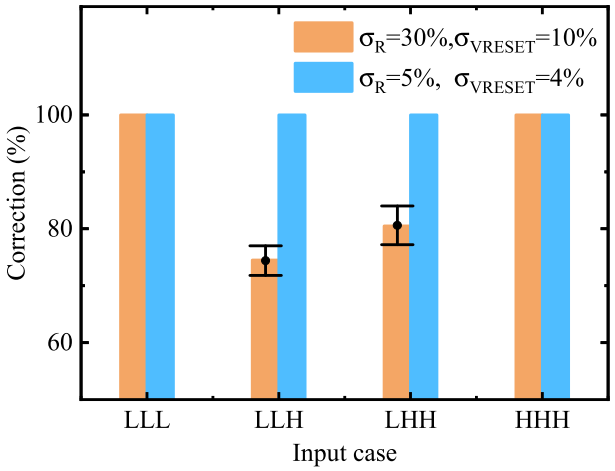


FIGURE 14. Simulation results of correction for each input case. The error bar shows different probabilities in 10 repetitions, with each repetition for 100 times simulation.

TABLE 3. Summary of resistance variation of ECM RRAM.

Structure	V_{SET} (V)	V_{RESET} (V)	HRS (Ω)	LRS (Ω)	$(\sigma/\mu)_{HRS}$	$(\sigma/\mu)_{LRS}$
Cu/h-BN/Ti/Au[50]	2	-1	8E3	1E2	0.62	0.4
Au/sheet-rich silk/Ag [43]	1.2	-1.2	1E7	200	0.5	0.2
Au/ZrO_2/Ag [45]	0.6	-0.4	1E8	1E3	0.25	0.5
Ag/ZnO:Mn/Pt [53]	2	-1.4	1E9	100	0.5	0.4
Cu/ZrO2/Pt [54]	1.4	-0.8	5E9	1500	0.8	0/26

can be written as:

$$V_o < (1 - 3\frac{\sigma_{VSET}}{\mu_{VSET}}) \cdot r \cdot \mu_{VRESET} \quad (4\text{-}6)$$

The relationship of the switching voltage ratio r with requirement on σ_{VSET} is shown in Fig. 13(b). For example, with switching voltage ratio $r = 2$, the maximum tolerable $\sigma_{VSET}/\mu_{VSET} \approx 0.05$, and if device has much more asymmetric I-V curve, it can tolerate more variation of SET voltage.

Simulation results of resistance variation $\sigma_L = 0.3$ and $\sigma_{VRESET} = 0.1$ are shown in Fig. 14, with partial error for the middle two cases.

According to Table 3, most existing ECM RRAM devices have resistance variation over 20%, which is because that conductive filament (CF) breaks at different positions and metal ions are reduced and accumulated at different positions of the bottom electrode or the branch of CF [55]. Origin of device-to-device variability is attributed to discrepancies in the fabrication processes such as variation in the switching oxide thickness, the surface roughness of the electrodes, etching damages [56]. It eventually leads to the uncertainty of the shape of metal filament and the contact area with the electrode in each switching process, which is reflected in the variation of resistance and switch voltage.

V. CONCLUSION

This paper analyzed the advantage of minority logic among other basic Boolean logic while implementing in-memory computing. Based on the analysis, we found that some requirements on RRAM device are necessary for realizing basic logic cell in circuit array. Since there is consensus that ECM RRAM has asymmetric V_{SET} and V_{RESET}, we fabricated Cu/ZnO/Pt device, and the I-V curve can exactly satisfy requirements. By demonstrating the feasibility of basic minority logic cell, four RRAMs were measured and analyzed. However, due to the failure of one input case, we found that the variation of resistance and switch voltage can affect the range of separating different cases. In summary, after exploring several emerging memory technologies that have strong potential to be commercialized in future, we find FELEX is incompatible with them due to the tight voltage and resistance variation requirement.

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