# Analysis and Reduction of Current and Voltage Ripple in DC-Link for Three-Level NPC Inverter-Fed Dual Three-Phase Motor Drives

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***Abstract*- In this paper, switching strategies for DC-link current and voltage ripple reduction have been studied. Considered topology is a neutral-point clamped three-level (NPC-3L) inverter feeding a dual three-phase permanent-magnet synchronous motor (PMSM). The mechanisms of DC-link current and voltage ripple generation in NPC-3L inverter-fed PMSM drive are analysed in detail. Then, a two-step collaborative switching strategy is proposed, where the optimum switching sequences, including opposite small vectors, are applied in the two inverters collaboratively. Furthermore, the switching vectors of two inverters are rearranged in the sequence of their corresponding DC-link capacitor currents so that the overlapping of their peaks is avoided. Consequently, both the voltage ripple and current ripple in the DC-link capacitors are mitigated with the proposed two-step collaborative switching strategy. For the mid-point voltage of the NPC-3L inverter, the amplitude of fluctuation is reduced under low modulation index operation, while the high-frequency harmonic components are mitigated under high modulation index operation. The experimental results are given to verify the validity of the theoretical analysis and the proposed switching strategy.**

***Index Terms*—Dual three-phase permanent-magnet synchronous motor (PMSM) drive, neutral-point clamped three-level (NPC-3L) inverter, DC-link capacitor, current and voltage ripple, switching strategy.**

## I. Introduction

Recently, with the increasing demands for power capacity and reliability, multiphase motor drives have received wide attention in industrial applications. When compared to three-phase drives, multiphase drives offer the merits of lower torque pulsation, lower current stress for switching devices, higher fault-tolerant capability, and additional degrees of control freedom [1-3]. Dual three-phase drive is an attractive solution with a capability to eliminate sixth-order torque harmonic pulsation and has been commercialized in various fields including wind energy generation [4]. On the other hand, the diode-clamped neutral-point clamped three-level (NPC-3L) converter is popular for medium-voltage high-power drives (typically 3-6.6kV) due to the superiority of lower voltage stress across the switching devices, lower output current and voltage harmonic distortion, and lower electromagnetic interference [5-7]. Therefore, it is a popular choice for high-power medium-voltage drives. By combining these technologies, the performance can be further improved in multilevel multiphase drives [8-9].

The reliability of drives involves evaluation of switching device modules, electric machines, current and voltage sensors, speed sensors, DC-link capacitors, and other components in the system [10-11]. It is found in [11] that capacitor failure accounts for 30% of all failures in a power converter. Therefore, the DC-link capacitor lifetime is one of the main factors concerning the reliability of motor drives. Usually, the electrolytic capacitors are used in the DC link due to large capacitance, relatively low cost, and small sizes. The expected lifetime of the electrolytic capacitor is extremely sensitive to the rise of operating temperature, which is caused by the ripple current in the equivalent series resistor (ESR) [12-14].

Consequently, research works have been published on capacitor current ripple reduction, for extension of capacitor lifetime and enhancement of system reliability [15-19]. An optimized switching strategy for a three-level T-type NPC (T-NPC) inverter is proposed in [15], where the two opposite active voltage vectors, rather than zero-state vectors, are utilized to synthesize the reference voltage vector. Thus, the large current ripple generated by the zero-state vector is avoided. The optimized switching strategy is further experimentally verified for a three-level photovoltaic inverter in [16]. However, current ripple reduction at low modulation indexes was not so significant. In [17], a reduction method of current ripple is proposed for active neutral-point clamped inverters for the full modulation-index range. In the low modulation index region, only the medium voltage vectors are used for the synthesis of the reference voltage vector. In the high modulation index region, hybrid modulation (including medium-vector modulation and the modulation of [15-16]) is utilized. However, the impact of power factor on the current ripple has not been considered in the above methods [18]. In [19], a generalized switching modulation method using the carrier shift method is proposed for a DC-DC-AC system to reduce the DC-link current ripple.

It should be noted that all the aforementioned analysis and control methods for the DC-link current ripple reduction are limited to three-phase drive systems, and related research on multiphase drive systems is very scarce. In [20], a collaborative method has been proposed to reduce the current ripple of a dual three-phase permanent-magnet synchronous

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motor (PMSM) drive by sorting the voltage vectors in a sequence corresponding to their DC-link currents. Thus, more dimensions of control freedom offered by multiphase drive systems have been utilized. However, a two-level inverter topology is used in [20]. For multilevel multiphase drives, the study of collaborative switching strategy for reducing DC-link current ripples is still absent.

Meanwhile, special attention is also required for the DC-link voltage ripple as it determines the sizing of the DC-link capacitors. In [21], the DC-link voltage ripple is analyzed for three-phase inverters under unbalanced load. In [22-23], the voltage ripple using space vector modulation (SVM) is compared to those using sinusoidal PWM (SPWM) and discontinuous PWM. In [24-26], studies have been presented for the DC-link voltage ripple in multiphase inverters. In [24], voltage ripple is analyzed for the seven-phase inverter. In [25], design guidelines are provided for the selection of DC-link capacitors in multiphase inverters based on the peak-to-peak value of the DC-link voltage ripple. However, only two-level inverters are discussed in these studies. In [26], mitigation of the DC-link capacitor voltage ripple is studied for T-NPC inverter-fed six-phase motor drive, where two sets of three-phase windings are wound in two separate halves of the stator. The output current of one three-phase T-NPC inverter is out of phase with that of the second three-phase T-NPC inverter, resulting in naturally balanced DC-link capacitor voltages. However, the DC-link voltage ripple caused by the switching actions was not studied. Moreover, output currents of each inverter are opposite to each other in [26], which may limit the performance if applied to other types of dual three-phase drives with different shift angles.

Therefore, to the best of the authors' knowledge, related studies of the DC-link voltage and current ripple for multilevel multiphase drives are still rare, in particular for systems with wide modulation index and power factor range. This paper tackles this problem by proposing a two-step collaborative switching strategy. With the proposed strategy, the DC-link capacitor current and voltage ripple can be reduced simultaneously.

The paper is organized as follows. Configuration and control of the analyzed NPC-3L inverter-fed dual three-phase PMSM drive are presented in Section II. Then, the mechanisms of capacitor current and voltage ripple formation, with the synchronous switching pattern, are analysed in Section III. In Section IV, a two-step collaborative switching strategy is proposed. Its performance is investigated in Section V for different modulation indexes and power factors. In Section VI, experimental results are presented to verify the effectiveness of the proposed switching strategy. Finally, conclusions are drawn in Section VII.

## II. Configuration and Control Scheme

Fig. 1 shows configuration of the analyzed NPC-3L inverter-fed dual three-phase PMSM drive. Note that although a diode-clamped NPC topology is used in this paper, the same derivations and results would also apply to the T-NPC topology because the modulation complexity of these two topologies is equivalent [27]. With the increase of semiconductor voltage ratings, the T-NPC converter is becoming a promising competitor to diode-clamped NPC converter, for high-power medium-voltage drives, due to its merits such as higher efficiency and lower device number [28]. The three-phase winding sets of the machine are shifted by 30°, and the neutral points of the two winding sets are isolated. The decoupled mathematical model of the dual three-phase PMSM can be obtained using vector space decomposition (VSD) as in [29].

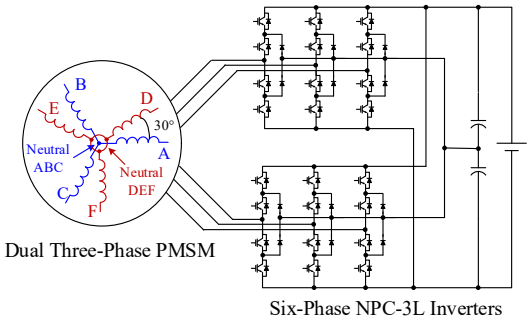



Fig. 1. Configuration of NPC-3L inverter-fed dual three-phase PMSM drive.

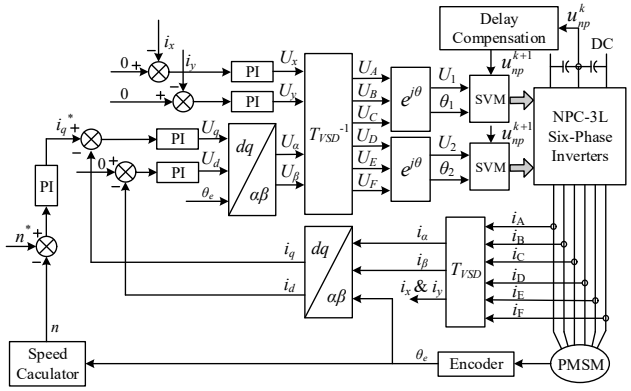



Fig. 2. Diagram of the basic control scheme.

Fig. 2 shows block diagram of the control scheme. The PI controller is used to regulate the speed of the machine. After application of VSD transformation, field-oriented control (FOC) scheme is utilized to regulate the current components in $\alpha$-$\beta$ subspace. Reference voltages $U_\alpha$, $U_\beta$ in $\alpha$-$\beta$ and $U_x$, $U_y$ in $x$-$y$ subspace, are generated by corresponding four closed-loop current controllers. As shown in Fig. 2, reference voltages $U_A$, $U_B$, $U_C$, $U_D$, $U_E$ and $U_F$ in the natural reference frame are obtained from $U_\alpha$, $U_\beta$, $U_x$ and $U_y$, using the inverse VSD transformation matrix $T_{VSD}^{-1}$. Then, three-phase SVM is conducted separately for each of the two sets using the algorithm of [30]. The delay compensation module is utilized to compensate for the digital controller delay effects.

## III. Analysis of Capacitor Currents and Voltages with Synchronous Switching Strategy

### A. Synchronous SVM Modulation

Fig. 3 shows the equivalent circuit of the dual three-phase motor drive, where $Z_s$ is the equivalent DC-source impedance, and $C_1$, $C_2$ are the DC-link capacitors. Capacitor currents are denoted by $i_{C1}$ and $i_{C2}$, respectively, whereas $i_a$, $i_b$, $i_c$ and $i_d$, $i_e$, $i_f$ are the stator set 1 and set 2 currents, respectively. The inverter input and the neutral point current are denoted by $i_{inv}$ and $i_{np}$, respectively. Furtherly, $i_{invI}$ denotes the input current of inverter I, whereas $i_{invII}$ denotes the input current of inverter

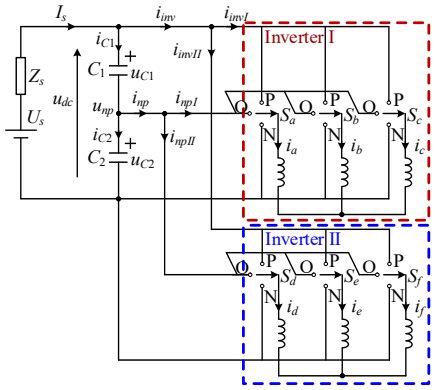



Fig. 3. Equivalent circuit of the three-phase drive.

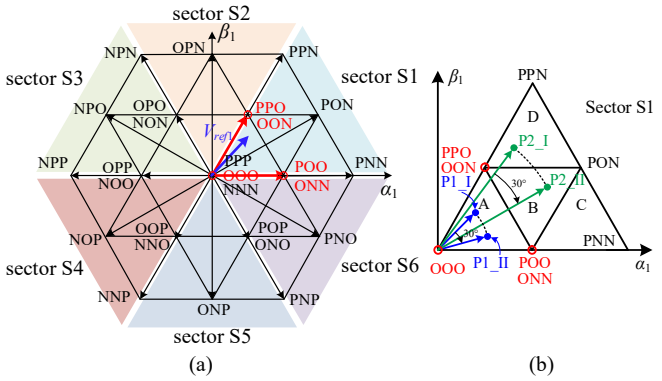



Fig. 4. Space vector diagram of three-phase NPC-3L inverter: (a) diagram of the whole inverter, (b) diagram of sector S1.

II. Similarly, $i_{npI}$ and $i_{npII}$ denote the neutral point currents generated by inverters I and II, respectively. Therefore, $i_{inv} = i_{invI}+i_{invII}$ and $i_{np} = i_{npI}+i_{npII}$. The DC-source voltage and current are denoted by $U_s$ and $I_s$, respectively.

Generally, the current ripple at the switching frequency can be assumed to only pass through the branch with the capacitors [25]. Based on the power balance principle, and the assumption that the power switches are ideal, one gets:

$$I_s = 3mI_0\cos\varphi \tag{1}$$

where $I_0$ represents the amplitude of the stator currents, $\varphi$ is the power factor angle, and $m$ is the modulation index ($m = V_0/u_{dc}$, where $V_0$ is the amplitude of the output phase voltage and $u_{dc}$ is the DC-link voltage). Each leg of the NPC-3L inverter can be regarded as a single-pole three-throw switch, which generates three voltage levels, i.e., P, O and N level. For convenience, the switch function is defined as:

$$S_x = \begin{cases} 1 & \text{output P level} \\ 0 & \text{output O level} \\ -1 & \text{output N level} \end{cases} \quad x \in \{a,b,c,d,e,f\} \tag{2}$$

Consequently, $i_{inv}$ and $i_{np}$ can be expressed as:

$$i_{inv} = \sum_x \frac{1}{2}(S_x^2 + S_x)\, i_x, x \in \{a,b,c,d,e,f\} \tag{3}$$

$$i_{np} = \sum_x (1 - S_x^2)\, i_x, x \in \{a,b,c,d,e,f\} \tag{4}$$

Capacitor currents $i_{C1}$ and $i_{C2}$ can be expressed as:

$$i_{C1} = I_s - i_{inv} = I_s - i_{C1\_s} \tag{5}$$

$$i_{C2} = i_{C1} - i_{np} = I_s - (i_{inv} + i_{np}) = I_s - i_{C2\_s} \tag{6}$$

where $i_{C1\_s}$ and $i_{C2\_s}$ denote the current components in $i_{C1}$ and $i_{C2}$, respectively, determined by the inverter switching actions. Both $i_{C1\_s}$ and $i_{C2\_s}$ contain current components influenced by both inverters, as:

$$i_{C1\_s} = i_{C1\_sI} + i_{C1\_sII} = i_{invI} + i_{invII} \tag{7}$$

$$i_{C2\_s} = i_{C2\_sI} + i_{C2\_sII} = (i_{invI} + i_{npI}) + (i_{invII} + i_{npII}) \tag{8}$$

where $i_{C1\_sI}$ and $i_{C2\_sI}$ denote $i_{C1\_s}$ and $i_{C2\_s}$ generated by inverter I, respectively, whereas $i_{C1\_sII}$ and $i_{C2\_sII}$ denote $i_{C1\_s}$ and $i_{C2\_s}$ generated by inverter II, respectively. Therefore, $i_{C1\_sI} = i_{invI}$, $i_{C2\_sI} = i_{invI}+i_{npI}$, $i_{C1\_sII} = i_{invII}$, and $i_{C2\_sII} = i_{invII}+i_{npII}$. Furthermore, the DC-link voltage $u_{dc}$ can be expressed as:

$$\begin{aligned} u_{dc} &= u_{C1} + u_{C2} = U_{dc\_ave} + \frac{1}{C}\int_{t_0}^{t_0+T_s}(i_{C1} + i_{C2})dt \\ &= U_{dc\_ave} + \frac{1}{C}\int_{t_0}^{t_0+T_s}[2I_s - (2i_{inv} + i_{np})]dt \end{aligned} \tag{9}$$

While setting the reference node as half of the DC-link, the actual mid-point voltage $u_{np}$ can be given as:

$$u_{np} = \frac{u_{C2} - u_{C1}}{2} \tag{10}$$

Above, $T_s$ denotes the switching period and $t_0$ is the initial instant of the switching period. $u_{C1}$ and $u_{C2}$ are the voltages of the capacitors $C_1$ and $C_2$, respectively. $U_{dc\_ave}$ is the average DC-link voltage, which also equals the initial value of $u_{dc}$ at instant $t_0$. $C$ is the capacitance value of $C_1$ and $C_2$. It is noted that the switching sequence applied from instant $(k+1)T_s$ to instant $(k+2)T_s$ is calculated based on the sampled information at instant $kT_s$. Therefore, there exists a delay effect in digital implementation, and crucial information at the future instant $(k+1)T_s$ requires to be predicted. The predicted mid-point voltage can be calculated as:

$$u_{np}^{k+1} = u_{np}^{k} - \frac{1}{2C}\sum_i^{seg^k} i_{np\_i}^{k} t_i^{k} \tag{11}$$

where $u_{np}^{k}$ is the value at instant $kT_s$, and $u_{np}^{k+1}$ is the predicted value at instant $(k+1)T_s$. $i_{np\_i}^{k}$ is $i_{np}$ generated in the $i$th segment by the applied switching state, $t_i^{k}$ is the dwell time of the $i$th segment from instant $kT_s$ to $(k+1)T_s$, and $seg^k$ is the total number of segments from instant $kT_s$ to $(k+1)T_s$. It can be observed from (3)-(11) that current and voltage expressions are directly related to the applied switching states. Therefore, the switching sequence of the modulation scheme can be optimized to improve the performance of the DC-link current and voltage.

Fig. 4(a) shows space vector diagram for the three-phase NPC-3L inverter. There are 27 vectors in total, which include six redundant small vectors and three zero vectors. The plane is separated into six sectors S1-S6, where each sector consists of four triangular regions. In the SVM scheme, the nearest three vectors are selected to synthesize the reference voltage vector. To reduce the switching actions while keeping good harmonic performance, the switching sequence is arranged as in [31], which is a kind of discontinuous PWM (DPWM) strategy [32]. The lower voltage levels are placed at the beginning and at the end of a switching period, while the higher voltage levels are placed in the middle, for each leg of the inverter. For instance, if the reference voltage vector is located in region A of sector S1 as shown in Fig. 4(b), the vectors PPO, OON, POO, ONN, and OOO are selected. Then,

the switching sequence with positive small vectors is OOO-POO-PPO-POO-OOO, whereas the switching sequence with negative small vectors is ONN-OON-OOO-OON-ONN. The choice of positive or negative small vectors is determined by control of the mid-point voltage. When the mid-point voltage is larger than the desired value, the negative small vectors are selected to reduce the mid-point voltage, and vice versa. Conventionally, both inverters would follow the same DPWM rules, and this category of switching sequence arrangement is called – synchronous modulation, in this paper.

### *B. Analysis of Current and Voltage Ripples*

As can be seen from Fig. 4(a), the space vector diagram of the three-level three-phase inverter has a radial symmetry with the base region spanning 60°. Assuming symmetric load, the current and voltage ripple pattern will follow the same symmetry, and therefore only one sector (1/6 of the fundamental period) is analysed. For further analysis, sector S1 has been chosen with few typical operating points as indicated in Fig. 4(b). Considering only the fundamental components and neglecting the switching harmonics, the output voltages and currents can be expressed as:

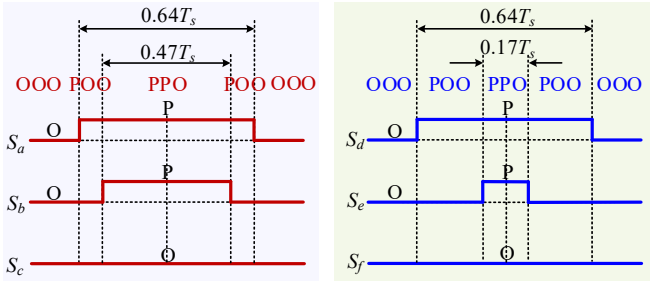
$$u_i = \begin{cases} V_0 \cos(\omega t - 2\pi/3\cdot(i-1)), & i \in \{1,2,3\} \\ V_0 \cos(\omega t - 2\pi/3\cdot(i-4) - \pi/6), & i \in \{4,5,6\} \end{cases} \quad (12)$$

$$i_i = \begin{cases} I_0 \cos(\omega t - 2\pi/3\cdot(i-1) + \varphi), & i \in \{1,2,3\} \\ I_0 \cos(\omega t - 2\pi/3\cdot(i-4) + \varphi - \pi/6), & i \in \{4,5,6\} \end{cases} \quad (13)$$

where $u_i$ and $i_i$ are the voltage and current in phase $i$, respectively, $V_0$ and $I_0$ are the corresponding amplitudes, and $\omega$ is the angular frequency. The values of $i$ equal to 1, 2 and 3 correspond to phases A, B and C (the first three-phase set), and similarly 4, 5 and 6 are used for D, E and F (the second three-phase set). The power factor angle $\varphi$ is given as $-\pi/6$ considering the normal operation of PMSM.

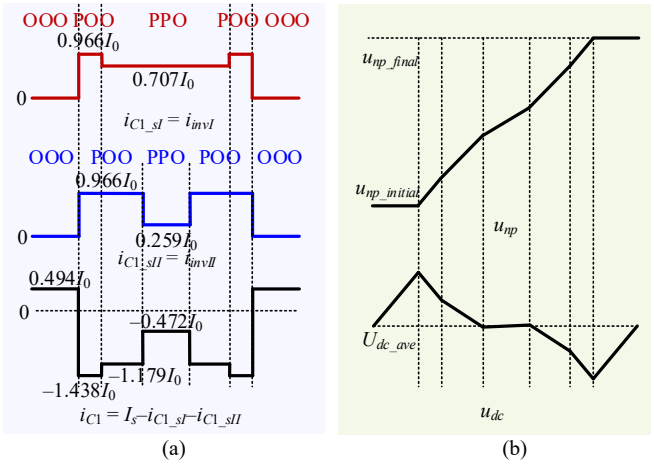
It is worth noting that the effect of parasitic inductance is ignored in the following DC-link current and voltage ripple analysis [20,25]. In reality, the actual capacitor current would not change in a step manner, as will be demonstrated later on in the experimental verification section. However, the used approach is accurate enough to indicate where the ripple has its peaks, and based on that, a new switching strategy is developed in this paper which effectively reduces the ripple.

As shown in Fig. 4(b), the first selected operating point is P1, where the reference vector for inverter I is located at point P1_I and at point P1_II for inverter II. In this example, the modulation index is $m$ = 0.19, and the phase angles of P1_I and P1_II are π/4 and π/12, respectively. Using (13) one gets: $i_a = 0.966I_0$, $i_b = -0.259I_0$, $i_c = -0.707I_0$, $i_d = 0.966I_0$, $i_e = -0.707I_0$ and $i_f = -0.259I_0$. Also, based on (1), the DC-source current $I_s$ is equal to $0.494I_0$. Fig. 5 shows the switching patterns using the positive small vectors, applied when the mid-point voltage $u_{np}^{k+1}$ is below the desired value. As shown in Fig. 5, the dwell times for vectors OOO, POO and PPO are $0.36T_s$, $0.17T_s$ and $0.47T_s$ in inverter I, respectively. On the



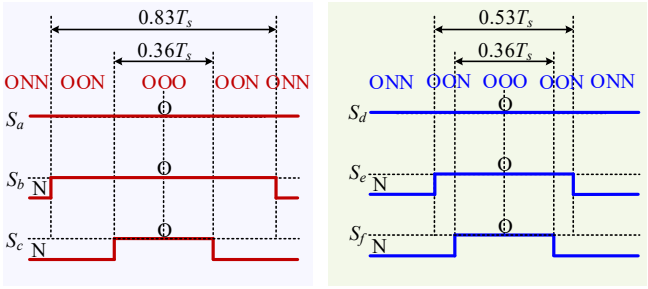

(a) (b)

Fig. 5. Switching patterns of the two inverters at points P1_I and P1_II with the sequence with positive small vectors: (a) inverter I, (b) inverter II.



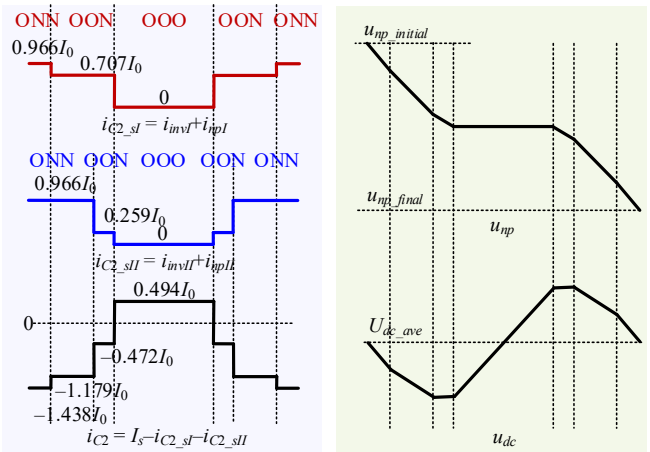

(a) (b)

Fig. 6. Current and voltage waveforms during a single switching period with the sequence with positive small vectors at points P1_I and P1_II: (a) current waveforms of capacitor $C_1$, (b) waveforms of mid-point and DC-link voltage.




(a) (b)

Fig. 7. Switching patterns of the two inverters at points P1_I and P1_II with the sequence with negative small vectors: (a) inverter I, (b) inverter II.




(a) (b)

Fig. 8. Current and voltage waveforms during a single switching period with the sequence with negative small vectors at points P1_I and P1_II: (a) current waveforms of capacitor $C_2$, (b) waveforms of mid-point and DC-link voltage.

other hand, the dwell times for vectors OOO, POO and PPO in inverter II are $0.36T_s$, $0.47T_s$ and $0.17T_s$, respectively.

With the switching patterns shown in Fig. 5, the waveforms of $i_{C1}$ and $u_{dc}$ are analysed as shown in Fig. 6. Based on (3), (4) and (6), $i_{C2}$ equals $I_s$ when positive small vectors or zero vectors are used. Therefore, the waveform of $i_{C2}$ is not discussed in Fig. 6. As shown in Fig. 6(a), $i_{C1\_sI}$ equals 0, $i_a$ ($0.966I_0$) and $i_a+i_b=-i_c$ ($0.707I_0$), when the vectors OOO, POO and PPO are used in inverter I, respectively. Similarly, $i_{C1\_sII}$ equals 0, $i_d$ ($0.966I_0$) and $i_d+i_e=-i_f$ ($0.259I_0$), when vectors OOO, POO and PPO are used in inverter II, respectively. It is observed that maximum as well as minimum current levels of $i_{C1\_sI}$ and $i_{C1\_sII}$ overlap each other. Consequently, large current ripple can be observed in the waveform of $i_{C1}$.

Fig. 6(b) shows the waveforms of the mid-point voltage $u_{np}$ and the DC-link voltage $u_{dc}$. Values $u_{np\_initial}$ and $u_{np\_final}$ are the mid-point voltage values at the initial and final instant of the switching period, respectively. As shown in Fig. 6(b), $u_{np}$ keeps rising in the middle of the switching period, where the positive small vectors are used. After the application of sequences with positive small vectors, $u_{np\_final}$ is larger than $u_{np\_initial}$. On the other hand, according to (9), the change of $u_{dc}$ is proportional to the integral value of ($i_{C1}$+$i_{C2}$). Therefore, the large current ripple in $i_{C1}$ leads to large ripple in $u_{dc}$ (considering that $i_{C2}$ has a constant value of $I_s$), as shown in Fig. 6(b). Additionally, the instantaneous DC-link voltage equals the average value $U_{dc\_ave}$ at the end of the switching period at steady-state operation.

On the other hand, when the mid-point voltage $u_{np}^{k+1}$ is larger than the desired value, negative small vectors are used. The corresponding switching sequence is applied as shown in Fig. 7. In inverter I, the dwell times for vectors OOO, ONN and OON are $0.36T_s$, $0.17T_s$ and $0.47T_s$, whereas for OOO, ONN and OON in inverter II are $0.36T_s$, $0.47T_s$ and $0.17T_s$, respectively. Fig. 8 shows the waveforms of $i_{C2}$, $u_{np}$ and $u_{dc}$. Considering that now, according to (6), $i_{C1}$ is equal to $I_s$ during the whole switching period, the waveform of $i_{C1}$ is not shown. Similarly, as in Fig. 6, the key values are shown in Fig. 8. As negative small vectors are used, now $u_{np}$ keeps decreasing and $u_{np\_final}$ is smaller than $u_{np\_initial}$, as shown in Fig. 8(b).

Similarly, another operating point P2 is selected to investigate operation at higher modulation indexes. As shown in Fig. 4(b), the reference vector is located at point P2_I for inverter I whereas the reference vector is located at point P2_II for inverter II. In this example, the modulation index is $m$ = 0.4, and the phase angles of P2_I and P2_II are $7\pi/24$ and $\pi/8$, respectively. By using (13), the phase currents are: $i_a$ = $0.924I_0$, $i_b$ = $-0.131I_0$, $i_c$ = $-0.793I_0$, $i_d$ = $0.991I_0$, $i_e$ = $-0.609I_0$ and $i_f$ = $-0.382I_0$, and by using (1), the DC-source current $I_s$ is equal to $1.039I_0$. Fig. 9 and Fig. 10 show the waveforms of $i_{C1}$ and $i_{C2}$ when the sequence with positive or negative small vectors is utilized, respectively. Note that now, neither $i_{C1}$ or $i_{C2}$ is constant, so both waveforms are shown.

As shown in Fig. 9(b), $i_{C2\_sI}$ equals $0.793I_0$ when vectors PON and PPN are utilized in inverter I while $i_{C2\_sII}$ equals $0.382I_0$ when vector PON is used in inverter II. Similarly, as shown in Fig. 10(a), $i_{C1\_sI}$ equals $0.924I_0$ and $0.793I_0$ when the vectors PON and PPN are used in inverter I, while $i_{C1\_sII}$ equals $0.991I_0$ when the vector PON is used in inverter II. Therefore, when the middle and large vectors are used, both sequences with positive and negative small vectors generate distinct ripples in $i_{C1}$ and $i_{C2}$. This was not the case for the operating points P1_I and P1_II, where the ripple was generated only in the upper/lower capacitor, if the sequence with positive/negative small vectors is used. The overlapping

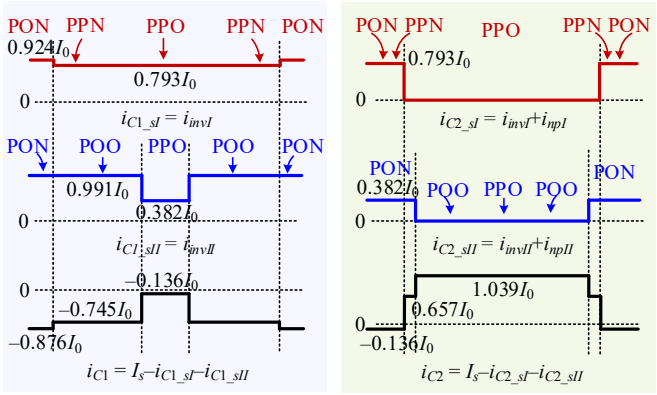



Fig. 9. Current waveforms during a single switching period with the sequence with positive small vectors at operating points P2_I and P2_II: (a) $i_{C1}$ and (b) $i_{C2}$ and their corresponding components in the two inverters.

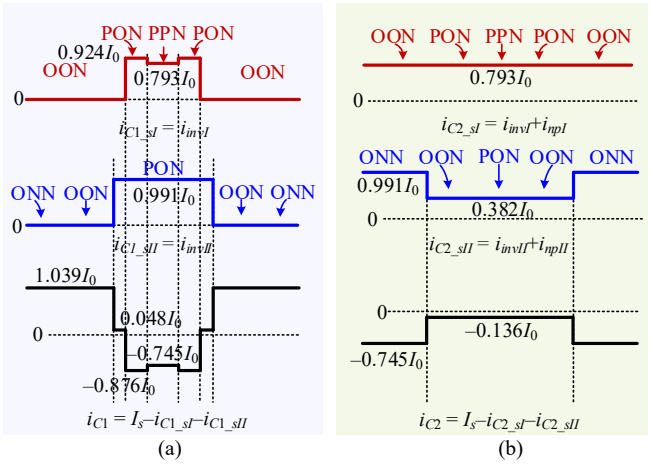



Fig. 10. Current waveforms during a single switching period with the sequence with negative small vectors at operating points P2_I and P2_II: (a) $i_{C1}$ and (b) $i_{C2}$ and their corresponding components in the two inverters.

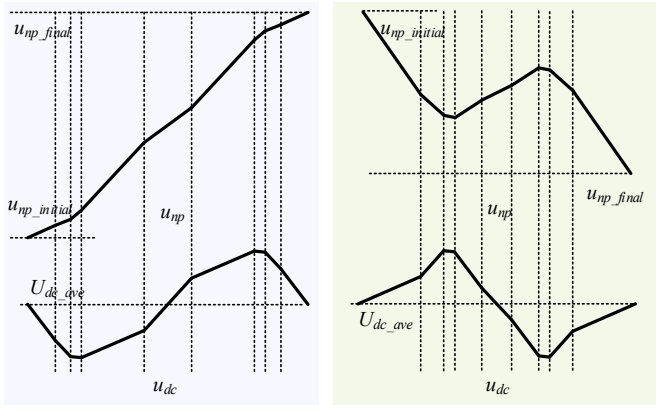



Fig. 11. Mid-point and DC-link voltage waveforms at operating points P2_I and P2_II, with a sequence with: (a) positive and (b) negative small vectors.

phenomenon still exists, and large current ripples can be observed in waveforms of $i_{C1}$ and $i_{C2}$.

The waveforms of $u_{np}$ and $u_{dc}$ at the operating points P2_I and P2_II with the sequence with negative or positive small vectors are shown in Fig. 11. Fig. 11(a) shows the mid-point voltage $u_{np}$ when the sequences with positive small vectors are used in the two inverters. It is observed that the middle vector PON increases $u_{np}$. Therefore, $u_{np}$ keeps increasing during the whole switching period, and $u_{np\_final}$ is larger than $u_{np\_initial}$. The waveform of $u_{np}$ using the sequence with negative small vectors is presented in Fig. 11(b). The value of $u_{np}$ decreases when negative small vectors are used but increases when the middle vector PON is used.

Fig. 11(a) and Fig. 11(b) also show the waveforms of $u_{dc}$. As mentioned before, the change of $u_{dc}$ is proportional to the integral value of ($i_{C1}$+$i_{C2}$). The overlapping of $i_{C1}$ and $i_{C2}$ leads to a longer duration for ($i_{C1}$+$i_{C2}$) being positive or negative. As a result, large voltage ripple occurs in the waveform of $u_{dc}$.

## IV. Two-Step Collaborative Switching Strategy

To mitigate the DC-link current and voltage ripple, a two-step collaborative switching strategy is proposed in this paper. Fig. 12 shows the principle of the proposed switching strategy. As shown in Fig. 12, the first step is to set two inverters to output switching sequences with small vectors with opposite polarities. There are obviously two ways how this can be done. If the sequence with positive small vectors is used for inverter I and the sequence with negative small vectors for inverter II, which is represented as the first combination 1P2N; or if the sequence with negative small vectors is used for inverter I and the sequence with positive small vectors is used for inverter II, represented as the second combination 1N2P. The choice of combination is determined by their influence on the mid-point voltage. The second step is to rearrange the switching sequence of the two inverters to avoid overlapping of the current peaks and hence reduce the DC-link voltage ripple.

### A. First Step: Switching Sequences of Opposite Small Vectors

Based on (5) and (6), the expressions of $i_{C1\_sI}$ and $i_{C2\_sI}$ are:

$$i_{C1\_sI} = i_{invI} = \sum_x \frac{1}{2}(S_x^2 + S_x)i_x, x \in \{a,b,c\} \quad (14)$$

$$i_{C2\_sI} = i_{invI} + i_{npI} = \sum_x (1 - \frac{1}{2}S_x^2 + \frac{1}{2}S_x)i_x, x \in \{a,b,c\} \quad (15)$$

For negative small vectors, $S_x$ is –1 or 0, both of which result in $i_{C1\_sI}$ = 0. On the other hand, $S_x$ is 1 or 0 for positive small vectors, and they result in $i_{C2\_sI}$ = 0. Therefore, the positive small vectors do not generate current ripples in the capacitor $C_2$, whereas the negative small vectors do not generate current ripples in the capacitor $C_1$. Similar equations to (14) and (15), with the same conclusion, can be written for $i_{C1\_sII}$ and $i_{C2\_sII}$, for $x \in \{d,e,f\}$. When two combinations with opposite small vectors are used, the current ripples caused by the two inverters are separated into two capacitors, respectively. Specifically, when the switching sequence with positive small vectors is used in inverter I and the switching sequence with negative small vectors is used in inverter II, $i_{C1\_s}$ only contains current peaks from inverter I and $i_{C2\_s}$ only contains current peaks from inverter II. Therefore, current ripples in $i_{C1}$ and $i_{C2}$ can be mitigated accordingly.

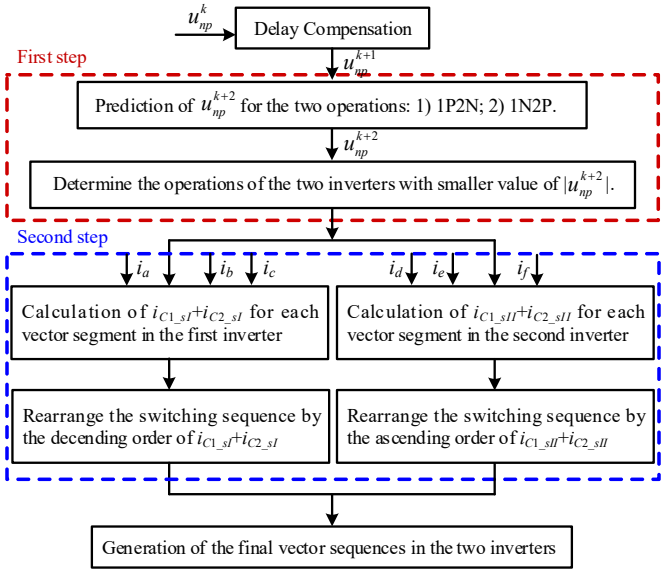



Fig. 12. Principle of the proposed two-step collaborative switching strategy.

Further, the mid-point voltage ripple is analyzed. As shown in Fig. 6(b), Fig. 8(b) and Fig. 11, the utilization of small vectors with the same polarity in the two inverters may cause large mid-point voltage fluctuations. Instead, when the small vectors of opposite polarities are used in the two inverters, the mid-point voltage will not keep increasing or decreasing during a single switching period. Thus, the mid-point voltage fluctuation will be reduced.

As shown in Fig. 12, the choice of 1P2N or 1N2P combination is determined by the balancing effect on the mid-point voltage. Based on (11), the mid-point voltage can be predicted as:

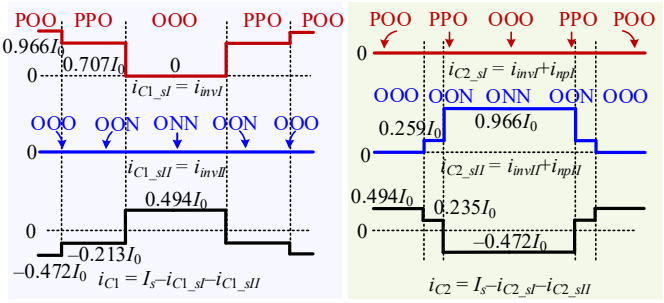
$$u_{np}^{k+2} = u_{np}^{k+1} - \frac{1}{2C}\sum_i^{seg^{k+1}} i_{np\_i}^{k+1} t_i^{k+1} \quad (16)$$

Using (16), the mid-point voltage is predicted for the 1P2N and 1N2P combinations. When $u_{np}^{k+1}$ is above the desired value, the combination with the lower predicted value of $u_{np}^{k+2}$ is selected. Contrarily, the combination with the higher predicted value of $u_{np}^{k+2}$ is selected when $u_{np}^{k+1}$ is below the desired value.

### B. Second Step: Rearrangement of Switching Sequences

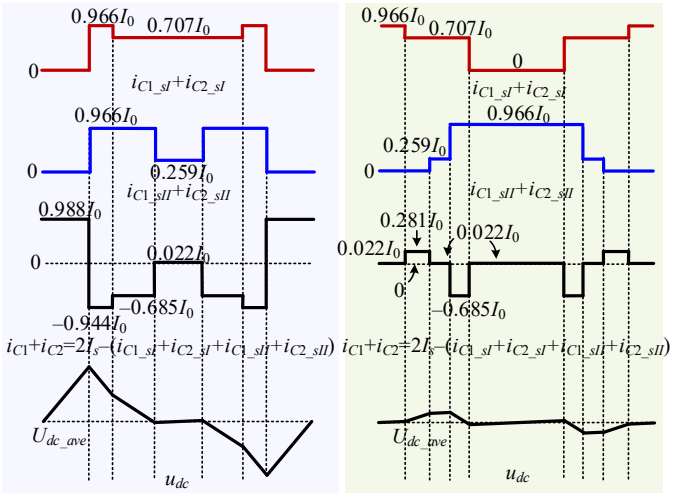
As analyzed above, an effective way to avoid the overlapping between current peaks and reduce ripples is to properly rearrange applied switching sequences in the two inverters. For that purpose, the applied vectors are rearranged in such a way that the considered current in the first inverter is sorted in descending order, whereas in the second inverter is sorted in ascending order during the first half of the switching period. It is noted that the ripple of $u_{dc}$ is proportional to the integral value of ($i_{C1}$+$i_{C2}$), and thus ($i_{C1}$+$i_{C2}$) is used for sorting for reduction of $u_{dc}$. Considering that the DC component of $I_s$ is ignored during evaluation of the voltage and current ripples, ($i_{C1\_s}$+$i_{C2\_s}$) is the current to be considered.

To clearly show the process and advantages of the two-step collaborative switching strategy, the operating point P1 using 1P2N mode is selected as an example. Fig. 13 presents the capacitor current waveforms at operating point P1 using 1P2N combination. As shown in Fig. 13(a), $i_{C1\_sII}$ is equal to zero




(a) (b)

Fig. 13 Current waveforms at operating point P1 with proposed switching strategy using 1P2N mode: (a) waveforms of $i_{C1}$, (b) waveforms of $i_{C2}$.

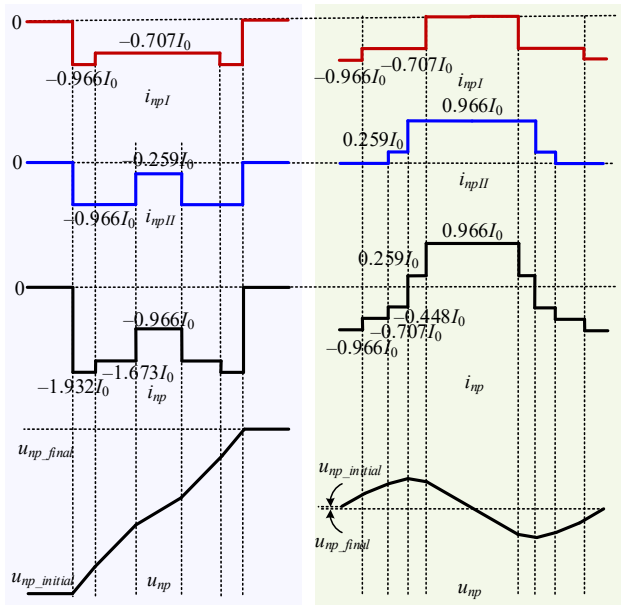



(a) (b)

Fig. 14. DC-link voltage waveform comparison at operating point P1 between (a) synchronous and (b) proposed switching method using 1P2N mode.

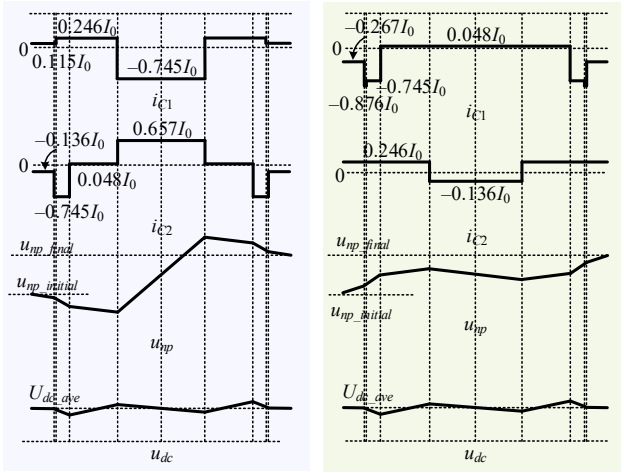
because the sequence with negative small vectors is used in inverter II. It can be seen that the switching sequence of inverter I is rearranged now so that ($i_{C1\_sI}$+$i_{C2\_sI}$) is sorted in descending order (during the first half of the switching period). Due to the fact that $i_{C2\_sI}$ equals zero during the whole switching period, $i_{C1\_sI}$ is in descending order, as shown in Fig. 13(a). Compared to the current waveforms in Fig. 6(a), it can be seen that the overlapping between current peaks of the two inverters is avoided and the current ripple is thus reduced. Similar ripple reduction effects can be observed in Fig. 13(b), when compared to the current waveforms in Fig. 8(a). Additionally, the switching sequence of inverter II is rearranged so that ($i_{C1\_sII}$+$i_{C2\_sII}$) is in ascending order. With $i_{C1\_sII}$ equaling zero, $i_{C2\_sII}$ is in ascending order. Hence, by comparison between Fig. 6, Fig. 8 and Fig. 13, it can be concluded that the two-step collaborative switching strategy reduces the DC-link capacitor current ripple.

The DC-link voltage ripple with the synchronous and with the proposed method is compared in Fig. 14. Since the DC-link voltage is equal to the integral of the sum of the capacitor currents (9), the waveforms of ($i_{C1}$+$i_{C2}$) and the corresponding components from the two inverters are also presented in Fig. 14. Fig. 14(a) corresponds to the synchronous switching method of Fig. 6, and Fig. 14(b) shows waveforms using 1P2N mode with the proposed switching method. As shown in Fig. 14(a), the overlapping of current peaks for ($i_{C1\_sI}$+$i_{C2\_sI}$) and ($i_{C1\_sII}$+$i_{C2\_sII}$) directly leads to a large current ripple in




(a) (b)

Fig. 15. Mid-point voltage comparison at operating point P1 between (a) synchronous and (b) proposed switching method using 1P2N mode.




(a) (b)

Fig. 16. Current and voltage waveforms at operating points P2_I and P2_II with the proposed switching strategy: (a) 1P2N and (b) 1N2P operation.

($i_{C1}$+$i_{C2}$). Subsequently, a large voltage ripple is produced in $u_{dc}$. On the other hand, the DC-link voltage ripple is significantly reduced with the proposed method in Fig. 14(b), where the switching sequences of two inverters are rearranged such that ($i_{C1\_sI}$+$i_{C2\_sI}$) is in descending order and ($i_{C1\_sII}$+$i_{C2\_sII}$) is in ascending order. Therefore, the overlapping of current peaks in ($i_{C1\_sI}$+$i_{C2\_sI}$) and ($i_{C1\_sII}$+$i_{C2\_sII}$) is avoided.

Fig. 15 compares the mid-point voltage ripple with the synchronous and the proposed switching method, where the waveforms of $i_{npI}$, $i_{npII}$ and $i_{np}$ are presented. It can be seen in Fig. 15(a) that both $i_{npI}$ and $i_{npII}$ are below or equal to zero. Therefore, $i_{np}$ is also below or equal to zero during the whole switching period. Consequently, a large deviation of the mid-point voltage appears in Fig. 15(a). On the other hand, $i_{npI}$ is below or equal to zero, whereas $i_{npII}$ is above or equal to zero, with the proposed switching method in Fig. 15(b). Hence, the polarity distribution of $i_{np}$ is more balanced within the

TABLE I
COMPARISON OF CURRENT RIPPLES BETWEEN SYNCHRONOUS METHOD AND PROPOSED TWO-STEP METHOD

| Operating point | Method type | $i_{C1}$ | $i_{C2}$ |
|---|---|---|---|
| P1 | Synchronous method | $1.932I_0$ | $1.932I_0$ |
| | Proposed method | $0.966I_0$ | $0.966I_0$ |
| P2 | Synchronous method | $1.915I_0$ | $1.784I_0$ |
| | Proposed method | $1.122I_0$ | $1.402I_0$ |

switching period. As a result, the deviation of $u_{np}$ in Fig. 15(b) is much smaller than in Fig. 15(a), and the mid-point voltage ripple is reduced with the proposed method.

Using similar analysis as in Figs. 13-15, operating point P1 for 1N2P mode can be also analyzed. As a final result, it can be obtained that $i_{C1}$ waveform would look like $i_{C2}$ waveform from Fig. 13(b); $i_{C2}$ would look like $i_{C1}$ from Fig. 13(a); $u_{np}$ would be a mirrored image of $u_{np}$ from Fig. 15(b) (multiplied by –1); and $u_{dc}$ would be of the same shape as $u_{dc}$ in Fig. 14(b). Of course, in 1N2P mode, different space vectors would be applied. Finally, for completeness, the final current and voltage waveforms for the operating point P2 (with the proposed method) are shown in Fig. 16. Similar ripple mitigation effects can be observed when compared to the adequate waveforms ($i_{C1}$, $i_{C2}$, $u_{np}$, $u_{dc}$) in Figs. 9-11 where the synchronous method was used. In summary, the amplitudes of peak-to-peak current ripples are compared in Table I. It can be observed that the peak-to-peak current ripple is significantly reduced with the proposed collaborative switching strategy.

## V. PERFORMANCE ANALYSIS

### A. Influence of Vectors on Mid-Point Voltage Balancing

As shown in (11), the reason for fluctuation in the mid-point voltage is the utilization of vectors containing O levels (small and middle vectors), which generate $i_{np}$. To verify the voltage balancing capability of the proposed strategy, the effect of small vectors and middle vectors are separated. Inverter I is selected for analysis, and the same applies to inverter II.

Firstly, effects of the middle vectors on the mid-point voltage are analyzed. The term $d(m,\theta)$ represents the duty cycle of the middle vector in sectors S1-S6, which is determined by the modulation index $m$ and the phase angle $\theta$ of the reference vector. In S1, the middle vector is PON, and $i_{np} = i_b$. The increment of the mid-point voltage influenced by PON during the whole sector S1, namely $\Delta u_{np\_S1}$, is:

$$\Delta u_{np\_S1} = -\frac{1}{2\omega C}\int_0^{\pi/3} i_b(\theta)d(m,\theta)d\theta \tag{17}$$

Similarly, the increment on mid-point voltage during the whole sector S2 (as a consequence of OPN), namely $\Delta u_{np\_S2}$, can be calculated as:

$$\begin{aligned}\Delta u_{np\_S2} &= -\frac{1}{2\omega C}\int_{\pi/3}^{2\pi/3} i_a(\theta)d(m,\theta)d\theta \\ &= -\frac{1}{2\omega C}\int_0^{\pi/3} i_a(\theta+\frac{\pi}{3})d(m,\theta+\frac{\pi}{3})d\theta\end{aligned} \tag{18}$$

where $d(m,\theta)=d(m,\theta+\pi/3)$ because of symmetry. Also, for a symmetrical three-phase system $i_b(\theta) = -i_a(\theta+\pi/3)$. Therefore, the total increment of the mid-point voltage caused by the middle vectors equals zero from the beginning of sector S1 to the end of sector S2, as:

$$u_{np}\Big|_{\omega t=2\pi/3} - u_{np}\Big|_{\omega t=0} = \Delta u_{np\_S1} + \Delta u_{np\_S2} = 0 \tag{19}$$

The same applies to sectors S3-S4 and S5-S6. Consequently, it can be concluded that the middle vectors do not generate mid-point voltage DC deviation. Instead, fluctuation of the 3rd harmonic frequency can be observed in the mid-point voltage, which is an inherent problem of SVPWM in NPC-3L inverters [33]. At low power factor operations, whether to enable the first step optimization (opposite small vector sequences) can be determined by the difference between the sampled and desired mid-point voltage value. In practice, this problem can be mitigated by appropriate sizing of the DC-link capacitors.

Secondly, the effect of the small vectors on the mid-point voltage is analyzed. Mid-point current $i_{np}$, generated by the sequence with positive small vectors is opposite to the one generated by the sequence with negative small vectors. For example, $i_{np}$ generated by the positive small vector POO is $i_b+i_c = -i_a$, whereas $i_{np}$ generated by the negative small vector ONN is $i_a$. Furthermore, $i_{np}$ generated in operation 1P2N is opposite to that in operation 1N2P. Accordingly, the integral values of $i_{np}$ in 1P2N and 1N2P combination are opposite to each other. Consequently, the opposite small vector sequences operation can ensure the balance of the DC-link capacitor voltages.

### B. Ripple Reduction under Different Operations

To comprehensively show the effect of the ripple reduction by the proposed switching strategy, Figs. 17-19 compare the amplitudes of ripples in $i_{C1}$, $i_{C2}$, $u_{dc}$ and $u_{np}$ with three different power factor angles, namely 0°, –30° and 30°, respectively. Specifically, the small vector sequences of the same polarity are used in the two inverters with the synchronous switching strategy (used polarity depends on deviation of the mid-point voltage). For the proposed switching strategy, 1P2N or 1N2P operation is used (as per the First Step of the algorithm in Fig. 12). The current and voltage values are given in per unit values in Figs. 17-19. The current base is $I_0$ and the voltage base is $I_0T_s/C$.

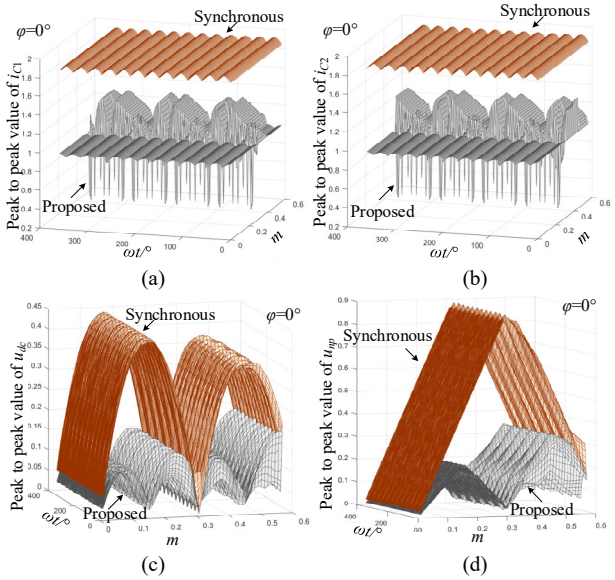



Fig. 17. Ripple amplitude comparison of $i_{C1}$, $i_{C2}$, $u_{dc}$ and $u_{np}$ with unity power factor: (a) $i_{C1}$, (b) $i_{C2}$, (c) $u_{dc}$ and (d) $u_{np}$.

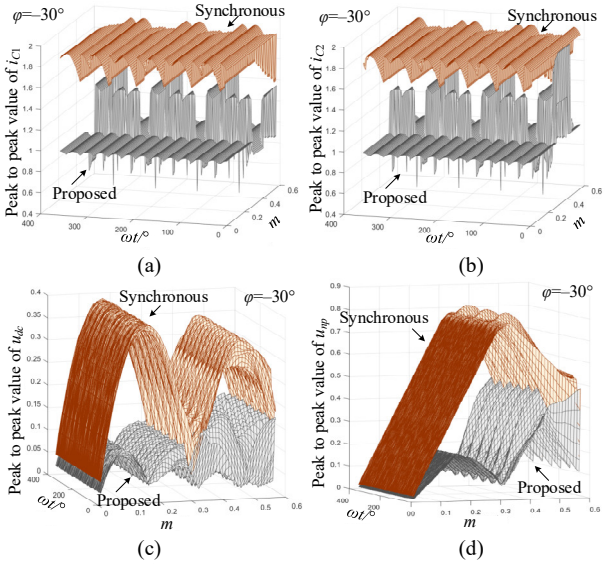



Fig. 18. Ripple amplitude comparison of $i_{C1}$, $i_{C2}$, $u_{dc}$ and $u_{np}$ with $\varphi$=–30°: (a) $i_{C1}$, (b) $i_{C2}$, (c) $u_{dc}$ and (d) $u_{np}$.

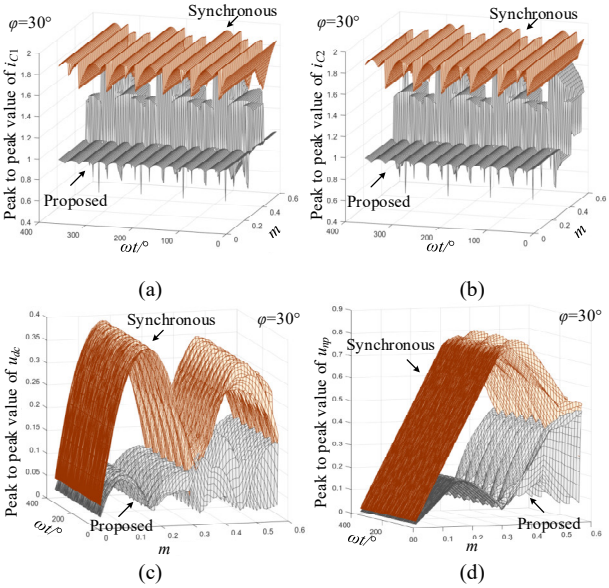



Fig. 19. Ripple amplitude comparison of $i_{C1}$, $i_{C2}$, $u_{dc}$ and $u_{np}$ with $\varphi$=30°. (a) $i_{C1}$, (b) $i_{C2}$, (c) $u_{dc}$ and (d) $u_{np}$.

Fig. 17(a) shows numerical comparison results of $i_{C1}$ ripple amplitude with unity power factor. It can be observed that the ripple of $i_{C1}$ using the proposed switching strategy is lower than that using the synchronous switching strategy (for any value of $\omega t$ and $m$). Similar results are obtained for $i_{C2}$, and are shown in Fig. 17(b). Fig. 17(c) shows the comparison results for $u_{dc}$. The ripple of $u_{dc}$ using the proposed switching strategy is lower than that using the synchronous switching strategy. Fig. 17(d) shows the comparison result for $u_{np}$. The ripple reduction of $u_{np}$ is significant under low modulation index operation while it is less effective under high modulation index operation. The reason is in the utilization of middle vectors. Both comparisons under phase-leading and phase-lagging power factor angles in Fig. 18 and Fig. 19 show similar results to those in Fig. 17 at unity power factor. Therefore, it indicates that current and voltage ripples in the DC link can be reduced under different power factors with the proposed collaborative switching strategy.

TABLE II
KEY PARAMETERS OF EXPERIMENTAL SETUP

| Name | Value |
|---|---|
| Pole pair number | 3 |
| *q*-axis inductance | 6.21 mH |
| *d*-axis inductance | 6.21 mH |
| PM flux (amplitude) | 0.20 Wb |
| Stator resistance | 0.21 Ω |
| DC-link capacitance | 1000 μF |
| Sampling frequency | 2 kHz |
| DC-link voltage | 100 V |

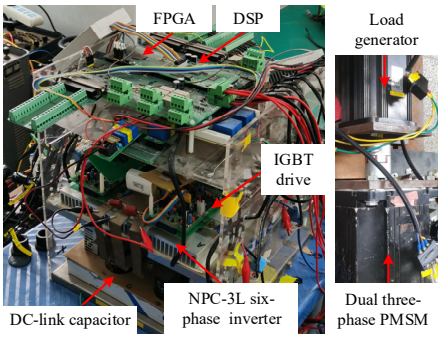
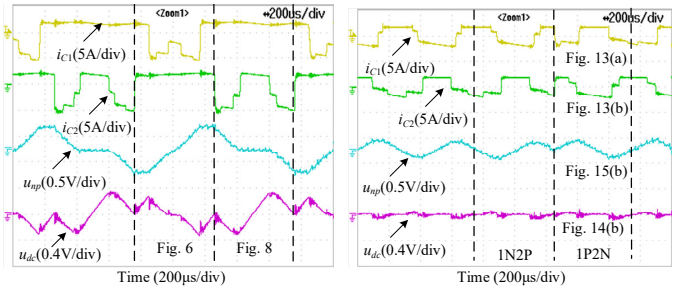



Fig. 20. Photograph of the experimental setup.

## VI. EXPERIMENTAL VERIFICATION

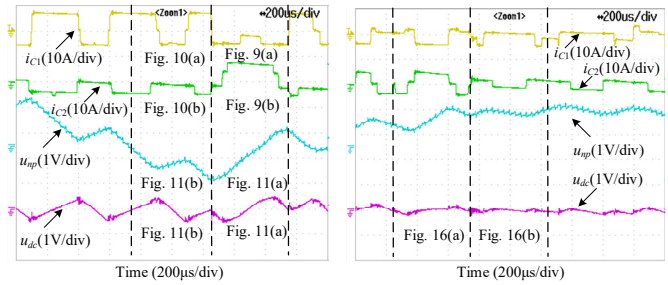
The experiments are carried out on a laboratory prototype of NPC-3L inverter-fed dual three-phase PMSM drive to validate the proposed switching strategy. The key system parameters are shown in Table II. A photograph of the experimental setup is shown in Fig. 20. The control algorithm is implemented on DSP (TMS320F28346), while the PWM inverter gating signals are generated by FPGA (Xilinx-Spartan6 XC6SLX25). A three-phase synchronous generator, mechanically coupled to the dual three-phase PMSM, is used as a load.

Firstly, the experimental current and voltage waveforms in Fig. 21 and Fig. 22, at typical operating points P1 and P2, and with different switching methods, are compared with the theoretical analysis (Fig. 6, Fig. 8, Fig. 9, Fig. 10, Fig. 11, Fig. 13, Fig. 14, Fig. 15 and Fig. 16). Fig. 21 shows the measurement results at P1. The synchronous switching method is used in Fig. 21(a) whereas the proposed two-step collaborative switching strategy is used in Fig. 21(b). Fig. 21(a) agrees well with the analysis in Fig. 6 and Fig. 8, while Fig. 21(b) corresponds to the analysis in Fig. 13-15. Note that the algorithm is dynamically choosing if the positive or negative vectors (i.e., 1N2P or 1P2N for the proposed method) are used in each switching period. Thus, the switching periods to be compared with the relevant theoretical analysis are clearly denoted in Fig. 21 and Fig. 22. Fig. 22 presents measurement results at operating point P2. The synchronous switching method is used in Fig. 22(a) whereas the proposed method is used in Fig. 22(b). Specifically, Fig. 22(a) corresponds to the analysis in Figs. 9-11. Fig. 22(b) corresponds to the analysis in Fig. 16. It should be noted that the actual duty cycle of each switching sequence is slightly different from theoretical




(a) (b)

Fig. 21. Current and voltage waveforms at operating point P1 with: (a) synchronous and (b) proposed switching method.



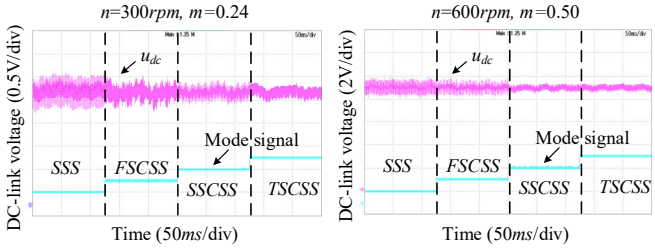

(a) (b)

Fig. 22. Current and voltage waveforms at operating point P2 with: (a) synchronous and (b) proposed switching method.

analysis since the waveforms are measured within two consecutive switching periods. From previous comparison, it can be concluded that the experimental results at both operating points well agree with the theoretical analysis. The concerned ripples are effectively mitigated after applying the proposed switching method.

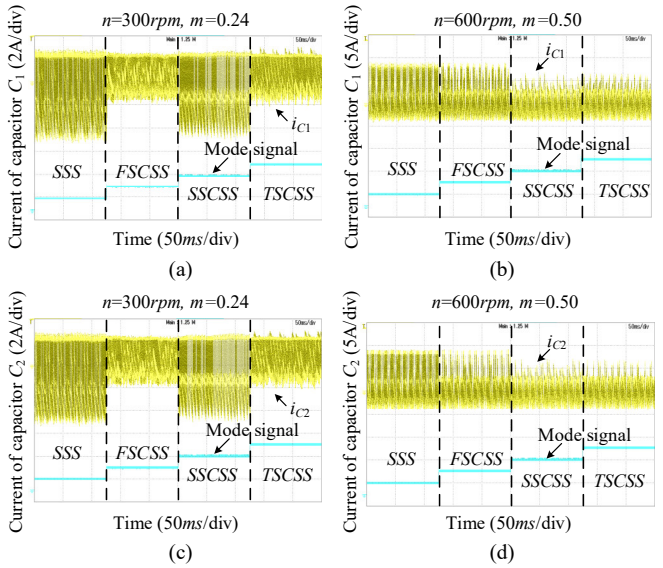
Secondly, the steady-state waveforms of current and voltage ripples are compared for different switching strategies in Fig. 23 and Fig. 24 ($n$ represents machine speed). Applied strategies are denoted as: SSS stands for synchronous switching strategy, FSCSS represents the switching strategy with opposite small vector sequences in the first step of the algorithm only, SSCSS represents the switching strategy with rearranged switching sequences in the second step of the algorithm only, and TSCSS represents the proposed two-step collaborative switching strategy. FSCSS and SSCSS are established from the proposed TSCSS to verify the necessity of both the two steps in the proposed algorithm. Operation at two different modulation indexes is achieved by changing the speed of the machine. Specifically, the modulation index equals 0.24 and 0.50 at speeds of 300rpm and 600rpm, respectively. The fundamental stator frequencies are 15Hz and 30Hz at the speed of 300rpm and 600rpm, respectively, and the corresponding power factor angles are –16° and –27°, respectively. All the capacitor current and voltage ripple waveforms are measured by AC coupling of probes. Fig. 23(a) and Fig. 23(b) show the comparison results of the DC-link voltage ripple. As shown in Fig. 23, SSCSS and TSCSS possess lower DC-link voltage ripple compared to SSS and FSCSS at both modulation index values. Therefore, it verifies that the rearrangement of the switching sequence in the second step of the proposed algorithm can effectively mitigate the DC-link voltage ripple.

Fig. 24 presents the comparison results of the capacitor current ripples using different switching strategies. As shown




(a) (b)

Fig. 23. Comparison of the DC-link voltage ripples with different switching strategies: (a) $m$=0.24, (b) $m$=0.50.




(a) (b) (c) (d)

Fig. 24. Comparison of steady-state current ripples of the capacitors. Current ripple of: $C_1$ at (a) $m$=0.24, (b) $m$=0.50; of $C_2$ at (c) $m$=0.24, (d) $m$=0.50.

in Fig. 24(a), the current ripple in $C_1$ with FSCSS and TSCSS is lower than that with SSS and SSCSS. The reason is that, as analyzed in Section IV-A, $i_{C1}$ equals $I_s$ when sequences with negative small vectors are used. Therefore, SSCSS can only reduce the peak-to-peak current ripple in $C_1$ during the intervals when using sequences with positive small vectors. However, sequences with positive and negative small vectors are used alternately in the two inverters in practical operation. Fig. 24(b) shows the comparison results at modulation index of 0.50. It is observed that both the proposed TSCSS and the SSCSS have lower current ripple amplitude than SSS and FSCSS. The reason lies in the fact that both middle and large vectors will generate current ripples in the two capacitors, respectively. Therefore, under high modulation index operation, only the opposite small vector operation in the first step cannot ensure that the current ripples caused by the two inverters are separated into two capacitors, respectively. Consequently, with the rearranged sequences in the second step, the ripples in the two capacitors can be mitigated more effectively. Fig. 24(c) and Fig. 24(d) are the current waveforms of capacitor $C_2$ under low and high modulation index operation, respectively. The results and conclusions are similar to those in capacitor $C_1$ (Fig. 24(a) and Fig. 24(b)).

Fig. 25 compares the control performance of the mid-point voltage using four different switching strategies. As shown in Fig. 25(a), the fluctuation range of the mid-point voltage with

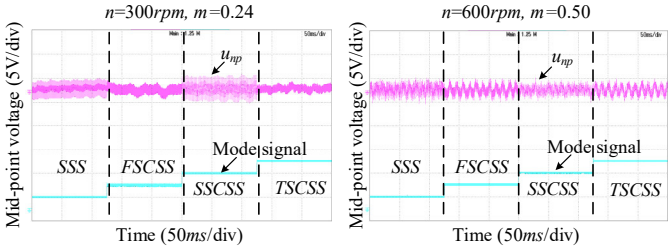



Fig. 25. Comparison of steady-state mid-point voltage waveforms with different switching strategies: (a) $m$=0.24, (b) $m$=0.50.

SSCSS is similar to that with SSS. The reason lies in the fact that the rearrangement of the switching sequence cannot influence the integral value of the neutral point current during the whole switching period. On the other hand, FSCSS and TSCSS can provide much smaller ripples in the mid-point voltage waveform by using the opposite small vector sequences in two inverters. As shown in Fig. 25(b), the mid-point voltage ripple amplitude is almost the same for all switching strategies under high modulation index operation. Furthermore, it can be observed that only the 3rd-order harmonic ripple exists when FSCSS and TSCSS are utilized. It verifies that the ripples generated by the small vectors can be reduced effectively with the proposed TSCSS while the 3rd-order harmonic ripple caused by the middle vectors cannot be mitigated under high modulation index conditions. According to the steady-state experimental results shown in Figs. 23-25, it can be concluded that the proposed TSCSS possesses the best ripple mitigation capability among the four switching strategies at both low and high modulation index operation.

To verify the influence of the power factor on ripple reduction, the power factor angle was changed by adjusting the $d$-axis current of the machine. However, the same conclusions were reached. For low modulation indexes all ripples are reduced, regardless of the power factor angle. Yet, for high modulation index values, capacitor current and the DC-link voltage ripples are reduced, while the high-frequency fluctuation in the mid-point voltage is mitigated with the proposed switching method.

Finally, the current ripple and the mid-point voltage fluctuation waveforms of SSS and the proposed TSCSS are compared during dynamic response. The speed reference value $n_{ref}$ is step changed from 300rpm to 600rpm. Fig. 26 presents the current ripple waveforms in capacitors $C_1$ and $C_2$, respectively. The same conclusions as for the steady state results in Fig. 24 can be drawn. During the dynamic response, the current ripples in the capacitors $C_1$ and $C_2$ using the proposed TSCSS are always smaller than those using SSS. Fig. 27 shows the comparison of the mid-point voltage during dynamic operation. Clearly, conclusions related to the ripple reduction are consistent with the steady-state results shown in Fig. 25. Besides, the total harmonic distortion (THD) values of stator current in phase A at modulation index of 0.24 using SSS and TSCSS are found to be 5.45% and 6.03%, respectively. The THD values at modulation index of 0.50 using SSS and TSCSS are 4.42% and 4.86%, respectively. The proposed TSCSS generates slightly higher but acceptable THD values in stator currents, which is due to the rearrangement of the switching sequences.

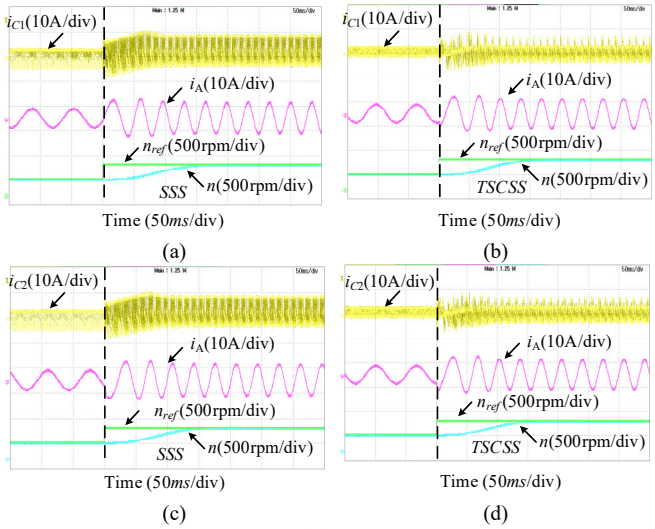



Fig. 26. Capacitor current ripples with different switching strategies during the transient. Current ripple of $C_1$ (a) with SSS, (b) with proposed TSCSS; and current ripple of $C_2$ (c) with SSS, (d) with proposed TSCSS.

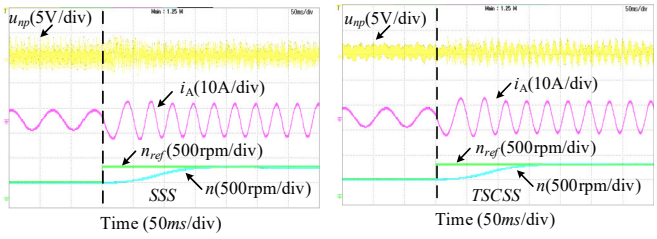



Fig. 27. Mid-point voltage waveforms with different switching strategies during the transient: (a) SSS, (b) proposed TSCSS.

## VII. Conclusion

In this paper, a two-step collaborative switching strategy has been proposed to mitigate the current and voltage DC-link ripples in an NPC-3L inverter-fed dual three-phase PMSM drive. The first step is to select switching sequences including opposite small vectors for the two inverters, and the second step is to rearrange switching states of the two inverters in order of the sum of their current components in the upper and lower capacitors in the DC-link. The proposed collaborative switching strategy possesses the following advantages: lower current ripples in the DC-link capacitors and smaller DC-link voltage ripples, which are achieved under both low and high modulation index operation. The peak-to-peak fluctuation of the mid-point voltage can be reduced under low modulation index operation, while the high-frequency voltage fluctuation can be mitigated under high modulation index operation. The experimental results have been presented to verify the validity of the proposed collaborative switching strategy. Reduced DC-link voltage and current ripples can not only reduce the DC-link capacitance but could also facilitate extension of the lifetime and reliability of the DC-link capacitors.

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