Reliability and Failure Modelling of Microelectronic Packages Based on Ultrasonic Nondestructive Evaluation Data

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Abstract

Reliability testing and failure modelling is crucial and very challenging for modern electronics, especially safety critical electronics-based systems working under harsh environmental conditions. In this paper, an approach based on ultrasonic Non-Destructive Evaluation (NDE) is proposed to establish a failure model for solder joints which is urgently needed for prognostic and health management of electronics. Printed Circuit Boards (PCB) containing flip-chip and Area Array packages were designed and aged using Accelerated Thermal Cycling (ATC) testing. During ATC testing solder joint degradation was regularly monitored by taking out the test boards from the temperature chamber at four thermal cycle intervals for ultrasonic micro-imaging. Data pre-processing techniques including dynamic range-based intensity normalization, gain compensation, and calibration for random transducer defocusing errors were developed to enhance the data consistency, integrity and accuracy. Furthermore, solder joint image labelling and segmentation methods were developed by exploiting the geometrical features of the solder joints to extract individual solder joints and Region of Interests (ROIs) from the sequential ultrasound images collected throughout the testing. The mean intensity of the ROIs was used as the precursor to degradation to build the solder joint failure model, from which cycles to failure for individual solder joints are finally derived for life prediction.

Keywords: Reliability, Ultrasonic Non-Destructive Evaluation, Accelerated Thermal Cycling, Failure model, Solder Joints

1. Introduction

Safety critical electronics systems and particularly those deployed in autonomous drive and avionics applications are powering a growing need in reliability engineering towards system health assessment and prediction of the remaining useful life of electronics systems [1,2]. As microelectronic packaging technology is moving to three-dimensional (3D) packaging with higher integration of functional components [3], the ever-increasing power density of the chip and the complex multi-layer structures have led not only the thermal management and heat dissipation challenges, but also significant impact on the reliability of microelectronic packages [4].

Establishment of accurate failure models of solder joints/electronics are critical for success of prognostics and health management of electronics. At present, the existing life prediction/failure models are mainly developed using empirical methods [5,6,7]. Based on the control variables in the models, the fatigue life models are often classified as stress type, strain type, energy type, fracture based mechanical type, and dam- age accumulation based mechanical type. The state of the art models are shown in figure 1 [8,9,10]. Each model has certain limitations and is only applicable to specific defects, packaging forms or over defined thermal boundary.

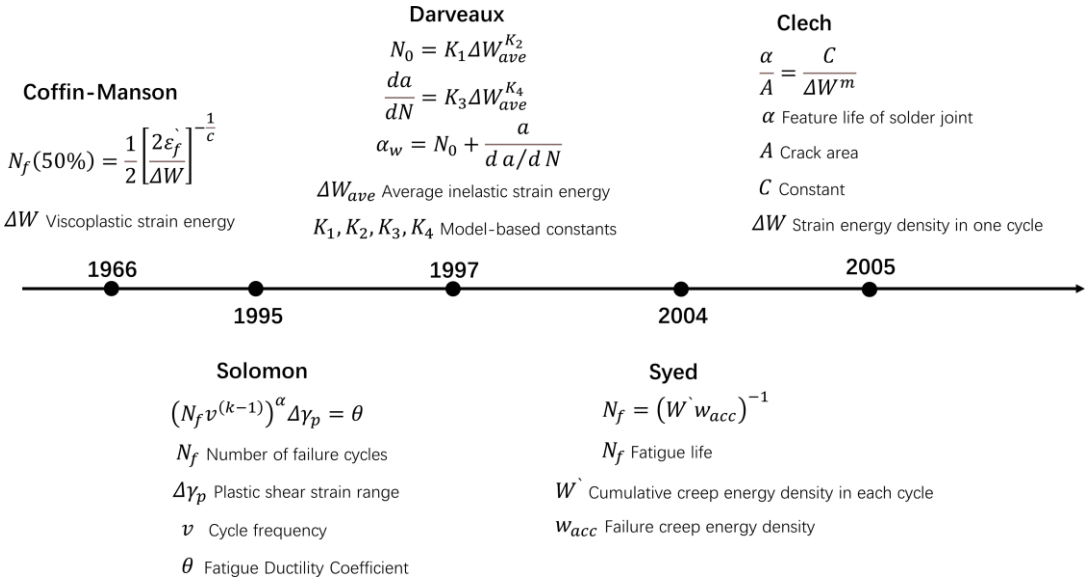

Figure 1: Electronic packaging fatigue life prediction model and its evolution [8,9,10].

Solder joints are difficult to model due to their exposure in field to multiaxial stresses, as a result, they are subjected to creep-based stress in combination with cyclic strain. There are also additional boundary. conditions that affect the accuracy of failure modelling, such as the joint geometry, dwell times at thermal extremes, usage factor, soldering defects, grain size, microstructure of the solder joints [11], and location of the packaged device on the circuit board floor plan [12]. The residual strains on the circuit board assembly introduced during the manufacturing process complicate the issue even further. The inclusion or exclusion of such behaviours contribute significantly to the limitations of existing models to replicate real world applications. Moreover, the model constants in the existing empirical models were often determined by correlating the measured crack growth data with calculated inelastic strain energy density per cycle in solder joints, and the crack location and size were measured throughout the thermal cycling using destructive techniques [13]. Undeniably, the accuracy of a life model greatly depends on the accuracy of measuring the crack size. However, the use of destructive failure analysis tools places a major hindrance on the development of failure models:

1. For each measurement, the solder joints are destroyed so that we cannot track the through-life of an individual solder joint. As a result, a failure distribution, e.g. a 3-paramter Weibull distribution, must be assumed in order to predict fatigue life;
2. Not all joints are subjected to identical stress [14]. Since the accelerated life prediction models are based on experimental observations, it is important to understand the behaviors of individual solder joint that are located in different positions of the package and PCB board.

Another widely-used approach to model the fatigue failure for specific components or solder joints is finite element analysis [15, 16, 17]. Notice that due to the complexity of the problem, almost all finite element models simplify the mechanical and thermal properties of the packaging material and the packaging structure to varying degrees. To avoid the limitations of finite element analysis, the simulation model can be improved through experimental verification.

Using Non-Destructive Evaluation (NDE) techniques in solder joint reliability testing, which do not influence joint behaviors, will be of great benefit to the development and verification of failure models. Scanning Acoustic Microscopy (SAM), also known as Acoustic Micro Imaging (AMI), is one of the non-destructive analysis tools widely used in the electronic industry to evaluate solder joints in flip-chip packages

due to its high resolution and strong penetration. Through the use of ultra-high frequency ultrasound, SAM can monitor solder joint defects better than other inspection methods at micron level [18].

In our previous preliminary research, we proposed a methodology for through life non-destructive monitoring of solder joints [19]. Test boards mounted with flip-chips and BGA packages were designed and aged using accelerated thermal cycling (ATC) testing. During ATC testing, solder joint degradation was regularly monitored by taking out the test boards from the temperature chamber for ultrasound inspection. Solder joint features from ultrasound images were extracted using a Hough transform for automated solder joint assessment. We also developed a finite element model to investigate the fundamental mechanism that causes edge effect in acoustic micro imaging of electronic packages [20, 21, 22]. Our preliminary results discovered that there exists a quantitative relationship between the crack size and the geometric features extracted from the ultrasonic images contaminated by edge effect, turning the negative edge effect phenomena into a positive tools able to characterise nano-crack propagation in the solder bump. However, a number of issues limited our further in-depth research work:

1. ATC testing was too harsh. As a result, the test samples were failed in 96 cycles. The samples were taken out for ultrasound scan at eight thermal cycle intervals. As a result, only 12 data points were available to model the failure curve, preventing from building an accurate solder joint failure model.
2. A low scan resolution was used during ultrasonic inspection. As a result, the number of image pixels in an extracted solder joint ultrasonic image are very limited, hindering the accurate extraction of features that are used to characterise the defect sizes.
3. The solder joint image segmentation was carried out based on imaging processing without physical interpretation.
4. The consistence, integrity and accuracy of the collected ultrasonic dataset are not up to a high standard.

In this paper we redesigned and carried out the experiment by carefully considering all the issues met in our previous work in order to pursue an in depth research for this very promising approach. The key contributions of this paper are summarized as follows:

1. Developed a systematically refined methodology for through life non-destructive monitoring;
2. Redesigned experiments ensure the acquisition of a very high-quality dataset. We spend more than 1-year to carried out the very fine experiment and collected >2Tbytes of ultrasound imaging data;
3. Developed novel data pre-processing methods to ensure data consistence, integrity and accuracy;
4. Developed a solder joint segmentation method to extract ROIs by utilizing the a-prior information obtained from our simulation study in [20, 21];
5. Established a fatigue life prediction model of solder joints, where the differences between individual solder joints located in different positions of the package and PCB board are defined, overcoming one of the shortcomings of conventional model development methods.

The rest of this paper is organized as follows. Section 2 describes the methodology of solder joint failure modelling and the design of the test board, thermal profile and scan scheme. Section 3 introduces the experimental results of dynamic range normalization, calibration and gain compensation before the Region of Interest (ROI) segmentation. Section 4 describes the principle and experimental results of the image segmentation algorithm based on local minimum. Section 5 presents the failure model and life prediction of individual solder joints. The conclusion is drawn in Section 6.

2. Ultrasonic NDE data-based Solder Joint failure modelling

2.1. Methodology

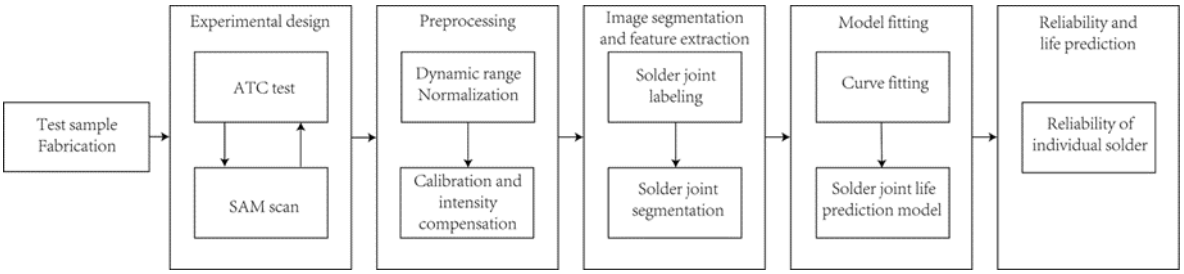

Figure 2: Flowchart of the proposed methodology

As mentioned above, the methodology for ultrasonic NDE data based solder joint failure modelling in this work is upgraded from our previous work as shown in Figure 2. The fatigue stresses/strains in the solder joints were accumulated as the thermal cycles increase, as a result, degrees of aging and degradation of the solder joints increase. Thus, we can assume the defect size in the solder joints increases as the cycle number increases. The collected ultrasonic NDE data contains information of internal defects from initiation through progression to failure. The use of SAM enables the through-life monitoring of solder joint reliability while maintaining the integrity of the test boards for further test cycles, facilitating the development of an accurate failure model for individual solder joints.

Due to the resolution limit and Edge Effect Phenomena (EEP) [20], it is impossible to visually measure micro-cracks and nano-cracks from the ultrasonic images of a solder joint that has a diameter smaller than 30μm for the modern microelectronic packages. Our previous finite elemental modeling study on EEP [21] showed that these images contain the hidden defect information that modifies the image features such as the geometric, frequency, and statistical features, especially in the edge effect area. We discovered that there is a quantitative relationship between the crack size and the geometric features extracted from the ultrasonic images contaminated by the edge effect. As a result, the negative EEP has a great potential to be turned into a positive tool to characterize nano-crack propagation in the solder joint. To achieve this, it is crucial to identify and extract the precursors/features from the ultrasonic images to track and monitor the internal defects of the solder joints. In this paper, image processing techniques were developed to segment images and determine ROIs. Using data analysis, the curve of the solder joint intensity variation was plotted against the ATC cycles and a solder joint failure model for individual solder joints was established.

2.2. Experimental Design

The experimental work required careful design to eliminate variation in the measurements that would impact the quality of the data set. Especially as the experimental data would be collected over a 1-year experimental period and depending on the measurement setup parameters would generate >2Tbytes of ultrasound imaging data.

2.2.1. Design and fabrication of test board

Four test boards as shown in Figure 4 were designed and fabricated. Two package types, plastic BGA and flip-chip, were assembled onto dual sided copper FR-4 substrate having either Hot Air Solder Levelled (HASL) surface finish or Electroless Nickel Immersion Gold (ENIG) surface finish to allow a multifactorial design of experiments to be performed. Also, the 3D X-ray image of flip-chip structure Schematic shown in figure 5 illustrate the layout of flip-chip packages in the PCB board. In order to study the impact of the floor plan layout on joint reliability [12]. The flip-chip packages were placed on both sides of the test board using four different configurations as illustrated in Figure 3. single sided placement, double sided breadth offset placement, Double sided length offset placement and mirror placement.

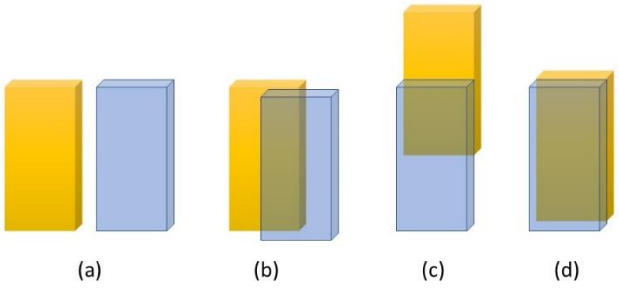

Figure 3. Diagram of four different configuration (a) single side placement, (b) double sided breadth offset placement, (c) double sided length offset placement, (d) mirror placement.

1. Single sided placement: single sided flip chip with no back-to-back connection. i.e., U23 and U26;
2. Double sided breadth offset placement: a pair of double sided flip chip placed back-to-back with an offset along the breadth. i.e., U19 and U35, U20 and U36.
3. Double sided length offset placement: a pair of double-sided flip chip placed back-to-back with an offset along the length. i.e., U27 and U39, U28 and U40.
4. Mirror placement: a pair of double sided flip chip placed exactly back-to-back with no offset. i.e., U34 and U46, U31 and U43.

Figure 4: Flip-chip packages on the front and back side of test board

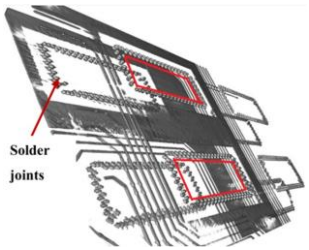

Figure 5: 3D X-ray image of flip-chip structure Schematic shows the layout of flip-chip packages in the PCB board.

Each flip-chip package contained 109 SnPb solder joints of 140μm diameter and 125μm height positioned in a staggered fashion as two rows at the periphery of the package. The rectangular die with a dimension of 3948μm$\times$8898μm and a thickness of 725μm was reflowed to the organic substrate without underfill, which aided the generation of joint failures within an affordable time period.

2.2.2. Design of the ATC Test

For ATC testing, a thermal cycling chamber having a range of -70˚C to 180˚C and the ramp rate of 12˚C/min was used throughout this experiment. Test boards were vertically hung by their mounting holes using wire clips attached to a mesh framed shelf internal to the chamber. This ensures airflow and

homogeneous temperature is achieved around the boards without influence from the thermal mass of the chamber shelf. Furthermore, the boards were instrumented with "T" type thermocouples to ensure that the components achieved the set point values and profile programmed on the climatic chamber temperature controller. In this experiment, a much softer thermal profile than our previous work in [12] was designed to enable finer tracking of crack propagation in solder joints and thus increase the data points significantly for the establishment of an accurate failure model. The accelerated thermal profile used was -40˚C to 85˚C with 30 minutes dwell time, and the ramp rate was 5˚C/min as shown in Figure 6. Testing was performed until the flip-chip parts fell off from the PCB, this occurred at 352 thermal cycles. Moreover, in order to increase the data points, the circuit board assemblies were removed from the chamber and solder joint integrity inspected nondestructively using SAM before returning them back to the environmental chamber to continue the accelerated testing at four-cycle intervals rather than eight cycles used in our previous work. Obviously, high data point generation was at a price of significantly increasing the experimental time. In addition, be- fore the start of the ATC test, SAM scans were performed on all flip-chip packages. This initial inspection provided baseline non stressed data at time zero.

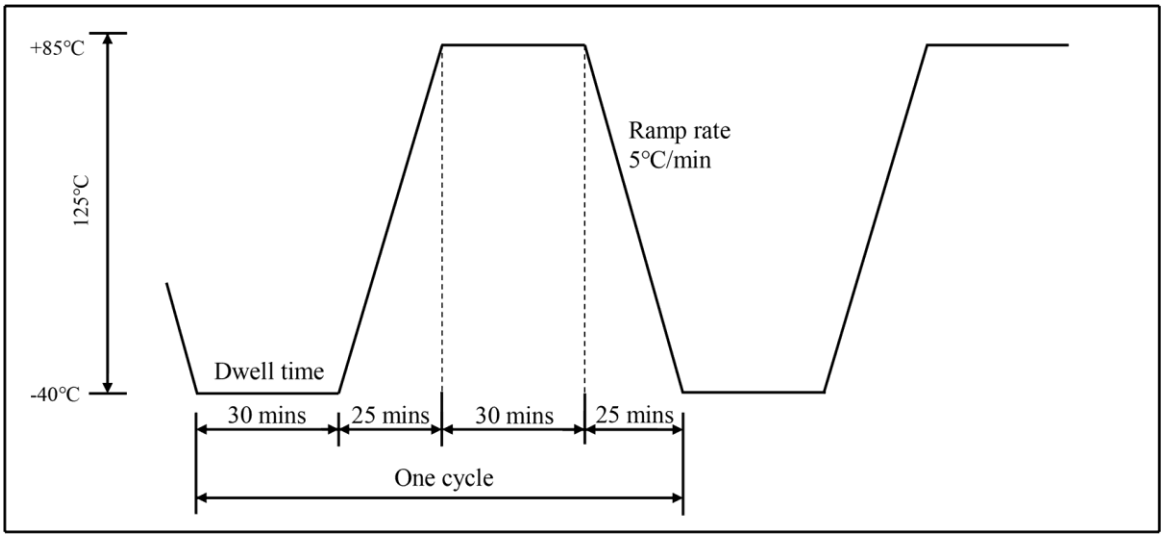

Figure 6: The thermal profile used in the accelerated thermal cycling test.

2.2.3. Design of the SAM scan scheme

The cross-section schematic of the flip-chip package is shown in Figure 7a. Solder joint degradation is inspected by mechanically scanning the flip-chip packages using a 230MHz transducer having a 0.25inch focal length in our Sonoscan Gen6^{TM} C-Mode SAM. The ultrasonic images obtained, like the one shown in Figure 7b, were stored electronically. Ultrasonic C-scan images are formed when the transducer is moved across the surface of the flip-chip and at each X-Y coordinate position, with the reflected ultrasonic RF signal (ultrasonic A-scan) gated to the interface being inspected using an electronic gate. The maximum amplitude of the gated signal is stored as the pixel value of the given X-Y position in the C-scan image. Since solder joint failures often occur at the die to bump interface, the electronic gate was thus selected to image this interface in our experiment. Moreover, 3D acoustic data (a virtual acoustic sample of the whole flip-chip package) was also collected using the 3D VRM mode of the SAM system, which can be used to generate enhanced C-scan images using our 3D acoustic micro imaging technique [13]. The 3D acoustic data can also be used to evaluate the other interfaces.

Imaging resolution of SAM systems is determined by the transducer spot size. The ultrasonic image size is governed by two parameters, the scanning area and scanning resolution. A scanning resolution normally smaller than the imaging resolution will generate redundant pixels for the ultrasonic images, as a result, a

larger pixel number will improve the accuracy of quantitatively evaluating the sizes of invisible defects that are hidden in the ultrasonic images. On the other hand, the smaller the scanning resolution, the longer the scan time is required to scan a package. From our experience and experimental work, with a scanning resolution of 1um/pixel, more than 30 hours are required to scan all 14 flip-chips, as a result, more than 2200 hours scan time are estimated in total for this experiment. On balance of time cost vs image quality, the scanning resolution was set to 3 μm/pixel.

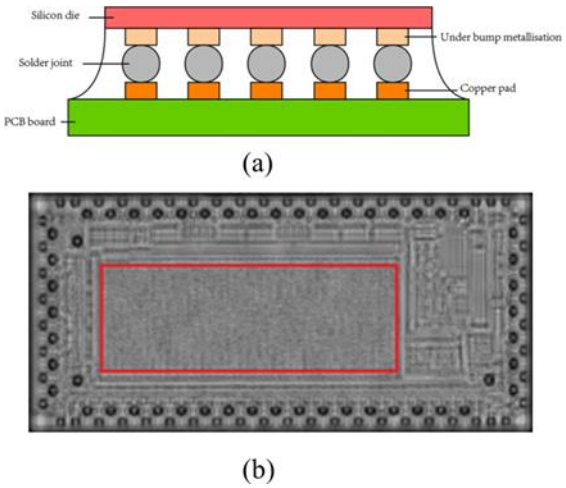

Figure 7: (a)Cross-section schematic of a typical flip-chip on board assembly; (b) An ultrasonic C-scan image of the silicon die to solder joint interface of the flip-chip assembly.

Figure 8 shows the ultrasonic images of the U19 flip-chip obtained after 0, 100, 200, 352 cycles ATC test respectively. From the enlarged solder joint images (far right) in Fig.7 it can be seen that the bright area in the middle of the solder joint is increasing and the black ring due to the edge effect was gradually weakening as the ATC test cycles increase. The physical interpretation on edge effect were studied and elaborated through finite element analysis in our research group [21, 22], which also revealed that older joint degradation can be monitored and tracked potentially by analyzing the time domain, frequency domain and statistical features of the solder joint images although we cannot visually detect the tiny defects inside the solder joints.

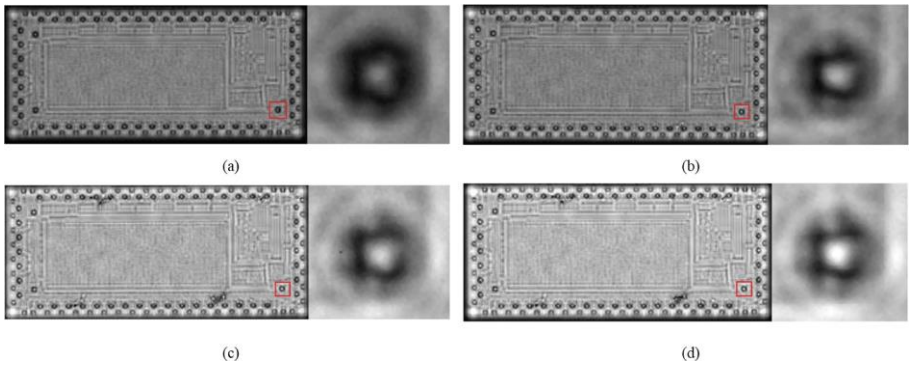

Figure 8: Ultrasonic images of a flip-chip package obtained after(a) 0 cycles ATC test; (b) 100 cycles; (c) 200 cycles; (d) 352 cycles. The enlarged images in the right side is from the solder joints marked in red in the left side images.

The solder joints located on the outer row are usually selected to monitor the aging because these solder joints are subjected to stronger stress, solder joint fail more quickly and changes in features are more easily to observed. However, the life prediction method proposed in this paper is based on the features from ultrasonic image. therefore, to demonstrate the method and the result of the algorithm more clearly, not only the position of the solder joint is important, but also the image quality of the solder joint during the accelerated thermal cycling experiment should be considered. According to our previous research [21,22], the edge effects can greatly affect image quality when imaging flip-chips using an ultrasound microscope system. That was because when the ultrasound signal hits the edge of the material, part of the signal is not reflected back to the receiver, but is scattered and reflected in an ambiguous direction, causing a loss of information.

Take the solder joint No.6 on the outer row as an example. The ultrasonic image of solder joint No.6 at 0, 100, 200 and 352 cycles of the thermal experiment are shown in the figure 9:

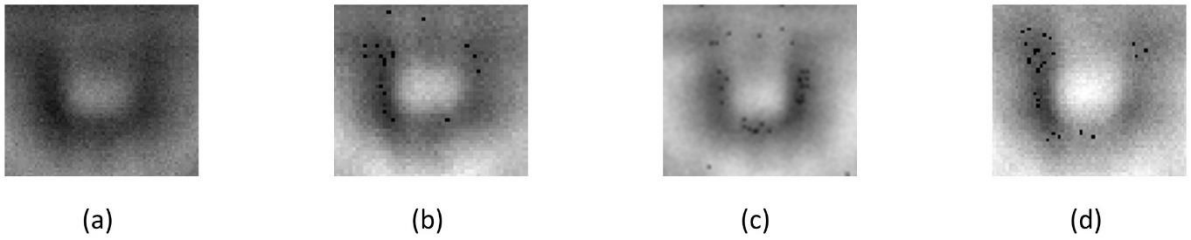

Figure 9. The ultrasonic image of solder joint No.6 on flip-chip U19 after (a) 0, (b) 100, (c) 200, (d) 352 cycles.

The small black dots in the figure are caused by system noise during imaging, which can be removed by median filtering.

Compared to solder joint No.52 in figure 8, solder joint No. 6 is more severely affected by the edge effect, the edges of the solder joint appear blurred and distorted, most of the solder joint in these images can not form a closed circle, which makes it difficult to determine the ROI of the solder joint image to extract the feature for the remaining life analysis in the subsequent section. It is important to notice that not only solder joint No.6, all the solder joint on the outer row are suffered from the same problem. And closer the solder joint is to the center of the flip-chip, the less it will be damaged by the edge effect. Therefore, solder joint No.52 in the innermost row was selected to demonstrate the performance of the algorithm in this paper.

3. Image Preprocessing

Preprocessing operations were proposed and carried out to ensure consistency, integrity and accuracy of the information extracted from the ultrasonic images.

3.1. Dynamic Range Based Intensity Normalization

Intensity in ultrasonic images is rich in information. During the acoustic scan, the gain of the SAM system was set up to ensure that high quality images were obtained in terms of image contrast. As thermal cycles increase, the solder joint degradation becomes more observable, causing stronger ultrasonic reflections and an increase in image intensity in regions of higher acoustic impedance. As a result, there is a need to lower the gain so that the images do not saturate. For images acquired between the gain changes, the dynamic range of intensity changes as shown in Figure 10, although the gain setting is the same. Figure 10 shows the histograms of ultrasonic images for the U23 flip-chip package obtained after 100, 104, 108, and 112 ATC cycles. Although these ultrasonic images are 8 bits, their actual dynamic ranges are 85, 100, 120, and 140 respectively. As a result, the same intensity value at different dynamic range will represent different meanings. Moreover, this leads to an inaccurate or wrong failure modelling. Consequently, dynamic range based intensity normalization was carried out to stabilize the dynamic range into 8 bits for all the images. The operation is summarized is as follows:

1. Searching all the pixels of the original image X to find the biggest intensity value x_{max} and smallest one $x_{min.}$
2. Calculating the dynamic range R_{orig} of X as $R_{orig}=x_{max}-x_{min.}$
3. Computing the middle number between x_{min} and x_{max}, i.e., the median $x_{med.}$
4. Scaling the original image X using a new range R_{norm}. Assuming that p and q are the lower and upper boundary of the new range, and keeping the median of R_{norm} to be x_{med}, then $p= x_{med} - R_{norm}/2$. The scaling operation is described by the following equation:

$$x_{ij} = p + \frac{x_{ij} - x_{\min}}{R_{orig}} \times (q - p) = x_{med} - \frac{R_{norm}}{2} + \frac{x_{ij} - x_{\min}}{R_{orig}} \times R_{norm} \quad (1)$$

x_{ij} is a pixel in the image X. For the 8bit range, $R_{norm}=256$. Notice that the intensity at some pixels may be bigger than 256 due to the fact that the lower boundary p may be significantly bigger than 0.

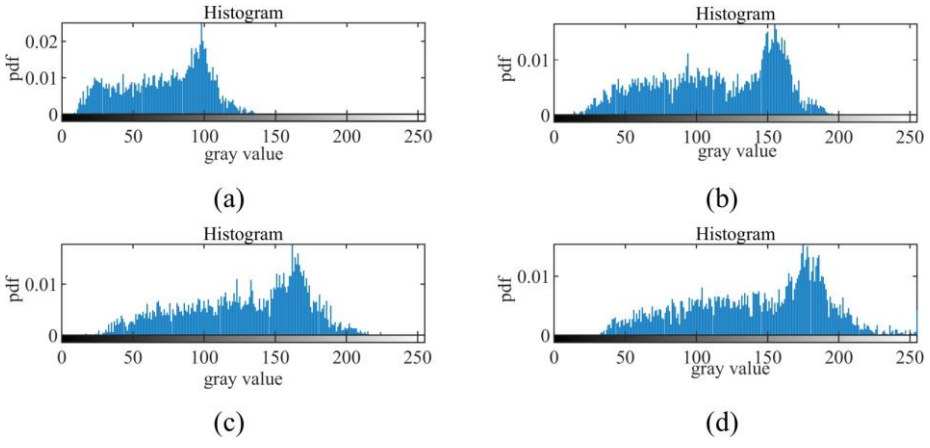

Figure 10: Grayscale distribution of solder joints in diverse cycles: (a) 100 cycle, (b) 104 cycle, (c) 108 cycle, (d) 112 cycle. Pdf: probability density function.

3.2. Gain compensation

Following dynamic range normalization, the next preprocessing step is gain compensation. As mentioned in Section 3.2, the gain is changed a few times by the operator during the SAM scan. For these

known gain changes, the absolute intensity values were directly compensated for the corresponding images.

3.3. Random transducer defocusing error calibration

Throughout the experimental work, test samples are repeatedly scanned and put back into the thermal chamber. Although fixtures were designed to keep the test samples and ultrasonic transducer located in the same positions throughout the whole experiment, minor deviations in transducer and test samples' position cannot be fully prevented. The resulting random 'defocus' could lead to a significant change in image intensity due to the short focal length of the 230MHz transducer. Calibration and intensity compensation have to be carried out to rectify the image intensity error caused by the random transducer defocusing.

Although solder joint degradation produces the intensity changes in the ultrasonic images during the ATC test, the intensity of the middle area circled in red in Figure 7b should not change for all the ultrasonic images acquired at different inspection points during the ATC cycles if the transducer is perfectly focused because this area was filled in with the coupling water during the imaging stage and the acoustic impedances of the silicon die and water will not change. Therefore, the average image intensity in this area is selected as the reference to calibrate and compensate all the ultrasound images. The intensity calibration is mainly composed of the following three steps:

1. We calculate the mean intensity Ci of the central area for all the ultrasonic images $I_{xi,yi}$.
2. Then, using the mean intensity C_0 of the 0 cycle image $I_{x0,y0}$ as the reference, subtract all the subsequent mean intensity values from the reference to obtain the gain compensation value $G_i=C_i-C_0$
3. Finally, feed the gain compensation value back to the corresponding image $I_{xi,yi}$ to derive the compensated images $I_{xg,yg}$.

Figure 11 shows solder joints images at 0, 100, 200, 352 cycles before and after intensity calibration respectively. The maximum intensity values are 128, 140, 180, and 220 before calibration and 170, 210, 280, and 300 after calibration, respectively. Notice that some images may look the same due to the same contrast but their intensity values were completely different.

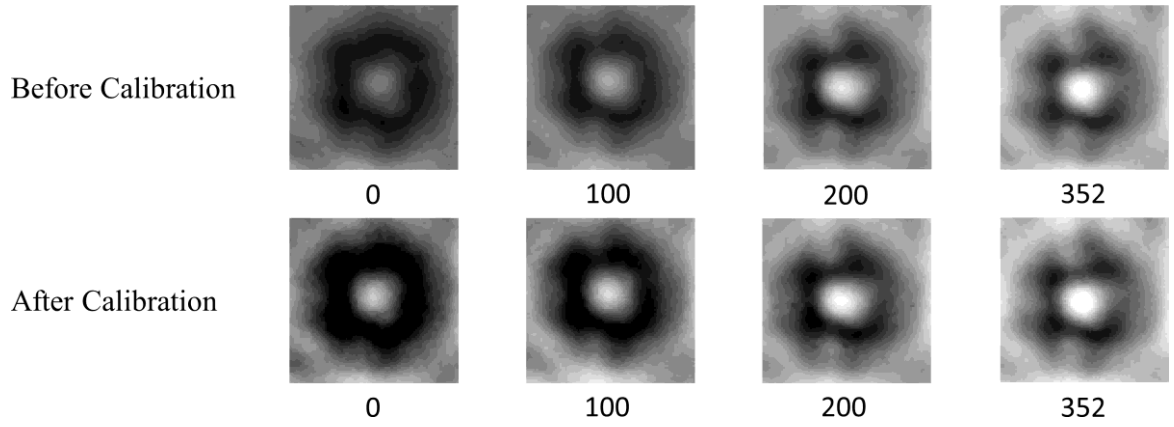

Figure 11: Solder joint images at 0,100,200,352 cycles before and after intensity calibration.

4. Labeling and Segmentation of Solder Joints

4.1. Labeling of Solder Joints

After image preprocessing, the solder joint labelling scheme depicted in Figure 12 was developed for the flip-chip packages. The labelling provides a unique identification and corresponding position information for the 109 individual solder joints. The solder joint in the upper left corner is labelled as No. 1, and then

the other joints are sorted in clockwise order.

Figure 12: Solder joint labelling scheme for the flip-chip packages.

Before labelling the solder joints, all the flip-chips are first aligned horizontally. Taking the end point of the lower left corner of a perfectly aligned image as the origin, with the lower edge as the x-axis and the left edge as the y-axis, a rectangular coordinate system is established as shown in Figure 13(a). Figure 13(b) shows a misaligned ultrasonic image. By moving the end point of the lower-left corner of the image to the origin O, $\angle COD = \theta$ and the coordinate of point C is $C(x_c, y_c)$. Drawing a vertical line through point C to intersect the x-axis at point D, the coordinate of point D is $D(x_c, 0)$. Therefore, θ can be calculated as $\theta = \arccos(x_c / \sqrt{x_c^2 + y_c^2})$. Finally, by using the rotate function in python to rotate the image, the alignment is completed. After image alignment, our experimental test shows that the 109 solder joints can be simply labelled by utilizing their known geometrical centres and no extra image processing is required.

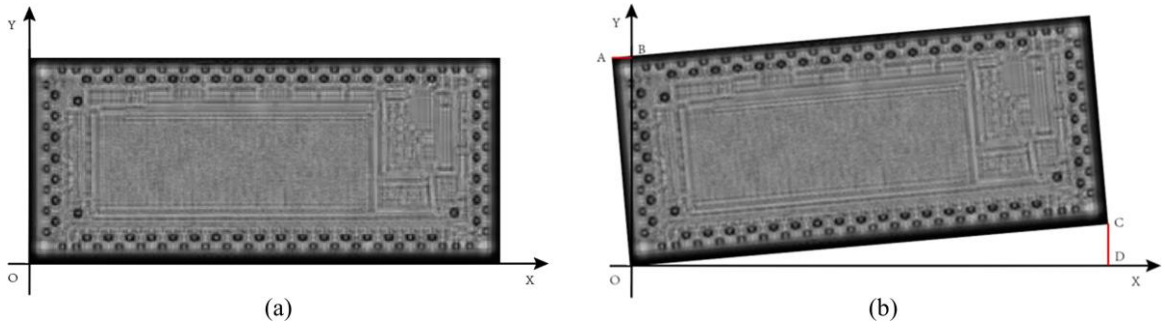

Figure 13: Ultrasonic image level alignment. (a) A perfectly aligned ultrasonic image; (b) a tilted flip-chip image

4.2. Segmentation of Solder Joints

4.2.1. Coarse segmentation of solder joints

Since the diameter of the solder bump is 140μm and the scanning rate is 3μm/pixel, a solder joint image should be 47 pixels in diameter. For coarse segmentation of solder joints, 80×80 pixels of solder joint

images as shown in Figure 14a are segmented based on their geometrical centres, which contains not only solder joints but also some surroundings.

4.2.2. Refined segmentation of ROIs

Our previous finite element modelling of ultrasonic wave propagation inside a flip-chip package [21], showed that the black ring in an ultrasonic C-scan image results from the edge effect phenomena and the central area enclosed by the black ring is strongly linked to the solder joint health condition. Therefore, from Figure 14a it can be observed that the area selected is an appropriate ROI to extract image features for through life monitoring and failure modelling of solder joints.

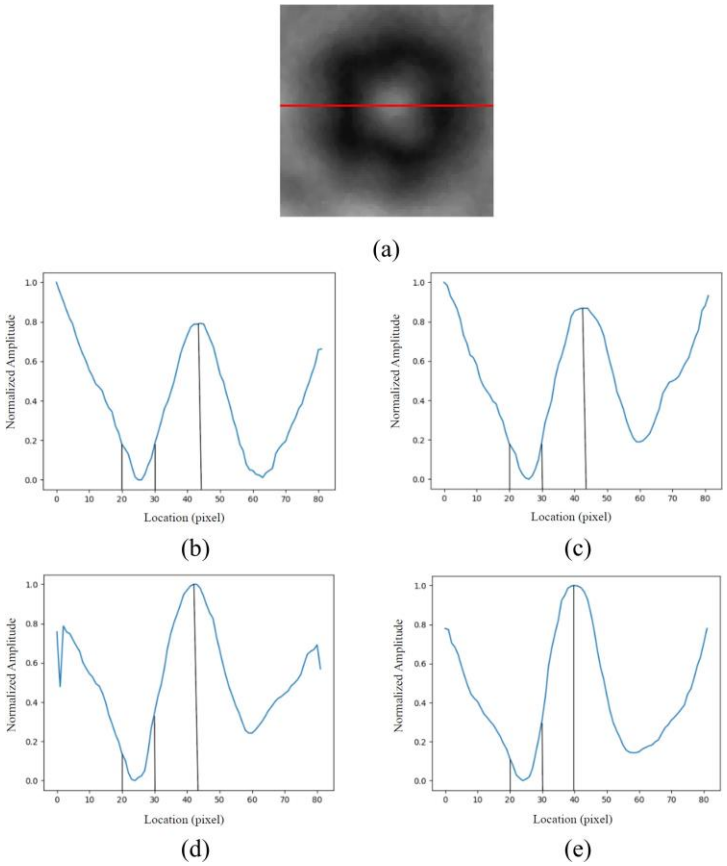

Figure 14: (a) A solder joint image; the C-line plots along the red line from the solder joint images of (b) 0 cycle, (c) 100 cycle, (d) 200 cycle, and (e)352 cycle.

Figures 14b to 14e show the C-line plots, i.e., the cross-sectional profiles of the solder joint images along the horizontal line shown in Figure 14a, after 0, 100, 200, and 352 cycles respectively. It can be observed that the obtained C-line plots are W-shaped, and that the valley points form a natural boundary/edge to the ROI. In this paper, a local minimum algorithm is proposed to detect this natural ROI edge as follows:

1. ***Finding the minimum points along each row and column.*** The valley points that constitute the edge should be the minimum points in their corresponding rows and columns. Since the edge is circular, each row or column of the image will have two edge points, and thus directly seeking the minimum value of each row or column will miss the edge point on one side. Therefore, when calculating the minimum value of each row, the image is divided vertically into two parts and calculated separately. In the same way, when calculating the minimum value of each column, the image level is divided into two parts and calculated separately.

2. ***Searching the valley points that constitute the ROI edge.*** This is achieved by merging the minimum points obtained in Step 1. Since the edge points are the minimum points in their ranks, the repeated points along the row and column are selected as edge points as shown in Figure 15.

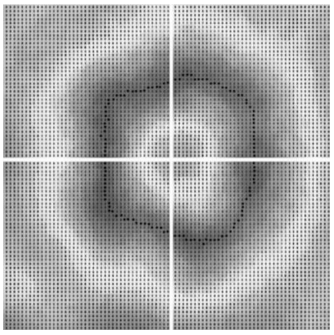

Figure 15: Edge points obtained by the proposed local minimum algorithm.

3. ***Forming a closed edge.*** To obtain a closed edge, the gap among the determined edge points needs to be filled. This is achieved by using the closing operation in mathematical morphology as follows:

$$A \bullet B = (A \oplus B) \Theta B \tag{2}$$

Where A is the original image, B is the structural element. To ensure edge accuracy, a $3_{\times}3$ square structural unit is used as the structural element. Figure 16 presents the examples of ROI edges at diverse cycles detected by the proposed local minimum algorithm.

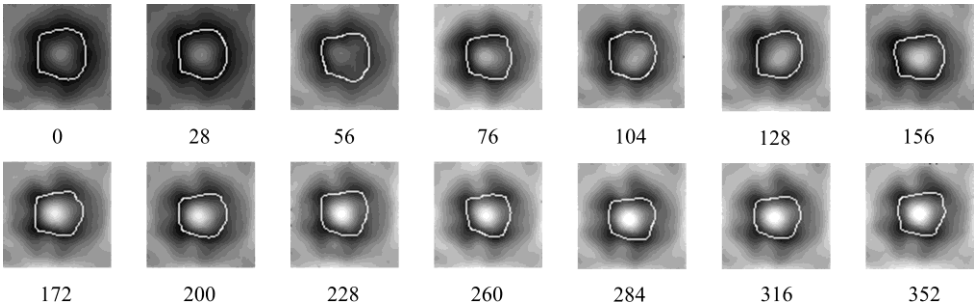

Figure 16: Examples of the ROI edges at diverse cycles detected by the proposed local minimum algorithm.

5. Failure modeling and reliability of individual solder joints

5.1. Establishment of a solder joint failure model

The failure model in this paper is built up using the ROI mean intensity as the precursor to solder joint degradation. Since the outer ring solder joints will be more severely affected by the edge effect, only the inner ring solder joints were investigated in this study. 28 flip-chips were used for experiments, each flip

chip containing 51 solder joints in the inner ring. Therefore, a total of 1428 inner solder joints were used as test sample. The mean intensity values of all the ROIs were calculated.

Since the solder joint No. 52 is the innermost solder joint and consequently it is least affected by the edge effect, solder joint No. 52 on the flip-chip package U19 is taken as an example. Figure 17 shows a plot of the ROI mean intensity versus the ATC test cycles for No. 52 solder joint on U19 flip-chip. In order to show the significance of image preprocessing proposed in Section 3, three plots obtained with and without image preprocessing are displayed. The blue curve is the original data obtained from the ultrasonic images (with no image preprocessing), due to the unnormalized dynamic range and the intensity change caused by deviations in transducer and test sample during ATC test. The obtained mean intensity value has neither accuracy nor consistency. The orange curve is the data after intensity compensation proposed in Section 3, compared to the blue curve, the accuracy of the obtained intensity value improve significantly, however, lack of dynamic normalization makes the value of the data points in this curve can not be performed under the same scale. Then the gray curve is the data after intensity compensation and dynamic range normalization. Not only the data points in this curve accurately reflect the intensity of the solder joint image, but all collected under a consistent dynamic range. The trend of this curve matches perfectly with the "bathtub curve" that electronics failures should be compatible with. The mean intensity versus ATC test cycles describes the relationship between the cumulative increase in the mean intensity of the central area of the solder joint image and the failure probability of the solder joint.

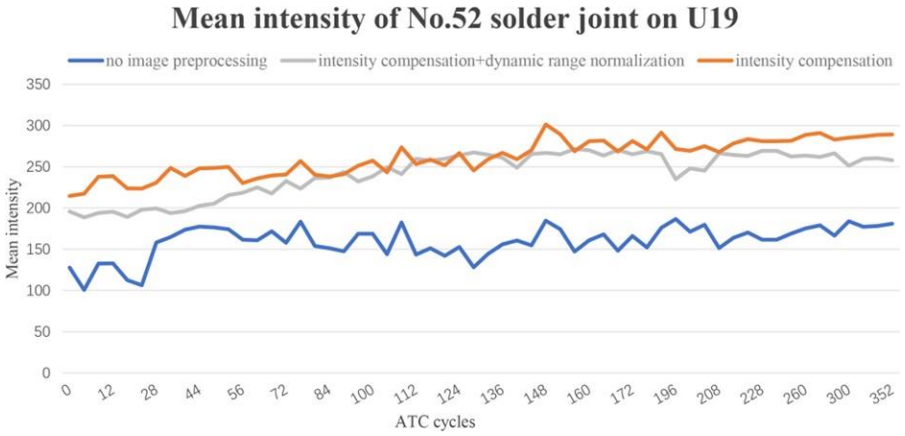

Figure 17: ROI mean intensity versus ATC test cycles.

The failure/life prediction model is then established by curve fitting as shown in Figure 18. As we know, Weibull distribution is widely used in reliability evaluation to represent the distribution of cumulative failures of mechanical products [23]. Therefore, the cumulative distribution function of the Weibull distribution is selected as the objective function for curve fitting. The probability density function and cumulative distribution function of the Weibull distribution are [24]:

$$f(t) = \frac{k}{\lambda}\left(\frac{t_i - \gamma}{\lambda}\right)^{k-1} \exp\left[-\left(\frac{t_i - \gamma}{\lambda}\right)^{k}\right] \tag{3}$$

$$F(t) = 1 - \exp\left[-\left(\frac{t_i - \gamma}{\lambda}\right)^{k}\right] \tag{4}$$

Where t is the time to failure, k is the shape parameter, λ is the scale parameter, γ is the position parameter.

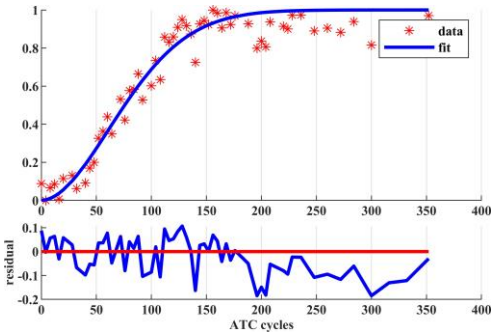

Figure 18: Establishment of the failure model by curve fitting.

For the No. 52 solder joint on the U19 flip-chip package, the parameter values obtained by curve fitting, with γ=0 are: k=1.86 and λ =92.13. Therefore, the failure and life prediction model established for solder joint No. 52 on the U19 flip-chip package is:

$$F(t) = 1 - \exp[-(\frac{t_i}{96.49})^{1.86}] \tag{5}$$

From Figure 18 it can be seen that after 50 cycles, the mean intensity of the solder joint increases steadily with the thermal cycles, and then stabilizes after 150 cycles. Due to the measurement error when the image was taken, the change in intensity fluctuates slightly.

After carrying out curve fitting for all the solder joints, it is confirmed that each solder joint can fit well with the cumulative failure function of the Weibull distribution with different shape parameter λ and scale parameter k. This means that each solder joint has its own aging rule. Taking U19 flip-chip as an example, the failure model of solder joints No.40, No.42, No.44 and No.46 are shown in figure 19.

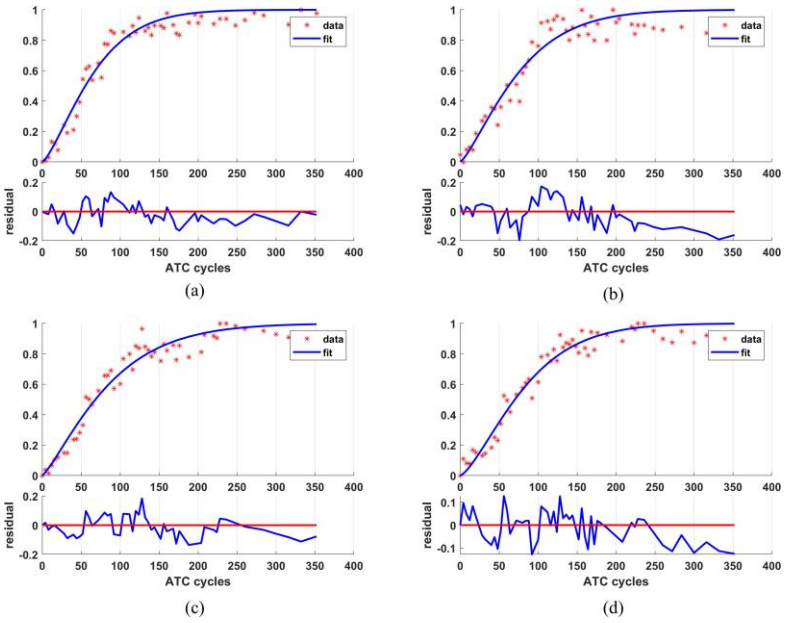

Figure 19: Failure model of solder joint (a)No.40, (b)No.42, (c)No.44, (d)No.46

The shape parameter k and scale parameter λ values obtained for solder joints No.40, No.42, No.44 and No.46 are shown in table 1. It can be seen that the value of the shape parameter k is always around 1.3, which proves that the failure curves follow the same Weibull distribution for all the solder joints.

Table 1: Scale parameter and shape parameter of solder joint No.40, No.42, No.44, and No.46

Solder joint	Scale parameter λ	Shape parameter k
No.40	74.2223	1.2490
No.42	80.3556	1.2653
No.44	82.2689	1.2987
No.46	89.8747	1.3599

5.2. Life prediction of solder joints

The failure model shown in Figure 18 is used for life prediction of solder joints. The cycles to failure for individual solder joints are obtained as follows:

1. The quadratic reciprocal G(t) of the curve in Figure 18 is calculated.
2. G(t) is set G(t)=0 to get two inflection points of the curve, with the second inflection point defined as the failure point of the solder joint. The test cycle corresponding to this point is the failure cycle.

Figure 20 shows a 3D representation of the cycles to failure obtained for the 48 solder joints in the inner row of the flip-chip U19. It is noticeable that the failure pattern forms a normal distribution which means the middle joints have significantly higher reliability compared to the corner joints.

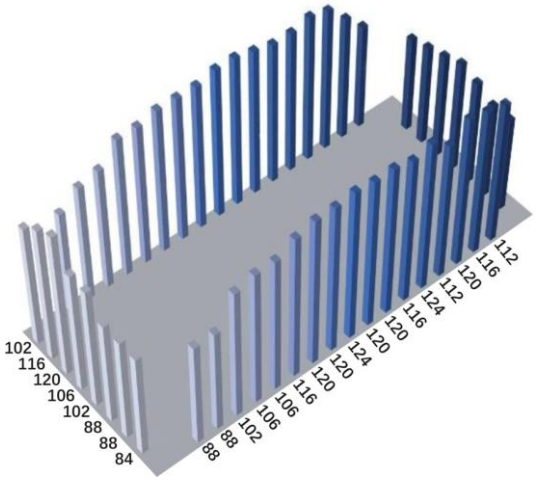

Figure 20: Reliability of individual solder joints.

6. Conclusion

This paper proposes an approach to establish the failure model of solder joints using ultrasonic NDE to monitor the through-life health status of individual solder joints. Flip-chip packages were mounted on PCBs as the test samples using solder joints. The aging process of the samples was achieved by subjecting them to ATC tests until all the silicon chips were fallen off. The degradation of the solder joints was monitored by taking out the samples from the temperature chamber and inspecting them using SAM at an interval of 4 ATC cycles. Ultrasonic images of all the solder joints were obtained from the ultrasonic NDE data. Dynamic range-based intensity normalization, gain compensation, and calibration for random transducer defocusing error were carried out to preprocess the ultrasonic images, enhancing the data quality. A local minimum edge detection algorithm was developed to segment the ROIs of solder joints. A failure model was finally established by exploiting the correlation between the mean intensity of ROIs and the ATC cycles using the cumulative distribution function of the Weibull distribution as the objective function. The failure model with ultrasonic image intensity as the characteristic quantity was further employed to estimate the reliability of individual solder joints.

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