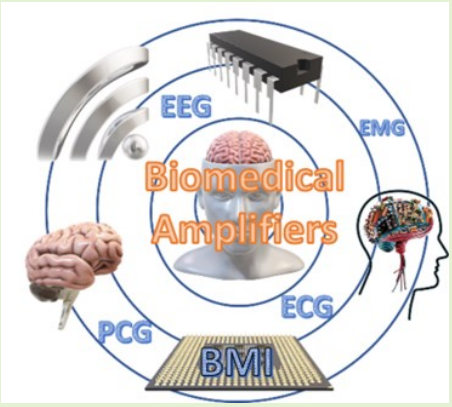
Biomedical Amplifiers Design Based on Pseudo-resistors: A Review

Israa AbuShawish, *Member*, Soliman Mahmoud, *IEEE Senior Member,* Sohaib Majzoub, *IEEE Senior Member,* and Abir Hussain *IEEE Senior Member*

***Abstract*—The demand for efficient, robust, and cost-effective Brain-Machine Interface (BMI) systems continues to increase in the last decade. One of the fundamental design blocks in such systems is the signal amplification and filtering. Generally, biomedical signals are characterized by low amplitude and low frequency in a noisy environment. Therefore they need to be amplified and filtered before passing the signal to the next processing stage. In this review paper, a comprehensive survey is conducted in existing literature of two-stage biomedical amplifiers, focusing on the impact of the pseudo-resistor non-linearity on the system's performance. First, the common categories of pseudo-resistors are presented and discussed. Then, different amplifier designs, targeted for biomedical applications, are identified and studied considering the influence of the pseudo-resistors on the performance. A special focus was given to the impact of the Process, Voltage, and Temperature variations where experiments are conducted to test the performance under different variation tests. Different two-stage biomedical amplifiers, used in bio-detection systems, with programmable gain and bandwidth features based on pseudo-resistors are implemented. The designs are realized and simulated using LTspice utilizing 90nm process technology, BSIM4, version 4.3, level 54.**



***Index Terms*— Biomedical amplifier; programmable gain; Brain-Machine Interfaces (BMIs).**

I. Introduction

Brain Machine Interface (BMI) systems are promising devices that can be used to sense, detect, and read neuron signals for monitoring, controlling, and treatment. BMIs are utilized to help patients experiencing disabilities and disorders, by spotting and diagnosing biomedical signals. These devices revealed an enormous potential for brain study and the growth of valuable solutions in many clinical applications. Some research was dedicated to aiding patients with amputated limbs as in [1], [2] through commanding robotic limbs. Other studies are devoted to controlling and monitoring human neuroprosthetics which are the bio-potential signals of the human brain. A typical BMI monitoring system requires a utilization of up to 300 electrodes to capture the brain's signals [3]. It is mandatory in many biomedical applications that these electrodes are connected and collecting neurons' signals contentiously during the diagnosis process. Consequently, patients were forced into this uncomfortable medical procedure on a daily basis.

Neural recording implants are devices made to capture, amplify, and digitize the biomedical signals, and finally transfer them outside the human body. Such implants should operate on minimum power and area. Bio-potential signals can be captured through non-invasive or invasive methods. The captured signals are expected to have very small amplitude and bandwidth (BW). Thus, specially designed amplifiers in the Analog Front End (AFE) amplify the signal and filter the noise, and then pass it to the ADCs to digitize it. Mostly, the digitized signals are compressed using the data compressors.

The vital block of the neural recording in the BMI system is the analog front-end (AFE) amplifiers. The important design parameters of a biomedical amplifier are low power consumption, low distortion, low noise, appropriate gain, and high Bandwidth (BW). One of the crucial elements in biomedical amplifiers is the pseudo-resistors. Designing a constant Tera Ohm (T Ω) pseudo-resistor over a wide range continues to be an interesting research area [4]. Pseudo-resistors are needed to achieve very low pole frequency since the weak amplitude and frequency of the neurons' signals. The frequency range of the captured bio-signals is 0.1 Hz - 10kHz, and the amplitude 20μV to 10mV. However, due to the DC offset, a low-frequency filter has to be designed to eliminate the DC as well.

Biomedical signal amplifiers are classified into two categories, based on the technique used to eliminate the DC offset. These two design types are DC-coupled and AC-coupled neural Amplifiers. The DC-Coupled Neural Amplifier employs

This work was supported in part by University of Sharjah, Department of Electrical Engineering. . (Corresponding author: Soliman Mahmoud.)

Israa AbuShawish, Department of Electrical Engineering, University of Sharjah, Sharjah, UAE (e-mail: iabushawish@sharjah.ac.ae).

Soliman Mahmoud, Department of Electrical Engineering, University of Sharjah, Sharjah, UAE (e-mail: solimanm@sharjah.ac.ae).

Sohaib Majzoub, Department of Electrical Engineering, University of Sharjah, Sharjah, UAE (e-mail: smajzoub@sharjah.ac.ae).

Abir Hussain, Department of Electrical Engineering, University of Sharjah, Sharjah, UAE (e-mail: abir.Hussain@sharjah.ac.ae).

the low pass filter (LPF) in the feedforward and the feedback (FB) path to eliminate the DC-offset voltages and to form a high pass (HP) pole transfer function. There are six different topologies of the DC-Coupled Neural Amplifiers presented in the literature [4]. Yet, this form of amplifier is not suitable for applications that require large-scale recording such as biomedical applications. Such designs are characterized by inaccurate gain due to the variation of the amplifier's mid-band gain value since it is sensitive to process variation. This sensitivity causes inaccurate and low-cutoff frequency. Furthermore, if the implementation is based on the passive analog integrator, a huge capacitor is required in the feedback network. On the other hand, higher power is consumed if the implementation is based on the active analog integrator.

The AC coupled neural amplifiers eliminate the DC offset voltages by employing AC coupling capacitors at the inputs. These capacitors are large to attain high amplification gain, which consumes a larger chip area and reduces the input impedance. There are six main topologies of the AC-Coupled Neural Amplifiers: Conventional capacitive FB network amplifier, capacitive FB network amplifier using T-capacitor FB network, AC coupling amplifier using electrode capacitance and resistive FB, capacitive amplifier FB network, open-loop network amplifier, and miller compensated capacitive FB network amplifier [5].

This work reviews different designs of the two cascaded stages biomedical amplifiers demonstrated in [5] based on conventional and highly linear pseudo-resistors presented in [6]–[8]. Furthermore, the paper demonstrates the design based on conventional op-amp and rail-to-rail programmable unity-gain bandwidth (UGBW) op-amp designed in [9]. The paper also showcases a comparison between different designs in the literature for the same application. PVT variation tests were performed on different designs of the two stages biomedical amplifier to examine the amplifier's robustness under process, voltage, and temperature variations. All the designs were analyzed, investigated, and tested through the LT-Spice simulation tool using 90 nm CMOS technology.

This paper comprises four sections. **Section II** studies the design of the constant, programable, and high TΩ CMOS pseudo-resistor presented in [6]–[8], compared with the conventional one. This section offers theoretical derivations, simulation results, and application in the two-stages op-amp-based amplifier. A performance comparison between the employment of the conventional and the highly linear pseudo-resistor [6]–[8] is provided in the section. **Section III** is dedicated to presenting the controllable UGBW op-amp-based biomedical amplifier with programmable Gain and BW illustrated in [9]. This section discusses the design and the simulation of a single-ended and fully balanced op-amp and its application in the first and second stages of biomedical amplifiers respectively. The section depicts the amplifier which comprises two cascaded stages, each utilizing the TΩ pseudo-resistors designed in [6]–[8] that are employed in the amplifier's FB. Finally, **Section IV** presents the concluding remarks of this work.

II. Pseudo-Resistors and Op-Amp Based Biomedical Amplifiers Design

The pseudo-resistors are vital devices in many biomedical amplifiers. The frequency range of the biomedical signals is between 0.1 Hz to 10 kHz, while the amplitude range is around $20\mu V$ – 10 mV [1]. Due to the DC offset voltage which ranges from 1 mV to 50 mV, a low-frequency filter has to be designed to eliminate this offset. The low-frequency pole is established by high FB resistance and low capacitance. Therefore, the necessity for the pseudo-resistors is needed to emulate the high resistance, meanwhile preserving low power usage and cheap design costs. The resistance in some works as in [10] reached several k Ω, while in others as in [11] the resistance reached few G Ω. In [12]–[14] the resistance emulated approach few T Ω. Furthermore, increasing the capacitance while keeping the resistance constant will result in a low cutoff frequency and a very low frequency pole as in [15], [16]. It's important to consider the trade-offs and design the filter appropriately to meet the required specifications.

These resistors are favored to be used over the conventional ones in several significant circuits such as the multipliers, operational transconductance amplifiers, trans-impedance amplifiers, and data converters, as a fundamental part of the low current sensing applications, bio-applications, temperature sensing applications, etc. [17]. The design of two types of CMOS pseudo-resistor is analyzed, discussed, and simulated in-depth in this section where the first type is (A two-NMOS transistor pseudo-resistor) designed in [17] as a FB resistor, while the second type is the NMOS and PMOS transistors pseudo-resistor with source follower designed in [6]–[8].

A. Conventional CMOS Pseudo-Resistor

The two-NMOS pseudo-resistors construction is built on the symmetrical biasing of the base voltage (V_B) and gate voltage (V_G) of two series NMOS transistors functioning in the weak inversion region [17]. This structure emulates a high resistance value, reaching tens of TΩ. The circuit structure of the pseudo resistor is shown in Fig. 1.

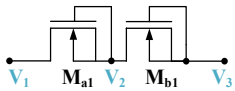


Fig. 1. The structure of the conventional two-NMOS transistor pseudo-resistor

The drain to source current expression of NMOS transistor in the weak inversion region [13] is given by:

$$I_{DS} = I_{D1}\left(e^{-\frac{V_{SB}}{U_T}} - e^{-\frac{V_{DB}}{U_T}}\right)e^{\frac{V_{GB}-V_{To}}{n\,U_T}} \quad (1)$$

$$I_{D1} = 2n\,\mu_n C_{ox} U_T^2 \frac{W}{L} \quad (2)$$

Where $U_T, n, \mu_n, V_{To}, C_{ox}$, W and L are identifying the thermal voltage (mostly 26 mV), subthreshold slope factor (typically 1.5), mobility of electrons, MOS threshold voltage, gate oxide capacitance/unit, channel width, and length, respectively. The biasing conditions of the pseudo resistor are; $V_{GBa} = V_{GBb} = 0$, $V_{Ba} = V_{Da} = V_{Ga}$, $V_{Bb} = V_{Db} = V_{Gb}$ and by $V_{SDb} = V_{SDa}$. Accordingly, the current passing through the two NMOS transistors from (port V_3) to (port V_1) is given by:

$$I_{3,1} = I_{D1}\left(e^{\frac{V_{3,1}}{2U_T}} - 1\right)e^{\frac{-V_{To}}{n\,U_T}} \quad (3)$$

The equivalent resistance of the two NMOS transistors under the assumption of $V_3 > V_1$ and $-0.6\,V \leq V_{3,1} \leq 0.6\,V$ is given by:

$$R_{3,1} = \frac{2U_T}{I_{3,1}}\left(1 - e^{-\frac{V_{3,1}}{2U_T}}\right) = \frac{2U_T}{I_{D1}}\,e^{\frac{V_{To} - 0.5\,nV_{3,1}}{n\,U_T}} \quad (4)$$

Which is the resistance of one transistor M_{a1} or M_{b1} times two, as both transistors were linked in series, and both were identical. Since both transistors, M_{a1} and M_{b1} were matched and meanwhile, both were connected in series, thus $V_{2,1} = V_{3,2} = V_{3,1}/2$. It's worth noting that if we assumed $V_3 < V_1$, the resistance expression of this pseudo-resistor will be the same as given in (4).

This exponential pseudo-resistor was theoretically analyzed and then simulated using MATLAB and then simulated through LT-spice to validate the obtained results. The testing was done under the same condition, where port V_1 is connected to the common mode node, 0 V, while port V_3 swept from -0.9 V to 0.9 V to test the bidirectional behavior of the pseudo-resistor. The pseudo resistor emulated a resistance value in the range of several tens of Tera ohm when $V_1 > V_3$, while the resistance value was reduced as negative values of $V_{3,1}$ reduced (approaching 0 V) [18].

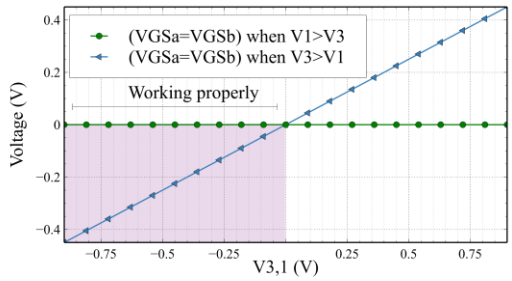


Fig. 2. The V_{GSa1} plot vs. $V_{3,1}$ under two conditions: when $V_1 > V_3$ and $V_3 > V_1$

In contrast, when V_3 is greater than V_1 the resistance value was almost constant in the range of tens of Giga ohm. Under the condition of $V_3 < V_1$, both V_{GSa1} and V_{GSb1} are equal to 0 V. Given the circuit structure and the gate to source voltage relationship shown in Fig. 2, both V_{GSa1} and V_{GSb1} are equal to 0 V and less than V_{To}. This ensures working in the subthreshold region. As the gate to source voltage for both M_{a1} and M_{b1} were shorted (i.e., equal to 0V), a proper and constant value is maintained. Therefore, a large resistance value over the negative range of the output voltage swing is maintained. When V_3 is greater than V_1, then V_{GSa1} and V_{GSb1} does not have a fixed value. However, up to a limited range on the positive side of $V_{3,1}$, the gate to source voltage is located below V_{To} by a small value, which forces M_{a1} and M_{b1} to operate at the edge of the subthreshold region. Consequently, a lower resistance in the order of 10s of GΩ was realized. It's worth noting that the resistance value obtained from the simulation in [18] was very close to those computed theoretically using the formula presented in (4). The simulation in [18] displayed a precise matching between the MATLAB and LT-spice simulations with an aspect ratio of $1\ \mu m/5\ \mu m$.

B. Highly Linear Pseudo-resistor with Source follower

The conventional two NMOS pseudo-resistors exhibited distortion when it is employed in a circuit with large output voltage swings [17]. Since the second stage has a large output swing, it is required to use a different type of pseudo-resistor to address this issue. This new type is represented by the NMOS and PMOS pseudo-resistor with a source follower. This type of highly linear pseudo-resistor was designed in [6]–[8] with two source followers (level shifters), which can handle the V_{GS} adjustment of the complementary CMOS structure of NMOS and PMOS transistors. This adjustment maintained a constant V_{GS} over a wide output voltage swing. In the meantime, by adjusting the biasing current (I_{Bias}) in the source followers, the resistance value is controlled. If the resistance is required to be high in the application, I_{Bias} could be reduced, and thus reducing $|V_{GS}|$.

The required biasing currents are in the range of the nano-Ampere. Such current sources are implemented using the techniques given in [19]. The current range is reduced in [20] to the sub-pico-Ampere. Utilizing both NMOS and PMOS transistors was suitable in implementing a large resistance over the full output swing, by guaranteeing at least one MOS transistor with proper source to gate voltage. The following sub-section is thoroughly discussing the circuit design of this type, representing each NMOS and PMOS transistor separately and the advantage of combining both in one cell.

1) NMOS TRANSISTOR WITH SOURCE FOLLOWER

The structure of the NMOS transistor with source follower pseudo-resistor is shown in Fig. 3 (in purple color). It is tested under the same conditions as the conventional type, where port V_1 connected to the common mode node = 0 V, while port V_2 swept from -0.9 V to 0.9V. The simulation of this cell was conducted given the size of the transistor M_{a2} to be W= 0.26 μm, and L= 65 μm, and M_{c2} to be W=200 μm, and L=1.5 μm. The current passing through M_{a2} and M_{c2} is formulated using (5) and (6) respectively:

$$I_{2,1} = I_{D1a}\left(1 - e^{-\frac{V_{2,1}}{U_T}}\right)e^{\frac{V_{4,1} - V_{To}}{n\,U_T}} \quad (5)$$

$$I_{SDc2} = I_{Doc}\left(1 - e^{-\frac{V_{SDc2}}{U_T}}\right)e^{\frac{V_{4,1} - V_{To}}{n\,U_T}} = I_{bias} \quad (6)$$

The equivalent resistance given by:

$$R_{2,1} = \frac{U_T}{I_{bias}}.\frac{I_{Doc}}{I_{D1a}}\left(\frac{1 - e^{\frac{-V_{SDc2}}{U_T}}}{e^{\frac{-V_{2,1}}{U_T}}}\right) \quad (7)$$

The voltage $V_{2,1}$ represented by V_{DSa2} and $V_{4,1}$ depicted in V_{GSa2}, under the condition of $V_2 > V_1$. It is deduced from the circuit architecture and the plot of V_{GSa2} behavior shown in Fig. 4, that $V_{4,1} = V_{GSa2} = V_{SGc2} < V_{To}$ which preserved an appropriate and constant V_{GS} for M_{a2}, ensuring that M_{a2} functioned in the weak inversion region. Accordingly, a large, constant, and linear resistance value was realized over the positive range of the output voltage swing. In contrast, V_{GSa2} did not maintain a fixed value when $V_1 > V_2$; (since $V_{GSa2} \neq V_{SGc2}$). Given the limited range on the negative side of $V_{2,1}$, V_{GSa2} is located below V_{To} by a very small value, which made the transistor M_{a2} operate at the edge of the weak inversion region, and accordingly, the

lower resistance reaches 1.5 GΩ, as shown by the V_{GSa2} curve in Fig. 4

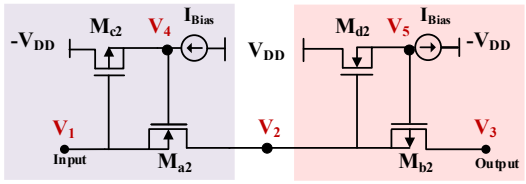


Fig. 3. The structure of the highly linear pseudo-resistor [6]

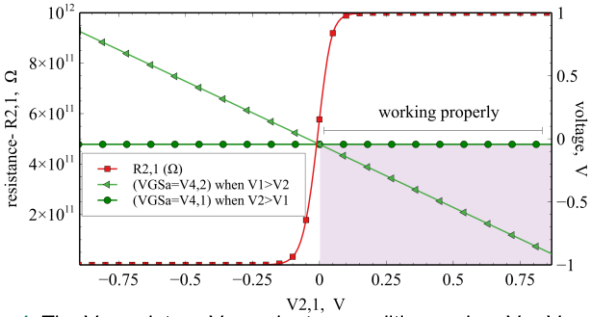


Fig. 4. The V_{GSa2} plot vs. $V_{2,1}$ under two conditions: when $V_2 > V_1$ and $V_1 > V_2$ along with the simulated resistance of the pseudo resistor using the transistor NMOS- M_{a2} with source follower

2) *PMOS Transistor with Source Follower*

The structure of this type of pseudo-resistor, shown in Fig. 3 (in pink color) is tested under the same conditions as the NMOS transistor pseudo-resistor. Port V_2 is linked to the common mode node, i.e. 0 V, and swept from -0.9 V to 0.9 V. The size of this cell is matched with the previous cell, where the aspect ratios of the transistors M_{b2} and M_{d2} are 0.26 μm / 65 μm and 200 μm / 1.5 μm, respectively. The source to drain current expression for the PMOS is given by:

$$I_{SD} = I_{Do}\left(e^{-\frac{V_{BS}}{U_T}} - e^{-\frac{V_{BD}}{U_T}}\right)e^{\frac{V_{BG}-V_{To}}{n\,U_T}} \quad (8)$$

$$I_{Do} = 2n\,\mu_p C_{ox} U_T^2 \frac{W}{L} \quad (9)$$

The currents passing through transistors M_{b2} and M_{d2} expressed by (10) and (11) respectively.

$$I_{3,2} = I_{Dob}\left(e^{\frac{V_{3,2}}{U_T}} - 1\right)e^{\frac{V_{2,5}-V_{To}}{n\,U_T}} \quad (10)$$

$$I_{DSd2} = I_{D1d}\left(1 - e^{-\frac{V_{DSd2}}{U_T}}\right)e^{\frac{V_{2,5}-V_{To}}{n\,U_T}} = I_{bias} \quad (11)$$

Its equivalent resistance given by:

$$R_{3,2} = \frac{U_T}{I_{bias}} \cdot \frac{I_{D1d}}{I_{Dob}}\left(\frac{1 - e^{\frac{-V_{DSd2}}{U_T}}}{e^{\frac{V_{3,2}}{U_T}}}\right) \quad (12)$$

$V_{3,2}$ represented V_{SDb2} and $V_{2,5}$ represented V_{DGb2}, under the condition of $V_3 > V_2$. The V_{SGb2} of PMOS does not have a fixed value. V_{GSb2} goes up to a partial range on the positive side of $V_{3,2}$, positioned underneath V_{To} by a small value, this puts M_{b2} at the edge of the subthreshold region. Consequently, a smaller resistance value is realized compared to the previous case (around 1.5 GΩ).

This scenario is demonstrated by the V_{SGb2} plot shown in Fig. 5. In contrast, $V_{3,2}$ denoted V_{DSb2} and $V_{2,5}$ defined V_{SGb2} when $V_2 > V_3$. Therefore, the circuit configuration and the plot of V_{SGb2} shown in Fig. 5 shows that $V_{2,5} = V_{SGb2} = V_{GSd2} < V_{To}$. Thus, a constant gate-to-source voltage for M_{b2} is reserved, and M_{b2} is guaranteed to operate in the subthreshold region. Accordingly, a large, constant, and linear resistance value is emulated over the negative range of the output voltage swing. The $R_{3,2}$ versus $V_{3,2}$ characteristic plot of this pseudo-resistor is presented in Fig. 5. It is clear from Fig. 5 that the curve of $R_{3,2}$ is exactly a mirrored version of the $R_{2,1}$ curve presented in Fig. 4.

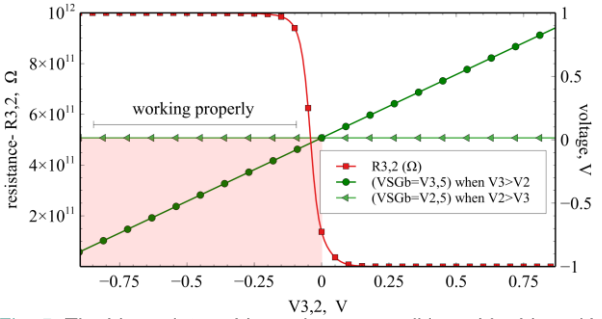


Fig. 5. The V_{SGb2} plot vs. $V_{3,2}$ under two conditions: $V_3 > V_2$ and $V_2 > V_3$ along with the simulated resistance of the pseudo resistor using the transistor PMOS- M_{b2} with source follower.

3) *NMOS and PMOS Transistors with Source Followers*

By combining the two cells of NMOS and PMOS mentioned in the previous sub-sections in a series connection, as declared in Fig. 3, the stated disadvantages of using only one cell can be overcome and thus guarantee that the cells emulate a large, constant, and linear resistance value over the entire range of the output voltage swing as presented in [6]–[8]. This fact is proven through the theoretical analysis, where the expression of $R_{3,1}$ derived under both conditions of $V_3 < V_1$ and $V_1 > V_3$ is expressed by the same equation, given by:

$$R_{3,1} = \frac{U_T}{I_{bias}}\left[\frac{I_{Dpc}}{I_{Dna}}\left(\frac{1-e^{\frac{-V_{SDc}}{U_T}}}{e^{\frac{-V_{2,1}}{U_T}}}\right) + \frac{I_{Dnd}}{I_{Dpb}}\left(\frac{1-e^{\frac{-V_{DSd}}{U_T}}}{e^{\frac{V_{3,2}}{U_T}}}\right)\right] \quad (13)$$

The power consumed by this pseudo resistor is 2.4 nWatt. The realized resistance value is around 1.08 TΩ over the $\pm 0.6V$ dynamic range excluding near zero volts. A 6.48% drop in the resistance value, i.e., down to 1.01 TΩ, is observed near $V_{3,1}$= 0V: as a result of the gap between the realized resistance by the NMOS pseudo-resistor and the PMOS pseudo-resistor. There is an exact matching between the $R_{3,1}$ curve plotted using LT-Spice and MATLAB as demonstrated in [6]. This ensures that the developed resistance expressions are trusted and very close to the simulations.

There are similar structures in the literature but with different connections. In [17] the authors presented two types of pseudo-resistors, one with fixed resistance and the second with a programmable one. The second type presented is similar to the one proposed in [6]–[8], but with different connections. From the structure point of view, the connection between the PMOS part with its source follower is flipped, unlike the connection in [6]–[8]. From the theoretical perspective, the expression over the two conditions are identical in [6]–[8] but not in [17].

C. Design Of Overall Two Stages Op-Amp Based Biomedical Amplifier

The biomedical amplifier demonstrated in Fig. 6 is designed using two amplifier stages to accomplish the filtering and the amplification process of the neuron signals. The restrictions of employing the typical single amplifier's stage in biomedical

applications are that if the application requires a high amplifier's gain, designers are forced to increase the input capacitance value [21]. Accordingly, the chip area will increase, and the input impedance will decrease, or we will need to have an off-chip capacitor. The multi-stage amplifier is one of the solutions to overcome these issues [5]. The transfer function (TF) of the first amplifier's stage is given by:

$$\frac{V_{o2}-V_{o1}}{V_{in1}-V_{in2}}=\frac{SC_1R_1}{SC_2R_1+1} \quad (14)$$

Where C_1, C_2, and R_1, are the input capacitance, FB capacitance, and FB resistance of the 1st amplifier's stage. The TF of the second amplifier's stage is given by:

$$\frac{V_{out}}{V_{o1}-V_{o2}}=\frac{SC_3R_2}{SC_4R_2+1} \quad (15)$$

Where C_3, C_4, and R_2, are the input capacitance, FB capacitance, and FB resistance of the 2nd amplifier's stage. The TF of the overall two stages amplifier is given by:

$$\frac{V_{out}}{V_{in1}-V_{in2}}=-\frac{S^2\left(\frac{C_1C_3}{C_2C_4}\right)}{S^2+S\left(\frac{1}{C_4R_2}+\frac{1}{C_2R_1}\right)+\frac{1}{C_2C_4R_1R_2}} \quad (16)$$

The gain requirements of the biomedical amplifier are 54.7dB gain achieved through 31.8dB gain in the first stage and 22.9dB in the second stage. The gain ratios in the first and second stages are C_1/C_2 and C_3/C_4 respectively. The FB capacitance C_2 and C_4 are selected in the range of 0.1 pF to 0.3 pF to be larger than the neighborhood parasitic capacitances, while the input capacitance C_1 and C_3 should be bigger than the FB capacitance by multiple times to achieve a higher gain [17]. The active block of the first amplifier's stage is designed using the fully differential folded cascode op-amp with a gain of 76.4 dB and 86.6° phase margin. As for the second stage, the active block utilized is the single-ended two-stage operational amplifier with a gain of 110.9 dB and 138.84° phase margin. It's worth noting that, forming an amplifier with a gain based on a capacitor ratio is an advantage since the process, voltage, and temperature (PVT) variations won't cause any effect on the capacitance value and thus leading to a robust amplifier's gain. Using a pseudo-resistor to control the lower cutoff frequency might cause problems under the PVT variations. This can be compensated using biasing currents provided in the highly linear pseudo-resistor. Consequently, a robust design has been preserved, in terms of the amplifier's gain and BW.

The design of the biomedical amplifier is discussed, analyzed, and simulated in-depth in the following discussions. The conventional pseudo-resistor is employed as a FB resistor in both stages of the biomedical amplifier and then it is replaced by the pseudo-resistor presented in [6]–[8] in the second stage. Finally, the pseudo-resistor in [6]–[8] has been utilized in both stages of the amplifier. The design parameters and components value of the biomedical amplifier are presented in Table I.

1) Employing the conventional Pseudo-resistor in both stages

The structure of this biomedical amplifier is presented in Fig. 7 (a), where the conventional pseudo-resistor (two-NMOS pseudo-resistor) is employed as a FB resistor in the first and second stages of the biomedical amplifier. An equal R design has been used in testing the overall biomedical amplifier. For the sinusoidal steady-state response test presented in Fig. 8 (a), a sinusoidal 1mV peak-to-peak signal with 100 Hz frequency has been applied at the input. The output voltage depicted in Fig. 8 (b) represents an amplified and inverted sine wave signal with an amplitude of 0.56 V peak-to-peak, which is the 54.9dB gain. The total harmonic distortion (THD) in Fig. 9 is measured with 1 mV input amplitude for input frequencies (50 Hz, 100 Hz, 250 Hz, 450 Hz, 600 Hz, and 650 Hz. The THD is decreased as the frequency increases, till reaching the frequency 250 Hz where the distortion reported is approximately 0.198% (-54.07dB). Above 250Hz frequency, the THD decreases as observed at frequencies 600 Hz and 650 Hz, where the corresponding THD are 0.165% (-55.65 dB) and 0.163% (-55.75 dB) respectively.

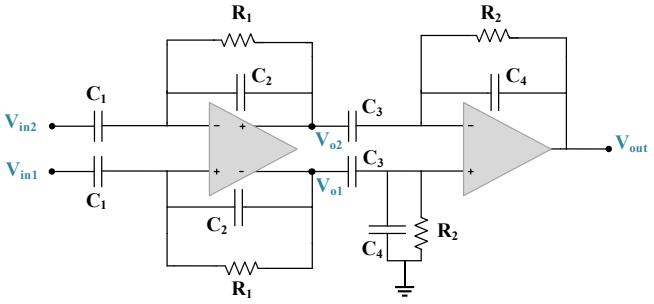
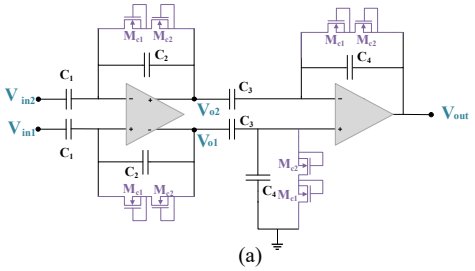
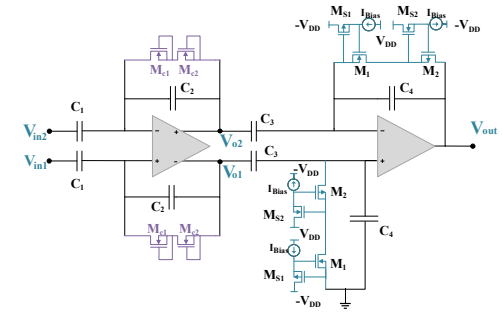


Fig. 6. The structure of the op-amp-based biomedical amplifier

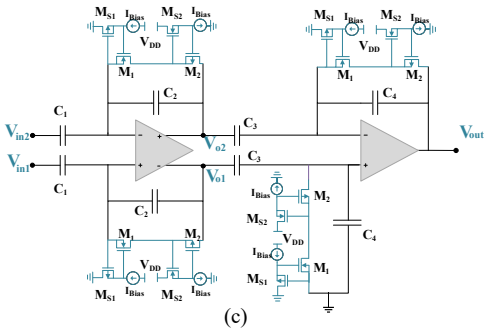
TABLE I
THE DESIGN AND COMPONENTS VALUE OF THE OP-AMP BASED BIOMEDICAL AMPLIFIER

Stage	Description	Value
First stage	**Components**	
	C_1	11.7 pF
	C_2	0.3 pF
	R_1	5.3 $T\,\Omega$
	Design parameters	
	Gain	31.8 dB
	Cutoff frequency ω_o	$1/C_2R_1 = 0.629\ rad/sec$
Second stage	**Components**	
	C_3	1.4 pF
	C_4	0.1 pF
	R_2	15.93 $T\,\Omega$
	Design parameters	
	Gain	22.9 dB
	Cutoff frequency ω_o	$1/C_4R_2 = 0.628\ rad/sec$
Overall biomedical amplifier	**Design parameters**	
	Gain	54.7 dB
	High pass pole at	0.1 Hz
	Cutoff frequency ω_o	$1/\sqrt{C_2C_4R_1R_2} = 0.629\ rad/sec$



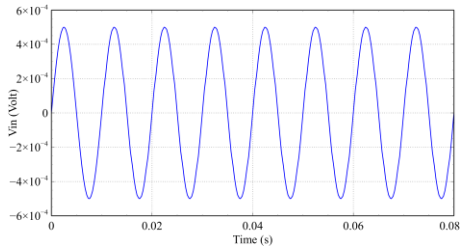


(b)

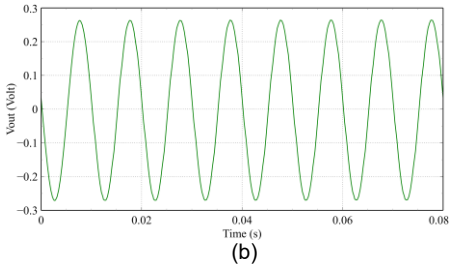


(c)

Fig. 7. The structure of the op-amp-based biomedical amplifier using the pseudo-resistor as FB resistors: (a) the conventional pseudo-resistor in both stages, (b) conventional pseudo-resistor in the 1st stage, and the new pseudo-resistor in the 2nd stage, (c) new pseudo-resistor in both stages



(a)



(b)

Fig. 8. The signal waveform simulation of the op-amp based biomedical amplifier using the conventional pseudo-resistor in both stages: (a) Input sinusoidal signal 1mV $_{pk-pk}$ amplitude with 100 Hz frequency (b) Output sinusoidal signal 0.56 V $_{pk-pk}$ amplitude.

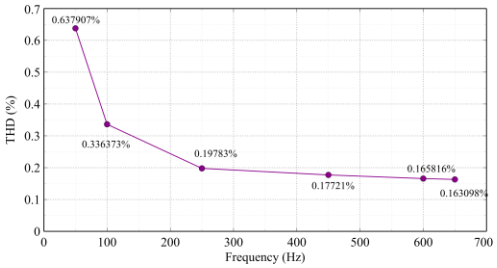


Fig. 9. The THD of the biomedical amplifier using the conventional pseudo-resistor in both stages.

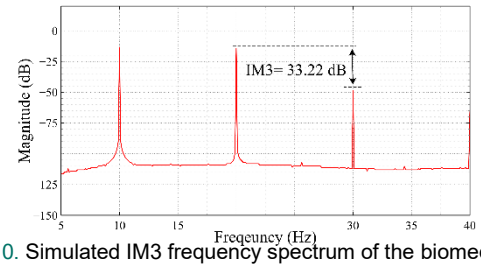


Fig. 10. Simulated IM3 frequency spectrum of the biomedical amplifier using the conventional pseudo-resistor in both stages at the amplitude of 1mV $_{pk-pk}$ via 10 Hz, and 20 Hz single tones frequencies.

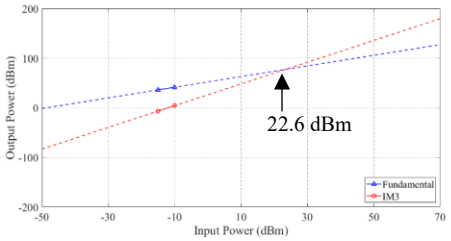


Fig. 11. The IIP3 of the biomedical amplifier using the conventional pseudo-resistor in both stages.

Fig. 10 represents the IM3 test to evaluate the linearity performance of the biomedical amplifier with two single tones at 10 Hz and 20Hz frequencies, where each signal has an amplitude of 1m V_{pk-pk}. The test demonstrates a value of 33.22 dB. The simulation conducted to find (IIP3) of the amplifier is offered in Fig. 11 and presented a value of 22.6 dBm.

2) *Employing the conventional Pseudo-resistor in the 1st Stage, and the one in [6]–[8] in the 2nd Stage*

In this sub-section, the conventional pseudo-resistor is employed as a FB resistor in the first stage of the amplifier; while the pseudo-resistor in [6]–[8] is used as a FB element in the second stage of the amplifier as presented in Fig. 7 (b). The advantage of this amplifier over the previous one is that the use of the pseudo-resistor in [6]–[8], will facilitate the tunability of the amplifier's lower cutoff frequency. The lower corner frequency is reduced by lowering the I_{Bias} in the source follower of the pseudo-resistor and vice versa. The magnitude response of the amplifier is simulated using the biasing currents; 1 nA, 1.5 nA, and 2 nA as provided in Fig. 12, where the corresponding lower cutoff frequencies are 1.8Hz, 2.3Hz, and 2.8Hz, respectively. The IRN spectral density of the biomedical amplifier under this case is (312.8 nV/$\sqrt{Hz}$) at the frequencies above 10 Hz, while the value is increasing at frequencies below 10 Hz till reaching (41.66 μV/$\sqrt{Hz}$) at 0.1 Hz.

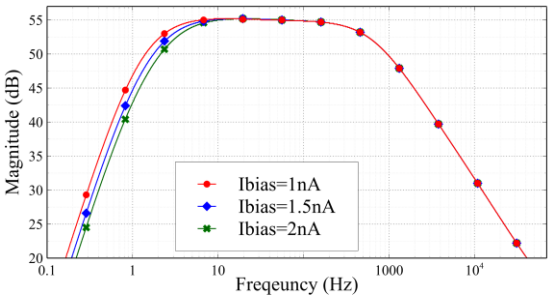


Fig. 12. The response of the overall op-amp-based biomedical amplifier using the conventional and the highly linear pseudo-resistor [6] over three different biasing current values; 1nA, 1.5nA and 2nA

For the sinusoidal steady-state response test, a sinusoidal 1mV$_{pk-pk}$ signal with 100 Hz frequency has been applied as an input presented in Fig. 13 (a). The output voltage depicted in Fig. 13 (b) represents an inverted sine wave signal and is amplified with an amplitude of 0.56 V$_{pk-pk}$, which is precisely the 54.9 dB multiple of 1mV input signal.

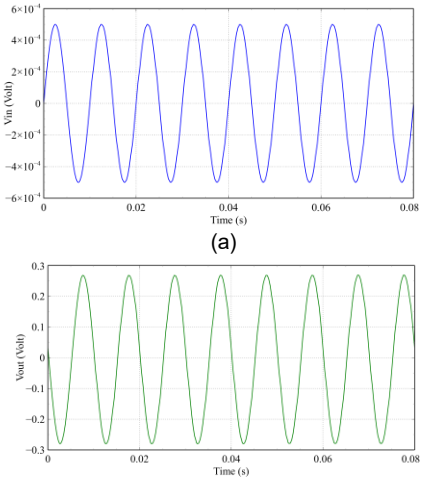


Fig. 13. The steady-state time response of the op-amp-based biomedical amplifier using the conventional and the highly linear pseudo-resistor [6]–[8]: (a) Input sinusoidal signal 1mV $_{pk-pk}$ amplitude with 100 Hz frequency (b) Output sinusoidal signal 0.56 V$_{pk-pk}$ amplitude

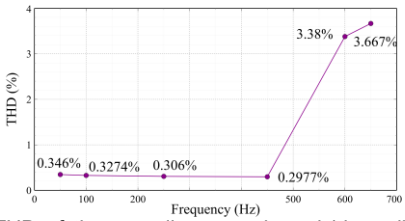


Fig. 14. The THD of the overall op-amp-based biomedical amplifier using the conventional and the highly linear pseudo-resistor [6]–[8]

The THD test was conducted with an input amplitude of 1 mV for different input frequencies of (50 Hz, 100 Hz, 250 Hz, 450 Hz, 600 Hz, and 650 Hz) as shown in Fig. 14. The frequency of 100 Hz is located at the flat band of the biomedical magnitude response, where the distortion reported is approximately 0.3274% (-49.7 dB). Above 450 Hz frequency, the THD increases as observed at frequencies 600 Hz and 650 Hz, where the corresponding THD are 3.38% (-29.42 dB) and 3.667% (-28.71 dB), respectively. Fig. 15 represents the IM3 test to evaluate the linearity performance of the amplifier with two single tones at 50Hz and 60Hz frequencies, each of 1 mV$_{pk-pk}$ amplitude, where the test demonstrates a value of 46.49 dB. The simulation conducted to find IIP3 of the amplifier which is 22.94 dBm is represented in Fig. 16.

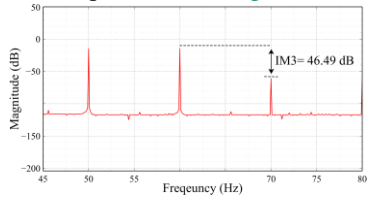


Fig. 15. The IM3 frequency spectrum of the amplifier using the conventional and the pseudo-resistor in [6]–[8] at the amplitude of 1mV $_{pk-pk}$ via two single tones of 50Hz and 60Hz frequencies

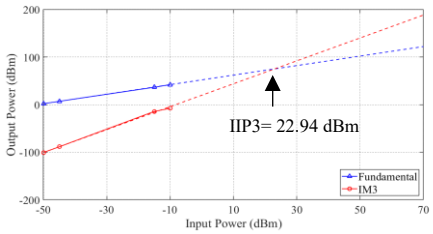


Fig. 16. The IIP3 of the amplifier using the conventional and the pseudo-resistor in [6]–[8]

3) *Employing the highly linear pseudo-resistor* [6]–[8] *in both stages*

In this section, the pseudo-resistor in [6]–[8] (PMOS-NMOS transistor pseudo-resistor with source follower) is employed as a FB resistor in the first and second stages of the amplifier, as shown in Fig. 7 (c). An equal R design is used in testing the overall bio-amplifier. The advantage of this amplifier over the one discussed in the previous section is that the use of highly linear pseudo-resistor [6] in both stages. This provides more tunability to the amplifier's f_L as we can control the lower cutoff frequency using four pseudo-resistors employed in the first and second stages. Hence, by reducing the biasing current in the source follower in both stages, the lower cutoff frequency tunability range will increase more than in the previous case. The response of the biomedical amplifier is conducted over three different biasing currents, namely 1n A, 1.5n A, and 2n A as shown in Fig. 17, where the lower cutoff frequencies are 1.54 Hz, 2.1 Hz, and 2.6 Hz respectively. It's noticeable that f_L is reduced more by using the same biasing currents.

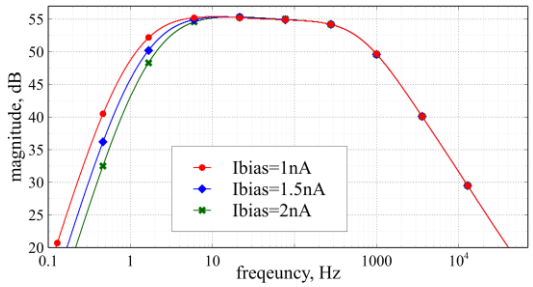


Fig. 17. The response of the biomedical amplifier using the pseudo-resistor in [6]–[8] in both stages over three different biasing current values; 1nA, 1.5nA, and 2nA

The IRN spectral density of the biomedical amplifier was conducted and showed a low value of (320 nV/$\sqrt{Hz}$) at frequencies above 10 Hz. IRN increases at frequencies below 10 Hz till reaching (24.76 μV/$\sqrt{Hz}$) at 0.1 Hz. A 1mVpk-pk input sinusoidal signal with 100 Hz frequency was applied to examine the steady-state response, as shown in Fig. 18 (a). The output voltage depicted in Fig. 18 (b) represents an inverted sine wave signal and is amplified with an amplitude of 0.56 Vpk-pk, which is exactly 54.9 dB multiple of 1mV input signal. The symmetricity in the resulting output sinewave is higher than in the previous case. The THD test was performed using an input amplitude of 1 mV for different input frequencies of 50 Hz, 100 Hz, 250 Hz, 450 Hz, 600 Hz, and 650 Hz as shown in Fig. 19, where it gave lower distortion than the previous case as the used pseudo-resistors is characterized by a constant value, thus the linearity of the design improved significantly.

TABLE II
THE DESIGN COMPONENTS AND PARAMETERS COMPARISON OF THE OP-AMP BASED BIOMEDICAL AMPLIFIER FOR THE THREE CASES OF EMPLOYING THE PSEUDO-RESISTORS AS A FEEDBACK-ELEMENTS

Components	Value	Design parameters	The values when employing pseudo-resistors as a FB resistor using:		
			Conventional Type in both stages	Conventional in 1st stage, and the type in [6] in 2nd stage	The type in [6] in both stages
C_1	11.7 pF	**Gain**	54.6 dB	54.9 dB	54.9 dB
C_2	0.3 pF	**Voltage supply**	± 0.6 V	± 0.6 V	± 0.6 V
C_3	1.4 pF	**BW**	650 Hz	678.2 Hz	678.5 Hz
C_4	0.1 pF	**IRN @ 0.1Hz**	70.2 $\mu V/\sqrt{Hz}$	41.66 $\mu V/\sqrt{Hz}$	24.76 $\mu V/\sqrt{Hz}$
M_{c1}, M_{c2}	1 µm / 100 µm	**IRN, above 10Hz**	405.33 $nV/\sqrt{Hz}$	312.8 $nV/\sqrt{Hz}$	320 $nV/\sqrt{Hz}$
M_1, M_2	0.26 µm / 65 µm	**Power**	4.69 µWatt	4.69 µWatt	4.69 µWatt
M_{S1}, M_{S2}	200 µm / 1.5 µm	**THD @250 Hz, 1 m V_{pk-pk}**	0.197% (-54.1 dB)	0.306% (-50.2 dB)	0.091% (-60.8dB)
		IM3 @10 and 20 Hz, 1 mV_{pk-pk}	33.22 dB	46.49 dB	49 dB
		IIP3	22.6 dBm	22.94 dBm	24.9 dBm

The frequency of 250 Hz was located at the flat band of the biomedical magnitude response, where the lowest distortion was reported at approximately 0.0931% (-60.82 dB). Above 450Hz frequency, the THD increases slightly as observed at frequencies 600 Hz and 650 Hz, where the corresponding THD are 0.1023% (-59.8 dB) and 0.1009% (-59.9 dB), respectively.

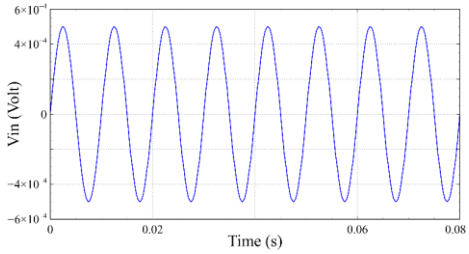


Fig. 18. The steady-state time response of the amplifier using the pseudo-resistor in [6]–[8] in both stages: (a) Input sinusoidal signal 1mV pk-pk amplitude with 100 Hz frequency (b) Output sinusoidal signal 0.56 V pk-pk amplitude

Fig. 20 represents the IM3 test of the biomedical amplifier with two single tones at 50 Hz and 60 Hz frequencies, each of 1 mV_{pk-pk} amplitude. This test also shows that the linearity of this design is better than the previous one as the IM3 value increased. The test revealed a value of 49 dB. The simulation conducted to find the IIP3 of the amplifier is demonstrated in Fig. 21 and represents a value of 24.9 dBm, which is higher than the previous design, which will emphasize that this test is better than the previous one in terms of linearity, symmetricity, and the fine-tuning of the f_L. The design components and parameters comparison of the op-amp based biomedical amplifier for the three cases employing the pseudo-resistors as FB elements are presented in Table II.

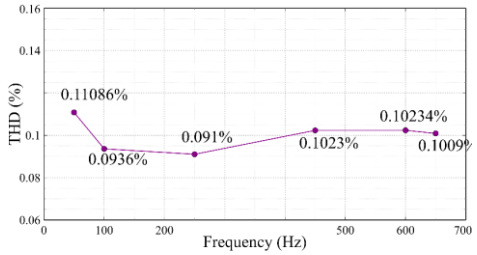


Fig. 19. The THD of the overall biomedical amplifier using the pseudo-resistor in [6]–[8] in both stages

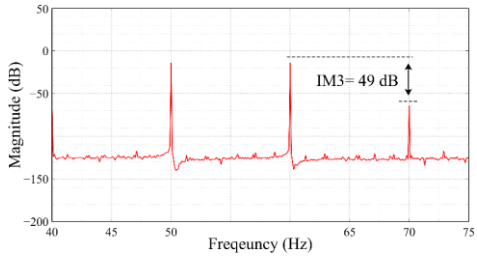


Fig. 20. The IM3 of the amplifier using the pseudo-resistor in [6]–[8] in both stages at the amplitude of 1 m V_{pk-pk} via 50 Hz and 60 Hz frequencies

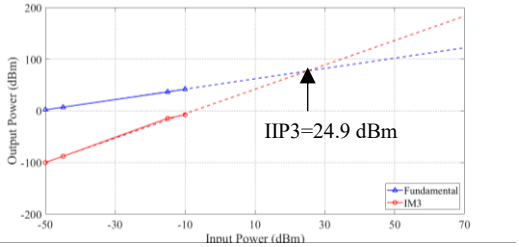


Fig. 21. The IIP3 test of the amplifier using the pseudo-resistor in [6]–[8] in both stages

Comparing the results obtained in the three different cases shown in Table II, it can be concluded that the 3rd case is having the best performance, with the lowest noises and THD, and highest IM3 and IIP3 values. Its noticeable that the noise value decreases from 70.2µV/√Hz to 24.762µV/√Hz, while the power remains 4.69 µW for all the three designs. However, the noises in amplifiers are usually reduced at the cost of increased supply currents, i.e. power dissipation. However, the improvement of noise in our case is not associated with the supply increase, but with replacing the conventional pseudo-resistor with the highly linear one presented in [6]–[8]. The pseudo-resistor in this amplifier controls the lower cutoff frequency of the amplifier, according to the following equation derived from the transfer function.

$$\omega_o = \frac{1}{\sqrt{C_2 C_4 R_1 R_2}} \quad (17)$$

Therefore, the IRN at 0.1 Hz was 70.2μV/√Hz when the conventional pseudo-resistor was utilized at both stages. Whereas when the conventional one was replaced with the pseudo-resistor designed in [6]–[8], the IRN was reduced to 24.762μV/√Hz. The power is unchanged in the 3 cases.

Process, voltage, and temperature variations were performed to study the robustness of the third amplifier case, shown in Fig. 7 (c), utilizing 1nA biasing currents in highly linear pseudo-resistors (I_{Bias}=1 nA). The tests were conducted under conventional circumstances and over different parameter variations. The NMOS and PMOS were examined under different conditions in the process variation test. The conditions are the typical (T), fast (F), and slow (S), which results in producing five process corners: TT, SS, SF, FF, and FS.

These corners are applied to the biomedical amplifier to identify the critical combinations and test the amplifier's performance as shown in Fig. 22 (a). The supply voltage variations were tested by generating an error of ±2% to the supply, so the values used are ±0.588V, ±0.6V, and ±0.612V as shown in Fig. 22 (b). For the temperature variation test, the biomedical amplifier was tested under a low temperature of -10° C, room temperature of 27° C and high temperature of 50° C as provided in Fig. 22 (c). The performance of the amplifier is robust against process, voltage, and temperature variations. A very slight reduction in the f_L (from 1.54 Hz to 0.78 HZ) is observed in the process variations test under both corners FS and SF. This can be compensated through the I_{Bias}. This can be done by providing a higher biasing current of 10 nA which will result in increasing the lower cutoff frequency as shown in Fig. 23.

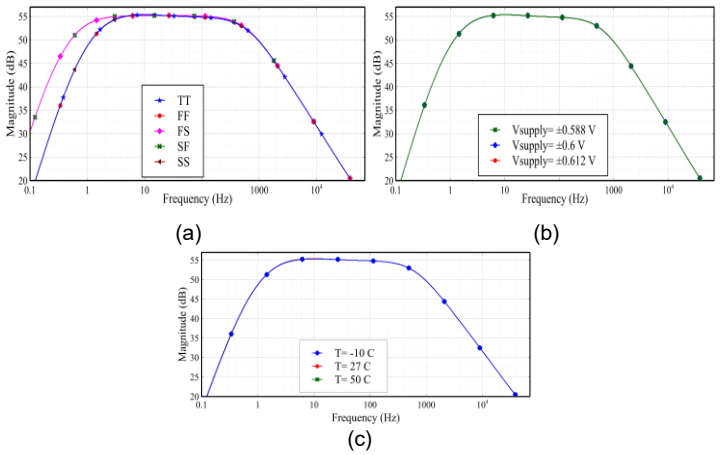


Fig. 22. The magnitude response of the overall amplifier under: (a) The 5 process corners, (b) V supply corners, and (c) T corners

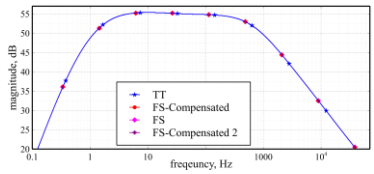


Fig. 23. The magnitude response of the overall amplifier under the 5 process corners after compensating the FS and SF corners using I_{Bias}= 10n A

The pseudo resistor is sensitive to the PVT variations which can cause a variation in the amplifier's gain [21]. In this work , the robustness of the amplifier's gain is observed to be due to the amplifier's structure. Such structure makes the gain independent from the pseudo-resistor. The amplifier's gain is a function of the input and FB capacitances, which are insensitive to the variations. This ensures a fixed gain value over wider PVT variations. Since the pseudo-resistor affects the lower cutoff frequency, this issue might be challenging under the PVT variations. The biasing currents can provide in this case a solution. If the variation causes a reduction in the amplifier's f_L, it can be easily compensated by providing higher biasing currents that lead to reducing the resistance of the pseudo-resistor and thus increasing the amplifier's f_L and vice versa. Consequently, a robust design in terms of amplifier's gain and BW can be preserved.

For further evaluation of the reliability, robustness and sensitivity of the pseudo-resistor, the Monte Carlo simulation is performed considering the third amplifier case shown in Fig. 7 (c) using 1nA biasing current in the pseudo-resistors. Monte Carlo simulated the PVT tests, by applying ±10% tolerance to the voltage source, and then repeated 100 times for each of the 5 process corners, 3 voltages variations and 3 temperature variation tests. According to the simulation results in Fig. 24 (a), the design showed lower sensitivity to the voltage variations under the 5 process corners (TT, FF, FS, SF and SS). The two corners FS and SF showed small impact in the lower cut off frequency. The critical combinations of the process variation demonstrated robust response using the Monte Carlo simulation. The tested supply voltage variation was examined under the same condition of ±10% voltage source tolerance, shown in Fig. 24 (b). The results demonstrated that the amplifier shows robust response against the voltage variation. The temperature variation with ±10% voltage source tolerance shown in Fig. 24 (c). The result represented strongly stable response.

Table III demonstrates the simulation results and parameters of the proposed amplifier compared to [4], [22], [23], [24], [25] and [26]. The amplifier in this work exhibits the lowest distortion among the listed previous work. It should be noted that this work combines between realizing a high resistance value (1.08 TΩ) over a wide dynamic range using a simple structure that consumes extremely low power (2.4 nWatt) while maintaining the lowest distortion among the prior work.

A figure of merit (FOM) was developed in (18) allocated to evaluate and compare the overall performance of similar designs in the literature. The FOM comprises the parameters: amplifier's bandwidth *BW* (kHz), input-referred noise *IRN* (μV), overall power consumed by the amplifier *P* (μWatt), total harmonic distortion *THD* (%), and the number of used transistors/pseudo-resistor (Complexity). The highest FOM among the previous work was presented by the proposed biomedical amplifier and shown in Fig. 7(c), as depicted in Table III.

$$FOM = 20\log\frac{R\,(\Omega).BW\,(Hz)}{IRN(\mu V).\text{THD}\,(\%).\text{P}(\mu\text{Watt}).\text{Complexity}} \quad (18)$$

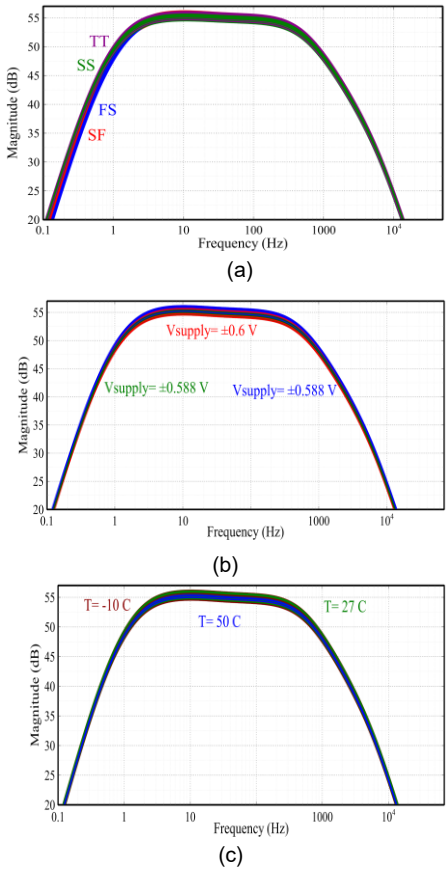


Fig. 24. The Monte Carlo simulation of the overall amplifier under: (a) The 5 process corners, (b) V supply corners, and (c) T corners

III. Programmable Gain And Band-Width Amplifier Based On Tenable UGBW Rail-To-Rail Op-Amps

The employment of conventional op-amps in biomedical amplifiers caused numerous restrictions on the amplifier. The biomedical amplifiers exhibited major challenges due to the fixed BW, accordingly, the amplifier bounded to target limited neuron's signals as in [27], [17], and [18] where the amplifier's BW were 7.8k Hz, 5 kHz, and 680Hz, respectively. As a result, the design might fall short of the expectations for recording all common bio-signals with frequencies between a few Hz up to 10kHz. Furthermore, if the application requires to capture a low frequency range, a large on-chip compensating capacitor will be needed. This results in consuming a larger area. Thus, amplifiers with typical, fixed UGBW op-amps, causes challenges to the designers. In [17], [26] and [27], the proposed amplifiers used tunable pseudo-resistors to provide controllability to the lower cutoff frequency (f_L), with ranges of (0.1Hz - 1Hz), (0.23Hz - 217 Hz), and (4 Hz - 300Hz), respectively. In [26], the programmability of the BW has been obtained throughout the range of 4 Hz to 10 kHz, which is compatible with the achieved ranges from other studies.

This section reviewed the design of the programmable BW and gain amplifier based on a tunable UGBW op-amp [9]. The fundamental idea behind this amplifier is to provide a programmable gain and BW amplifier to surpass the restrictions imposed by using typical op-amps.

The amplifier's capacity to tolerate diverse signals with a BW ranging from (50Hz - 10kHz) permits wide signals detection. Electromyogram (EMG), Phonocardiogram (PCG), Electroencephalogram (EEG), Electrocardiogram (ECG), and Intra-cellular and Extra-cellular Action Potentials are among the biomedical signals detected by the amplifier (APs). The UGBW is tuned with a fixed and tiny capacitive load to achieve higher cutoff frequency controllability. The constant high resistance pseudo-resistor in [6] is used to control the lower cutoff frequency from 1Hz to 100Hz. While the amplifier's gain controllability was achieved by altering the input capacitors without influencing the amplifier's BW. The biomedical amplifier's overall power consumption is low, and the stability is preserved over the entire range. The design of the amplifier is dependent on an op-amp construction that operates without an internal compensator, instead, it relies on a load capacitor. The op-amp is operating from the minimum to the maximum supply due to the utilized CMOS input differential stage.

TABLE III

THE DESIGN PARAMETERS AND PERFORMANCE COMPARISON OF THE BIOMEDICAL AMPLIFIER (AFTER EMPLOYING THE PSEUDO-RESISTOR IN [8]IN THE 1ST AND 2ND STAGES) WITH PREVIOUS WORK

Parameters of amplifier	**This work**	**Ref.** [4]	**Ref.** [22]	**Ref.** [23]	**Ref.** [24]	**Ref.** [25]	**Ref.** [26]
Supply voltage	±0.6 V	1 V	3 V	±0.6 V	3.3 V	2.5 V	1.8 V
CMOS Technology	180 nm	180 nm	350 nm	350nm	350 nm	130 nm	180 nm
Power consumption	4.69 µWatt	1.6 µWatt	11.4 µ Watt	---	541.2 µW	1.25 µW	20.8 µWatt
Bandwidth	678.5 Hz	500 Hz	10K-10M Hz	8 k Hz	4.27 kHz	2k Hz	4/300 -10 K Hz
Input Referred Noise	1.3 µV, over the mid-band	0.61 µV, over the mid-band	39.9 µV	---	2.49 µV	38.5 µV	2.6/2.38 µV at 50 kHz
THD	0.091% (60.8 dB) at 250 Hz, 1mV$_{pk-pk}$	4.2% (27.5 dB)	0.33%(49 dB)	Below 3% at 500 Hz, 150 mV	0.126% (58 dB) at 1 kHz	0.19% (54.42) at 10 Hz	1.34%/ 0.503% (37.45dB/45.97 dB) at 4Hz / 10k Hz
Pseudo-resistor	**This work**	**Ref.** [4]	**Ref.** [22]	**Ref.** [23]	**Ref.** [24]	**Ref.** [25]	**Ref.** [26]
Resistance value	1.08 TΩ	650 GΩ	20M-20GΩ	823 MΩ	2.9994 TΩ	200 GΩ	0.7 TΩ
Dynamic range	±0.6 V (rail-to-rail)	±1 V	0 – 3V	±0.5 V	1.8 – 3.3 V	0.1-0.4V	±0.2 V
Sensitivity to process variations	Yes	Yes	Yes	Yes	--	--	Yes
Compensated	Yes	Yes	Yes	No	No	No	Yes
Circuit complexity:	Low	High	Low	Low	Low	Low	Medium
No. of MOS transistors in each pseudo-R	4	11	2	4	2	2	6
No. of used Pseudo-R in the amplifier	4	4	1	2	2	1	4
Power consumed by each pseudo-resistor	2.4 nWatt	-----	0.1 µWatt	88.8 nWatt	21.8 µW	---	0.9*I$_{tune}$
FOM(dB)	570.37	537.15	556.47	274.88	558.534	546.79	544.136

A. Programmable Op-Amp and It Is Application In Biomedical Amplifier

A fully balanced and single-ended op-amp demonstrated in [9], was designed using input differential pairs (IDPs), current mirrors (CMs), and load capacitors which are responsible to compensate for the operation of the op-amp and preserve high stability. To improve the performance of the circuit, the nested CM technique was applied, where the IDPs have been divided into three pairs. Their combined I_{out} was summed through 3 subdivided CMs. Each subdivided CM was given a certain gain factor. This method offers the overall operational amplifier's gain by allocating the appropriate CM ratio.

This configuration of the op-amp presented in [9] was provided with a programmability feature over the UGBW. The controllability was achieved by controlling (I_{UGF1} and I_{UGF2}), where I_{UGF1} and I_{UGF2} are the common tail currents of the input differential pairs of the NMOS and PMOS respectively.

By tuning the biasing voltages V_{B1} and V_{B2}, controlling I_{UGF1} and I_{UGF2}, respectively, the UGBW was programmed. Two additional CMs were incorporated with each pair of the 3 DPs, to sum the currents of the N and P types in each DP. These added currents were mirrored in the 3-step NCMs.

The simulations were conducted using the 90 nm CMOS model under +1V supply. At certain biasing voltages of V_{B1}=0.82V and V_{B2}=0.3V, Table IV summarized the design specifications of the fully balanced and single-ended op-amps. In the first amplifier stage shown in Fig. 25, a fully balanced rail-to-rail op-amp was used. This stage contained C_1, C_2, and R_1 as mentioned in the previous section, where R_1 was realized using the pseudo-resistor in [8]. The simulations were performed using different biasing voltages to explore the UGBW controllability of the op-amp. As a result of this controllability, the biomedical amplifier's BW was maintained.

A single-ended op-amp was employed in the second stage of the amplifier shown in Fig. 25. Similar to the fully differential op-amp, the simulation was performed over a wide voltage biasing range to observe the controllability of the UGBW of the op-amp, which leads to controlling the amplifier's BW.
The gain, BW, phase margin, and power consumption of the fully balanced and single-ended op-amp for designated V_{B1} and V_{B2} and the corresponding amplifier's f_h are summarized in Table V.

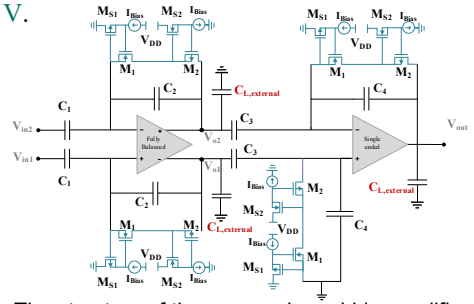


Fig. 25. The structure of the op-amp-based bio-amplifier using the new pseudo-resistor as FB resistors

B. OVERALL BIOMEDICAL AMPLIFIER DESIGN AND SIMULATION

The first and second stages of the amplifier were cascaded to form a two stages amplifier with 54.9 dB gain. The programmability feature of the BW was proposed by controlling the UGBW parameters of both applied op-amps, namely: V_{B1} and V_{B2}. The amplifier was able to accommodate diverse signals, which was represented by the magnitude response shown in Fig. 26. It was obtained at a fixed load capacitor of 30 pF throughout a wide range of V_{B1} and V_{B2}. This controllability enables the capture of a variety of bio-signals, including ECG, EEG, PCG, EMG, and intra and extracellular (APs). Programmability over the lower cutoff frequency was achieved as illustrated in Fig. 27, by adjusting the biasing currents in the Feedback pseudo resistors. The programmability over the lower cutoff frequency (f_L) reached 100 Hz using 70nA current source. Having a high f_L is desirable in some cases to detect the Intra-cellular and Extra-cellular Action Potentials (APs) which are in the range of (100Hz-10kHz) [5]. For certain selected V_{B1} and V_{B2}, the corresponding f_h, IRN, and the consumed power of the overall biomedical amplifier are shown in Table V.

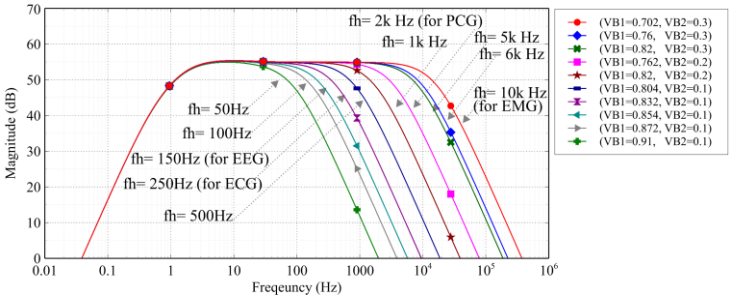


Fig. 26. The magnitude response of the overall amplifier over diverse f_h for certain biasing voltages

TABLE IV
THE DESIGN PARAMETERS OF THE RAIL-TO-RAIL OP-AMP AT V_{B1} = 0.82V & V_{B2}= 0.3V

Design parameters	Fully differential op-amp	Single-ended op-amp
Supply Voltage	+1 V	+1 V
C_L	30 pF	30 pF
Gain	77.7 dB	74.14 dB
Gain bandwidth	639.7 kHz	487.5 kHz
Phase margin	64.7°	77.2°
Slew rate	0.29 V/μs	0.05 V/μs
Power	1.198 μW	1.17 μW
Offset Voltage	330 nV	240 nV

Table VI represents the parameters and components of the overall amplifier at f_h of 10k Hz. This amplifier's design does not only provide BW controllability but also provides gain tunability which is another distinguishing feature [9]. The amplifier's gain was controlled by controlling the input capacitors of each stage (C_1 and C_3) since the gain of the first and second stages were C_1/C_2 and C_3/C_4, respectively. C_2 and C_4 are dependent on the cutoff frequencies, nevertheless they are independent from each other. Adjusting C_1 and C_3 controls the amplifier's gain without affecting the BW. However, a small impact was detected on the f_h, where it was decreased as the input capacitances increased. However, this influence was compensated using an external capacitive load, which is an extra noteworthy characteristic in this circuit. The capacitive load is inversely proportional to the higher cutoff frequency, therefore by providing fine-tuning of load capacitance, the amplifier's gain was programmed at a fixed BW. Fig. 28 demonstrated the controllability of the amplifier's gain between (44.3 dB - 65dB) by tuning the input capacitance C_1 from (7.8pF- 20 pF) and tuning input capacitance C_2 from (0.6 pF - 2.7pF) at f_h and f_L of 10k Hz and 1.4Hz, respectively. The capacitive load is tuned between 61.5pF to 0.7pF to compensate for the frequency response. The PVT variation tests were

performed and showed that the responses of the design under the critical corners are very close to the typical one. It is noteworthy that the amplifier's gain is insensitive to the PVT variations since the amplifier's gain is dependent on the capacitance ratio, which leads to having a robust response in terms of the amplifier's gain. Knowing that the amplifier's f_h is dependent on the UGBW of the utilized op-amps which is sensitive to temperature variations, yet it was compensated through the capacitive load. While the lower corner frequency is a function of the pseudo-resistor which is sensitive to the process corners FS and SF which also compensated using the biasing currents of the pseudo-resistors. The design parameters of the biomedical amplifier and simulation results are compared with [17], [27], and [26]. It is shown that the biomedical amplifier-based rail-to-rail op-amp done in [9] combines the programmability feature over the amplifier's BW, and the mid-gain while preserving the lowest consumed power. A figure of merit (FOM) was identified in [9] to assess the overall performance. It revealed that the biomedical amplifier in [9] exhibits the highest FOM compared to similar designs in literature.

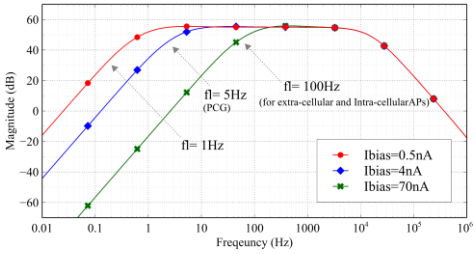


Fig. 27. The magnitude response of the overall amplifier over different f_L for different biasing currents

TABLE VI

THE DESIGN PARAMETERS OF THE AMPLIFIER BASED ON THE RAIL-TO-RAIL OP-AMP AT A F_H OF 10K HZ

Component	Value	Design parameters	Value
C_1	11.7 pF	**Gain**	54.9 dB
C_2	0.3 pF	**Technology**	90nm
C_3	1.4 pF	**Supply**	1 V
C_4	0.1 pF	**BW**	10k Hz
$M_1 - M_2$	0.26 µm /65 µm	**IRN @ 100 Hz**	1.3 $\mu V/\sqrt{Hz}$
$M_{S1} - M_{S2}$	200 µm /1.5 µm	**IRN @ 1k Hz**	426.1 $nV/\sqrt{Hz}$
		Power consumption	3.28 µWatt
		THD@4k Hz - 1mV$_{pk-pk}$	0.68% (-43.3dB)
		IM3@6k & 7kHz 1mV$_{pk-pk}$	40.59dB
		IIP3	19.44dBm

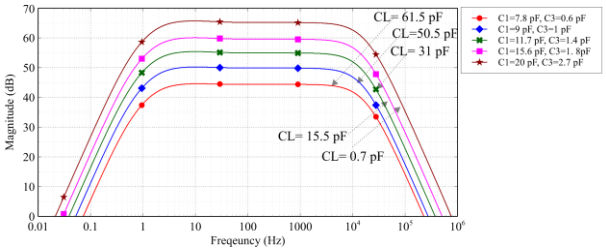


Fig. 28. The magnitude response of the overall amplifier over diverse amplifier's gain for certain input capacitance

IV. CONCLUSION

This paper presented a review of different types of biomedical amplifiers reported in the literature taking into consideration the different types of pseudo-resistors. This survey follows multiple directions. Firstly, it represents the different pseudo-resistor designs in the literature. Then, it studies the effect of these pseudo-resistors as a feedback element on the performance of the biomedical amplifier. It also demonstrates the impact of utilizing different active blocks on the biomedical amplifier performance. This work also analyzed pseudo-resistors parameters such as the emulated resistance, power consumption, dynamic range, sensitivity to PVT, compensation feature, and complexity. It also highlighted critical parameters for the biomedical amplifiers, such as power consumption, supply voltage, IRN, THD, CMOS technology, amplifier's BW, and gain. It demonstrated the design of a conventional and programmable Tera ohm MOS pseudo-resistor. For better illustration, all the parameters were summarized in a tabular form. The pseudo-resistors were employed as feedback elements in a two-stage biomedical amplifier. The simulations showed that the programmable Tera ohm pseudo-resistor revealed a robust response against PVT variation tests. The paper showcased the design of a biomedical amplifier with programmable gain and bandwidth based on tunable unity gain bandwidth CMOS Op-amp and programmable pseudo-resistor. The observation from the survey is that most of the pseudo-resistors are sensitive to process variation since their resistance value is dependent on the process parameters and the threshold voltage. This drawback attracts the researcher's attention towards providing programmability features to compensate for the unwanted variations. However, there is almost no research-designed pseudo-resistor that is not sensitive to process variation. This research gap is a potential work for further research work in the future.

TABLE V

THE DESIGN PARAMETERS OF THE RAIL-TO-RAIL OP-AMP FOR SELECTED BIASING VOLTAGES AND THE CORRESPONDING HIGHER CUTOFF FREQUENCY OF THE BIO-AMPLIFIER IN EACH STAGE

Biasing voltages		**Fully balanced op-amp**				**1st Amplifier stage**	**Single-ended op-amp**				**2nd Amplifier stage**	**Two stages of bio-amplifier parameters**			
V_{B1} (V)	V_{B2} (V)	Gain (dB)	ω_t (Hz)	φ_m (°)	f_h (Hz)	f_h (Hz)	Gain (dB)	ω_t (Hz)	φ_m (°)	Power (Watt)	f_h (Hz)	f_h (Hz)	Power (Watt)	IRN ($V/\sqrt{Hz}$) @ 100 Hz	IRN ($V/\sqrt{Hz}$) @ 1k Hz
0.702	**0.3**	78.8	1.182M	60.22	10 k	10 k	75.3	775.2k	76.3	1.64 µ	16.8 k	10 k	3.282 µ	1.3 µ	426 n
0.76	**0.3**	78	751 k	63.3	6 k	6 k	74.5	548 k	77	1.26 µ	5 k	6 k	2.522 µ	1.48 µ	489.5 n
0.82	**0.3**	77.7	639.7 k	64.7	5 k	5 k	74.1	487.5 k	77.2	1.17 µ	4.5 k	5 k	2.342 µ	1.58 µ	522.6 n
0.762	**0.2**	72	247.7 k	64.8	2 k	2 k	68.9	143.2 k	79	0.2 µ	2.7 k	2 k	0.402 µ	1.16 µ	439.3 n
0.82	**0.2**	68.5	127.3 k	68	1 k	1 k	66.9	82.2 k	79.2	0.11 µ	1.5 k	1 k	0.222 µ	1.33 µ	569.4 n
0.804	**0.1**	62.5	59 k	74.9	500	500	56.8	29.3 k	84.3	43 n	1.4 k	500	87.92 n	1.17 µ	566.4 n
0.832	**0.1**	57.2	31.4 k	78.7	250	250	51.9	15.6 k	85.6	24 n	690	250	49.92 n	1.25 µ	738 n
0.854	**0.1**	53.1	17.9 k	81.4	150	150	47.9	9.01 k	86.7	17 n	417	150	35.92 n	1.39 µ	949.5 n
0.872	**0.1**	49.8	12 k	83	100	100	44.8	6.13 k	87.8	13 n	270	100	27.92 n	1.56 µ	1.17 µ
0.91	**0.1**	44	6 k	85.6	50	50	39.9	3.14 k	88.5	9.4 n	130	50	20.72 n	2.05 µ	1.78 µ

REFERENCES

[1] L. R. Hochberg, D. Bacher, B. Jarosiewicz, N. Y. Masse, J. D. Simeral, and J. Vogel, "Reach and grasp by people with tetraplegia using a neurally controlled robotic arm," *Nature*, vol. 485, no. 7398, pp. 372–375, 2012, doi: 10.1038/nature11076.

[2] J. L. Collinger *et al.*, "High-performance neuroprosthetic control by an individual with tetraplegia," *The Lancet*, vol. 6736, no. 12, pp. 1–8, 2012, doi: 10.1016/S0140-6736(12)61816-9.

[3] L. R. Hochberg *et al.*, "Neuronal ensemble control of prosthetic devices by a human with tetraplegia," *Nature*, vol. 442, no. 7099, pp. 164–171, 2006, doi: 10.1038/nature04970.

[4] M. U. Abbasi and I. C. London, "A wearable EEG amplifier using a novel teraohm low-distortion tunable hybrid pseudo-resistor," *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 7–11, 2021, doi: 10.1109/ISCAS51556.2021.9401111 A.

[5] F. H. Noshahr, M. Nabavi, and M. Sawan, "Multi-Channel Neural Recording Implants : A Review," *sensors*, pp. 1–29, 2020, doi: 10.3390/s20030904.

[6] I. Y. Abushawish and S. A. Mahmoud, "Two Stage CMOS Bio-medical Amplifier Based on a highly Linear TΩ Pseudo-Resistor," pp. 143–144, 2021, doi: 978-1-6654-0174-6.

[7] I. Y. Abushawish and A. M. Soliman, "Constant Tera-ohm Pseudo-resistor Over Wide Dynamic Range." pp. 470–475, 2021. doi: 10.1109/IEMTRONICS52119.2021.9422490.

[8] I. Y. Abushawish and S. A. Mahmoud, "Robust CMOS Pseudo-resistor and its Applications in Bio-medical Amplifiers," in *IEEE International Symposium on Circuits and Systems (ISCAS 2022)*, 2022, pp. 46–50. doi: 978-1-6654-8485-5/22/$31.00.

[9] I. Y. Abushawish and S. A. Mahmoud, "A programmable gain and bandwidth amplifier based on tunable UGBW rail-to-rail CMOS op-amps suitable for different bio-medical signal detection systems," *AEUE - International Journal of Electronics and Communications Contents*, no. 1434–8411, p. 153952, 2021, doi: https://doi.org/10.1016/j.aeue.2021.153952.

[10] R. R. Harrison *et al.*, "A low-power integrated circuit for a wireless 100-electrode neural recording system," *IEEE J Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, 2007, doi: 10.1109/JSSC.2006.886567.

[11] J. N. Y. Aziz *et al.*, "256-channel neural recording and delta compression microsystem with 3D electrodes," *IEEE J Solid-State Circuits*, vol. 44, no. 3, pp. 995–1005, 2009, doi: 10.1109/JSSC.2008.2010997.

[12] R. R. Harrison, C. Charles, and S. Member, "A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications," *IEEE J Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, 2003, doi: 10.1109/JSSC.2003.811979.

[13] K. Sharma, A. Pathania, R. Pandey, J. Madan, and R. Sharma, "MOS based pseudo-resistors exhibiting Tera Ohms of Incremental Resistance for biomedical applications : Analysis and proof of concept," *Integration, the VLSI journal*, vol. 76, no. March 2020, pp. 25–39, 2021, doi: 10.1016/j.vlsi.2020.08.001.

[14] N. M. Laskar *et al.*, "Design of high gain, high bandwidth neural amplifier IC considering noise-power trade-off," *Microsystem Technologies*, vol. 5, 2018, doi: 10.1007/s00542-018-4142-5.

[15] R. Mancini, "Op Amps For Everyone," 2022.

[16] A. B. Williams, "Analog Filter and Circuit Design Handbook," 2014.

[17] K. Abdelhalim, L. Kokarovtseva, J. L. Perez Velazquez, and R. Genov, "915-MHz FSK/OOK wireless neural recording soc with 64 mixed-signal fir filters," *IEEE J Solid-State Circuits*, vol. 48, no. 10, pp. 2478–2493, 2013, doi: 10.1109/JSSC.2013.2272849.

[18] I. Y. Abushawish and S. A. Mahmoud, "CMOS Bio-medical Amplifier based on Tera-Ohm Pseudo-resistor for Bio-detection System," in *International Multi-Conference on Systems, Signals & Devices (SSD'21)*, Monastir, Tunisia, 2021, pp. 403–408. doi: 10.1109/SSD52085.2021.9429430.

[19] T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, "A Nano-Ampere Current Reference Circuit and its Temperature Dependence Control by using Temperature Characteristics of Carrier Mobilities," in *2010 Proceedings of ESSCIRC*, 2010, pp. 114–117. doi: 10.1109/ESSCIRC.2010.5619819.

[20] T. Serrano-gotarredona, R. Serrano-gotarredona, and C. Serrano-gotarredona, "Current Mode Techniques for Sub-pico-Ampere Circuit Design," *Analog Integr Circuits Signal Process*, vol. 1, pp. 103–119, 2004, doi: https://doi.org/10.1023/B:ALOG.0000011162.52504.39.

[21] E. Bharucha, H. Sepehrian, and B. Gosselin, "A survey of neural front end amplifiers and their requirements toward practical neural interfaces," *Journal of Low Power Electronics and Applications*, vol. 4, no. 4. MDPI AG, pp. 268–291, Nov. 14, 2014. doi: 10.3390/jlpea4040268.

[22] E. Guglielmi *et al.*, "High-value tunable pseudo-resistors design," *IEEE J Solid-State Circuits*, vol. 55, no. 8, pp. 2094–2105, Aug. 2020, doi: 10.1109/JSSC.2020.2973639.

[23] D. Palomeque-Mangut, J. L. Ausín, F. Duque-Carrillo, and Guido Torelli, "Design of Robust Pseudo-Resistors with Optimized Frequency Response," in *European Conference on Circuit Theory and Design (ECCTD)*, IEEE, 2017. doi: 10.1109/ECCTD.2017.8093269.

[24] Yu-Chieh Huang, Tzu-Sen Yang, Shun-Hsi Hsu, Xin-Zhuang Chen, and Jin-Chern Chiou, "A Novel Pseudo Resistor Structure for Biomedical Front-end Amplifiers," in *International conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, 2015, pp. 2713–2716. doi: 978-1-4244-9270-1/15/$31.00.

[25] P. Luiz Benko, M. Galeti, C. Fidelix Pereira, J. Cesar Lucchi, and R. Camargo Giacomini, "Bio-Amplifier based on MOS bipolar Pseudo-Resistors: A New Approach using its non-linear characteristic," *Journal of Integrated Circuits and Systems*, vol. 2, pp. 132–139, 2016, doi: 10.29292/jics.v11i2.437.

[26] H. Rezaee-dehsorkh *et al.*, "Analysis and Design of Tunable Amplifiers for Implantable Neural Recording Applications," *IEEE J Emerg Sel Top Circuits Syst*, vol. 1, no. 4, pp. 546–556, 2011, doi: 10.1109/JETCAS.2011.2174492.

[27] W. Liew, X. Zou, L. Yao, and Y. Lian, "A 1-V 60-μW 16-Channel Interface Chip for Implantable Neural Recording," in *IEEE 2009 Custom Intergrated Circuits Conference (CICC)*, 2009, pp. 507–510. doi: 10.1109/CICC.2009.5280795.

ISRAA Y. I. ABUSHAWISH received the B. Sc degree in electrical and electronics engineering in 2018/2019 (Hons.). She joined the M.Sc. in electrical and electronics engineering from the University of Sharjah in 2019 and in September 2022 she received the degree. She has been working as a teacher assistant with the Department of Electrical and Computer Engineering, University of Sharjah, UAE since 2019. Currently, she is completing her PhD working as a researcher with the research group: Mixed Analog-Digital Smart Electronic Circuits and Systems (MADSECS) in University of Sharjah, which is one of the specialized Research Groups affiliated to the Research Institute for Sciences and Engineering. Her master's thesis involves the design of low-frequency amplifiers based on highly linear pseudo-resistor and using programmable Analog Building Blocks, such as CMOS rail-to-rail operational amplifiers and Digital programmable operational transconductance amplifiers. She has published several research papers in international conferences and Journals. Her research interests include mixed analog digital IC design, Biomedical amplifiers, and operational amplifier circuit design.

SOLIMAN A. MAHMOUD (IEEE Senior Member) was born in Cairo, Egypt, in 1971. He received the BSc degree with honors in 1994, the MSc degree in 1996, and the PhD degree in 1999, all from the Electronics and Communications Department, Cairo University, Egypt. He is Professor and the department chairman at the Electrical and Computer Engineering Department, University of Sharjah, Sharjah, UAE. Prof. Mahmoud is actively engaged in scholarly research work and has authored and co-authored more than 150 journal and conference publications since joining academia in 1996. His articles received more than 2000 citations and his Google Scholar h-index is 25 (h-index from Scopus is 22). Prof. Mahmoud also published 6 refereed research books His research interest lies in the area of mixed analog/digital integrated electronic circuit (IC) design including mixed mode (Voltage/Current) analog circuits IC design, mixed (analog/ Digital) programmable CMOS Electronics Systems, Biomedical Circuits, Field Programmable Analog arrays (FPAA), and Multi-standard wireless receiver design. He supervised 2 PhD students, 15 MSc. students and more than 30 senior design projects. Prof. Mahmoud have received

“The German - Egyptian Research Fund” Grant. The Grant has been used to finance the project “Design of CMOS Field Programmable Analog Array and its Applications”. The project has been carried out in collaboration with Ulm Microelectronics Institute, ULM university, Germany. Prof. Mahmoud was decorated with the Distinguished research award for the year 2014-2015 and for the year 2011-2012 from University of Sharjah, UAE. In 2005, He was decorated with the Science Prize in Advanced Engineering Technology from the Academy of Scientific Research and technology, Higher Ministry of Education, Cairo, Egypt. From January 2010- until now, Prof. Mahmoud joined the Electrical and Computer Engineering Department at University of Sharjah and he is currently an assistant dean for research and graduate studies since Sept. 2016. In October 27, 2010, He is promoted to a professor of Electronics and Communications Engineering, Fayoum University, Egypt. Prof. Mahmoud was a visiting Professor at ULM University, Germany (Summer 2008) and (Summer 2009). From 2007-2010, Prof. Mahmoud served as acting Chairman of Electronics and Communications Engineering Department, Fayoum University, Egypt. He was also Associate Professor at the Electrical and Electronics Engineering Department, German University in Cairo, Egypt. In September 2005, Prof. Mahmoud is promoted to an Associate professor of Electronics and Communications Engineering, Cairo University, Egypt. From 1999-2005, he served as an Assistant Professor in Electronics and Communications Engineering, Cairo University, Egypt.

SOHAIB MAJZOUB completed his BE in Electrical Engineering, Computer Section at BAU 2000, and his ME degree from AUB, 2003 Lebanon. Then he worked for one year at the Processor Architecture Lab at the Swiss Federal Institute of Technology, Lausanne Switzerland. In 2010, he finished his PhD working at the System-on-Chip research Lab, University of British Columbia, Canada. He worked for two years as assistant professor at American University in Dubai, Dubai, UAE. He then joined King Saud University in 2012, KSA. In 2015, he joined University of Sharjah, UAE, as a faculty in the electrical engineering department. He was promoted to Associate Professor in June 2020. His research work cover areas in digital design, CAD algorithms, optimization using AI and ML. He is senior member IEEE, and member in the IEEE Computer Society, Solid State Society, and Circuits and Systems member.

Dr. Abir Jaafar Hussain is a professor of Image and Signal Processing at the Department of Electrical Engineering, University of Sharjah, UAE since 2021 and she is also a visiting professor at Liverpool John Moores University, UK in which she spent more than 22 years working at the Department of Computer Science. She completed her PhD study at The University of Manchester (UMIST), UK in 2000 with a thesis title Polynomial Neural Networks for Image and Signal Processing. She has published numerous referred research papers in conferences and Journal in the research areas of Neural Networks, Signal Prediction, Telecommunication Fraud Detection and Image Compression. She has worked with higher order and recurrent neural networks and their applications to e-health and medical image compression techniques. She has developed with her research students a number of recurrent neural network architectures. She is a PhD supervisor and an external examiner for research degrees including PhD and MPhil. She is one of the initiators and chairs of the Development in e-Systems Engineering (DeSE) conference series. She is a Senior member of the IEEE.