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A discharge-based pulse technique for probing the energy distribution of positive charges in gate dielectric

R. Gao, Z. Ji, *Member, IEEE*, J. F. Zhang, W. D. Zhang, S. F. Wan Muhamad Hatta, J. Niblock, P. Bachmayr, L. Stauffer, K. Wright and S. Greer

***Abstract*— Characterizing positive charges and its energy distribution in gate dielectric is useful for process qualification. A discharge-based technique is introduced to extract their energy distribution both within and beyond substrate band-gap. This work investigates the difficulties in its implementation on typical industrial parameter analyzer and provides solutions. For the first time, we demonstrate the technique's applicability to the advanced 22 nm fabrication process and its capability in evaluating the impact of different strains on the energy distribution. The test time is within several hours. This, together with its implementation on industrial parameter analyzer, makes it a useful tool in the semiconductor manufacturing foundries for process monitoring and optimization.**

Keywords*— *Energy distributions, energy profiles, positive charges, hole traps, negative bias temperature instability (NBTI).

I. Introduction

Negative Bias Temperature Instability (NBTI) has been identified as a major reliability issue for pMOS devices. It is well-known that both positive charges (PCs) formation within the gate dielectric and the generation of interface states contribute to the long-term degradation [1-4]. PCs shift important parameters, such as threshold voltage [5] and mobility [6], eventually shortening the transistor lifetime and causing circuit failure [7]. To simulate the impact on circuit performance, the energy distribution of PCs is required. Conventionally, the charge pumping (CP) technique [8-10] is a widely used method for probing PCs' energy distribution. However, it can only probe traps within the Si band gap. A modern pMOSFET typically operates with the Fermi-level at the interface below the top edge of the valence band, where the CP cannot probe. The Charge Injection and Sensing (CIS) technique proposed recently [11] requires no new trap generation and all the traps being charged and discharged repeatedly. However, these conditions cannot be met for PCs in pMOSFETs.

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R. Gao, Z. Ji, J. F. Zhang and W. Zhang are with the School of Engineering, John Moores University, Liverpool L3 3AF, U.K. (e-mail: z.ji@ljmu.ac.uk).

S. F. Wan Muhamad Hatta is with Department of Electrical Engineering, University of Malaya, Malaysia.

J. Niblock, P. Bachmayr, L. Stauffer, K. Wright and S. Greer are with Keithley, Cleveland, Ohio, 44139, USA.

An energy profiling technique is introduced, enabling probing the energy distribution of positive charges both within and beyond band gap, based on the customized test facilities [12]. In this work, we investigate the difficulties in implementing it on a typical industrial parameter analyzer, the Keithley's 4200-SCS analyser with 4225 pulse IV modules, and provide solutions. To demonstrate it as a robust tool for material and process optimization, the energy distributions of PCs are compared for processes with and without strains. It also provides the charge density for a given surface potential required by device modelling.

II. Devices

pMOSFETs with 22nm planar fabrication process are used in this work to demonstrate the applicability of the technique to advanced CMOS nodes. The dielectric stack of the samples is HfO2 with an Al_2O_3 cap layer. The gate is TiN. To demonstrate the capability of this technique in evaluating different processes and materials, two pMOSFETs fabricated with and without applying compressive strain in the channel are used for comparison. Unless specified, the channel length and width of the device used is 1 μm and 10 μm, respectively.

III. Distribution Extraction Technique

A. Principle and procedure for energy distribution extraction

The principle of the discharge-based technique [13] for positive charge (PC) energy distribution extraction is shown in Fig. 1.

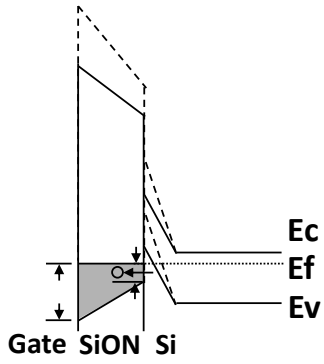

Fig 1: The energy diagram to show the principle for the new discharge-based technique

Firstly, a high negative bias was applied on a pMOSFET (i.e. the sample is with the n-type substrate) for PC formation. Then $|V_g|$ will be lowered by a small step, ΔV, to $|V_g\text{-}\Delta V|$. Some of the charged PC will fall below Fermi level, E_f, as marked by the grey shade in Fig.1. As a first order approximation [12, 14-16], below E_f, positive charges are assumed to be neutralized throughout the oxide, if a sufficient discharge time is given. When $V_{discharge}$ moves further towards positive for each step, ΔV, the energy level of positive charges is lowered against the substrate, bringing a new shaded region below E_f for discharging.

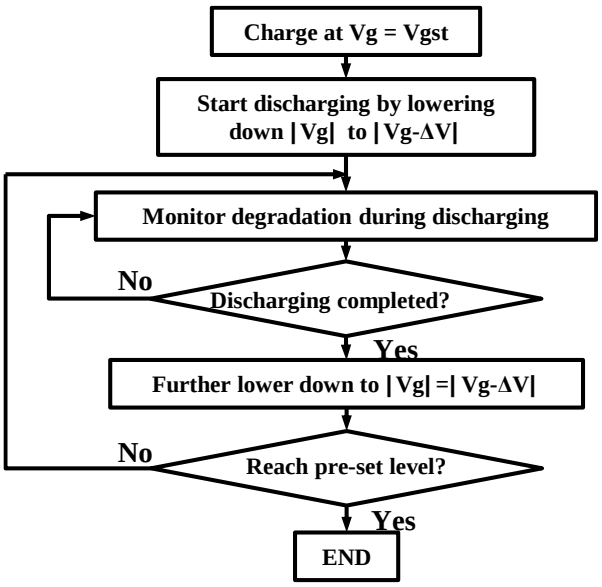

Fig 2 Flowchart of the test procedure.

By varying $V_{discharge}$ over a sufficiently large range, one can sweep E_f over a wide energy range at the interface, including the region beyond Ec and Ev of silicon.

The flowchart and the typical V_g waveforms are given in Fig. 2 and Fig. 3. The device was firstly stressed at V_g=V_{gst} for a pre-specified time. Fig. 3 shows that $|V_g|$ was then lowered to $|V_{discharge},1|$. The degradation, is evaluated by measuring current, I_d, under a constant sensing voltage, V_{g_m}. Its conversion to ΔV_t will be introduced in Section B. Degradation can be evaluated against discharge time until its change becomes negligible (e.g. ΔV_t<3mV). After completing discharge at $|V_{discharge},1|$, $|V_g|$ was further reduced to $|V_{discharge},2|$ and the same procedure is followed. To capture a wide energy range, Vdischarge eventually becomes more positive than the V_{g_m} for the sensing current level. The direction of pulse will be reversed then, as illustrated.

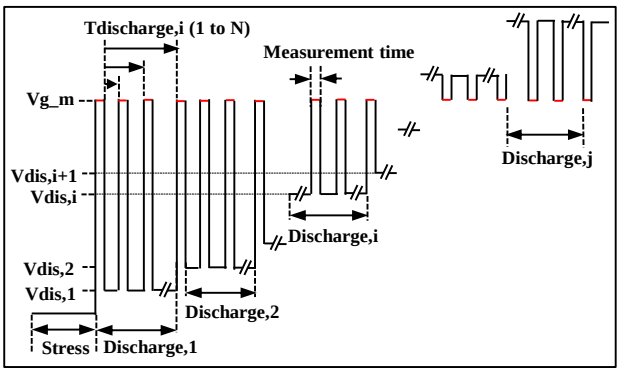

Fig 3 Vg waveforms for the proposed discharge-based energy profiling technique

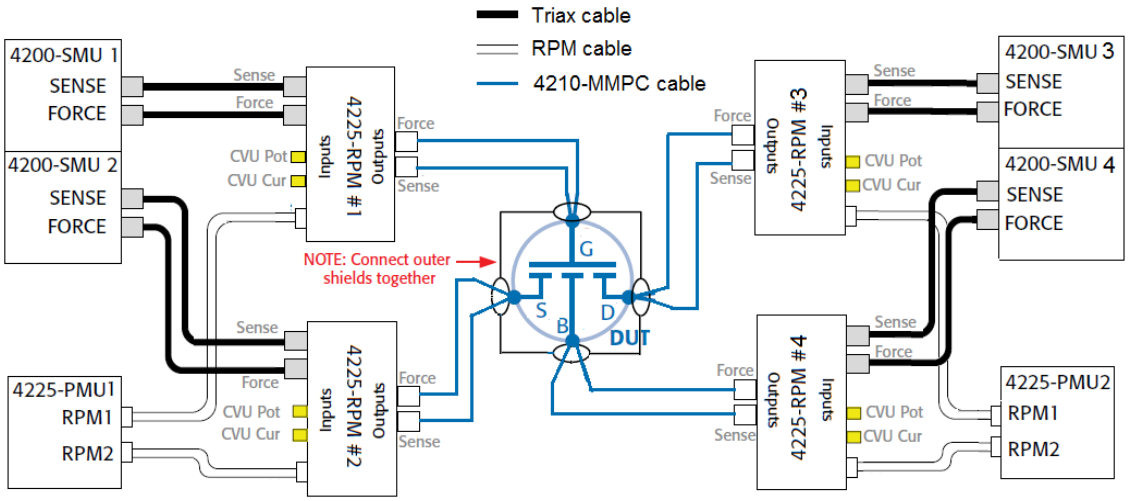

Fig 4: Experimental setup for the proposed technique. Two Keithley dual-channel 4225-PMUs are used for transient measurements. Four Keithley 4225-RPMs are used to reduce cable capacitance effect and to achieve accurate measurement below 100 nA.

B. Characterization methodology with commerical test equipment

To make the technique a useful tool for semiconductor foundries in material and process qualification, the technique should be implemented on commercial equipment. In this section, we use Keithley 4200-SCS system as an example, which is one of the mainstream semiconductor testing equipment available in the market. In order to monitor degradation during discharging period, two requirements must be met: 1) the measurement must be fast enough to assure there is no further discharging during the

measurement. 2) The Vth measured under different discharging levels must correspond to the same surface potential.

The first requirement can be met by using the fast measurement capability provided by 4200-SCS system with transient Current-Voltage measurement setup [17], as shown in Fig. 4. Two Keithley dual-channel 4225-PMUs were used for performing transient measurements and four Keithley 4225-RPMs were used to reduce cable capacitance effect and achieve accurate measurement below 100 nA within several μs. The impact of measurement speed is checked and shown in Fig. 5. After stressing the device for 1 ks, the degradation is monitored with different sweep speeds. When measurement speed is slow, clear recovery can be observed. However, when the measurement time is kept shorter than 20 μs [3, 12], the recovery becomes negligible.

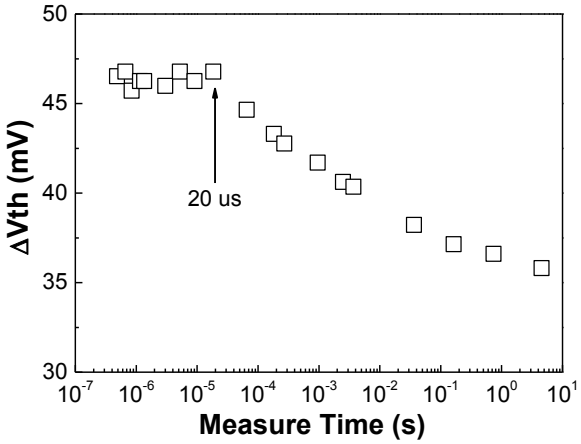

Fig 5 Measurement time effect on monitoring the degradation. When measurement time increases, the monitored degradation becomes smaller due to the well-known recovery. However, when the measurement time is kept shorter than 20 μs, the degradation is fully captured.

Conventionally, the second requirement is met by measuring the entire I_d~V_g and then extracting V_t by using either the constant current method [12, 18] or the max-gm extrapolation method [19]. This is supported by typical instruments for the standard Stress-Measure-Stress (SMS) sequence. However, if transient Current-Voltage measurement setup is applied, due to the limitation of maximum available data storage provided by the mainstream commercial equipment, only a limited number of I_d-V_g curves can be saved in the memory (at most 15 curves). To overcome this difficulty, we propose using a constant voltage method [20]: degradation is monitored by only measuring a single Id current under a certain sensing V_{g_m}. By measuring under a constant V_{g_m}, a change of positive charges in the gate dielectric will change the substrate surface potential, so that the positive charges are actually measured at different surface potential during charging or discharging process.

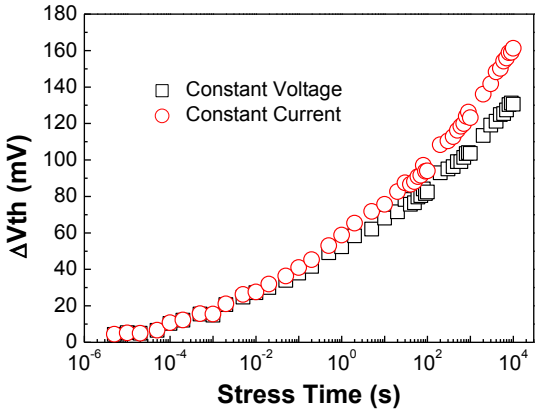

Fig 6 The impact of different sensing techniques on the degradation. The increase of ΔVth will reduce the surface potential if the constant sensing Vg is used and thus leads to the lower degradation when compared with sensing at the constant current level which is approximately at the same surface potential.

As can be seen in Fig. 6, if the degradation is small (<30mV), ΔVth from two methods (constant current v.s. constant voltage) are comparable. However, when ΔVth further increases, degradation from constant voltage method becomes lower than constant current method. This is because high ΔV_t lower the Fermi level if V_g is kept as a constant.

We propose a solution to enable the conversion between measured ΔI_d under V_{g_m} and ΔV_t sensed under the same surface potential. The device is firstly stressed under typical NBTI conditions. A series of full I_d-V_g curves were measured where both the ΔV_t from a constant current extrapolation and the $\Delta I_d/I_{d0}$ at a constant sensing V_{g_m} were extracted. Fig. 7 shows that the relation between them is independent of stress conditions and can be fitted by a cubic equation. Once this unique relation is established, it can be used to convert the $\Delta I_d/I_{d0}$ measured under a constant V_{g_m} with the procedure described in section A to ΔV_t.

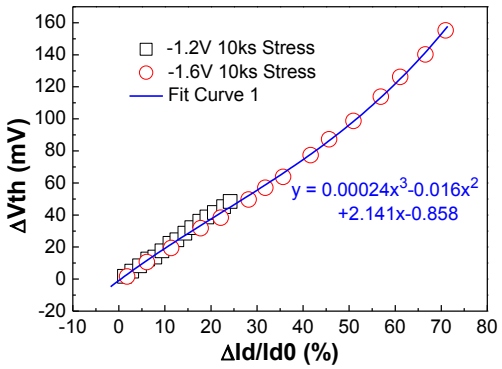

Fig 7 Experimental extracted unique relationship between ΔId/Id0 and ΔVth. Wherein, ΔId/Id0 is taken from the constant sensing Vg_m and the ΔVth is from constant current method. This relationship is independent of stress condition and can be used to perform the conversion.

To demonstrate the applicability of this technique to advanced CMOS nodes, it is applied to one pMOS

fabricated by a 22 nm process. The typical result is shown in Fig. 8. Under each $V_{discharge}$, the discharging process completes quickly after about 20s.

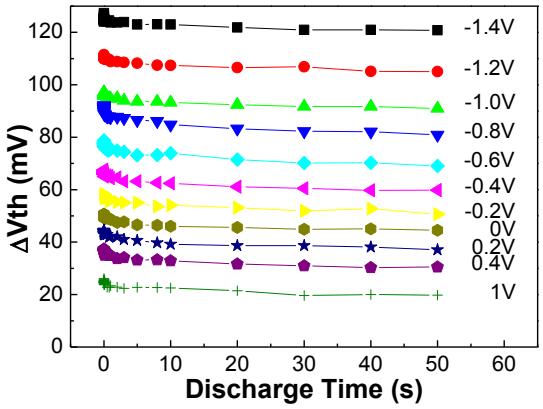

Fig 8: Typical results for discharging under different Vdischarge, The discharge time is the time under a given Vdischarge as marked in Fig. 3. The device is stressed at -1.6 V for 10 ks before the discharging.

C. *Extraction of energy distribution*

The proposed technique assumes ΔN_{ox} are the PCs above $E_f(V_{discharge})$. However, in principle, the PCs above $E_f(V_{discharge})$ also have small possibility to discharge. Its impact can be assessed by comparing the energy distribution extracted from different discharge time. The ΔV_t obtained from discharge time of 10s, 50s and 100s under each $V_{discharge}$ in Fig.8 is converted to effective charge density [21, 22], i.e. $\Delta N_{ox}=|\Delta V_t| \times C_{ox}/q$, and plotted against $V_{discharge}$ in Fig. 9(a). The extracted energy distribution overlap each other indicating the impact is negligible.

To obtain the energy distribution, $V_{discharge}$ must be converted to the energy level E_f relative to E_v, i.e. E_f-E_v. As shown by the inset of Fig. 9(c), E_f-E_v = $E_g/2$+ ΦB- ΦS. A theoretical $(E_f$-$E_v)$~V_g curve is first calculated using the CVC simulator [23]. By shifting the theoretical curve towards left until E_f-E_v=$E_g/2$-ΦB (i.e. the strong inversion condition) occurs at the measured V_t, the E_f-E_v versus Vdischarge were obtained and used to convert Vdischarge into E_f-E_v. Fig. 10(a) plots ΔN_{ox} against E_f-E_v. By differentiating ΔN_{ox} against E_f-E_v, the energy density, ΔD_{ox}, was obtained as shown in Fig. 10(b).

The impact of generated interface states, ΔN_{it}, has not been taken into account in the analysis above. ΔN_{it} can affect the analysis in two ways: 1) ΔN_{it} contributes to ΔN_{ox} measured at the sensing I_d; 2) ΔN_{it} causes a distortion of (E_f-E_v)~V_g curve. The effect of ΔN_{it} has been corrected and a comparison is made before and after correction in Fig.9(a) & Fig.10(a) [12]. The contribution of ΔN_{it} to ΔN_{ox} is modest and its impact on ΔN_{ox} is insignificant under our test conditions.

A closer observation of Fig. 10(a) indicates that PCs behave differently in different energy regions. When E_f-E_v is swept towards positive, ΔN_{ox} declines quickly initially, leading to a high energy density, ΔD_{ox}. The declining of ΔN_{ox} slows down around E_f-E_v=0.1 eV, giving a smaller ΔD_{ox}. Fig. 10 shows that this technique can probe the energy distribution of PCs both within and beyond the band gap for advanced CMOS nodes.

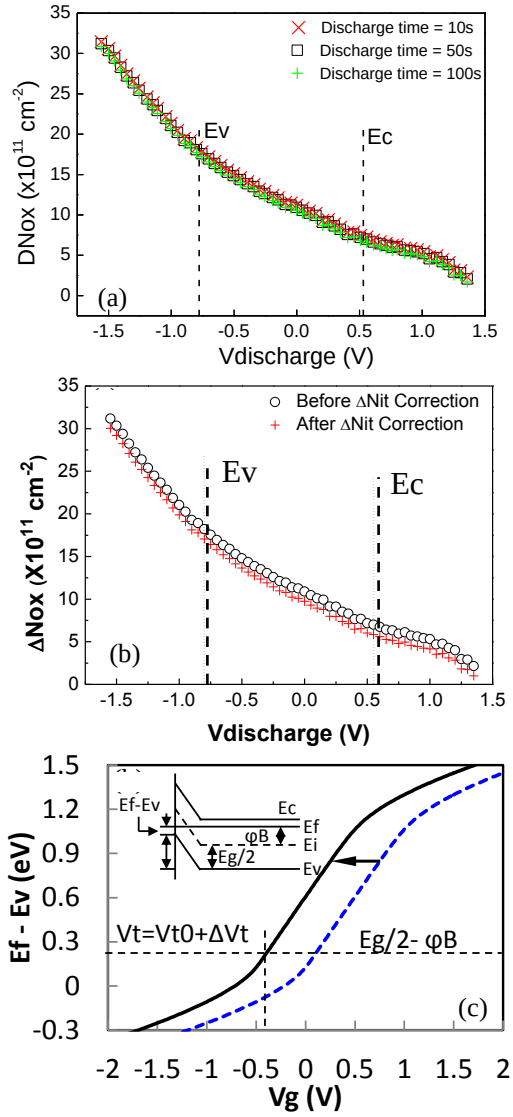

Fig 9: (a) shows the PCs after completing discharging at each Vdischarge, i.e. ΔNox, converted from ΔVt at different discharge time. (b) shows the comparison before and after Nit correction. (c) shows the conversion between Ef-Ev and Vdischarge. The dashed curve is the theoretical (Ef-Ev)~Vg, calculated from the CVC simulator**.** By aligning Ef-Ev=Eg/2-ΦB to the threshold voltage of stressed device, the solid line is obtained with which Ef-Ev can be found for a given Vg=Vdischarge. The inset of (c) shows the relationship between Ef-Ev and surface potential, Φs and, ΦB.

IV MATERIAL AND PROCESS EVALUATION WITH DEFECT ENERGY DISTRIBUTION

The ever evolving advanced sub-micron technologies result in the complex and varying materials and processes for the gate stacks. This energy probing technique can evaluate the impact of different fabrication processes on PCs distribution. As an example, the impact of strain on the degradation and PC energy distribution is studied here. Two

pMOSFETs are used, one without and the other with strain along the channel direction.

The typical NBTI results of these two samples are shown in Figure 11(a). The degradation is compared under the same stress field. The result shows that strain enhances the device degradation, agreeing with the literature [24]**.** In order to find out where this enhancement comes from, the developed energy profiling technique is applied and the effective charge density, ΔN_{ox} and its corresponding energy density, ΔD_{ox}, against E_f-E_v is shown in Fig. 11(b) and (c) respectively. Clearly, the PCs can be separated into two regions. Region I is below E_v where E_f-E_v is negative. ΔN_{ox} against E_f-E_v are in parallel, leading to the same energy density of the PCs in this region. However, for Region II when E_f-E_v is positive (i.e. above E_v), ΔN_{ox} and ΔD_{ox} are larger for the strained pMOSFET. The substantial strain-enhanced aging in Figs. 11(a) & (b) originates from PCs above E_v, therefore. Early works [25, 26] reported that the PCs are from as-grown hole traps below E_v and from the generated defects above E_v. This work supports this framework by showing, for the first time, that the as-grown hole traps are insensitive to strain, whilst the strain enhances trap generation.

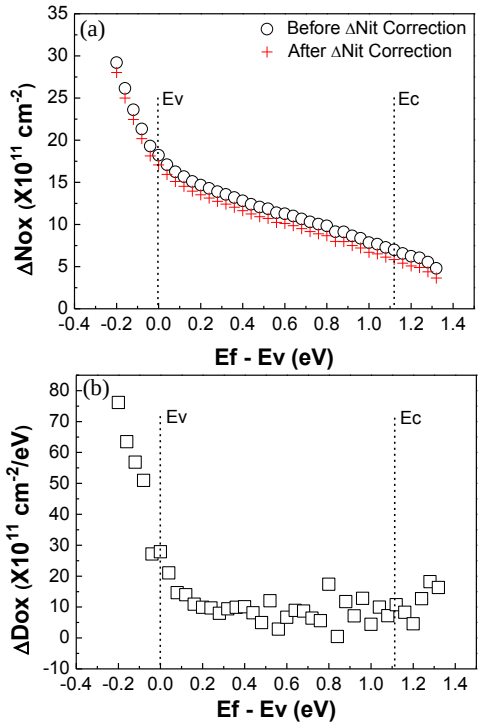

Fig 10: (a) The ΔNox is plotted against Ef-Ev. The symbol '+' denotes the data after ΔNit contribution is corrected. The ΔDox in (b) is the energy density of PCs, obtained by differentiating the data in (a): To extract ΔDox at Ef(i), the differentiation is calculated by using two neighboring points i+1 and i-1 through the equation ΔDox(i) = (ΔNox(Ef(i+1)-Ev) - ΔNox(Ef(i-1)-Ev))/(Ef(i+1)-Ef(i-1)).

IV. Conclusion

Discharge-based pulse technique for probing the energy distribution of positive charges in the gate dielectric is developed based on a typical industrial parameter analyser, after finding a solution to overcome the difficulties. Its applicability to the advanced CMOS nodes has been demonstrated. It was then used to study the impact of strain on the NBTI aging. For the first time, we report that the strain-enhanced aging originates from the generated defects above the Si E_v, whilst the as-grown hole traps below E_v are not affected by the strain. The test takes several hours, acceptable for a typical foundry. This makes it a useful tool for process monitoring and optimization. The technique also allows evaluation of effective PCs for a given surface potential, one key information needed for device and circuit modelling.

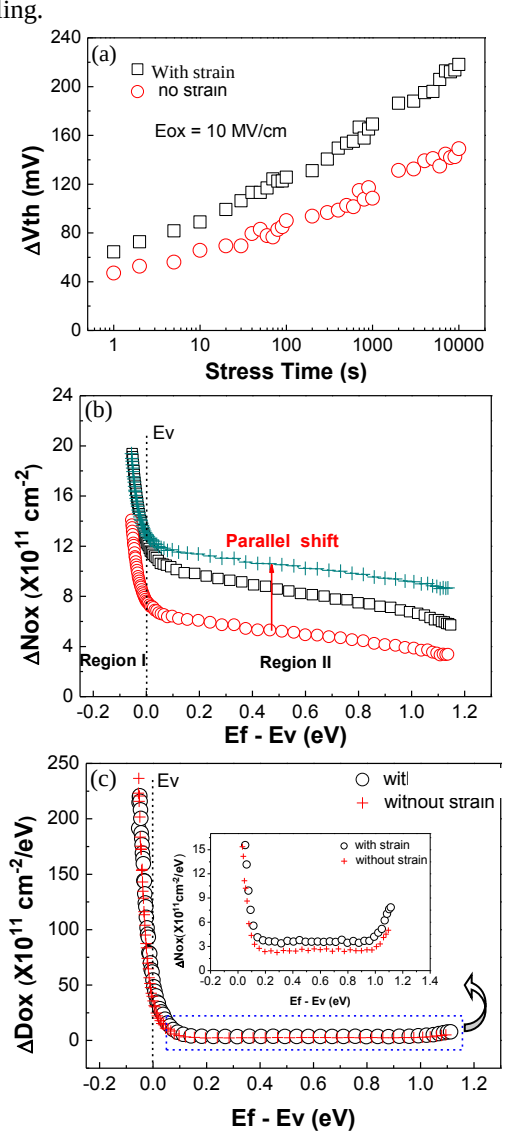

Fig. 11 (a) Typical NBTI stress test on the unstrained and strained pMOSFET. The same electric field is applied during the stress which is 10 MV/cm. (b) PCs energy profiling comparison for the two devices. The ΔNox is plotted against Ef-Ev, which is converted from Vdischarge by applying the proposed procedure explained in Fig. 9(b). (c) The PC energy density, ΔDox, is plotted against Ef-Ev.

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