An investigation on border traps in III-V MOSFETs with an $In_{0.53}Ga_{0.47}As$ channel

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***Abstract*— Continuing CMOS performance scaling requires developing MOSFETs of high-mobility semiconductors and InGaAs is a strong candidate for n-channel. InGaAs MOSFETs, however, suffer from high densities of border traps, and their origin and impact on device characteristic are poorly understood at present. In this work, the border traps in nMOSFETs with an $In_{0.53}Ga_{0.47}As$ channel and Al_2O_3 gate oxide are investigated using the discharging-based energy profiling technique. By analyzing the trap energy distributions after charging under different gate biases, two types of border traps together with their energy distributions are identified. Their different dependences on temperature and charging time support that they have different physical origin. The impact of channel thickness on them is also discussed. Identifying and understanding these different types of border traps can assist in future process optimization. Moreover, border trap study can yield crucial information for long-term reliability modelling and device time-to-failure projection.**

***Index Terms*—Border trap, III-V, InGaAs, Quantum well, characterization, mobility, reliability.**

I. INTRODUCTION

International Technology Roadmap for Semiconductors (ITRS) predicts a power supply of 0.72V will be needed for transistors in high performance logic applications in 2018 [1]. To address this, attention is turning to the use of high mobility channel materials such as InGaAs and Ge for n- and p-MOSFETs, respectively. The development of InGaAs devices has made encouraging progresses in recent years: high intrinsic electron mobility of 3000 $cm^2/V{\cdot}s$ has been demonstrated by several groups [2, 3]. With Al_2O_3 as gate oxide, a low interface state density (e.g. $2x10^{11}$ $cm^{-2}eV^{-1}$ [4]) and a subthreshold swing of 75mV/dec [2] were obtained. However, intolerable number of border traps are found in the oxide, resulting in I-V hysteresis and C-V frequency dispersion [5]. These border traps further cause severe Positive Bias Temperature Instability (PBTI) issue in the long term, shorten the devices' lifetime to an unacceptable level, and therefore impede the practical use of such devices [6] at the current status.

Conventionally, border traps are investigated using Multi-Frequency Charge Pumping (CP) technique [7]. Unlike bulk-Si FETs, devices with InGaAs channel are usually grown on insulating substrate and thus only have three terminals, making the CP impossible to be applied. To overcome this difficulty, a number of drain-current-based methods are proposed, such as those based on noise [8-10] and pulsed Id~Vg measurements [11]. The noise-related techniques, such as TDDS method [10], extract trap information from the steps of drain current due to individual defects' detrapping [8]. The pulsed Id~Vg method investigates the drain current response to gate pulses. The ac-transconductance (AC-gm) method [12] extracts the traps' energy and spatial location from the frequency dependence of transconductance, which is attributed to charge trapping as modulated by an ac gate voltage. The Trap Spectroscopy by Charge Injection and Sensing (TSCIS) technique [13] has been proposed to extract the energy distribution of border traps based on charging under the assumption that the charging process takes place through elastic tunneling, which does not apply to III-V devices, as we will show in this paper.

In this work, the border traps will be investigated using our recently proposed discharging-based energy profile technique [14]. By analyzing the trap energy distribution after charging at different Vg levels, two different types of border traps are identified. They have dramatic different dependences on the charging time and temperature, strongly supporting that they are of different origins.

The paper is organized as follows: in Section II, the test samples as well as the details of test procedure will be introduced. In Section III, the technique for energy distribution extraction is firstly explained. It is then used to analyze the border traps. Two different types of traps are clearly separated. To further justify their separation, their charging time and temperature dependences are investigated. The channel thickness dependence is also discussed by the end of this Section. Their potential impact on the circuit operation is briefly discussed in Section IV. Finally, Section V concludes this paper.

II. DEVICES AND EXPERIMENTAL DETAILS

A. Devices

The nMOFETs with n-type channel are used in this work. The devices received a $(NH_4)_2S$ treatment prior to the gate oxide deposition. The gate oxide is a 10 nm ALD Al_2O_3 with a TMA initial surface cleaning. ALD Al_2O_3 on InGaAs using TMA as the precursor have been reported to effectively reduce As and Ga oxides through an interfacial "self-cleaning" reaction

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process and can yield a good quality interface [15]. Forming gas anneal at 370 ºC was performed on the finished devices. The detailed fabrication process flow, the cross section of the device and the TEM micrograph of the gate stack can be found in [2].

B. Experimental procedure

The discharging-based energy profiling technique [14] is used in this work to investigate border traps. The test sequence is shown in **Fig.1(a)**. V_g is firstly raised to a certain charging level $V_{g,ch}$ for a pre-specified time to fill the traps. V_g was then lowered to $V_{g,disch1}$ and the degradation is monitored against discharge time until its change becomes negligible (e.g. <2mV). Once discharge under $V_{g,disch1}$ completed, V_g was further reduced to $V_{g,disch2}$ and the same procedure is followed. Full I_d-V_g measurement is taken at the pulse edge with a speed of 3μs, as marked as thick red lines in **Fig.1(a)** [16, 17]. V_{th} is evaluated using constant current method with the level around fresh $V_{th,0}$ [18]. When $V_{g,disch}$ is higher than $V_{th,0}$, I_d-V_g sweeps negatively from 'on' towards 'off', i.e. from $V_{g,disch}$ to $V_{th,0}$ - 0.5V. However, to capture the trap energy location both within and beyond the InGaAs band gap, $V_{g,disch}$ eventually becomes lower than $V_{th,0}$ and therefore the direction of pulse needs be reversed and I_d-V_g will sweep positively from 'off' towards 'on' , i.e. from $V_{g,disch}$ to Vth0+0.5V.

A typical measurement result is shown in **Fig.1(b)**. After charging under $V_{g,ch}$ for 1ks, Vg is then lower down to each $V_{g,disch}$ level for 200s. Under each $V_{g,disch}$, the discharging reaches saturation quickly after several seconds and will become almost a flat line up to 200s. In order to check the impact of discharge time, the device was first charged under $V_{g,ch}$ for 1ks, and then discharged until 10ks under each $V_{g,disch}$. **Fig.1(c)** shows that further increasing the discharging time to 10ks will only introduce an extra discharging of 5~6 mV. This indicates that the trap discharging at a given discharge voltage is dominated by its energy level. In the rest of this work, the discharge time of 1s is used for each $V_{g,disch}$.

III. BORDER TRAPS IN III-V DEVICES

A. Energy distribution extraction

To obtain the trap energy distribution, ΔVth after completing discharging under each $V_{g,disch}$ (the last point of each trace in **Fig.1(b)**) is firstly converted to the effective charge density, ΔN_{ot}, which is the equivalent charge density by assuming all charges being at the interface. It is calculated based on the charge sheet model with the equation: $\Delta N_{ot} = (C_{ox} * \Delta V_{th})/q$. Where q is the elementary charge and C_{ox} is oxide capacitance. The typical ΔN_{ot} is plotted against $V_{g,disch}$ and shown in **Fig.2(a)**. The next step is to convert V_g=$V_{g,disch}$ to the corresponding energy level denoted by E_f with respect to Ec of the InGaAs at the surface, $E_f - E_c$, as illustrated in **Fig.2(b)**. This requires the relationship between V_g and E_f. This relationship can be obtained by simulating with 1D Schrödinger-Poisson solver [19]. The result is given in **Fig.2(c)**. It should be noted that the horizontal axis of **Fig.2(c)** is $V_g - V_{th}$ and $V_{th} = V_{th,0} + V_{th}$ varies during discharging. **Fig.2(d)** shows the extracted trap energy distribution by plotting the ΔN_{ot} against E_f-E_c. It is worth noting that the contribution of the interface states will be the same under all the $V_{g,disch}$ since the Fermi level at sensing condition is kept constant. Therefore, if new interface states are generated, they would induce only a parallel upshift of the extracted N_{ot} distribution, as observed in Si devices [14, 20]. However, **Fig.2(d)** shows that complete discharging can be achieved (i.e., ΔV_{th}=0V at the end of the discharging sequences), indicating that interface state generation is negligible during the test and that the extracted energy distribution represents solely the border traps.

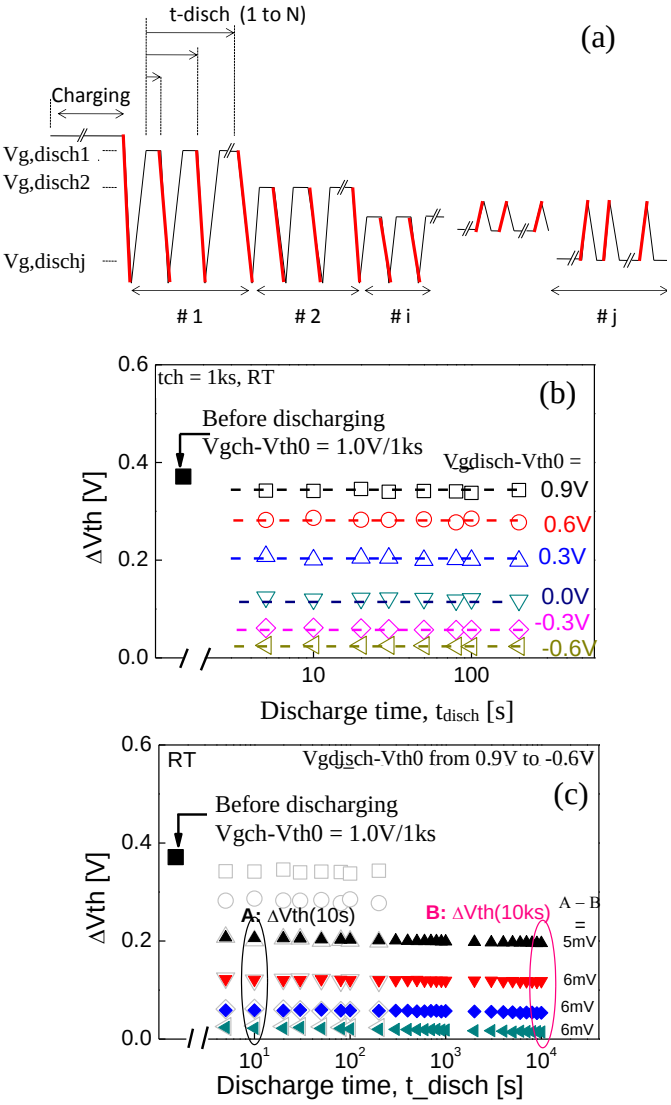

Fig. 1 (a) V_g waveform used for the test. Full I_d-V_g measurement is taken at the edge with a speed of 3μs (marked in thick red lines). (b) Typical results for discharging under different $V_{g,disch}$. The device was charged at $V_{g,ch} - V_{th,0}$ = 1.0 V under room temperature for 1ks and discharged for 200s under each $V_{g,disch}$. The total threshold voltage shift before discharge is given by the symbol "■". The dash lines are guides to the eye. (c) The discharging traces with discharging time of 10ks after charging at $V_{g,ch} - V_{th,0}$ = 1.0 V for 1ks. The empty grey points represented the same discharging traces shown in Fig.1(b).

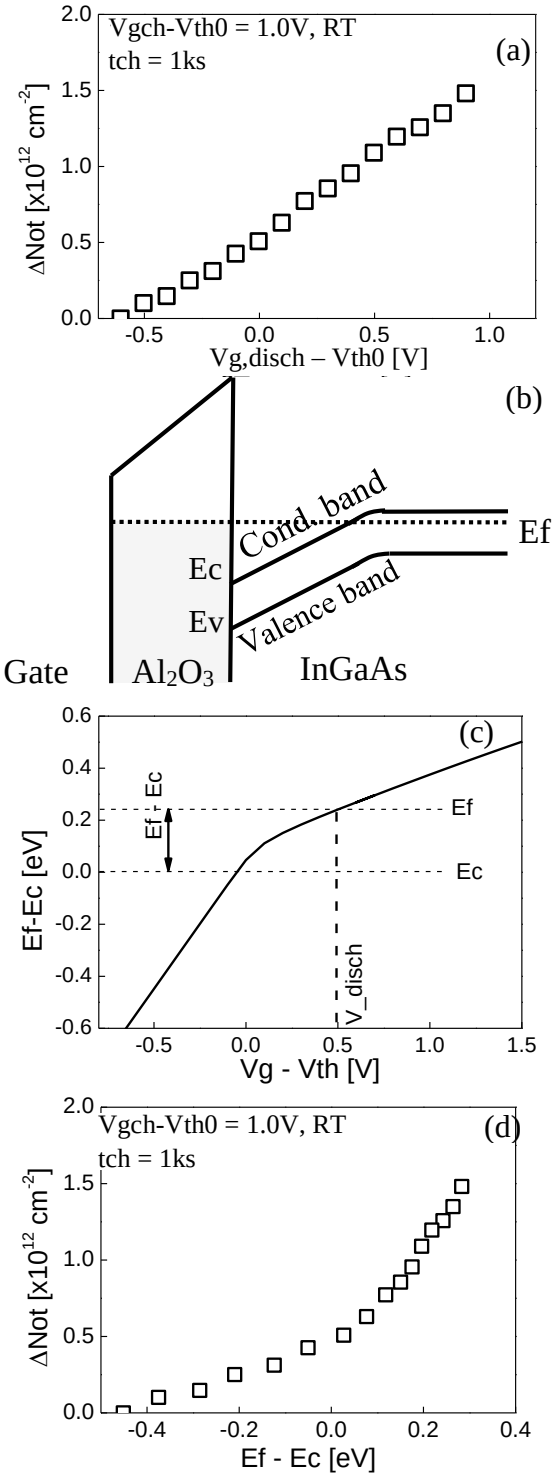

Fig. 2 Energy profiling extraction ΔN_{ot} in (a) is the charged electron traps after completing discharging at each $V_{g,disch}$. The data is taken from the last point of each trace in Fig.1(b). (b) Illustration of the relationship between E_f-E_c and the energy level of the charged electron traps. E_c is the conduction band of InGaAs at the interface and the shaded area denotes the charged electron traps. (c) The E_f-E_v against V_g−V_{th} from 1D Poisson simulator [19] for converting each $V_{g,disch}$ to an E_f-E_v. (d) The extracted energy distribution of the charged electron traps after charging under $V_{g,ch}$-$V_{th,0}$=1.0V for 1ks.

B. Separation of two types of border traps

Following the procedure described in **Fig.2**, the trap energy distributions are extracted under different $V_{g,ch}$. The result is shown in **Fig.3(b)** and the distributions for several high and low $V_{g,ch}$ levels are zoomed-in in **Figs.3(a) and (c)**, respectively. For filling the Type-A under relatively low $V_{g,ch}$, ΔN_{ot} is found to increase with surface potential and their relation is independent of $V_{g,ch}$, as shown in **Fig.3(c)**. There are two possible explanations: 1) More traps at higher energy become accessible under higher surface potential; and/or 2) more traps deeper into the dielectric become accessible [21]. These traps have the same energy level for their ground and charged states, as illustrated in **Fig.4(a)**. In the rest of the work, this type of trap will be referred to as the **Type-A traps**.

However, as shown in **Fig.3(b),** when $V_{g,ch}$ further increases, it is found that the trap distribution starts to deviate. With higher $V_{g,ch}$, more charged traps can be observed under the same E_f-E_c. As enlarged in **Fig.3(a)**, this difference is a constant when E_f-E_c is close to the charging level and then gradually diminishes when Ef approaches to E_c. This cannot be explained by the Type-A traps which predict the same ΔN_{ot} under the same E_f-E_c regardless of $V_{g,ch}$. Therefore, there must exist another type of trap.

It is known that there exists traps which can change their energy level after capturing an electron due to the change of their orbital configurations [22]. In the rest of the work, these traps are called as the **Type-B traps**. The schematic energy diagram is shown in **Fig.4(b)**. Once these traps are charged, their energy levels will be shifted downwards and therefore they become too low to be discharged when E_f is close to the charging level. These traps start to discharge when E_f further lowers down. Once they are fully discharged, the discharging traps overlap each other, as shown in **Fig.3(b)**. According to *ab-initio* calculations [22], Oxygen vacancies with various configurations can exist in Al_2O_3 wherein the V_o^- configuration has an energy level above the InGaAs conduction band and therefore it could be potentially act as an electron trap. For capturing an electron, the defect will reconfigure to its charged state V_o^{2-} which has an energy level lower than V_o^-, i.e. the trap becomes deeper, after trapping. This behavior expected from theoretical calculations is in line with our experimental observations for Type-B traps: we therefore conclude that oxygen vacancies in Al_2O_3 are a possible candidate for the Type-B defects. We note that since Al_2O_3 is amorphous, it is reasonable to assume that the energy levels of each individual oxide defect in the V_o^- and V_o^{2-} configurations are distributed around the theoretically predicted levels. Notably, however, the *ab-initio* calculations predict an energy gap between V_o^- and V_o^{2-} [22]. As a result, it is expected that all the charged Type-B traps will not discharge when E_f is close to their charging levels. This explains the parallel shift of two consecutive discharging trace as observed in **Fig.3(a)** and therefore the observed discharging in this region is to be ascribed to Type-A traps only.

One simple method can be applied to separate these two types of traps by exploiting the parallel region of the distributions extracted for two consecutive $V_{g,ch}$ levels, as illustrated in **Fig. 5(a)**: starting with the distribution trace at the lowest $V_{g,ch}$ in which only Type-A traps are involved, the discharging trace under the next charging level, $V_{g,ch}+\Delta V_{g,ch}$, is shifted down to align these two curves within the region of 0.1eV from the charging level. Following this procedure up to the highest $V_{g,ch}$, the distribution of Type-A traps can be extracted. Type-B traps can be extracted by subtracting Type-

A traps from the total. The extracted Type-A and Type-B traps are shown in **Fig.5(b)** and **Fig.6**.

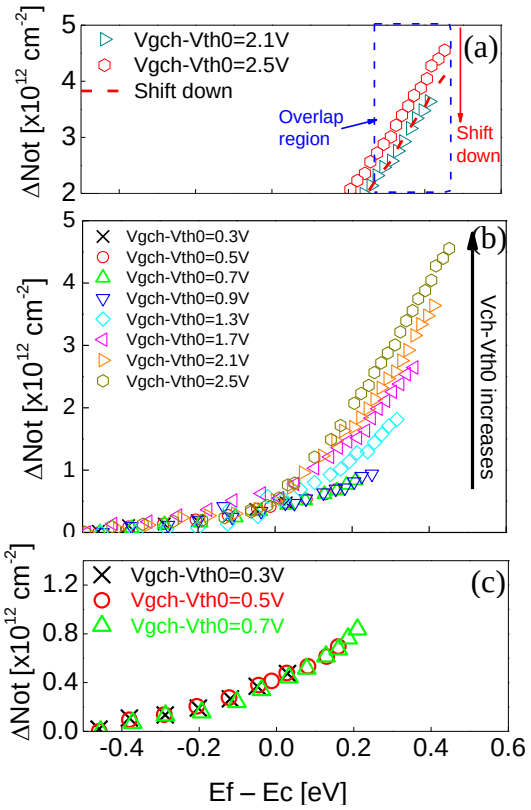

Fig. 3 Trap energy distribution after charging under different levels, $V_{g,ch}$ for 1000sec at room temperature. The distribution traces under all $V_{g,ch}$ are shown in (b). The distribution traces under two highest $V_{g,disch}$ and three lowest $V_{g,disch}$ are enlarged and shown in (a) and (c) respectively.

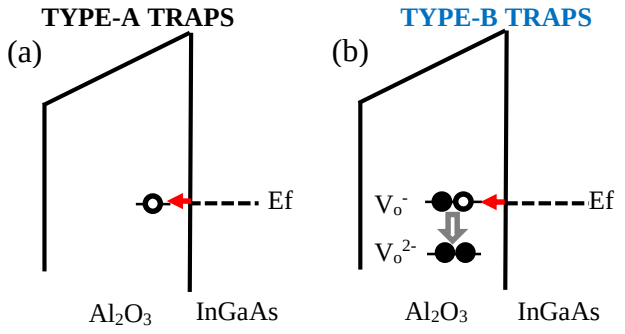

Fig. 4 Illustration of charging Type-A (a) and Type-B (b) traps. After charging at Ef, Type-A traps will not change the energy level while Type-B traps drop from the ground states to the charged states at lower energy level. Simulation results [22] show that the oxygen vacancy may be the candidate for Type-B traps in which V_o^- and V_o^{2-} for the ground states and the charged states respectively. For V_o^- configuration (●○), it can act as an electron trap to capture one electron from the substrate and change to V_o^{2-} configuration (●●).

It is worth noting that the extracted distribution of Type-B traps shown in **Fig.6(b)** represents the charged state of such type of traps (i.e., switching traps) because the discharging traces used for the extraction are recorded after charging under certain $V_{g,ch}$ (as illustrated in **Fig.6(a)**). More traps are switched when higher $V_{g,ch}$ is applied and these switched traps are mainly above the Ec of InGaAs. Although the ground state of the Type-B traps are electrically neutral, their energy distribution can also be obtained. Under each $V_{g,ch}$, Type-B traps with their ground states below $E(V_{g,ch})$ can be charged: i.e. $E(V_{g,ch})$ is the energy level for the ground state. The total Type-B traps, ΔN_{ot}, charged under this $E(V_{g,ch})$ can be estimated from the flat region of the relevant discharging trace shown in **Fig.6(b)**. By plotting ΔN_{ot} against $E(V_{g,ch})$, the energy distribution for the ground state of the Type-B traps is obtained, as shown in **Fig.7(a)**. Type-A traps are also shown for comparison. The result shows that Type-A traps spread within and beyond the band gap of InGaAs, while Type-B traps are mainly beyond the band gap. By differentiating ΔN_{ot} against E_f-E_c, the trap density per eV, ΔD_{ot}, is obtained in **Fig.7(b)**. Type-A traps have a peak around 0.4 eV above Ec of InGaAs, while Type-B traps increase monotonically with higher ground levels.

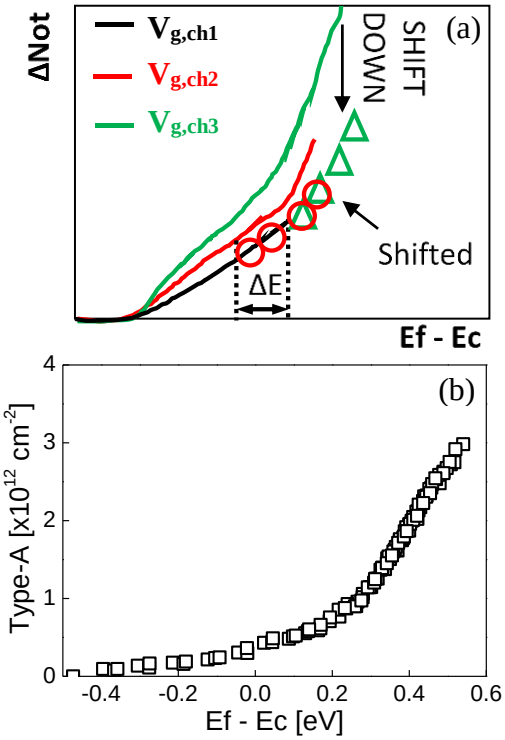

Fig. 5 (a) Illustration for Type-A traps extraction. The Solid lines denote the total trap distribution under different Vg_ch level. Aligning two distributions between $V_{g,ch1}$ and $V_{g,ch2}$ to assure the region within ΔE away from $V_{g,ch1}$ overlap each other ('**O**'), Type-A traps in the energy range between $V_{g,ch1}$ and $V_{g,ch2}$ can be extracted. By following the procedure, the entire Type-A traps distribution can be obtained. (b) The Type-A traps extracted from the real measured data shown in Fig.3(b).

C. Impact of charging time

The charging time dependence of Type-A and Type–B traps are shown in **Fig. 8**. The number of charged Type-A traps does not increase for longer charging time, indicating that all the pre-existing Type-A traps can be quickly filled to saturation. On the contrary, the number of charged Type-B traps increases with charging time. Compared with higher E_f-E_c, the Type-B traps under low E_f-E_c increases relatively slow. One speculation is because the channel electrons closer to Ec of the InGaAs are relatively less and therefore Type-B traps in this region take longer time to get charged.

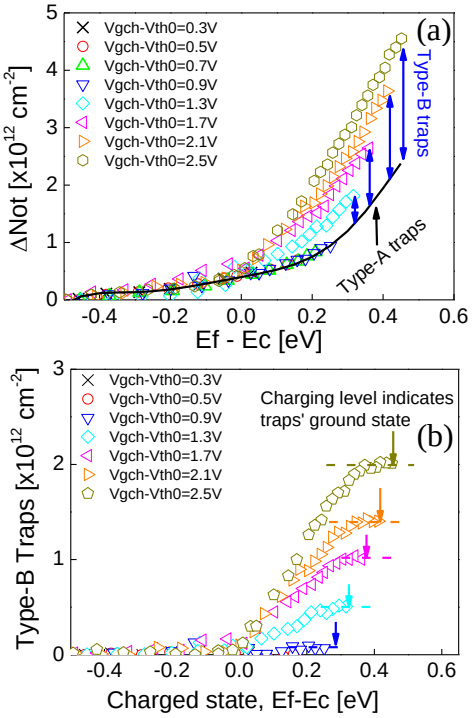

Fig. 6 (a) Procedure for extracting Type-B traps. Type-B traps can be extracted by subtracting Type-A traps from the total traps for each $V_{g,ch}$ (b) Type-B defects extracted from the same set of data shown in Fig.3(b).

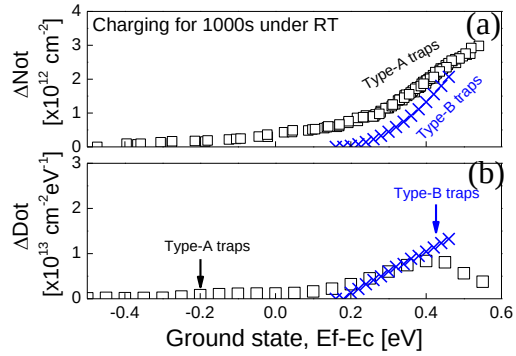

Fig. 7 (a) Energy distribution of Type-A traps and the ground states of the Type-B traps. For Type-B traps, each point is taken from the highest trapping level of distribution trace for each $V_{g,ch}$. ΔD_{ot} in (b) is the trap density by differentiating the data in (a). 5nm channel thickness are used.

D.Impact of Temperature

The impact of temperature is also checked in this section. The Type-A traps will not switch their energy levels after charging and it is expected that their charging should be independent of the temperature [23]. On the contrary, Type-B traps can switch their energy levels after charging. If their trapping process can be described by the lattice relaxation multi-phonon emission (LRME) model, it is expected that their capture times reduce with higher temperature and therefore a strong temperature dependence in trapping can be observed [24]. Following the same extraction method, the energy distribution for the Type-A and Type-B traps are obtained under three temperatures in **Fig. 9(a) and (b)** respectively. As expected, the energy distribution for Type-A traps is independent of temperature in **Fig.9(a)**. The distributions of the Type-B traps in **Fig.9(b)** have a strong temperature dependence: for a fixed charging time, more traps are charged at higher temperatures due to the phonon-assisted charging process. The different dependence on temperature and charging time supports that there exists two different types of traps with different physical origin.

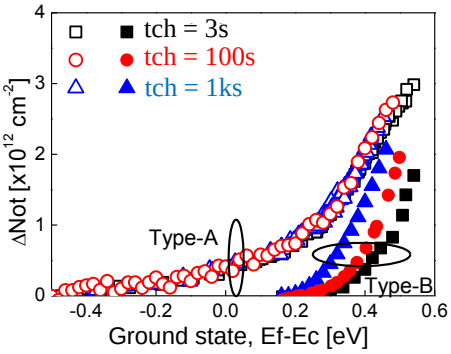

Fig. 8 Charging time dependence of the Type-A and Type-B traps at room temperature. Devices with channel thickness of 5nm are used.

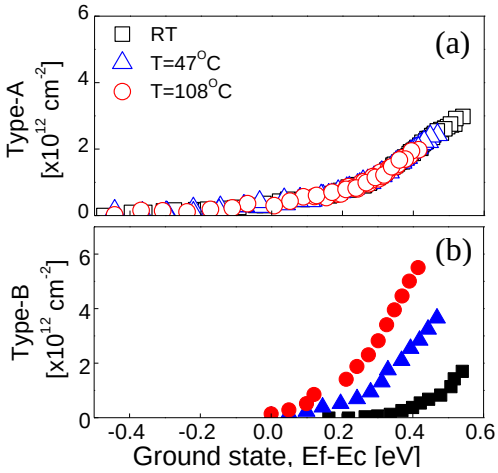

Fig. 9 Temperature dependence of the Type-A (a) and Type-B (b) traps after charging for 3s. Devices with channel thickness of 5nm are used.

E. Impact of Channel thickness

The impact of channel thickness on these two types of traps is given in **Fig.10**. Both traps are sensitive to the InGaAs channel thickness. More charged traps are observed for thinner channel layer. This is unlikely caused by a poor interface for a thinner channel device, since similar sub-threshold swing values are found [2] for different channel thicknesses. The following reasons are likely to cause this thickness dependence: 1) the channel carriers get closer to the interface for thinner channels and the local electrical field can increase leading to higher trapping. 2) The quantization effect can be enhanced in the thinner channels, as corroborated by device simulations [2]. Enhanced quantization can populate higher energy levels, making the channel electrons energetically favorable for charging traps. This leads to larger PBTI in thinner channel [25] and might jeopardize the use of thin channels, although thinner channels could yield improved subthreshold swing [26] and reduced off-current for better L_G-scalability [27]. III-V material has the potential to meet the high driving current/low Vdd requirement in future. For successful introduction of InGaAs devices in real production, a stable high-k gate stacks is equally important as optimizing transport properties of III-V channels, warranting further research and development.

Both Type-A and Type-B traps must be suppressed. One potential solution is to reduce defect density through process optimization [28]. For example, it has been reported that the border traps can be supressed through various passivation methods, such as $(NH_4)_2S$ passivation and forming gas annealing [29]. Another possible solution is to use a different high-k layer which have a much narrower energy distribution of defect levels centred at shallower energy level in order to provide sufficient carrier-defect energy decoupling [25].

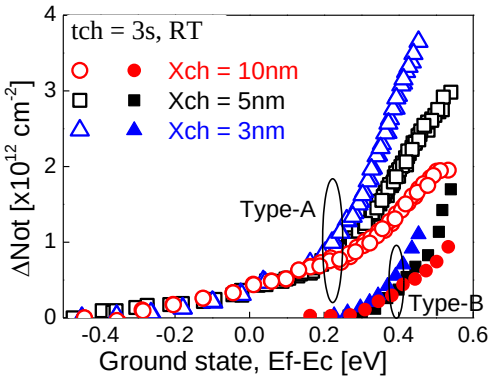

Fig. 10 Channel thickness dependence of Type-A and Type-B traps after charging for 3s under room temperature.

IV. Conclusions

We investigated the border traps in InGaAs nMOSFETs with Al_2O_3 gate oxide and different channel thicknesses by using the discharging-based energy profiling technique. By analyzing the extracted trap energy distribution, two different types of border traps are identified. The Type-A traps do not change their energy level after charging, while Type-B traps will switch to a lower energy level after charging. Their different dependences on charging time and temperature strongly suggests that they have different physical origins. The number of charged traps of both types is found to increase when InGaAs channel becomes thinner. This is due to the enhanced quantization effect increasing the channel Fermi level and therefore making more defect levels thermodynamically favorable for trapping channel electrons. This effect jeopardizes the use of thin channels for improved L_G scalability. Distinguishing these two different types of border traps is useful for process optimization.

V. References

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