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Perspective: Zinc-Tin Oxide Based Memristors for Sustainable and Flexible In-Memory Computing Edge Devices

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As the Internet of things (IOT) industry continues to grow with an ever-increasing number of connected devices, the need for processing large amounts of data in a fast and energy-efficient way becomes an even more pressing issue. Alternative computation devices such as resistive random access memories (RRAM), or memristors, started taking centre stage as prime candidates to tackle this issue due to their in-memory computation capabilities. Amorphous oxide semiconductors (AOSs), more specifically eco-friendly zinc-tin oxide (ZTO), show great promise as a memristive active material for flexible and sustainable applications due to its low required fabrication temperature, amorphous structure, low-cost, and critical-raw-material-free composition. In this perspective article, the research progress on ZTO-based memristors is reviewed in terms of device structure and material compositions. The effects on the electrical performance of the devices are studied. Additionally, neuromorphic and optoelectronic capabilities are analyzed with the objective of finding the best approaches toward implementing these devices in novel computing paradigms.

1. Introduction

Over the last 50 years, Moore´s law has proven to be the guideline for electronics development. However, limits to further miniaturization, thermal budget and increased manufacturing costs have led to a halt in performance growth. [1] Furthermore, the last decade has introduced a big change in computational focus, moving from computing intensive tasks to data intensive ones (**Figure 1**). Considering that the memory hierarchy employed on today's computer systems has been developed and optimized taking into account the needs that existed at the time, these architectures are no longer able to satisfy today's demands. Thus, a shift in computing paradigms is now taking place. Nowadays, the typical computer structure follows the von-Neumann model, meaning that the processing and memory units exist in separate blocks. This separation becomes a major setback when tasks requiring the processing of large amounts of data are targeted, as the movement of data between these blocks poses a series of problems: non-negligible latency, limited data transfer rates and high energy consumption. As an example, the movement of data between the processing core and an off-chip memory cell of a von-Neumann system requires ≈100 times the energy of a floating point operation.[2] Taking graphical processing unit (GPU) operations into perspective, in order to perform a double precision addition on a GPU fabricated under a 22 nm node, the energy spent in data movement is 500 times the energy spent on the actual addition operation[3] Considering the overall system energy consumption, a study running scientific software applications as computing benchmarks has shown that up to 40% of the overall energy is spent on data movement and up to 36% is wasted on stalled cycles.[4]

In order to avoid this problem commonly referred to as the von-Neumann bottleneck, there has been an attempt to bring the processing and memory units closer to each other, leading to the study of system architectures and devices that allow for near/in-memory computation.[5] Although in-memory processing is possible in today's SRAM (static random access memory) technology, it is likely to run into limitations such as its volatile storage properties, high leakage currents, and lack of support for a big number of in-memory operations, often relying on the use of accessory logic to perform more complex tasks.[6] Although different memory technologies such as spin transfer torque magnetic RAM (SSTM-RAM), phase change memory RAM (PCM) and conductive bridge RAM (CBRAM) have been considered

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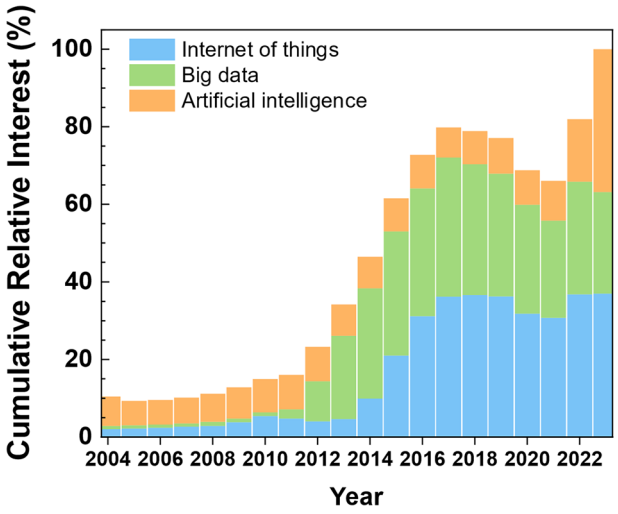

Figure 1. Normalized cumulative relative interest over time of topics involving large data applications. Values obtained from Google Trends (https://www.google.com/trends), representing search interest relative to its peak popularity. The plotted data refers to search queries performed from January 2014 to March 2023. Data was gathered in March of 2023 by searching the topics "Internet of Things","Big Data" and "Artificial Intelligence".

suitable candidates, one of the most promising device options to be presented has been resistive redox RAM (ReRAM). The low power consumption and fast switching speeds of ReRAM, coupled it its high scalability potential, make this the prime resistive switching device class for in-memory computation tasks. However, it is worth noting that due to its inherently stochastic resistive switching mechanism, device variability is one of its main drawbacks.[7] When compared to other state-of-the-art alternative computing architectures, such as quantum computing, RRAM technologies show the same scalability and CMOS compatibility potential, however, they need considerably less energy and can function under room temperature conditions, unlike quantum processors that require working environments in temperature range of milli-kelvin. Optical computing has emerged as another alternative. While avoiding the energy and working temperature requirements of quantum computing, this technology still shows limitations not only due to its wavelength-limited scaling but also its incompatibility with CMOS technologies.

Resistive switching devices, commonly referred to as memristors, are two terminal metal-insulator-metal (MIM) structures that allow for the control of their conductance state by an external electric stimulus. Not only are these devices able to store their conductance state in a non-volatile manner, but they are also capable of performing computations over this stored value by exploiting their intrinsic physical characteristics. Taking machine learning (ML) tasks as an example, and more specifically neural network (NN) architectures, a vast majority of these calculations require atrix-vector multiplications (MVM) to be performed.[2] Memristive crossbar arrays excel at these calculations. By exploiting Kirchhoff's current law and Ohm's law, these highly dense structures can perform multiply-accumulate (MAC) operations with minimal energy consumption and in a single time step due to its high parallelism (**Figure 2**). It is in these cases where large amounts of data movement are required to perform simple arithmetic operations, that memristive structures can show the best performance gain when compared to typical computing architectures.[8]

Another area where RRAM devices can show great potential is in low-cost flexible/ transparent system on panel (SOP) applications. Amorphous oxide semiconductors (AOS), processed at moderate temperatures (<200 °C), are used in pixel driver thin-film transistors (TFTs) in commercially available large-area active-matrix flat-panel displays. Over time, binary oxides such as TaO_x [9] and HfO_2[10] have received the biggest research effort amongst inorganic memristive materials. This interest comes in big part from their low-cost and simple fabrication processes, while still maintaining CMOS compatibility. However, AOS materials can also be employed as the active layer of resistive switching devices. Hence, AOS-based technologies offer advantages over silicon or hybrid technologies in terms of low-cost, low-temperature manufacturing, and compatibility between memristor and TFTs by applying the same material and fabrication techniques for both active crossbar design and periphery circuit on a single flexible substrate.[11] Indium gallium zinc oxide (IGZO) has been thoroughly studied, originally as a channel material for TFT technologies,[12] and more recently as a memristive active layer.[13,14] Recently, a flexible all-IGZO memristive 1T1R (1 transistor 1 memristor) crossbar structure has even been reported,[11] using critical raw materials (CRMs), more specifically, gallium. These materials pose a problem not only due to their scarcity but also due to the high environmental and social burden associated with their extraction and processing.[15] In order to implement a high-performance hardware neural network architecture that is fully flexible and free of CRMs, indium and gallium in IGZO should be replaced by tin. It is notable that zinc-tin oxide (ZTO) thin-film transistors are typically slower than their IGZO siblings, due to their low mobility. However, recently a record performance with ZTO MESFETs,[16] presents a great potential to pave the way for highly efficient active crossbar arrays solely made from ZTO. Taking into account its high visible light transmittance, its large-area deposition under low temperatures, the flexibility of its amorphous structure and its sustainable material composition, ZTO is one of the ideal candidates for the implementation of memristive structures on flexible and see-through electronics. In this perspective report, we will highlight the research efforts that have been put into the development of ZTO-based memristive devices by analysing not only their material structures but also the influence of these material choices on the electrical performance of the device. Lastly, we will show the progress that has been made concerning the use of these devices in neuromorphic applications and conclude with some final remarks about the main challenges that must be tackled in order to further advance this field of study.

2. Materials and Deposition Methods

2.1. ZTO Thin-Film Deposition Methods

As is evident in **Table 1**, starting from 2011 until 2023, a vast number of different ZTO-based memristive structures have been studied. Regarding these structures, both radio-frequency sputtering and solution-based processing have gathered the biggest

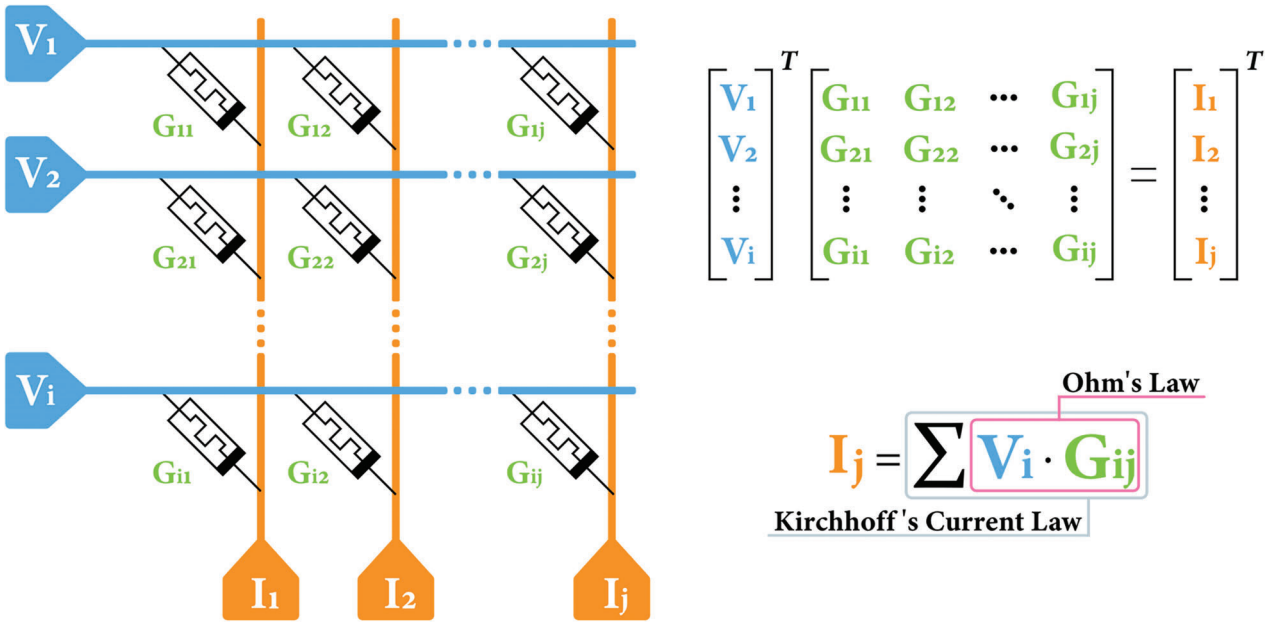

Figure 2. Schematic of matrix-vector multiplications performed over a memristive crossbar array.

research interest by a long margin, covering over 90% of all studies that were found in the literature (**Figure 3**).

Binary metal oxides tend to have easier preparation processes and simpler compositions than ternary oxides. SnOx as an active memristive layer is one of the least studied elements of the binary oxide group. When compared to their ZTO equivalents, lower uniformity, endurance, and higher operating power are evident.[48–50] Nevertheless, it is worth noting that by varying the oxygen content of SnOx thin films it is possible to obtain both p-type (SnO) and n-type (SnO2) conductivity,[49] showing CMOS compatibility and easier circuit integration.

On the other hand, there is a considerable number of reports showing the use of ZnO as an active layer. In this review work[51] ZnO-based memristive structures are analyzed and their performance is shown to be almost comparable to that of ZTO memristors. However, there are clear advantages to the use of tin as a doping agent in ZnO thin films. As an example, ZTO films with Sn content up to 50% have shown significantly increased electron mobility.[52] Furthermore, the presence of tin doping on ZnO films has produced improved rectifying ratios when paired with a Schottky contact.[53] These rectifying properties can be of great use when trying to solve current sneak-path issues on memristive crossbar structures. Another factor to consider is the fact that while both SnO_x and ZnO are crystallin, ZTO can exhibit an amorphous structure when processed at low temperature.[54]

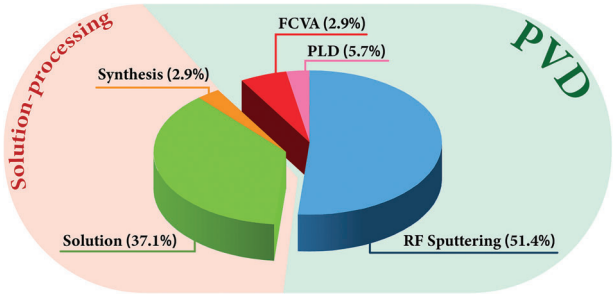

Figure 3. ZTO Deposition methods are used throughout the literature for the fabrication of memristive devices, divided by solution-based and physical vapor deposition (PVD) processes.

2.1.1. PVD Processes

As an already mature and very well-studied deposition method, RF sputtering allows for the low-temperature fabrication of ZTO films with controllable thickness and high uniformity, which are requirements for device implementation on flexible substrates. Typically, when RF sputtering is used as the deposition method, the fabrication temperatures never surpass 200 °C, with the majority of these being performed at room temperature. Sputtering deposition parameters can change considerably over different studies depending on deposition chamber configuration and the desired thin film properties. However, when the objective is to obtain an undoped ZTO memristive active layer through sputtering, the use of a single multicomponent target is the preferred method. Even though it is possible to obtain thin films by co-sputtering using Zn and Sn targets, involving an oxidation process in an oxygen-rich environment,[55,56] this approach is often avoided due to its more complex fabrication method. Fan et al. have extensively studied memristors based on Aluminium-doped zinc tin oxide,[18,26] in order to easily integrate these structures with AZTO TFT´s targeting flat panel display applications[57] (**Figure 4**a). A single AZTO ceramic plate was used with a 3:67:30 mol.% ratio of Al_2O_3, ZnO, and SnO_2, respectively. Furthermore, other works have presented additional PVD methods for ZTO active layer deposition, including pulsed laser deposition (PLD)[36,47] (Figure 4b) and filtered cathodic vacuum arc (FCVA).[32]The typical *I–V* characteristic of a memristor is represented in a semi-log scale in Figure 4a. In order to change

Table 1. ZTO-based memristors present in literature (Dep. Meth.: deposition method; Tmax: maximum temperature; BE: bottom electrode; TE: top electrode Op. Vol.: operating voltages; DC End: DC endurance; AC End: AC endurance; RF Spt.: RF Sputtering; RT: room temperature; *: devices fabricated in cross-point structures; underline: values obtained from plot analysis; double underline: measurements performed under high temperatures. Results were obtained in March 2023 through Google Scholar by searching the combination of the following terms: memristor, resistive switching, ZTO, ZnSnO, zinc-tin oxide, Zn—Sn—O, zinc stannate.

Year	Material	Dep. Meth.	T_{max} [°C]	Size [μm^2]	BE/TE	Op. [V]	ON/OFF	Retention (sec)	DC End. (cycles)	AC End. (cycles)
2011 [17]	ZTO	Solution	500	1963	Ir/Al	−3/1	10^6	–	25	–
2012 [18]	AZTO	RF Spt.	RT	282 743	Pt/Ti	−2/2	>10	10^4	256	–
2012 [19]	ZTO (NW)	Synthesis	800	0.018	Pd/Cu	−1/2	$> 10^5$	1.3×10^7	7	–
2012 [20]	ZTO	Solution	500	100*	Pt/Al	−4/2	$> 10^3$	10^4	50	–
2013 [21]	ZTO	RF Spt.	100	100*	Pt/Al	−3/1	$> 10^4$	10^4	30	–
2014 [22]	AZTO/HfO_2	RF Spt.	–	–	Pt/Ti	−2/2	≥100	10^4	100	10^7
2014 [22]	AZTO	RF Spt.	–	–	Pt/Ti	−2/3	≥100	–	100	–
2014 [23]	AZTO	RF Spt.	–	31 416	Pt/Ti/TiN	−1.5/1.5	≈ 100	–	50	–
2014 [24]	GZTO	Solution	350	31 416	ITO/Al	−1/1.5	≥100	130	–	–
2015 [25]	AZTO/HfO_2	RF Spt.	–	7854	Pt/Ti	−3/3	>10	10^4	10	10^8
2015 [26]	AZTO/Al_2O_3	RF Spt.	–	–	Pt/Ti	−2.5/3	>10	10^4	100	10^3
2015 [27]	ZTO NC	Solution (EHDA)	500	–	Ag/Ag	−2/2	≈10	8.6×10^4	100	–
2016 [28]	PVOH-ZTO_3	Solution (EHDA)	110	3000*	Ag/Ag	−1.5/1.5	>100	1.3×10^5	500	–
2016 [29]	ZTO	Solution (EHDA)	130	200 000	ITO/Ag	−8/8	>100	1.2×10^4	200	–
2016 [30]	AZTO	Solution	120	196 350	N^+Si/In	−4.5/4.5	≈2	10^3	500	–
2017 [31]	ZTO NC	Solution (EHDA)	110	7854	ITO/Ag	−3/3	$> 10^3$	10^4	500	–
2017 [32]	ZTO/Ag_xO	FCVA	375	7854	Al/Pt	−5/5	–	–	–	–
2018 [33]	ZTO	Solution	300	196 350	N^+Si/In	−2/2	>100	Volatile	10^3	–
2018 [34]	AZTO	Solution	250	31 416	Ti/Pt/Ti	−1/1	> 3	10^4	10^3	–
2018 [34]	AZTO	Solution (CTA)	400	31 416	Ti/Pt/Ti	−1/1	> 5	10^4	10^3	–
2018 [34]	AZTO	Solution (MWI)	250	31 416	Ti/Pt/Ti	−1/1	> 10	10^4	10^3	–
2019 [35]	AZTO	Solution	250	19 800	Ti/Pt/Ti/Au	−1.5/1.5	>10	10^4	100	–
2019 [36]	ZTO	PLD	600	–	Al/Al	−12/8	$\approx 10^3$	–	5	–
2020 [37]	ZTO	RF Spt.	RT	196 350	Pt/Ti/Au	−2/4	$>10^3$	10^5	100	–
2020 [38]	ZrO_2/ZTO	RF Spt.	RT	7854	TiN/Ta	−3/2	> 100	3×10^3	300	10^5
2020 [39]	ZTO	RF Spt.	RT	7854	N^+Si/Ni	−3/3	>10	10^4	–	–
2020 [40]	SnO_2/ZTO	RF Spt.	RT	7854	TiN/W	−1.5/1.5	>10	–	300	–
2021 [41]	ZTO	RF Spt.	RT	7854	ITO/ITO	−3/5	$\geq 10^3$	–	150	–
2021 [42]	ZTO	RF Spt.	RT	7854	TiN/Ta	−2/1.5	≈ 10	10^4	2×10^3	–
2021 [42]	ZTO	RF Spt.	RT	7854	TiN/Ti	−3/1.5	< 10	10^4	100	–
2021 [43]	ZTO	RF Spt.	RT	25*	Pt/Ti/Au	−4/4	>100	Volatile	100	–
2022 [44]	ZTO(Bilayer)	RF Spt.	RT	7854	ITO/ITO	−1/1	≈100	10^5	120	10^8
2022 [45]	TaO_x/ZTO	RF Spt.	RT	10 000	ITO/ITO	−1.5/2	> 10	10^4	10^4	10^6
2022 [46]	ZTO	RF Spt.	200	17 671	ITO/ITO	−3/2	> 10	10^4	1.2×10^4	–
2022 [47]	ZTiTO	PLD	RT	–	Au/Au	−3.5/2	≈100	–	128	–

the conductance level of the device, voltage sweeps are applied to the top electrode of the stack while the bottom contact stays grounded. In this case, assuming the memristor is in a high resistive state (HRS), when stressed under a positive voltage sweep the device changes from a high to a low resistive state (LRS), thus increasing its conductance level. This shift is typically referred to as the SET process. On the other hand, by applying a negatively biased voltage sweep, the resistance level changes from LRS back to HRS, leading to a conductance decrease. This change is often referred to as the RESET process.[58]

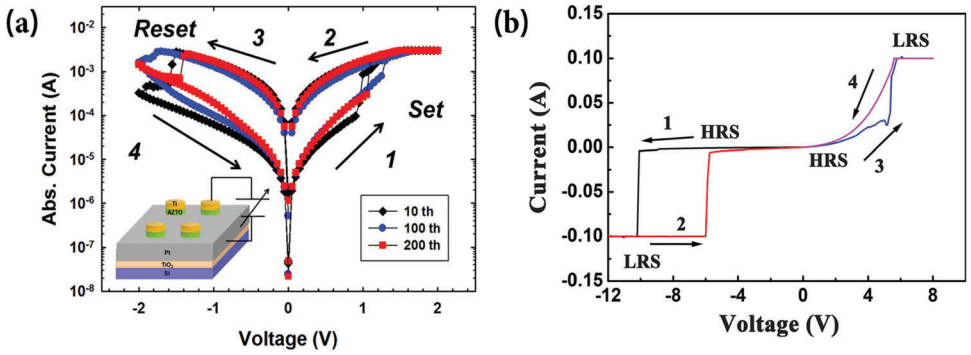

Figure 4. *I–V* characteristics of memristors with ZTO-based active layers fabricated through PVD processes. a) RF Sputtering. Adapted with permission.[18] Copyright 2012, American Institute of Physics. b) PLD process. Adapted with permission.[36] Copyright 2019, Elsevier B.V.

2.1.2. Solution Processing Techniques

Solution-based deposition processes have been improving during the last decade and have steadily developed into a promising technique, mainly due to the low-cost approach, simple fabrication procedure, and high versatility.[59] Typical precursors for ZTO solutions are tin chloride ($SnCl_2$) and zinc chloride ($ZnCl_2$),[17,20] with zinc acetate ($Zn(CH_3COO)_2$) also being reported as an alternative.[33] AZTO solutions have also been analyzed for the fabrication of memristive active layers. With an optimal amount of aluminium doping, solution-processed ZTO TFT´s have shown enhanced electrical properties. By fine-tuning the ratio of aluminium in the AZTO solution, it is possible to control the quantity of oxygen vacancies present in the memristive layer.[60] Kim et al. have reported on the effect of convention thermal annealing (CTA) and microwave irradiation (MWI) on AZTO solution films[34] (**Figure 5**). Both aluminium chloride ($AlCl_3$) and aluminium nitrate ($Al(NO_3)_3$) have been reported as precursors for AZTO solutions.[35,30] Gallium-doped ZTO based on solution processing was also achieved by Oh et al. by using gallium nitrate ($Ga(NO_3)_3$) as a precursor.[24]

Moving one step forward, printed memristive devices using ZTO nano-cubes as the switching medium have also been reported by Siddiqui et al.[27,28] Here an electro-hydrodynamic atomization (EHDA) process was used. This method consists of the deposition of thin films through the injection of ink by a syringe pump into a metallic nozzle, which in turn forms a Taylor cone allowing for the controlled deposition of the material. Parameters such as flow rate, applied voltage, nozzle to substrate distance, nozzle diameter and substrate movement speed can all be controlled in order to achieve the desired film properties. Like other printing techniques, one of its main advantages is the reduced solution waste during deposition when compared to spin-coating. ZTO nanowires synthesis has also been reported as a possible fabrication option.[19]

However, there are no evident performance advantages that can be obtained based on a certain deposition technique, apart from the simplicity and sustainability of solution processing methods. In fact, the performance of ZTO memristors is dictated in most part by the engineering of the interface layers.

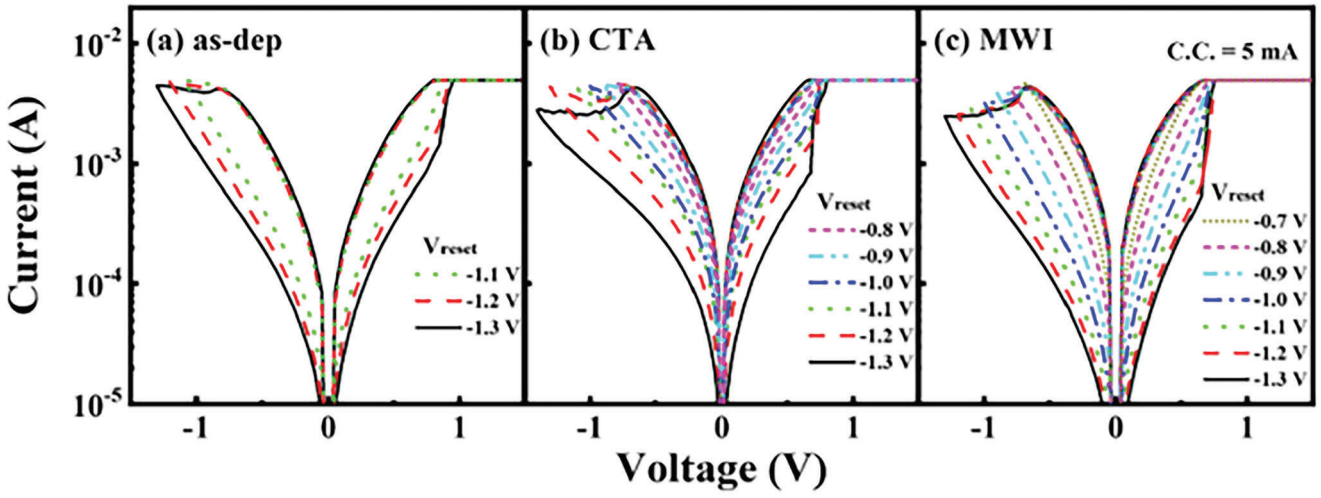

Figure 5. Effect of different annealing processes on Ti/AZTO/Pt memristors fabricated through spin-coating. a) as deposited; b) CTA; c) MWI. Reproduced with permission.[34] Copyright 2017, Elsevier Ltd.

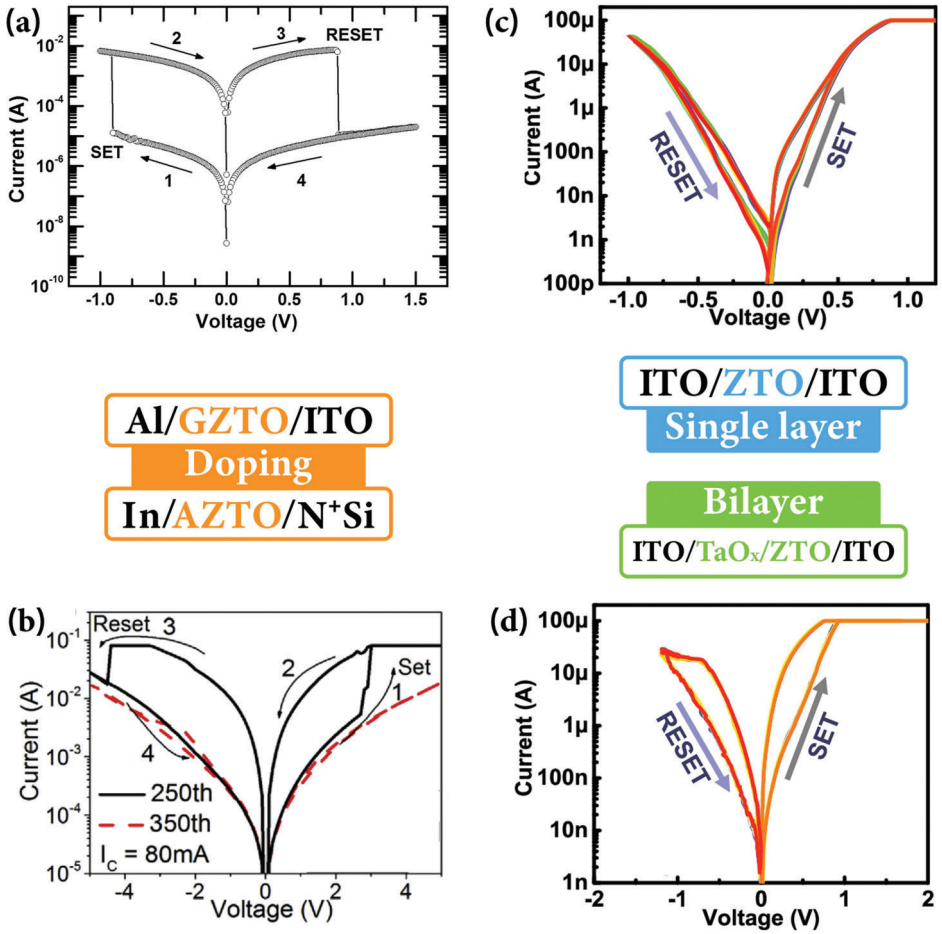

Figure 6. *I–V* characteristics of memristive devices using differently engineered ZTO-based switching layers: a) Gallium doped layer. Reproduced with permission from[24] Copyright 2015 Elsevier B.V. b) Aluminium doped layer. Reproduced with permission.[30] Copyright 2016, Elsevier B.V. c) Single layer structure; d) Bilayer structure; Adapted with permission.[45] Copyright 2022, American Chemical Society.

2.2. ZTO Doping and Bi-Layer Structures

One way to improve switching stability and uniformity in RRAM devices, is to better control the creation and destruction of conducting filaments (CFs) in devices ruled by filamentary resistive switching. It is worth noting, however, that AOS memristors have also shown area-dependent resistive switching that can be related to modulation of Schottky-type barrier profile into various resistance states. In these cases, the resistive switching performance optimization is usually done by doping the active layer or stack engineering, creating multi-layered structures.

For example, not only has gallium been studied as a ZTO dopant[24] (**Figure 6**a), but it has also been shown that using aluminium as a doping agent can improve the retention performance of devices (Figure 6b). Hsu et al. presented two identical metal-insulator-metal (MIM) memristive structures varying only in their switching layer.[30,33] Al-doped and undoped ZTO were deposited by spin-coating using the same precursors and solvent. However, comparing the performance of both devices, the non-doped structure showed lower operating voltages, higher R_{ON}/R_{OFF} ratio and better DC endurance, while showing volatile resistive switching. Whereas the Al-doped counterpart was able to retain its state for over 1000 s. In terms of transport mechanisms at different regions of voltage bias, the volatile un-doped device was reported as being governed by trap-assisted tunnelling ([0 V;2 V] and [0 V;−2 V]), trap-controlled space-charge-limited conduction ([2 V;0 V]) and hopping conduction ([−2 V;0 V]). Whereas the Al-doped device follows trap-filled space charge limit conduction in LRS, and HRS until 1 V, and afterward is governed by Poole-Frenkel effect.

Besides the doping effect, comparative studies have been performed between single layer and bilayer ZTO (Figure 6c,d). In this regard, Liu et al., fabricated a bilayer structure by inserting a HfO_2 layer in between the AZTO and the bottom contact of a Ti/AZTO/Pt structure, obtaining considerably lower operating voltages, higher R_{ON}/R_{OFF} ratios, and lower cycle to cycle variability.[22] These improvements were mainly attributed to the difference in Gibbs free energy between the formation of HfO_2 and SnO_2. As a result of this difference, the oxidation reactions occur more easily in the HfO_2 layer leading to the conducting filament forming locally in the HfO_2 region. Ismail et al. have also presented two structurally identical devices, varying only the active layer properties. The first uses ZTO as the sole switching material (**Figure 7**a), while in the second, ZTO takes the role of

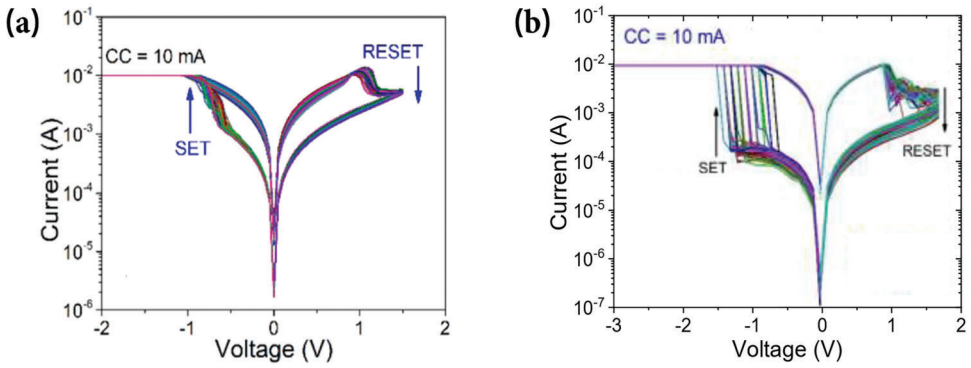

Figure 7. *I–V* characteristics of memristors with identical material structures, varying only the ZTO-based active layers and maintaining the contact properties. a) MIM structure using a single ZTO monolayer as the memristive layer (Ta/ZTO/TiN). Adapted with permission.[42] Copyright 2020, Elsevier B.V. b) MIM structure using a memristive layer containing both ZTO and ZrO_2 layers (Ta/ZrO_2/ZTO/TiN). Adapted with permission.[38] Copyright 2020, Elsevier B.V.

an oxygen reservoir layer coupled with a ZrO_2 switching layer (Figure 7b).[38,42] Comparing the performance of both, the monolayer structure requires lower SET/RESET voltages, maintains its state for longer, and shows considerably better endurance. However, it shows a considerably lower R_{ON}/R_{OFF} (≈10) than its bilayer equivalent (>100). Tseng et al. also reported on ZTO memristive devices with different active layers. Structures using ITO as both top and bottom contacts were fabricated, one using a single 35 nm ZTO layer, and another with two ZTO layers with different oxygen proportions with a combined 20 nm thickness.[46,44] While the difference in operating voltages can be attributed to different layer thicknesses, the bilayer device showed considerable increases not only in R_{ON}/R_{OFF} ratio but also in retention time. This improvement is attributed to the difference in the oxygen vacancy quantity between the two ZTO layers. Due to this difference, the forming and rupture of the conductive filament start taking place at the interface between the ZTO layers in a more controlled fashion, resulting in better performance.

2.3. ZTO-Based Flexible Structures

By applying the EHDA deposition process previously described, Siddiqui et al. were able to combine different polymers (PMMA and PVOH) with ZTO nano-cubes to form nanocomposite-based active memristive layers compatible with flexible polyethylene terephthalate (PET) substrates.[28,31] In both cases the addition of these polymers resulted in the improvement of switching characteristics due to their intrinsically large bandgaps. However, the addition of these polymers also had a very significant positive effect on the mechanical strength and resilience of the devices. In the case of Ag/PVOH-ZTO/Ag structures, the array was tested in bending diameter ranges between 50–4 mm, maintaining its resistive switching behavior until a 5 mm diameter (**Figure 8**a). Furthermore, the DC endurance of the device was tested, preserving its HRS and LRS over 1500 bending cycles at a fixed 15 mm bending diameter (Figure 8b). The influence of the bending diameter and bending repetitions on the *I–V* characteristics was also studied (Figure 8d,e), showing very uniform behavior.

Polymer-free ZTO active layers have also been reported on flexible substrates.[29] Through the same EHDA process, ZTO powder-based inks were printed on a PET substrate precoated with ITO. In this case, the devices were able to withstand bending until the 8 mm diameter range, showing a decrease in flexibility when compared to the polymer-based counterparts. The breakdown was attributed to mechanical failure of the active ZTO layer and silver top contacts.

3. Electrical Characteristics of ZTO-Based Devices

3.1. Influence of R_{ON}/R_{OFF} on Device Endurance

When analysing the difference in the ratio between the high and low resistive states (HRS and LRS, respectively) of memristive structures, several factors need to be taken into consideration, even when the same active material is used. As an example, Kim et al. showed how different post-deposition annealing treatments influence the performance of solution ZTO films, more specifically its ON/OFF ratio.[34] Since the current values of the HRS do not vary significantly, the improvement of this ratio often comes at the cost of increased maximum currents, e.g., compliance current. Generally speaking, cycling failure in MIM device structures is attributed to microstructure degradation and in the cases where high operating current is used in LRS, problems such as Joule heating accelerate this degradation process, affecting the integrity of the structure and leading to eventual device failure. This effect is even more prevalent in cases where the switching between states occurs in an abrupt fashion and current levels increase (during SET) and decrease (during RESET) many orders of magnitude over a short time interval. Taking the devices referenced in Table 1 and considering their DC cycling endurance as a function of their R_{ON}/R_{OFF} **Figure 9**, we can confirm that ZTO-based devices also follow this trend, where devices with a smaller ratio between states are able to perform more reliability during endurance testing. More specifically, memristors showing the biggest ON/OFF ratios (higher than five orders of magnitude) are not capable of withstanding 100 DC cycles, whereas devices showing the highest cycling endurance (over 10^4 cycles) show R_{ON}/R_{OFF} in the range of ten. In accordance with what was previously mentioned regarding typical device failure, the devices that can endure a higher number of cycles show gradual resistive switching, whereas the memristors with a higher window

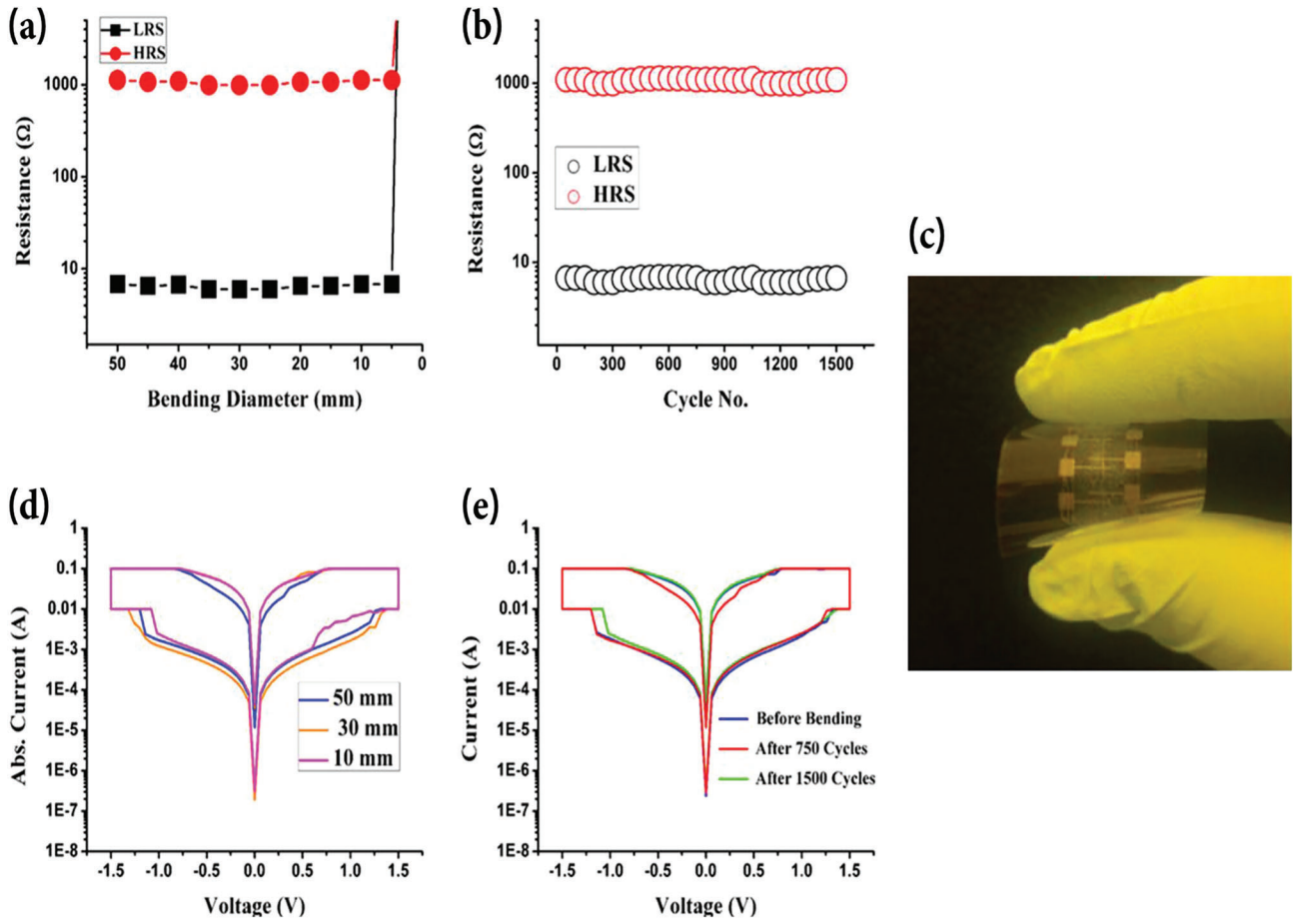

Figure 8. Mechanical bending tests of Ag/PVOH-ZTO/Ag structure. a) HRS and LRS values over different bending diameters; b) Device endurance over 1500 bending cycles at a fixed 15 mm bending diameter; c) Image of fabricated Ag/PVOH-ZTO/Ag array on flexible PET substrate; d) Typical *I–V* behavior under different bending diameters; e) *I–V* behavior changes over multiple bending cycles. Adapted with permission.[28] Copyright 2016, Elsevier Ltd.

show abrupt switching. Gradual non-volatile behavior tends to be preferred for conventional AI applications using deep neural networks,[61] where there is symmetry and linearity of the current responses to the train of pulses.

3.2. Switching Behavior and Contact Materials Influence in Valence Change Mechanism

A "standard" memristor is a metal-insulator-metal (MIM) structure where the resistive switching active layer is sandwiched between a noble metal layer (Schottky type contact) and a chemically active electrode (Ohmic contact). If we consider that the input signal is connected to the noble metal contact and the bottom contact is grounded, there will be a typical VCM-type (valence change memory) memristive behavior when the change from HRS to LRS (the SET operation) takes place during negative biasing whereas the RESET operation takes place under positive bias. On a linear scale, the switching loops look like the hand-written number eight but written in the opposite direction, which is why this pinched hysteresis is sometimes referred to as counter eight-wise.[62] However, in many reports, a semi-logarithmic representation is preferred. In this graphical representation, the switching appears as two clockwise loops. If the connections are reversed, and instead the input is connected to the Ohmic contact, the inverse behavior takes place and the switching shows counter clockwise direction (or eight-wise) (**Figure 10**a).[63] In cases where symmetric contacts are used, the resistive switching phenomena is obtained through a virtual electrode created by an oxygen-deficient gradient in the switching oxide.[63]

Considering the devices listed previously in Table 1, it can be concluded that most device structures presented follow the conventional switching behavior mentioned earlier. However, one of the cases where this behavior is not present is when aluminum is used as a contact material. In cases where ZTO-based memristors use aluminum as the Ohmic contact (in this case the Ohmic contact is the one on top, connected to the input), the devices show clockwise resistive switching, instead of the expected counter clockwise behavior (Figure 10b). [17,20,21] This behavior is shown while varying the bottom contact material between iridium and platinum. Murali et al. attributed this behavior to the fact that during its deposition the aluminum gets oxidized, extracting oxygen ions from the ZTO layer and leading to the formation of a thin AlO_x interfacial layer. Consequently, during the forming process, when a sufficiently high negative voltage is applied, the migration of native defects (either positively charged metal ions

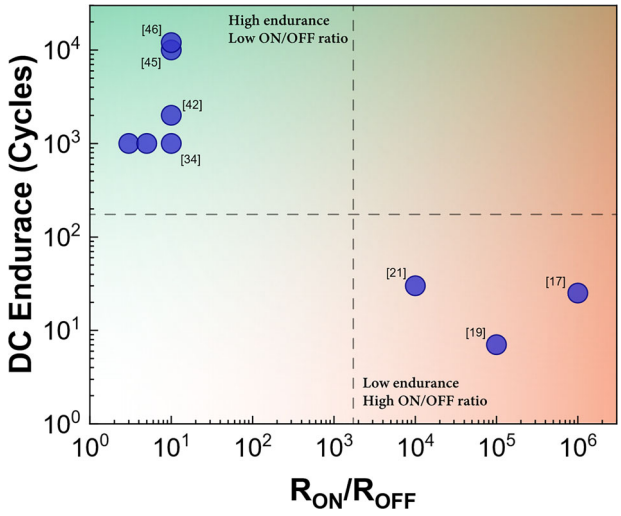

Figure 9. ZTO RRAM device endurance performance as a function of the resistance ratio between HRS and LRS.

or negatively charged oxygen vacancies) results in the formation of conducting filaments inside the interfacial layer, resulting in a SET operation. On the contrary, when a sufficiently positive voltage is applied, the conducting filaments in the AlO_x layer rupture, restoring the HRS. Hence, the switching is dominated by the AlO_x layer, and not the ZTO.

In 2019, an interesting device structure of ZTO sandwiched between platinum and titanium/gold electrodes was able to perform both clockwise and counter clockwise resistive switching depending on the direction of the forming/initialization process (**Figure 11**). [37] When the initialization (or electroforming) was performed by applying a positive voltage to the Ohmic top electrode, the device showed both counter clockwise non-volatile bipolar and unipolar switching behaviors (Figure 11a,b, respectively). Both switching behaviors were attributed to conventional filamentary switching, with the filament formation taking place in the oxygen-deficient interface of the titanium top electrode toward the platinum bottom electrode. On the other hand, resistive switching in the clockwise direction was obtained when a negative voltage was applied to the Ohmic top contact during the initialization process (Figure 11c), meaning that a forming voltage higher than the SET voltage was not required for this mode of switching. By comparing the LRS of devices with different areas it was possible to confirm the area scaling resistive switching properties. Adding an Al_2O_3 layer between the ZTO/Ti interface confirmed that no significant change was seen in the switching behavior, thus, the area-dependent switching does not require an oxygen-deficient region in the ZTO/Ti interface. Taking both these factors into consideration, it was concluded that when the device is initiated under negative voltages, the resistance state is modulated by ion exchange and/or trapping mechanisms at the platinum bottom contact interface. This mechanism is referred to as interface-type resistive switching, in accordance with other works from the literature.[57] Further studies were carried out on the same structure by miniaturizing the size and fabricating the devices in a cross-point form.[43] When reduced to dimensions as small as 25 μm^2, the devices no longer showed both switching directions. Under these new conditions, the memristors only performed switching in the clockwise direction according to the interface-type switching, as attempts to form the device in positive polarity yielded no resistive switching behavior. Their operating currents were also reduced considerably (Figure 11d), which was expected due to the significant difference in device size.

In order to avoid confusion between clockwise and counter clockwise directions when comparing different studies that use opposing contacting schemes, it shall be suggested here to differentiate between the two mechanisms by referring to them as either volume-type switching or interface-type switching. Usually, the volume-type switching mechanism is filamentary, whereas the interface-type mechanism scales with the device area. Alternatively, in cases where little is known about the nature of the VCM, the two types of switching polarities may also be differentiated by considering the device a diode structure: Then the volume-type VCM mechanism is a reverse-SET/forward-RESET switching, whereas the interface-type VCM mechanism is a forward-SET/reverse-RESET switching.[43] Note, that this categorization is universally valid for both n-type and p-type switching materials, provided the VCM switching is dominated by intrinsic dopants.

The vast majority of devices listed in Table 1 show VCM-type switching behavior, as their contact materials are often inert metals (such as platinum and gold). Under the valence change mechanism, voltage pulses can induce the oxidation or reduction of the metal oxide. These processes are caused by the migration of ions that can be either anions, such as oxygen vacancies, or cations such as cation interstitials. This stoichiometry change leads to a variation in the electronic conductivity close to the electrode interface, thus controlling the overall conductance of the memristive device. The polarity of the applied voltage pulse determines if an oxidation or a reduction process takes place.[58] However, in cases where memristive structures use active metal electrodes, such as silver or copper, most show filamentary electrochemical metallization memory-type switching (ECM, also referred to as conductive bridge RAM). By using silver as their contact material, Lee et al.[29] showed ECM-type switching characteristics in their ZTO devices. In this case, when a voltage pulse was applied, highly conductive filaments were formed in the active layer by the drift of highly mobile Ag^+ cations toward the inert electrode leading to the conductance change of the device. Inverting the polarity of the applied pulse reverts the device to its original HRS. Unlike VCM switching, ECM devices typically show abrupt switching behavior, nevertheless, multi-level cell (MLC) properties can be achieved by controlling the RESET stop voltage and compliance level.

3.3. Retention Performance

Depending on the application, the time that different resistive states (in both digital and analog tuning) maintain their programmed resistance values (usually referred to as the retention time) is one of the most important factors for many power-efficient memristor-based neural network hardware applications. Commonly, filament-based memristive devices tend to have longer retention times than their area-dependent coun-

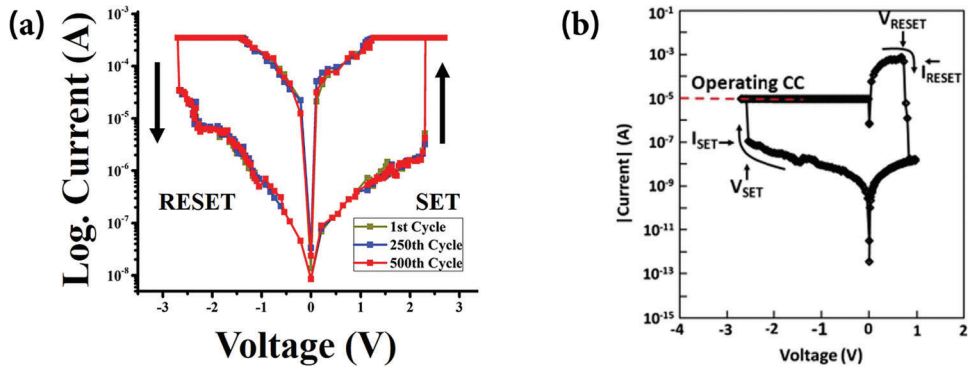

Figure 10. a) Typical VCM-type memristive behavior (Adapted with permission.[31] Copyright 2017, Elsevier B.V.) and b) atypical VCM-type memristive behavior in relation with device electrode configuration. Adapted with permission.[20] Copyright 2012, Elsevier Ltd.

terparts. This can be attributed to the fact that trapping and de-trapping of charge carriers[64] and barrier modulation,[65] the main reasons for retention failure in area-dependent devices, is easier to occur than undesired ion migration, usually responsible for retention failure in filamentary devices.

When analyzing retention measurements, it is very important to take into consideration the temperature at which the measurement has been performed. The Arrhenius equation relates temperature with the rate of chemical and physical reactions. Since the degradation time follows the Arrhenius law, retention measurements performed under high temperatures (usually at 85 °C) can be extrapolated to longer retention times. In this perspective article, it is evident that most device retention measurements were not performed under high-temperature conditions (8 out of 35) (**Figure 12**). Although most publications tend to show device retention performance up to 10^4 s, Dong et al. reported ZTO nanowire structures which were able to maintain the resistance states over a period of five months (≈10^7 s).[19] However, the testing methodology used for the measurement is not conventional. First, two distinct devices were used, one programmed to be always in the LRS state, and another to be always in the HRS state. The measurements for the LRS and HRS currents where then

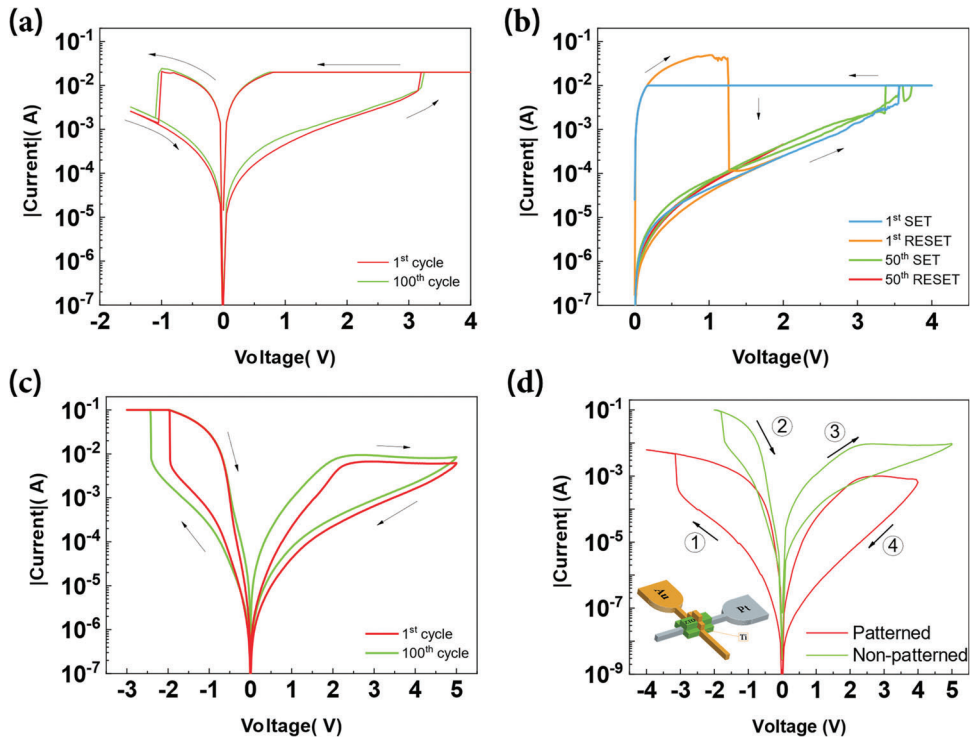

Figure 11. Different operating modes of Pt/ZTO/Ti/Au memristors were obtained by changing the electroforming direction and device size. a) Counter clockwise resistive switching caused by reverse electroforming; b) Unipolar resistive switching caused by reverse electroforming; c) Clockwise resistive switching caused by forward electroforming. Adapted with permission.[37] Copyright 2019, Wiley-VCH. d) Clockwise resistive switching occurring in 5μm*5 μm patterned devices (inset: device schematic in cross-point configuration). Adapted with permission.[43] Copyright 2021, MDPI.

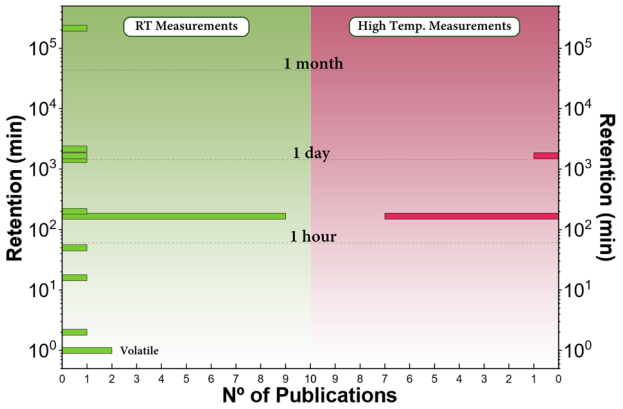

Figure 12. Retention performance of ZTO-based RRAM devices presented in Table 1 is separated between RT (room temperature) measurements and high-temperature measurements (performed between 80 and 90 °C).

performed on the respective devices. With this methodology, it is not possible to consider the effect that multiple write/read cycles might have on the performance of the device. Secondly, the measurements were performed only once a month, not taking into account the influence of the reading conditions on the device over the period of testing, making it unsuitable for reporting a proper retention measure.

Like it was previously mentioned, the retention performance of ZTO devices has been improved considerably by the addition of aluminum as a doping agent.[30,33] By applying spectroscopy studies, Dittman et.al. revealed that in fact resistive switching (or retention) failure of VCM-type devices can be attributed to the alteration of valence states of the cations derived by nanoscale migration of oxygen.[66] By introducing new design rules based on the addition of low oxygen transport layers such as Al_2O_3, a tremendous improvement in retention time was obtained. The same effect might be responsible for the retention improvement reported on Al-doped ZTO devices.

4. ZTO-Based Memristors for in-Memory Computation and Neuromorphic Applications

4.1. Neuromorphic Properties

Although reports of resistive switching ZTO-based structures date back to 2011, with devices responding to pulses in the ns-range being shown as early as 2012, it took five more years for the first neuromorphic tests on this material to be reported.

In 2017, Murdoch et al. showed that by applying varying amplitude pulse trains, on a zinc-tin oxide/silver oxide interface, it was possible to gradually modulate the conductance level of the memristor.[32] In this test, successive positive voltage pulses ranging from 1 to 10 V resulted in the increase of device conductance. The opposite was demonstrated for negative bias pulses ranging from −1 to −10 V. Even though the overall conductance level change was not significant (taking the pulse amplitude and width into account) and the response was not completely symmetrical, this test successfully showed that gradual conductance modulation of ZTO-based memristors during short pulses was possible. Subsequently, the response to different pulsing frequencies was also tested. First, 10 V pulses with the duration of 400 ms were applied with a 20 s interval. This resulted in a behavior akin to the human "forgetting" process, where a high conductance state was reached after the spike, and decreased over time while no other programming pulse was applied. If, however, the timing between pulses was reduced to 2 s, after some pulses the conductance level increased significantly and the state was maintained, leading to a change from short-term-memory to long-term-memory (or STM to LTM). Lastly, it was shown that the ZTO/Ag_xO structure was also able to perform spike-timing dependent plasticity (STDP) following the anti-symmetric Hebbian learning rule, the same learning rule that guides the synaptic strength update on biological synapses. According to this rule, the timing between pre- and post-synaptic pulses defines whether synaptic potentiation or depression occurs. In the case where the pre-synaptic stimulation occurs before the post-synaptic spiking, the result is an increase in synaptic weight inversely proportional to the time between stimuli. The opposite is also correct, since when the post-synaptic spike precedes the pre-synaptic stimuli, a decrease in synaptic strength takes place, also inversely proportional to the time interval. However, if enough time has elapsed between both pre-and post-synaptic spikes, the rule no longer applies. Although the pulse scheme used to control the conductance level of the memristor required considerable energy, this was still an important step, as it was the first time that ZTO memristive devices were used as biological synaptic emulators.

In 2020, Ismail et al. demonstrated the potential of ZrO_2/ZTO memristors for neuromorphic systems (**Figure 13**).[67] For this bilayer structure, pulses of 100 µs with voltages of −1 and 1.5 V were sufficient to perform long-term potentiation (LTP) and long-term depression (LTD), respectively (Figure 13b). Through the application of spiking pulses, LTP and LTD are processes that allow for long-term increase or decrease of the device conductance level, respectively. The overall device conductance was increased from 0.5 to 2.5 mS over the 50 potentiating pulses, and almost returned to its original state after the 50 depressing pulses, while showing near-linear behavior. To test spike-rate dependent plasticity (SRDP), -1 V pulses with the duration of 50 µs were applied at varying frequencies and the current response of the device was studied (Figure 13c). Behaving in a similar way to that of a human synapse, shorter time intervals between pulses resulted in a bigger synaptic weight increase (or current level increase in the case of the memristor) than when a longer period between successive pulses was chosen. This can be attributed to the fact that if the second pulse occurs while the device is still under the effect of the first applied pulse´s excitatory post-synaptic current (ESPC), the current increase on the device is benefited by both pulses, leading to a higher current gain. This phenomenon is usually referred to as pared-pulse facilitation (PPF) and is obtained by calculating the relative difference between the current of both spikes $((I_2-I_1)/I_1)$ (Figure 13d). The value of PPF as a function of the time interval between pulses can usually be fitted by an exponential decay. STDP is also shown in Figure 13e by varying the time between pre and post-synaptic pulses from −80 to 80 µs.

The earliest reports of ZTO monolayer devices showing neuromorphic properties were presented by Ryu et al.[39] in 2020. In this work both LTP and LTD were performed with different pulse amplitudes and widths, resulting in different levels of linearity and symmetry. The increase in pulse amplitude during the

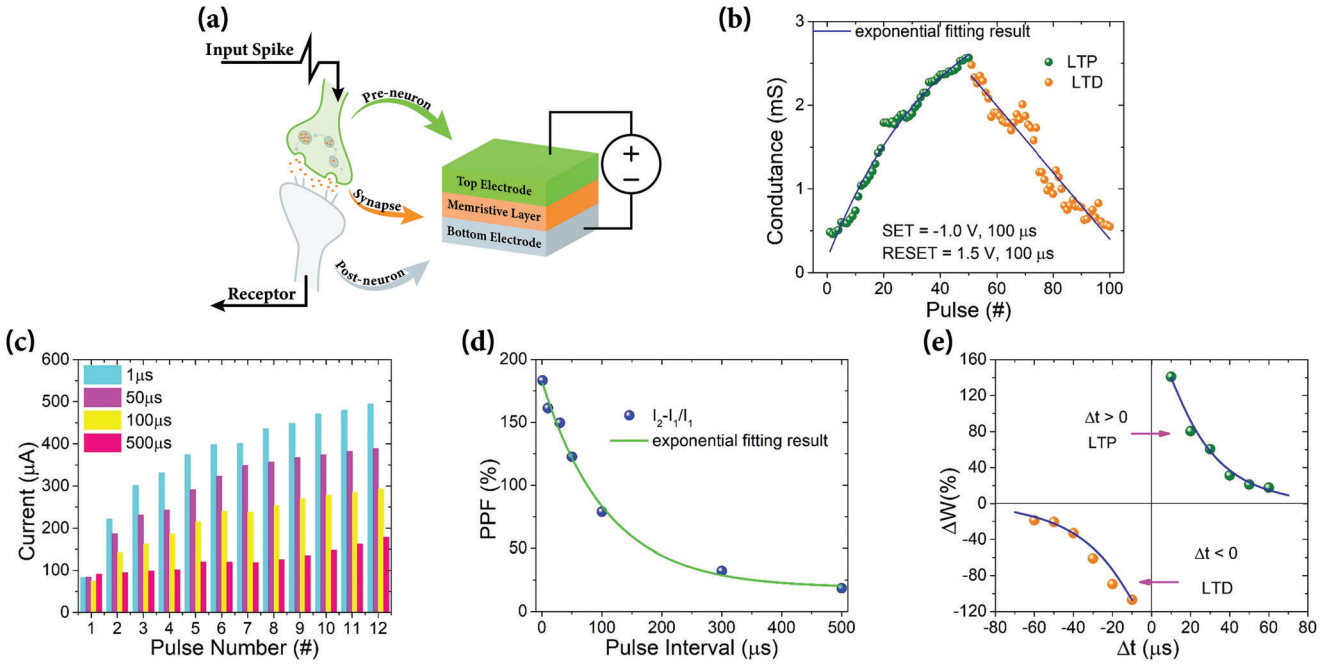

Figure 13. a) Schematic of synaptic emulation performed by memristive devices; Synaptic functions demonstrated by TiN/ZrO_2/ZTO/Ta structures: b) LTP/LTD; c) SRDP; d) PPF; e) STDP. Adapted with permission.[67] Copyright 2020, Elsevier B.V.

potentiating process resulted in an increase in maximum device conductance after the initial 30 pulses. Regarding the depression process, the increase in voltage affected the device in other ways. As expected, the conductance state reached after the depression process was considerably closer to the initial pre-potentiation state. However, higher voltages contributed to a higher decay in conductance after the first depressing pulse, decreasing its linearity. To obtain a more linear and symmetrical response during LTP and LTD, pulse trains with varying widths and amplitudes were studied. In one case the pulse width was fixed, and the pulse voltage was gradually increased over the potentiation and depression processes, whereas in the second case the opposite was done, a pulse amplitude was defined, and the width was gradually increased producing considerably better results. STDP behavior was also studied over five different memristor cells, with the average behavior being close to the theoretical approximations. The device performance was tested for image pattern classification using the MNIST dataset on a single-layer neural network consisting of 784 input neurons (world lines) and ten output neurons (bit lines), with two Ni/ZTO/Si devices connecting the inputs and outputs so that negative weight values could be implemented. All LTP and LTD variations were tested for their MNIST pattern accuracy: the identical pulse, amplitude increment, and width increment. As expected, the best results were achieved when the width of the pulse was gradually increased during the potentiation and depression processes, as neural network architectures greatly benefit from linear weight responses.

The first neuromorphic tests performed on transparent ZTO-based structures, in this case using ITO as both top and bottom contacts, were reported by Ryu et al.[41] in 2021. They were able to reproduce the transition from STM to LTM as well as the potentiation and depression processes. Two different pulse schemes were used for LTP and LTD, one with higher amplitude and wider pulses, which resulted in a more abrupt (less linear) response but with a considerably higher maximum conductance, and another requiring less pulse voltage and width, thus achieving a more linear response with the trade-off of showing a lower ratio between the initial and the maximum conductance levels. When tested in the same neural network set-up as shown in their previous work, the network presented better results when using the low-powered pulse scheme, again due to its more linear conductance updates.

However, careful interpretation of artificial neural network (ANN) simulation results has to be done not only in this case but in most simulation environments presented in the literature. In a vast number of cases, when simulating the potential accuracy of a memristive device in, for example, a pattern recognition neural network application, not all relevant factors are taken into account. Usually, one ideal cycle of device potentiation and depression is chosen to represent the behavior of all memristive elements in the network, and the recognition rate is calculated based on such characteristics. However, in practice, a potential physical implementation of the simulated network is influenced by many more factors. The most important issue that is often overlooked is the variation between individual devices (device-to-device, or d2d variation), as even devices sharing the same sample substrate fabricated under the same conditions can, and usually do, show considerably different characteristics. One way of mitigating this issue is the reduction of device size, however, the overwhelming majority of reports showing neuromorphic properties on ZTO memristors still use common bottom electrode structures.[68] In fact, only 4 ZTO-based devices mentioned in the literature were fabricated using a cross-point structure (Table 1). Another aspect that should be accounted for is the cycling variation of the device itself (cycle-to-cycle, or c2c variation), as the be-

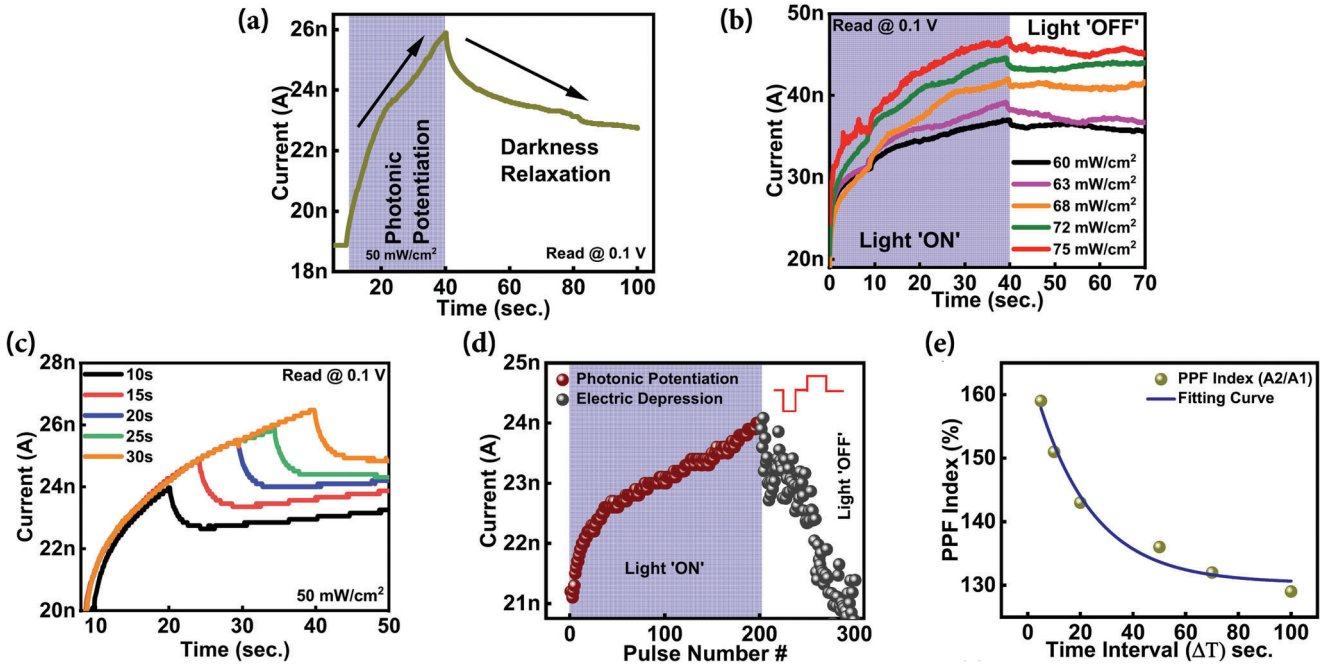

Figure 14. Photosensitive tests performed on ITO/ZTO/ITO structures: a) Positive photoresponse under blue light; b) Device response to optical pulses with different intensities; c) Device response to optical pulses with different durations; d) Current level modulation trough photonic potentiation and electric depression; e) Photonic PPF response. Adapted with permission. [46] Copyright 2022, American Chemical Society.

havior of the device can change or degrade over time. Although many publications claim remarkable endurance metrics on their devices, they are seldom accompanied by the required data to justify such claims.[69] Long retention times also need to be targeted, as current drift should be completely avoided, or at least it should be guaranteed that it only occurs after sufficient time.[61] Furthermore, if we assume that these memristors will be implemented in a crossbar-like structure, factors such as current sneak-paths and parasitic voltage drop effects can have a significant influence on the performance of the network. As crossbar sizes increase, so does the effect of voltage drop-off through the rows and columns. In order to prevent this effect, devices should be engineered in order to reach lower conductance levels.[61] The LRS/HRS ratio of access devices must also be sufficiently big in order to avoid large power consumption derived from read/write disturbances.[61]

Kumar et al. continued to study the synaptic capabilities of transparent ZTO-based devices. In one of their works, a TaO_x/ZTO bilayer was used as the switching medium sandwiched between two ITO electrodes, showing fairly linear and symmetrical LTP/LTD over 790 cycles.[45] When applied to a Hopfield neural network (a recurrent ANN) containing 784 synapses, the network showed a training accuracy of 96% over 17 iterations. In another publication, while using another bilayer structure comprised of two ZTO layers with different oxygen doping levels, device potentiation, and depression were also shown.[44] When compared to the TaO_x/ZTO bilayer, the programming pulse power was reduced, while improving the curve linearity over 5000 potentiation/depression cycles. However, as it is typically observed, this spiking endurance comes at the cost of the ratio between maximum and minimum conductance.

Zinc-tin oxide films have been used as interlayers to improve the neuromorphic performance of other memristive materials. In the work published by Rahmani et al., a bilayer structure was formed by adding a thin a-ZTO film to the SnO_2 switching medium, resulting not only in more linear and symmetrical LTP/LTD behaviors but also in a power consumption decrease, when compared to a simple SnO_2 monolayer structure.[40] This change in electrical behavior is explained by the change in the location of rupture and formation of the conductive paths in the device stack, taking place in the new TiON interfacial layer created in the TiN/oxide interface during ZTO deposition.

4.2. Optoelectronic Properties

More recently ZTO has also been studied as a potential switching material for optoelectronic memories targeting neuromorphic applications (**Figure 14**).[46] In this work, the effect of an annealing treatment of the ZTO layer in a nitrogen environment was studied. It showed that the 200 °C annealing process significantly improved the linearity of the potentiation/depression curves. The device was able to perform 350 potentiation and depression cycles, totaling over 17.5×10^4 pulses, with STDP properties also being confirmed. Perhaps more interesting is that positive photo response (PPR) properties were also shown and investigated on this ZTO monolayer structure (Figure 14a). Artificial optoelectronic synaptic behavior was demonstrated by using blue light at different intensities (Figure 14b) and illumination times (Figure 14c) resulting in different photonic potentiation curves, indicating a dependence between the applied light properties and the relaxation process. A "hybrid" test was also performed where

Table 2. Neuromorphic properties of ZTO-based memristors are present in literature.

			LTP/LTD Pulsing					
Year	Material	STM/LTM	Amplitude [V]	Width [µs]	ΔG [µS]	SRDP	PPF [µs]	STDP
2017[32]	Ag_xO/ZTO	✔	± [1; 10]	–	[24;28]	–	–	–
2020[73]	ZrO_2/ZTO	–	−1/1.5	100	[500;2500]	✔	[1;500]	✔
2020[39]	ZTO	–	3/−3	[50;5000]	[0;12]	–	–	–
2020[40]	SnO_2/ZTO	✔	1/−1.1	100	[1150;1450]	–	–	–
2021[41]	ZTO	✔	2/−2	100	[980;1090]	–	[10;105]	–
2021[42]	ZTO	–	−1/1.3	40	[22;36]	–	[40;400]	✔
2021[43]	ZTO	–	−2.2/2	700	[1;2.5]	–	–	–
2022[47]	ZTiTO	–	−2.75/0.68	50 000	[0;600]	–	–	–

blue light was used to perform photonic potentiation with depression being conducted through the typical electronic process (Figure 14d). By testing different time intervals between light pulses, photonic PPF properties were also shown with the time interval varying between 5 and 100 s (Figure 14e). Later on, Kumar et al. demonstrated that their ZTO_y/ZTO_x bilayer structure, obtained by RF Sputtering depositions under different oxygen concentrations, was able to perform the RESET process through light pulsing stimulus as well, with particularly good endurance and retention characteristics.[70]

In **Table 2** the neuromorphic properties of the ZTO-based memristive are summarized. Regarding energy consumption, when comparing the ZTO memristors presented in literature to other memristive devices using AOSs, such as IGZO, they show comparable performance of less than 10nJ per programming pulse.[13] However, there are still several orders of magnitude separating these devices from the 10 fJ that are spent on a biological synaptic event.[71] Although many memristive devices have reported programming energies well below their biological counterparts (as low as <10zJ), better optimization of ZTO devices in terms of material properties, electrical performance, and device structure has to be performed in order to reach these figures-of-merit.[72]

5. Conclusion and Future Perspectives

In this work, the research progress toward the use of ZTO as a sustainable memristive semiconductor has been assessed by evaluating ZTO-based memristors not only in terms of their physical structure (contact materials, fabrication temperatures, deposition methods, size) but also their electrical performance (*I–V* characteristics, retention, endurance, neuromorphic, and optoelectronic capabilities).

One of the most pressing issues regarding the current state of research is the large device sizes reported in most studies. Only 13% of studies demonstrated cross-point device structure and with sub 100 μm^2 dimensions present only in one of the works. With a vast majority of works reporting on common bottom contact structures, it is not viable to consider the application of these devices into crossbar arrays, as the characteristics of a memristor frequently change when the adaptation towards a cross-point structure happens. Power consumption would also benefit greatly from reduced device sizes as both the operating voltages necessary to perform state changes and the overall current levels would be considerably reduced.

In cases where flexible and transparent implementations are targeted, it is also important to note that most ZTO sputtering processes require sufficiently low temperatures to allow for the use of flexible substrates. More sustainable solution processing methods, such as inkjet printing, still require a reduction of processing temperature to allow the use of flexible substrates.

Regarding the performance of memristors using ZTO-baed active layers, there is no denying that they still lack the capabilities of more maturely studied material structures, such as TaOx and HfOx, in most performance metrics. However, a shift in research efforts has been taking place over the last few years, now moving towards cheaper and more sustainable material alternatives. As not only ZTO, but amorphous oxides in general start to gain a higher interest by the research community, it is expected that the pace of progress will also start to increase. Another advantage of this material class is the coexistence of both filamentary and interface resistive switching mechanisms. Since the switching phenomena take place at the entire interface between the metal oxide and the oxide, through interface-type switching, volatile accumulative weight updating is easily achieved.[58] Furthermore, due to the inherent light-sensitive properties of ZTO, it is possible to induce resistive switching with light stimuli, widening the potential for artificial visual system applications.[74]

The choice of contact materials is also an important factor to consider. Although rare metals such as platinum are widely used, it would not be sensible to aim toward a sustainable active layer alternative while overlooking the choice of electrode materials. Alternatives to noble metals and critical raw materials (e.g., molybdenum) are essential to decrease the dependence on scarce resources, reduce the overall cost, and minimize the environmental impact of fabrication.

Although further research and optimization are still required, such as alternative fabrication processes to CVD and solution-processing, there is a clear potential for ZTO-based memristive devices to be a disruptive force in sectors that take into account biocompatibility, sustainability, and low power consumption, such as medical and display applications.

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

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