

# Towards Reliability- & Variability-aware Design-Technology Co-optimization in Advanced Nodes: Defect Characterization, Industry-friendly Modelling and ML-assisted Prediction

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**Abstract—** Reliability- & variability-aware Design Technology co-optimization (RV-DTCO) becomes indispensable with advanced nodes. However, four key issues hinder its practical adoption: the lack of characterization technique that offer both accuracy and efficiency, the lack of defect model with long-term prediction capability, the lack of compact model compatible with most EDA platforms, and the low efficiency in circuit-level prediction to support frequent iterations during co-optimization. Demonstrating with 7nm technology, this work tackles these issues by developing an efficient characterization method for separating defects, introducing a comprehensive test-data-verified defect-centric physical-based model & an industry-friendly OMI-based compact model, and proposing a machine learning-assisted approach to accelerate circuit-level prediction. With these achievements, a RV-DTCO flow is established and demonstrated on 3nm GAA technology to bridge the material level to the circuit level. The work paves ways in boosting adoption of RV-DTCO in both circuit design & process development for ultimate nodes.

**Index Terms—** Design Technology co-optimization (DTCO), FinFET, reliability, variability, Discharging-based multi-pulse technique (DMP), OMI, ST-GNN

## I. Introduction

IN the era of post-Moore where performance growth becomes difficult from simply the technology scaling, Design-Technology co-optimization (DTCO) has been considered indispensable [1]. Comparing with the optimization for power/performance/area (PPA), the incorporation of reliability and variability considerations becomes essential for mission-critical applications, such as those found in the automotive [2] and healthcare sectors [3]. While DTCO with time-zero variability has been well-established [4], addressing

time-dependent reliability and variability within the DTCO framework remains a challenging endeavor. Recent efforts have been made to develop a reliability- and variability-aware DTCO (RV-aware DTCO) flow to tackle these challenges [5]–[9]. However, for the practical adoption of the RV-aware DTCO flow, several critical issues need to be addressed and resolved, which include:

**i. Efficient and accurate characterization technique is required.** Existing characterization methods can be broadly categorized into bottom-up and top-down approaches. The bottom-up approach, such as random telegraph signal (RTS) [10], [11] and time-dependent defect spectroscopy (TDDS) technique [12], investigate the statistics of individual fluctuations in selected samples and thus are quite time-consuming. The top-down approach, such as extended measure-stress-measure (eMSM) [13], [14] and on-the-fly (OTF) [15], [16], captures the devices' macroscopic degradation and relies on mathematical fitting to decompose the contributions of different types of traps, however, too many fitting parameters may lead to uncontrollable errors in long-term prediction.

**ii. Existing effects (reliability, variability) lack test-proven capability for long-term prediction, which is critical for analog & mixed-signal designs.** Due to the stochastic nature of oxide defects, time-dependent variability induced by device degradation becomes critical, potentially impacting the end-of-life performance of circuits. Consequently, there is an urgent need for a test-proven prediction methodology that can accurately assess long-term variability, in addition to reliability. To the best of our knowledge, a comprehensive and reliable solution that addresses these challenges has yet to be developed.

**iii. Solutions based on the standard model interface are needed.** As an interface for the modification of SPICE model parameters that is supported by mainstream simulators, the CMC open model interface (OMI) [17]–[19] has gradually become an industry standard platform for evaluating circuit reliability. By developing reliability models that are compatible with the standard interfaces such as OMI, the proposed solutions can be applied to various circuit simulators, thus reducing the support costs and improving accessibility for both suppliers and end-users alike.

**iv. A fast assessment methodology that applicable for (large-scale) circuit-level reliability is needed.** Since RV-aware DTCO necessitates numerous iterations between

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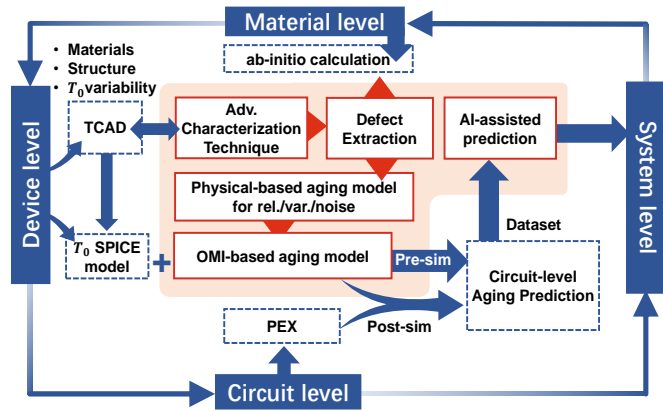


Fig.1. Reliability- & Variability-aware Design-Technology Co-optimization (RV-aware DTCO) methodology from material to circuit level proposed in this work. Based on the proposed defect-centric characterization and extraction technique, Physical-based and OMI-based aging model is established. ML-assisted prediction method is proposed to accelerate aging prediction of large-scale circuits.

process and circuit design, efficient evaluation techniques are crucial for minimizing development time and costs. Traditional approaches employed in commercial EDA tools often require substantial computational resources for circuit-level reliability prediction, resulting in slow and time-consuming analyses. Therefore, developing a fast and efficient (large-scale) circuit-level reliability evaluation methodology would not only reduce costs but also significantly shorten the development period of DTCO, paving the way for rapid innovation and the implementation of reliable electronic devices in various applications.

In this work, we proposed a novel RV-aware DTCO framework aiming to resolve above issues and accelerate the practical adoption of RV-aware co-optimization from material to circuit (Fig.1). This is made possible by achieving the following advances in this work:

1) An analytical method is proposed to separate different types of defects directly from the measured degradation, enabling accurate characterization of each type of defect while eliminating the need for time-consuming and laborious statistical analysis.

2) Proposed a defect-centric physical-based model that enables accurate long-term reliability and variability predictions, as well as an OMI-based compact model for effective simulation in the circuit level.

3) The proposed physical model is not only verified by

TABLE I

|   | This work | 2022 IRPS [5] | 2021 VLSI [6] | 2019 TED [7] | 2013 IEDM [8] |
|---|-----------|---------------|---------------|--------------|---------------|
| Experimental extraction of defect             | ✓         | ✓             | ✗             | ✗            | ✓             |
| Ab-initio verified                            | ✓         | ✓             | ✗             | ✗            | ✗             |
| Independent-verified long-term physical model | ✓         | ✓             | ✗             | ✗            | ✗             |
| Compact model                                 | ✓         | ✗             | ✓             | ✓            | ✓             |
| Industry standard Interface(OMI)              | ✓         | ✗             | ✗             | ✗            | ✗             |
| Acceleration for fast iteration in DTCO flow  | ✓         | ✗             | ✗             | ✗            | ✗             |

Advances of the existing solutions to address the challenges of RV-aware DTCO. Our proposed methodology includes all the listed features from Ab-initio calculation, experimental extraction of defect, reliability & variability simulation to acceleration technique for large-scale circuits assessment.

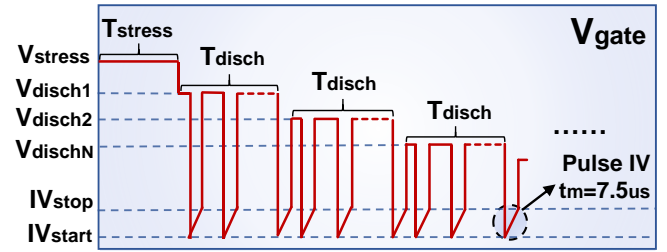


Fig.2. Illustration of the discharging-based multi-pulse (DMP) technique. In the charging phase, NBTI stress is applied to the DUT under desired stress level ( $V_{stress}$ ) for pre-set time ( $T_{stress}$ ). And in the discharging phase, gate voltage is lowered down step-by-step to gradually discharge the traps. Drain, source and substrate terminals should be connected to ground all the time except for  $I_d$ - $V_g$  measurement.

independent test results but the extracted trap properties can be well correlated to ab-initio calculation, which can be used in investigating the physical origins of traps and helpful for process optimization.

4) Proposed a Machine learning (ML)-based approach for the fast circuit-level RV prediction, providing a feasible solution for accelerating iterative processes in the DTCO framework.

**Table.I** summarizes the key advancements of our proposed framework over existing solutions in the field.

## II. ADVANCED DEFECT SEPARATION AND CHARACTERIZATION TECHNIQUE

### A. Discharging-based multi-pulse technique

By trap filling and the following gradual discharging, the discharging-based multi-pulse technique (DMP) [20] has been shown as a powerful tool in understanding oxide traps in transistors with different structures [21], channel materials [22], and dielectrics [23]. The test pattern of DMP is shown in Fig.2. In the charging phase, the device under test (DUT) is prepared by biasing the gate to the desired stress level ( $V_{gstress}$ ) for the pre-set time ( $T_{stress}$ ) while connecting the other terminals (source, drain & substrate) to ground. In this work, the time duration of 10s, 100s, 1000s, and 10000s are used during stress phase. And then in the discharging phase, the gate voltage is lowered down by  $\Delta V$  to the first discharging level,  $V_{disch1} = V_{gstress} - \Delta V$ . This discharging phase will last for  $T_{disch}$ , during which several  $I_d$ - $V_g$  measurements will be carried out. To reduce trap's recovery during the measurement,  $I_d$ - $V_g$  curve is captured at the pulse edge within 7.5us. Once reaching  $T_{disch}$ , the discharge voltage lowers down to  $V_{disch2} = V_{gstress} - 2 * \Delta V$  for another  $T_{disch}$ . By repeating this procedure until  $V_{dischN}$

TABLE II

| Detailed information of DMP test in this work |   |
|---|---|
| $V_{stress}$ (or $V_{gstress}$ )              | -0.8V \ -1.0V \ -1.2V \ -1.4V \ -1.5V \ -1.6V \ -1.7V \ -1.8V |
| $T_{stress}$                                  | 10s \ 100s \ 1000s \ 10000s                                   |
| $V_{disch1}$                                  | $V_{stress} - \Delta V$                                       |
| $\Delta V$                                    | -0.1V   |
| $V_{dischN}$                                  | +1V   |
| $T_{disch}$                                   | 5s  |

1.  $V_{dischN}$  is the last discharge voltage in DMP procedure.

2. At each  $V_{dischN}$ , the measure-stress-measure (MSM) sequence was carried out and lasts for 5s ( $T_{disch}$ ).

Detailed information of DMP test in this work.

reaches +1.0V in the  $N_{th}$  step. This  $V_{dischN}$  is properly selected to ensure the probing of deep traps while not introducing extra e-trapping. As mentioned above, we call the test pattern of **Fig.2** as one DMP test, if we repeat the DMP test on the same device, and each time the stress voltage ( $V_{gstress}$ ) is greater than the last time, we call this test procedure as multi-DMP (m-DMP) test [23]–[25].

In this work, we chose the industrial-grade 7nm pFinFETs for the demonstration. The test is carried out by using the Keysight B1530A equipped with waveform generator / fast measurement unit (WGFMU). The pulse IV is performed in linear region ( $I_{dlin}$ ) with  $V_d = -0.05V$ , and the threshold voltage  $V_{th}$  is monitored at a constant drain current of  $1 \mu A \times W/L$ . The testing temperature is  $125^\circ C$ , and other detailed information of DMP test is shown in **Table.II**.

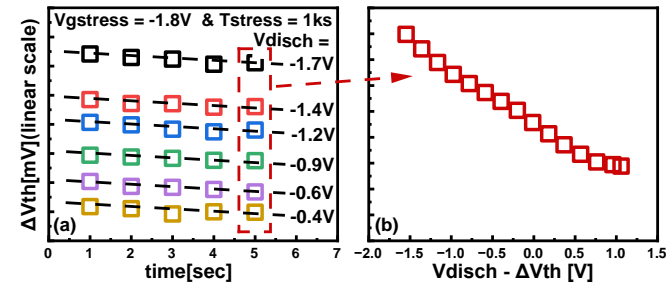


Fig.3. (a) The discharging trace under each  $V_{disch}$  in DMP test. (b) By extracting the last point under each  $V_{disch}$ , the relationship between the discharging voltage and the corresponding degradation can be obtained.

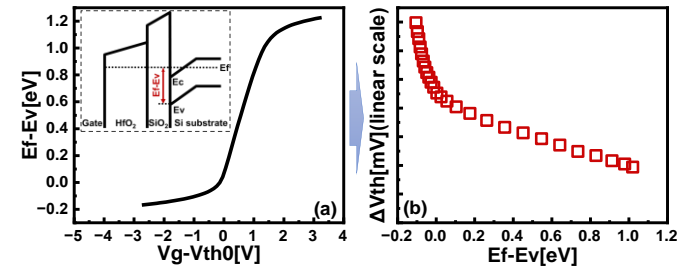


Fig.4. (a) The  $E_f - E_v$  against  $V_g - V_{th0}$  from calibrated TCAD simulation.  $V_{th0}$  is the threshold voltage of a fresh device without suffering degradation. (b) By converting  $V_{disch} - V_{th0} - \Delta V_{th}$  to the  $E_f - E_v$ , the trap's equivalent energy level can be obtained. ( $V_{disch}$  is equivalent to  $V_g$ )

### B. DMP test result preprocessing

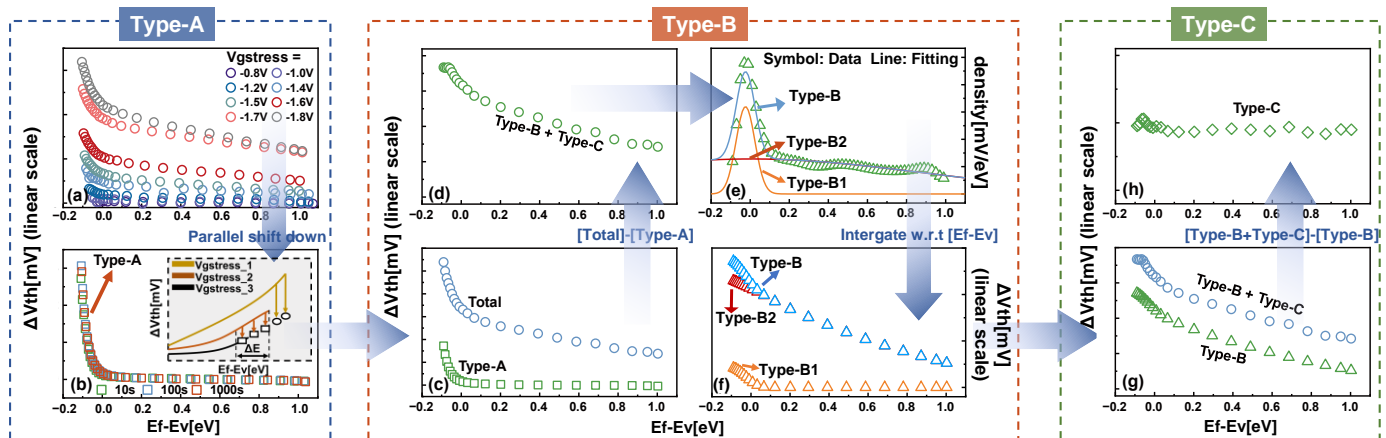


Fig.5. Proposed procedure to separate different types of traps. Based on DMP technique under different stress biases, three types of traps are clarified and separated. Type-A captures holes without changing energy levels while type-B shifts energy levels after hole capturing. Type-C presents constant energy levels and agree with interface states.

After NBTI stress for preset stress voltage ( $V_{stress}$ ) and stress time ( $T_{stress}$ ), the traps are gradually detrapping under each discharge voltage ( $V_{disch}$ ) as shown in **Fig.3a**. By extracting the last point under each  $V_{disch}$ , the relationship between the discharging voltage and the corresponding degradation can be obtained as shown in **Fig.3b**. Through the relationship between  $E_f - E_v$  and  $V_g - V_{th}$  obtained by calibrated TCAD simulation (**Fig.4a**), we can convert  $V_{disch} - V_{th} - \Delta V_{th}$  to the energy level of  $E_f$  with respect to  $E_v$  at the Si/interfacial layer (IL) interface, i.e. ( $E_f - E_v$ ) [26], and then the trap's density distribution against different energy levels can be obtained (**Fig.4b**). It is worth noting that such an energy level is the equivalent energy level that assumes the traps are located at the interface between the Si/IL, but not the true trap level in the system. Such transformation aims at the separation of different traps based on their energy profiles in the next section.

### C. Equivalent energy profile of different traps

The separation flow of different traps based on their equivalent energy profiles is shown in **Fig.5**: When the

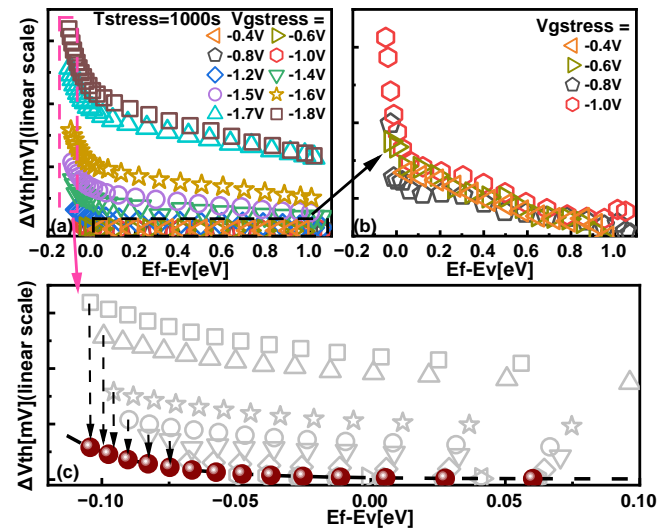


Fig.6. (a) The trap's energy profiles under different charging bias. (b) When charging bias is low, the energy profiles at different  $V_{gstress}$  overlap well, indicating that the trap energy level does not change after charging. (c) By shifting down the energy profiles of the higher bias and aligning them with profiles under lower bias, the energy profile of Type-A trap can be obtained.

charging bias ( $V_{gstress}$ ) is low, the energy profiles extracted from discharging after filling at different  $V_{gstress}$  overlap well (Fig.6b), while they deviate from each other for higher  $V_{gstress}$  (Fig.5a & Fig.6a), suggesting that there exist two types of traps in the oxide for such phenomenon [22]. For Type-A traps, if filled at a certain voltage, it can also be released at the same voltage when the bias is lowered, indicating that the trap energy level does not change after charging. In contrast, Type-B traps need to be released at an energy level lower than where they are filled, implying that Type-B may shift energy levels to a deeper level after hole capturing and exhibit the nature of switching traps. Because Type-B can only be discharged at a much lower energy level, for every two neighboring curves, by shifting down the energy profiles of the higher bias and aligning them with profiles under lower bias, Type-B traps will be removed. As illustrated by the red points in Fig.6c, the aligned curve represents the energy profile of Type-A trap.

According to the above method of separating Type-A, the Type-A traps extracted from multi-DMP measurements under different charging time is shown in Fig.5b, they overlap each other, suggesting the nature of fast saturation.

We then subtract Type-A from the total degradation, as shown in Fig.5c&d, the remaining part contains both oxide traps and interface traps. What is worth noting is that even during discharging under different  $E_f - E_v$ , the threshold voltage ( $V_{th}$ ) is always sensed at the constant current, which can be approximately considered as the same surface potential. Therefore, the contribution from interface traps (labeled as Type-C traps) in the measured  $V_{th}$  shift is the same for different  $E_f - E_v$ . The impact of interface traps can thus be removed through the mathematical differentiation with respect to the energy levels. As shown in Fig.5e, Type-B shows a broad distribution in energy levels and it cannot be fitted by a single Gaussian distribution. Therefore, we introduce a dual Gaussian distribution and a good fitting can be achieved, which indicates the existence of two types of oxide traps. We label the narrow one as Type-B1 and the wider one as Type-B2. By fitting with two Gaussian distributions and integrating along the energy

levels, the total Type-B traps (Type-B1&Type-B2) can be extracted, as shown in Fig.5f. Finally, by subtracting Type-A, Type-B1, and Type-B2 from the total degradation in Fig.5g, Type-C can be obtained, exhibiting a constant value against energy level in Fig.5h, which seems that it is hard to be "discharged". However, just as mentioned above, its independence of energy level is just because of the same sensing level.

#### D. Charging kinetics of different traps

Understanding the charging kinetics of each type of traps can be critical for modelling long-term reliability and variability. To separate different traps from their charging kinetics, the extended measure-stress-measure (eMSM) sequence is adopted. The kinetics of Type-C trap (i.e. interface traps) should be extracted first from DMP test of different stress time as shown as '◇' in Fig.7a. Since Type-A can quickly saturate (Fig.5b), the kinetics of Type-B at longer time can be derived by subtracting Type-C and the saturated Type-A ('Δ' in Fig.7a). By assuming both Type-B and Type-C traps exhibit a power law relationship, and back-extrapolating them, the kinetics of the Type-A trap can be obtained ('□' in Fig.7a) via subtracting

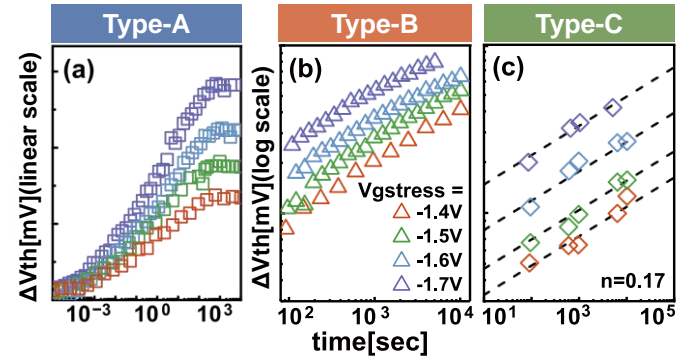


Fig.8. The extracted charging kinetics of (a) Type-A traps, (b) Type-B traps and (c) Type-C traps with stress time under varying stress biases. The charging kinetics can be well fitted by power law relationship with the time exponent of 0.17.

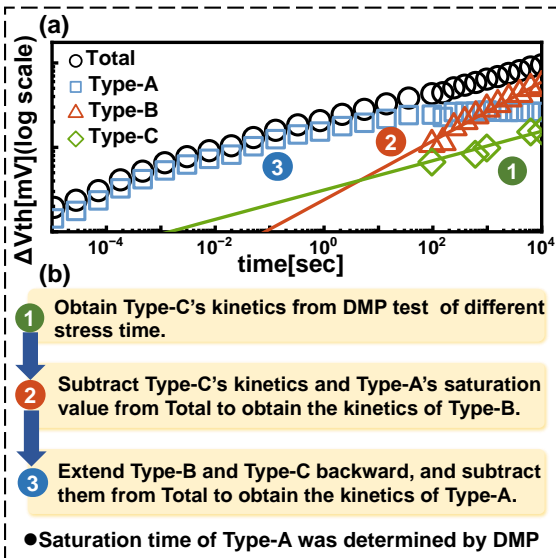


Fig.7. (a) The extracted charging kinetics of three types of traps under specific stress condition. (b) Charging kinetics extraction procedure of three types of traps.

TABLE III

|                      | Model   | Fitting parameters  |
|----------------------|---|---|
| Type-A (2 state NMP) | $k_{12} = p v_{th} \sigma \vartheta e^{-\beta \epsilon_{12}}$ $k_{21} = N_v v_{th} \sigma \vartheta e^{-\beta \epsilon_{21}}$   | $(\langle E_T \rangle, \sigma_{ET}, \langle S \rangle, \sigma_S, \sigma_{ccs}, N_T)$                    |
| Type-B (3 state NMP) | $k_{11} = A * \exp(B * E_{ox}) * [1 - \exp(-(t/\tau)^\beta)]$ $k_{12} = p v_{th} \sigma \vartheta e^{-\beta \epsilon_{12}}$ $k_{21} = N_v v_{th} \sigma \vartheta e^{-\beta \epsilon_{21}}$ | $(\langle E_T \rangle, \sigma_{ET}, \langle S \rangle, \sigma_S, \sigma_{ccs}, N_T, A, B, \tau, \beta)$ |
| Type-C (power-law)   | —   | $\Delta V_{th} = A * V_g^m * t^n$ $(A, m, n)$   |

Established Physical-based defect model for three types of traps and their corresponding parameters used for fitting. In these equations,  $p$  is the concentration of holes in the channel,  $N_v$  is effective density of states valance band,  $v_{th}$  is the thermal velocity of the carriers within the channel,  $\sigma$  represents capture cross section, and  $\vartheta$  denotes Wentzel-Kramers-Brillouin (WKB) tunneling factor,  $\epsilon_{12}$  and  $\epsilon_{21}$  denote the barrier heights for transitions between these two wells, respectively. Other parameters such as  $A, B, \tau, \beta, m, n$  are fitting parameters.



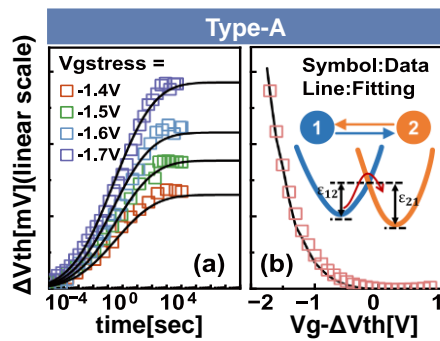


Fig.9. (a) The charging kinetics and (b) equivalent energy level distribution of Type-A traps can be well modelled by the two-state non-radiative multiphonon(NMP) theory.

Type-B and Type-C from the total degradation. Fig.7 summarizes the entire extraction procedure. By repeating the procedure, the kinetics of different types of traps under different voltages can be obtained (Fig.8).

### E. Physical-based Defect Model

After directly separating different types of traps from the experimental data following the characterization technique above, we can extract physical parameters of each trap according to their respective physical-based model by fitting. In this work, we assumed that, for each type of trap, its physical property including the energy level and the relaxation energy follows the Gaussian distribution. Their mean values and variances are obtained by fitting each trap's charging kinetics and their equivalent energy level distributions (Fig.9&10) with their respective model in Table III. What is worth noting is that due to the incomplete discharging at each discharge phase in DMP test, we also put discharging time, discharging voltage of each discharge phase and the corresponding  $\Delta V_{th}$  into energy profile's fitting.

**Type-A traps:** Type-A traps capture a hole without altering their energy levels, which suggests that the microscopic structure undergoes negligible rearrangements. This behavior is consistent with the properties of structural defects that are widely observed in amorphous systems, where the disordered nature of these materials leads to a variety of defect states [27]. To better understand the trapping/de-trapping process of Type-A traps, a simplified two-state model based on the non-radiative multiphonon (NMP) theory is employed [28], [29]. This model effectively captures the fundamental mechanisms governing the transitions between the two states.

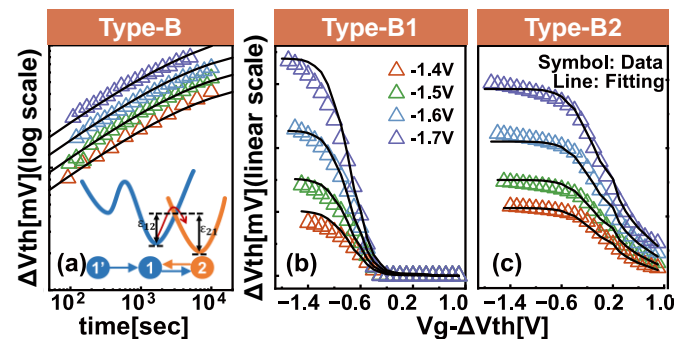


Fig.10. (a) The charging kinetics of Type-B (B1&B2) traps, (b) equivalent energy level distribution of Type-B1 traps, and (c) equivalent energy level distribution of Type-B2 traps can be modelled by incorporating the activation state into the two-state NMP theory.

The schematic of the two-state model is shown in Table.III, in which energy wells 1 and 2 represent the energy of two states before and after trapping, respectively.  $\epsilon_{12}$  and  $\epsilon_{21}$  denote the barrier heights for transitions between these two wells, respectively. Once the negative stress voltage is applied, the barrier height  $\epsilon_{12}$  is lowered, which facilitates more holes jump over the barrier through thermal emission. To account for the distribution, a Gaussian distribution for the trap energy ( $E_T$ ) and relaxation energy ( $S$ ) is assumed. As shown in Fig.9, the charging kinetics and equivalent energy level distribution of Type-A traps can be well described by the 2-state NMP model.

**Type-B traps:** To account for the lattice relaxation process, the behaviors of both Type-B1 and Type-B2 traps are modelled by a three-state process as shown in Table.III, which captures the complex dynamics involved in the charging process and provides a more accurate representation of such type of traps. During charging, the trap needs to be initially activated from state 1' to state 1, after which the charging can proceed from state 1 to state 2. By fitting the charging kinetics of Type-B traps (i.e. Type-B1&Type-B2 obtained from Fig.8(b)) and the DMP results of both Type-B1 and Type-B2 (data from Fig.5f), the model parameters can be determined. As demonstrated in Fig. 10a-c, the lines generated from the model exhibit a good agreement with the experimental results. It is worth noting that without considering the activation process ( $1' \rightarrow 1$ ), the kinetics of Type-B traps cannot be well fitted, which further confirms the switching nature of Type-B traps, highlighting the necessity of incorporating this additional state into the modeling process.

**Type-C traps:** As depicted in Fig. 8c, the degradation behaviour of Type-C traps can be described using the classical power law relationship. The time exponent is found to be 0.17, which is also broadly observed in recent years across multiple technologies by using the delay-corrected DCIV technique [30] or by probing  $V_{th}$  degradation under conditions where hole trapping is minimal. Historically, the time exponent was considered as a signature of interface state generation controlled by the Reaction-Diffusion (R-D) process. In this process, it is assumed that the Si-H bond breaks at the Si/IL interface and diffuses as a hydrogen molecule into the oxide [31]. However, theoretical studies have suggested that the Si-H bond can be rather stable [32], casting doubt on the validity of the R-D process as the primary mechanism. Recently, an alternative explanation has been proposed, suggesting that the breakage of Si-H bonds may be resulted from their reaction with atomic hydrogen originating from either the substrate [33] or the gate [34]. This reaction proceeds through an exothermic process:  $\text{Si-H} + \text{H} \rightarrow \text{Si} + \text{H}_2$ . This new hypothesis provides a more plausible mechanism for the observed behaviour, taking into account the stability of the Si-H bond.

## III. AB-INITIO CALCULATION

### A. Discussion on the physical origin

The trap level ( $E_T$ ) and relaxation energy ( $S$ ) can be used as the signature to pursue the physical origin of the traps. Therefore, we can compare the  $E_T$  and  $S$  values obtained by fitting the experimental data with the results calculated by ab-initio calculation for the defects of different configuration to explore the potential physical origin of the three types of traps.

The formation energy of defects can be evaluated as

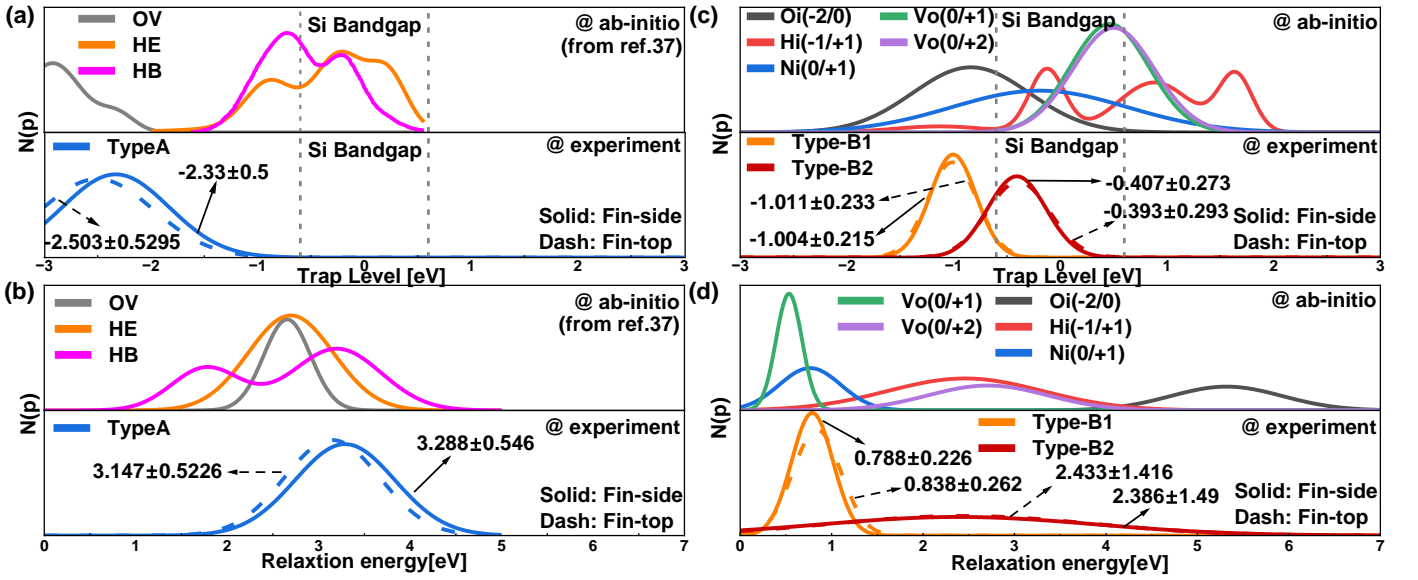


Fig.11. Comparison of the Ab-initio calculation and experiment for (a) energy level and (b) relaxation energy of Type-B (B1&B2) in the HK layer.

$$E_F = E(\partial, q) - E(host) + \sum_i n_i (E_i + \mu_i) + q[E_{VBM}(host) + E_f + \Delta V]$$

where  $\partial$  is the type,  $q$  is the charge state,  $E(\partial, q)$  is the system energy with defect and charge,  $E(host)$  is the energy of the perfect system,  $n_i$  is the number of element,  $\mu_i$  is the chemical potential relative to the element material,  $E_{VBM}$  is the host valence band maximum (VBM).  $\Delta V$  is the difference of electric potential between perfect and defect systems with a place far away from the defect.  $E_T$  between the charge  $q_1$  and  $q_2$  can be extracted from the Fermi level where the formation energy of  $q_1$  is equal to that of  $q_2$ .  $S$  can be obtained through relaxing the configuration from the equilibrium for charge state  $q_1$  to the equilibrium for another charge state  $q_2$  [35].

For defects in SiO<sub>2</sub>, several candidates have been suggested, including the oxygen vacancies (Vo) [36], the hydrogen bridge (HB) and the hydroxyl E' centers (HE) [37].  $E_T$  and  $S$  have been systematically calculated in ref.37. The comparison between the theoretical and the experimental values is shown in Fig.11a&b. Both HB and HE defects have a considerable part of components within the Si bandgap. However, Type-A traps are situated below the Si valence band, and their energy levels are relatively deep. Consequently, these two defect types may not be suitable candidates for Type-A traps. Oxygen vacancies (Vo) are the only defects exhibiting deep energy levels. Although the energy level of Type-A traps is slightly shallower than that of Vo, considering the potential calculation error of 0.5eV in density functional theory (DFT) [37], a strong correlation between Type-A and Vo is plausible. Furthermore, the experimental and theoretical values of  $S$  are in good agreement. Therefore, Type-A can be considered as the pre-existing trap originating from oxygen vacancy. From this perspective, this finding aligns with the aforementioned assertion that Type-A traps are structural defects introduced during the fabrication process due to imperfections.

As depicted in the lower panel of Fig.11c, both Type-B1 and Type-B2 traps are shallower than Type-A traps. We constructed several potential defect structures commonly

observed in high-k (HK) layers, including oxygen vacancy (Vo) [38], Interstitial hydrogen (Hi) [39], Interstitial Nitrogen (Ni) [40] and Oxygen interstitials (Oi) [38]. The amorphous nature of the HK layer is also taken into consideration. The calculated results are presented in the upper panels of Fig.11c&d. The comparison with the experimental data suggests that Type-B1&B2 traps may originate from Ni and Hi, respectively. Since the concentration of H can be much larger than that of N, Type-B2 traps are far more abundant than Type-B1 traps, which is confirmed by the experimental data (Fig.5e-f). Interstitial H could be stabilized as either the hydrogen bridge (HB) or the hydroxyl E', which undergoes a transition to the excited vibronic state after capturing a hole. By dissipating the excess energy through the multi-phonon emission process, they can relax to a lower energy level.

#### IV. MODEL VALIDATION FOR PREDICTIVE CAPABILITY

##### A. Validation for Reliability Predictive Capability

Irrespective of the device geometry, degradation is perceived as an ensemble of traps of different types with different filling statuses. Once the average trap number of each type of traps is determined by the extracted areal density, the average degradation can be estimated by calculating the filling occupancy through the corresponding physical processes and

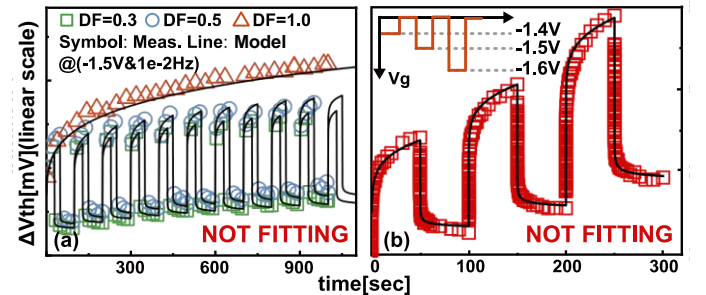


Fig.12. Comparisons of the proposed model and experiment data under (a) DC & AC conditions and (b) arbitrary waveform condition. All show good agreement between the prediction and the measurement.

summing up the results for all traps.

To demonstrate the prediction capability of the proposed model, we calculated degradation kinetics under direct current (DC) conditions, alternating current (AC) conditions with varying duty factors (**Fig.12a**), and arbitrary waveform conditions (**Fig.12b**). The results were then compared with experimental data. The comparison for duty factor and frequency dependences is also shown in **Fig.13**. Good agreement between model's predictions and the measured data serves as robust evidence supporting the validity of the proposed model. ("NOT FITTING" is used to highlight that good agreements are not from fitting data.)

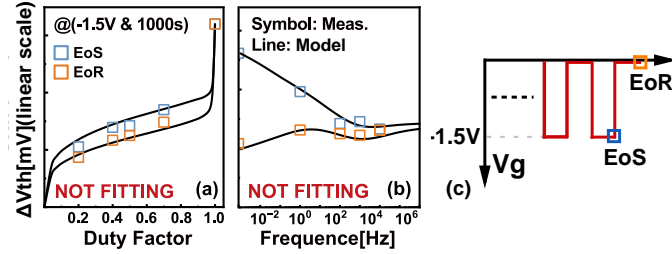


Fig.13. Comparisons of the proposed model and experiment data under AC conditions with different (a) duty factors and (b) frequencies. (c) The degradation is measured both under end of stress (EoS) and end of recovery (EoR).

Traditionally, long-term reliability under low stress voltage conditions can be predicted through extrapolation using simple power-law [41], log-law [42], or saturation power-law [43] relationships against voltage and time. We extracted the relevant model parameters by fitting experimental data under high stress voltages (ranging from -1.4V to -1.7V), and compared our model with traditional methods under  $V_g = -1.2V$  and  $T_{\text{stress}} = 50ks$ , as illustrated in **Fig.14**. The results demonstrate that our model has good long-term reliability prediction capability, whereas the power-law method tends to overestimate device degradation, and both log-law and

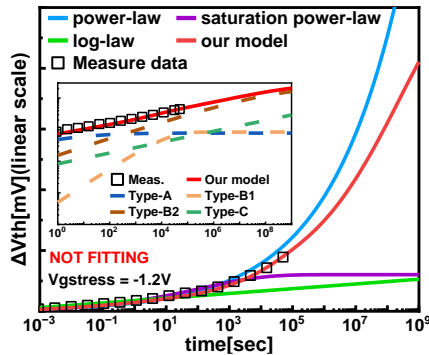


Fig.14. Comparison of our model with traditional models in long-term reliability prediction.

saturation power-law methods tend to underestimate it.

### B. Validation for Variability Predictive Capability

When time-dependent variation (TDV) needs to be considered, the average threshold voltage shift ( $\eta$ ) resulting from a single defect can be estimated through the charge sheet model. By assuming the Poisson-distributed trap number and the exponential-distributed  $\Delta V_{th}$  fluctuation [44], [45], Monte-Carlo simulations can be performed to predict the

temporal degradation for multiple devices over time. As shown in **Fig.15**, the red line represents the TDV measured on small-size devices under  $V_{g\text{stress}} = -1.3V$ , while the gray line represents the simulation results obtained through the aforementioned method. The red line essentially falls within the range of the gray line, indicating that our model also has good variability predictive capability. However, to establish a more accurate TDV model, it is necessary to obtain the average number of defects ( $N$ ) for small devices and the average threshold voltage shift ( $\eta$ ) caused by a single defect through statistical experimentation. This will be addressed and improved in our subsequent work, further refining the model's

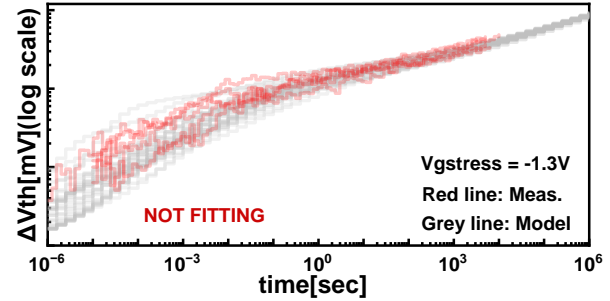


Fig.15. Monte-Carlo simulation results of the temporal device-to-device variation (DDV) induced by device degradation. The red line essentially falls within the range of the gray line, indicating that our model also has good variability predictive capability.

predictive capabilities.

We emphasize that all model parameters were extracted from DC stress data and energy profiles in **Fig.8-10** only. All the test data shown in **Fig.12-15** were not used for fitting. Moreover, all the predictions using the proposed model are based on the single set of model parameters.

## V. OMI-BASED AGING MODEL

To facilitate the circuit-level prediction with good compatibility with various circuit simulators and EDA platforms, the CMC (Compact Model Council) open model interface (OMI) is adopted. By simplifying the proposed model and assuming that the waveforms of each node can be approximated as square waves, we can model different

TABLE IV

|          | Stress stage   | Recovery stage   |
|----------|--|--|
| Type-A   | $TypeA = AR_{1(A)} \cdot \left[1 - \exp\left(-\left(\frac{t}{\tau}\right)^n\right)\right]$       | $\frac{TypeA}{TypeA(0)} = AR_{3(A)}$   |
| Type-B1  | $TypeB_1 = AR_{1(B_1)} \cdot t_s^{n_1}$  | $\frac{TypeB_1}{TypeB_1(0)} = AR_{3(B_1)}$   |
| Type-B2  | $TypeB_2 = AR_{1(B_2)} \cdot t_s^{n_2}$  | $\frac{TypeB_2 - 0.4 \cdot TypeB_2(0)}{TypeB_2(0) - 0.4 \cdot TypeB_2(0)} = AR_{3(B_2)}$ |
| Type-C   | $TypeC = AR_{2(C)} \cdot t_s^{n_3}$  | —  |
| Age Rate | $AR_1 = p_1 \cdot \exp(p_2 \cdot V_{g\text{stress}})$<br>$AR_2 = p_3 \cdot V_{g\text{stress}}^m$ | $AR_3 = \frac{1}{1+B \cdot t_r} \cdot f(V_{g\text{stress}}, t_{\text{eff\_stress}})$     |
| Total    | $TD = TypeA + TypeB_1 + TypeB_2 + TypeC$   |  |

Simplified OMI-based compact model for all types of traps, including the stress and recovery stages. In the stress stage, voltage is converted into the Age Rate (AR) with the exponential model and power-law model, the time kinetic of type-A was characterized by the stretch-exponential model, and time kinetics of other types of traps were characterized by the power-law model. In the recovery stage, recovery rate ( $AR_3$ ) was characterized by an expression with stress time and stress voltage and recovery time. The total degradation (TD) is obtained by linear superposition of all types of traps.



operating voltages and fixed recovery voltages at 0V. The Simplified OMI-based compact model is presented in **Table IV**. This compact model encompasses all characterized traps, and their kinetics can be divided into two stages: stress stage and recovery stage.

During the stress stage, operating voltage is converted into the Age Rate ( $AR$ ) with the exponential model for Type-A & Type-B traps and the power-law model for Type-C traps. Time kinetics are characterized by the stretch-exponential model for Type-A traps and the power-law model for other trap types.

During the recovery stage, the recovery rate ( $AR_3$ ) is characterized by an expression incorporating stress time, stress voltage, and recovery time. Degradation after the recovery stage is determined by the pre-recovery degradation multiplied by  $AR_3$ . Recovery is only considered for oxide traps while not for interface traps.

The total degradation ( $TD$ ) is obtained through the linear superposition of all trap types. This compact model enables handling of both stress and recovery stages with arbitrary workloads, making it a versatile tool for predicting and analyzing device degradation and circuit performance.

To validate the accuracy of the OMI-based compact model, we integrate the model into the EDA environment and perform simulations under various operating voltages over an extended period in arbitrary waveform. **Fig.16** shows the device degradation results calculated by both the **defect-based physical model** and the OMI-based compact model. It is evident from the figure that the results from both models are consistent under any working voltage over a long duration. Good agreement between the two methods demonstrates that the OMI-based compact model is well-suited for circuit-level reliability

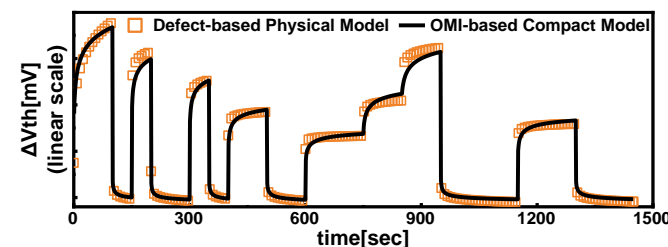


Fig.16. Good agreement between the data calculated by Defect based physical model and OMI-based compact model, making it ready to use for circuit-level reliability assessment.

assessment.

## VI. RV-AWARE DTCO DEMONSTRATION

By integrating the developed method for the trap property extraction, the physical and compact modelling into the proposed DTCO flow, the co-optimization from material level to circuit level become possible (**Fig.1**). The proposed DTCO

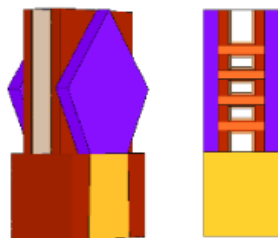


Fig.17. Illustration of the nanosheet structure simulated in this work

TABLE V

| Parameter of GAA PMOSFET                          | Value                     |
|---|---------------------------|
| Length of Channel ( $L_{ch}$ )                    | 27nm                      |
| Width of Channel ( $W_{ch}$ )                     | 35nm                      |
| Thickness of Channel ( $H_{ch}$ )                 | 5nm                       |
| Thickness of Oxide ( $T_{ox}$ , $SiO_2 + HfO_2$ ) | 0.8nm + 1.5nm             |
| Doping Conc. of Substrate ( $N_{sub,D}$ )         | $10^{15} \text{ cm}^{-3}$ |
| Doping Conc. of Source & Drain ( $N_{sd,D}$ )     | $10^{21} \text{ cm}^{-3}$ |
| Doping Conc. of Channel ( $N_{ch,D}$ )            | $10^{17} \text{ cm}^{-3}$ |

Related parameters of nanosheet structure in TCAD simulation.

framework flow is demonstrated on 3nm Gate-All-Around (GAA) technology, considering both process and aging induced device variation.

**Fig.17** illustrates the 3D structure of the GAAFET, comprising 4 nanosheets with a thickness of 5 nm individually. The length ( $L_{ch}$ ) and width ( $W_{ch}$ ) of each nanosheet is 27 nm and 35nm, respectively. The dielectric layer is composed of 0.8-nm-thick  $SiO_2$  and 1.5-nm-thick  $HfO_2$ . Related device parameters are listed in **Table V**.

Based on TCAD simulation, the variation induced by random dopant fluctuation (RDF) [46], metal gate granularity (MGG) [47] and oxide thickness variation (TOV) [48] are taken into account in device time-zero performances simulation using the impedance field method [49]. The impedance field method (IFM) offers a highly convenient, efficient, and accurate technique for statistical variability analysis. The core essence of IFM is to treat randomness as perturbation of reference device. Rather than solving the Poisson and drift-diffusion equations for numerous random device realizations, a 3D TCAD solution is required only once for the reference device. The simulation process can be outlined in the following two steps:

- Conduct a perturbation simulation at each grid point, evaluating the variation of each relevant quantity;
- Calculate the linear current response of the TCAD solution based on the precomputed quantities to obtain the corresponding I-V characteristics, and subsequently compute the statistics for all relevant quantities.

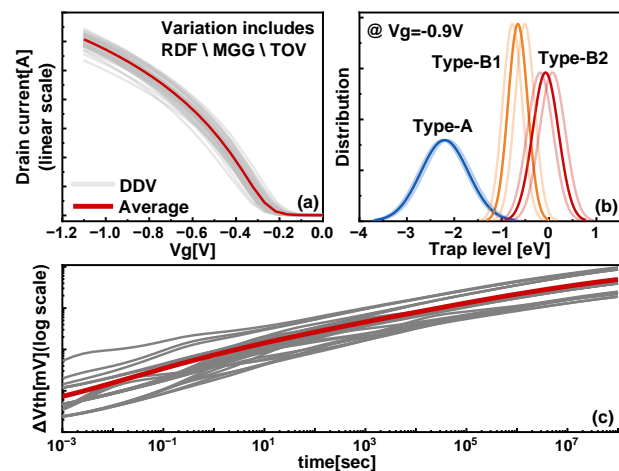


Fig.18. (a) Simulated time-zero performances considering RDF, MGG and TOV variation sources. (b) The modulation of process variation on energy levels of different types of traps. (c) Simulated temporal device variations considering both process variation and aging induced variation by stochastic nature of each type of trap.



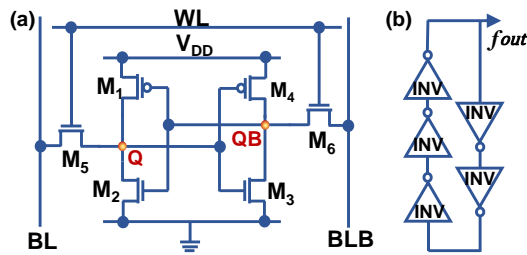


Fig.19. Schematics of the simulated (a) 6T-SRAM cell and (b) ring oscillator (RO). By analyzing the SRAM static noise curve (SNM) and the output frequency of the RO to assess circuit-level reliability.

As is shown in Fig.18a, the variation of  $I_d$ - $V_g$  curve induced by unsatisfactory process factors can be well simulated. Due to the modulation of process variation on the defect's local electrical field, the alignment of defect energy levels with the valence band will be changed, even under identical gate biases, indicating the coupling between process and aging-induced variation (Fig.18b). By combining these two sources of variation, the device's variation induced by aging & process induced variation can be predicted (Fig.18c).

Extending to circuit level, Fig. 19 showcases circuits used to evaluate circuit-level reliability, including a 6T-SRAM cell (Fig.19a) and 5-stage ring oscillator (RO) (Fig.19b). To assess the reliability of the SRAM, we analyze the degradation of the static noise margin (SNM) over time. For the RO, we evaluate its reliability by examining the degradation of the output frequency with aging time and different operating voltages.

Fig. 20(a) shows the degradation of SRAM. The green curve represents the initial SNM with a fresh device, and the dashed rectangle indicates the maximum noise tolerance. As the two pull-up transistors (M1&M4) degrade over time (with only PMOS degradation considered in the simulation), it becomes increasingly difficult for nodes Q and QB to transition from GND to VDD, necessitating a larger negative bias to drive M1 and M4 to pull the nodes up to the VDD level. Consequently, the butterfly curve shifts from green to red, and the solid rectangle, which represents the maximum noise tolerance, continually decreases. Fig.20(b) demonstrates the degradation of output frequency in the RO. As the transistors degrade, the

inverter's driving ability weakens, and the propagation delay increases, resulting in a continuous decline in the RO's frequency. When the operating voltage (VDD) is 0.7 V, the degradation of output frequency reaches nearly 10% after 10 years. As VDD increases, the RO's lifetime correspondingly decreases.

The above results highlight the severity of circuit-level aging, underscoring the importance of identifying which type of trap causes such significant degradation. By pinpointing the source of this degradation, we can develop strategies to optimize the fabrication process and improve device reliability.

Fig. 20c&d exhibit the contributions of each type of traps to the SRAM and RO cells, respectively. In the initial stage of the SRAM cell, the degradation is relatively small, as shown in Fig. 20c. Type-B's contribution rapidly increases with aging time, with Type-B1 and Type-B2 accounting for approximately 40% and 60% after 0.5 years, respectively. Due to the saturation of Type-B1 and the growth of Type-B2, Type-B2's contribution rises to about 90% after 10 years. A similar situation occurs in the RO cell, where Type-B1 and Type-B2 are the primary contributors to circuit degradation, while the impacts of Type-A and Type-C can be largely disregarded.

Consequently, to enhance circuit performance and reliability, it is crucial to eliminate Type-B traps (especially Type-B2) during the process optimization stage.

## VII. AI-ASSISTED PREDICTION

Traditional approach of circuit-level aging simulation adopted in commercial EDA tools requires high computation resources. Besides, changing simulation conditions requires re-analysis of the circuit, which takes a long iteration time and significantly increases the cost. The above shortcomings may hinder its use for the large-scale circuit reliability-aware design. To address this challenge, a fast assessment methodology based on spatial-temporal graph neural network (ST-GNN) is proposed. By taking both the structural topology and dynamic operation of the circuit into consideration, reliability prediction can be achieved with both high accuracy and efficiency.

In order to analyze circuits using GNN, it is necessary to convert circuits into graph. From circuit schematic diagram, the device can be treated as the node vector of the graph, and the connection between the device ports can be treated as the edge of the graph. The considered nodes include MOS transistors four terminals, without considering grounding, DC power supply, and AC sources. The impact factors on device reliability are included in the node feature. For example, transistor node  $X_g$  is composed of four features, namely effective channel length  $L_{eff}$ , effective width  $W_{eff}$ , gate source voltage  $V_{gs}$ , and drain source voltage  $V_{ds}$ . To simplify the

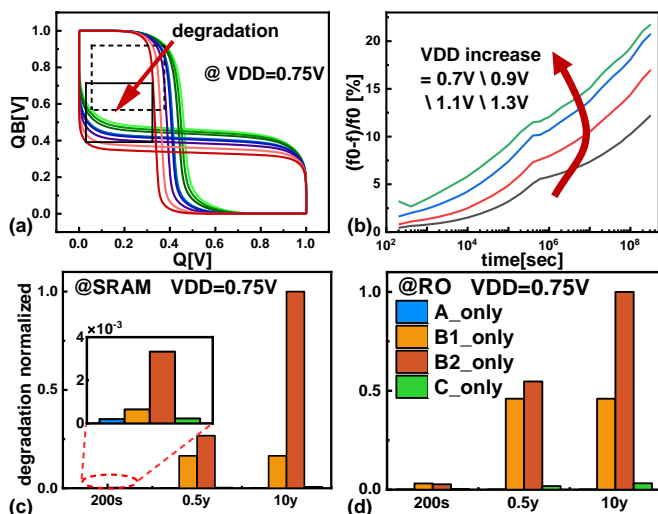


Fig.20. (a) SNM of SRAM and (b) Frequency of RO degrades with VDD and operation time. The contributions of each type of trap to (c) SRAM and (d) RO cell degradation.

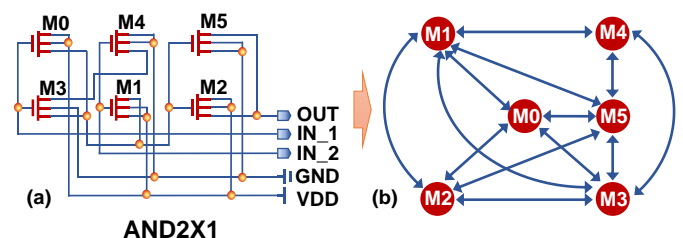


Fig.21. Illustration of how the topology of two-input AND is represented as a graph.

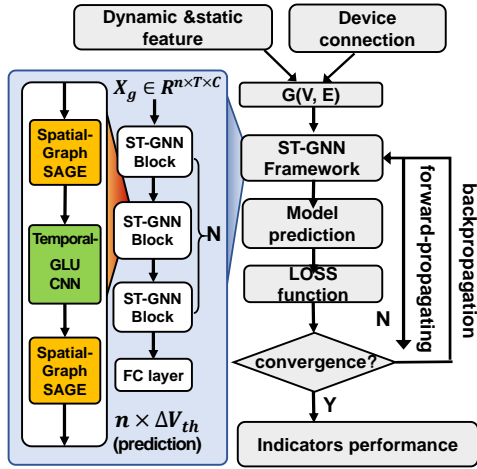


Fig.22. Training flow of the proposed ST-GNN framework. Both circuit topology and temporal information are considered.

procedure, the circuit diagram is treated as an unweighted graph, with weight values only associated with each node while not with edges. Regarding to the edge of the graph, the connections of MOS transistors: gate, source, drain, and substrate is considered as the same type of edge. **Fig.21** shows a dual input AND gate represented as an unweighted isomorphic undirected graph.

To consider both the structural topology and dynamic operation information of the circuit, the ST-GNN includes GNN of spatial domain and improved CNN (Convolutional Neural Networks) of temporal domain. GraphSAGE is adopted as the GNN model [50], which is a classical model that applies the message passing paradigm. In addition, it is a universal graph neural network that samples and aggregates neighboring nodes and generates target node embeddings in a graph. The improved CNN model of time domain processes time series composed of node features at different simulation steps, taking changes of circuit device parameters in dynamic stress simulation into account. Improved CNN adds gate linear units GLU and residual connections methods on the basis of two-dimensional convolution [51]. The GLU algorithm has a fixed length time window, in which the time series features can be compressed using convolution operations, and output control based on time information can be achieved through gating.

The ST-GNN framework consists of two blocks and one

TABLE VI

| circuit | Freq[Hz] | max error [%] |
|---------|----------|---------------|
| DFFSR   | 5.00E+09 | 1.1752825     |
|         | 2.00E+09 | 1.149435      |
| OAI21X1 | 5.00E+09 | 0.3736537     |
|         | 2.00E+09 | 0.5067706     |
| FAX1    | 5.00E+09 | 2.2061551     |
|         | 2.00E+09 | 1.119634      |
| MUX2X1  | 5.00E+09 | 0.6838623     |
|         | 2.00E+09 | 1.0061294     |
| NOR2X1  | 5.00E+09 | 0.3887624     |
|         | 2.00E+09 | 0.3836282     |
| TBUF2   | 5.00E+09 | 0.5663097     |
|         | 2.00E+09 | 1.4122184     |
| XNOR2X1 | 5.00E+09 | 0.8741502     |
|         | 2.00E+09 | 0.3939159     |
| XOR2X1  | 5.00E+09 | 0.6520148     |
|         | 2.00E+09 | 0.6376211     |

The prediction error of the proposed ST-GNN for various standard cells.

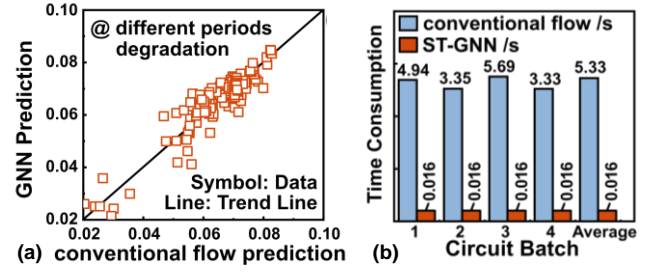


Fig.23. Comparison of the (a) prediction results and (b) time consumption between ST-GNN and conventional flow.

fully connected layer. Each block contains two GraphSAGE layers and one improved CNN layer. The GraphSAGE layer aggregates and updates nodes based on circuit diagram structural information. The improved CNN layer captures relevant temporal information in the temporal dimension. The fully connected layer is used to synthesize features and generate predicted values for device degradation. Besides, the standard library circuits with 45nm PTM are used for model training [52]. **Fig.22** shows the model framework and the process of model training.

From **Table VI**, it shows that the ST-GNN model achieves good performance in predicting aging values for different circuits and frequencies of AC source, with maximum percentage errors maintained within 2.3%. **Fig.23** (a) shows the fitting curve between predicted data and data from conventional approach, which presents small deviations compared to each other under AC source with different frequency. In addition, **Fig.23** (b) compares the calculation time of the traditional reliability model and the ST-GNN model, which indicates that the inference time of the ST-GNN framework model is significantly shorter than conventional approach for all batches of circuits, and the average acceleration ratio can reach over 200 times.

In conclusion, the ST-GNN framework can balance prediction accuracy and time overhead, laying the groundwork for future aging prediction tasks of large-scale circuits. Furthermore, applying the ST-GNN framework to EDA to predict transistor aging will contribute to improving designers' circuit design efficiency and reducing the DTCO time efforts.

## VIII. CONCLUSION

Four key issues, including efficient and accurate characterization technique, long-term prediction capability, compatibility in most EDA platforms, and the prediction efficiency to enable fast iteration, hindered the practical adoption of RV-aware DTCO. This work tackles them by 1) proposing an analytical method to separate different types of traps directly from the measured degradation, 2) proposing a unified defect-based model for accurate long-term reliability and variability aging prediction, 3) developing an OMI-based compact model for the circuit-level aging assessment, 4) developing an ML-assisted approach based on ST-GNN that enables the efficiency improvement by over 200 times compared with conventional methods. With these key advances, a new RV-aware DTCO flow is established, which bridges material properties to circuit design.

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