Study on the Degradation Mechanism of GaN MMIC Power Amplifiers under on-state with High Drain Bias

Hao Zhang, Xuefeng Zheng, Danmei Lin, Yuehua Hong, Jiuding Zhou, Ling Lv, Yanrong Cao, Hongbo Han, Weidong Zhang, Jianfu Zhang, Xiaohua Ma, and Yue Hao

***Abstract*—In this work, the electrical performance degradation and circuit burnout in gallium nitride (GaN) based microwave monolithic integrated circuit (MMIC) power amplifiers under on-state with high drain bias have been studied in-depth. It is found that when the drain bias increases from 30 V to 90 V, the saturation drain current decreases by 16%, and the output power drops significantly by 4.5 dB. With the aid of photon emission measurements (PEM) and scanning electron microscopy (SEM), it is found that catastrophic burnout occurs in the power-stage GaN HEMTs and the MIM capacitors, respectively. For the GaN HEMT, electrons in the channel can gain enough energy with the transverse high electric field to become hot electrons. One part of hot electrons can surmount the AlGaN/GaN interface barrier and then induce leakage paths in the AlGaN layer, resulting in a significant leakage current. The other part of hot electrons will collide with the lattice near the drain edge and induce significant electron trapping, which will result in a significant longitudinal local electric field. When a critical electric field is achieved, catastrophic burnout occurs. Results obtained from TCAD simulation verified it. For the MIM capacitor, the failure is attributed to the dielectric breakdown at the edge of the capacitor, which also plays an important role in the circuit deterioration.**

***Index Terms*—GaN MMIC power amplifiers, HEMTs, MIM capacitors, hot electron, electron trapping.**

I. Introduction

Gallium nitride (GaN) based microwave monolithic integrated circuit (MMIC) power amplifiers (PAs) are promising candidates for high-power and high-frequency applications due to their superior properties such as high efficiency, high output power, low loss, and compact size [1], [2]. Currently, reliability issue is still the major concern for GaN MMIC PAs. Especially, in some cases, GaN MMIC PAs operate at high voltage levels with pulse mode. It will induce a strong voltage overshoot, which may be much higher than the rated operation bias [3]-[7]. The co-existence of overshoot voltage and on-state current motivate high-energy hot electrons, aggravating the circuit deterioration of GaN MMIC PAs.

Previous investigations on the hot electron effect are mainly focused on the degradation in GaN HEMTs instead of GaN MMICs [7]-[17]. These works have reported that the worst degradation may occur in semi-on-state condition [13], [14], including on-resistance (R_{on}) increases, threshold voltage shifts, saturation current decreases, transconductance and cutoff frequency degradation, power drop, breakdown walkout, etc. Several failure mechanisms have been proposed, such as the trapping effect, the defect in the epitaxial barrier layer at the edge of the gate on the drain side [8], [9], bulk and surface traps located between gate-source (G-S) and gate-drain (G-D) [8], [12], and hot electron assisted defect formation and propagation [10], etc. However, the degradation of GaN MMICs may differ from that of discrete GaN HEMTs due to higher integration and more complex circuit structure. To the best of our knowledge, there is rare research on the degradation of GaN MMIC PAs under on-state with high drain bias. Accordingly, the failure mechanism in this case is still not well known. It hinders our understanding on the degradation of GaN MMIC PAs in high drain bias cases.

In this work, the degradation mechanism of GaN MMIC PAs under on-state with high drain bias has been investigated in-depth. It is found that the electrical degradation of GaN MMIC PAs exhibits a significant bias dependence, and the circuit burnout phenomenon is also observed. The failure mechanism based on hot electron and trapping effects was analyzed and proposed with the aid of the PEM and SEM techniques. It reveals that both the drain edge of the power-stage HEMTs and MIM capacitors in GaN MMIC PAs are the sensitive positions for circuit failure under on-state with high drain bias.

II. MMIC Process and Circuit Design

A 9.0-11.0 GHz three-stage power amplifier with a GaN-on-SiC MMIC process is studied in this work. This process provides 0.25 μm gate-length AlGaN/GaN Schottky-HEMTs. The gate-to-source and gate-to-drain distances of the devices are 0.8 μm and 2 μm, respectively. The MMIC process also provides other passive devices, such as NiCr resistor, MIM capacitor, active layer GaN resistor, low

This work was supported in part by the National Key Research and Development Project of China (Grant Nos. 2021YFB3602404 and 2023YFB3611900), by the National Natural Science Foundation of China (Grant Nos. U2241220, 12035019 and 62234013), and by the fund of National Innovation Center of Radiation Application (No. KFZC2022020401). (Corresponding author: Xuefeng Zheng)

H. Zhang, X. Zheng, D. Lin, Y. Hong, J. Zhou, L. Lv, Y. Cao, H. Han, X. Ma and Y Hao are with the State Key Laboratory of Wide-bandgap Semiconductor Devices and integrated technology, School of Microelectronics, Xidian University, Xi'an 710071, China (e-mail: xfzheng@mail.xidian.edu.cn).

W. Zhang and J. Zhang are the School of Engineering, Liverpool John Moores University, L3 3AF Liverpool, U.K.

loss microstrip lines, and through substrate via hole. The backside is electroplated with 10 μm metal for grounding.

The chip was designed as a reactively matched three-stage amplifier with three separate GaN HEMTs. The corresponding circuit design is given in Fig. 1. The first and second-stage HEMTs were used as the predriver and the driver stages, respectively, to ensure that sufficient output power and appropriate half-sinusoidal output waveforms were delivered to the final power-stage HEMT. Gate ground design, as the resistors R_1, R_3, and R_5, is used to ground the gate to achieve the self-biasing function. The source ground resistances R_2, R_4, and R_6 are used to control the current in each stage. Capacitors C_1, C_3, C_5, C_8, C_{10}, and C_{15} are used as DC blocks to isolate every bias port. The remaining capacitors and inductors are used for filtering and inter-stage matching. The output power (P_{out}) of this PA is 29.5-30.5 dBm within the band, and the breakdown voltage is greater than 130 V.

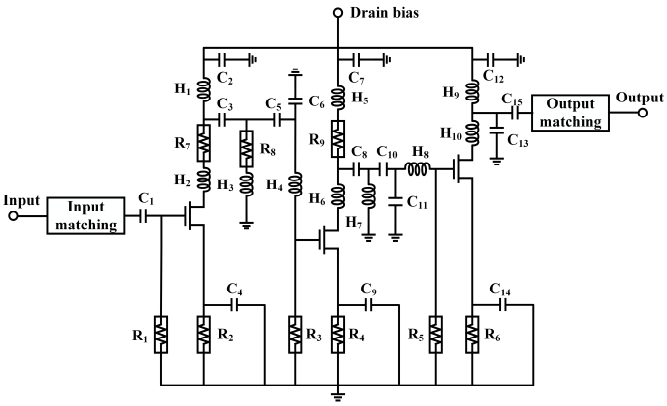

Fig. 1. Circuit diagram for the designed GaN MMIC PA in this work.

III. Experiments and Discussion

A. The Electrical Performances Degradation

The electrical characteristics of the fabricated GaN MMIC PAs are measured at room temperature. The DC output characteristic is measured with V_{DS} sweeping from 0 to 28 V with the step of 0.1 V. The RF performances are measured at 10 GHz, and biased at V_{DS} = 28 V with a quiescent current of 180 mA.

In order to investigate the degradation mechanism of GaN MMIC PAs, stress tests were performed under semi-on-state with multiple DC bias conditions, including $V_{DS\text{-}Stress}$ = 30 V, 60 V, and 90 V, respectively. Even with different V_{DS} biases, the drain current was kept at a constant value of 180 mA, which can ensure the quantity of hot electrons is constant. The maximum stress time was set to 100 ks in total or until breakdown. For each stress condition, the junction temperature was held constant at 85 °C, which can eliminate the effect of temperature-related degradation [9], [18]. The junction temperature was estimated using infrared temperature measurement system under the same conditions [24], [25]. In order to ensure the junction temperature was constant, the baseplate temperature of the thermal platform was set and adjusted actively as the drain bias increased.

The electrical characteristics of the stressed GaN MMIC PAs were measured and compared. Fig. 2(a) depicts the DC output characteristic of GaN MMIC PAs under different $V_{DS\text{-}Stress}$. It is clearly observed that DC output performance degrades as $V_{DS\text{-}Stress}$ increases and the maximum reduction of the saturation drain current (I_{dsat}) reaches 16% under $V_{DS\text{-}Stress}$ = 90 V. Fig. 2(b) shows the degradation of I_{dsat} with stress time under different $V_{DS\text{-}Stress}$. It is found that the degradation of I_{dsat} under $V_{DS\text{-}Stress}$ = 30 V is negligible. With the increasing $V_{DS\text{-}Stress}$, obvious degradation occurs. Especially when $V_{DS\text{-}Stress}$= 90 V, I_{dsat} decreases dramatically with increasing stress time, and breakdown occurs eventually when the stress time reaches 10.5 ks. It should be noted that RF parameters are more important for PA's performance evaluation in most cases. Fig. 3 depicts PAs' RF performance degradation. As shown in Fig. 3(a), it is observed that the P_{out} degradation under $V_{DS\text{-}Stress}$ = 30 V is negligible. With the increasing $V_{DS\text{-}Stress}$, however, the degradation becomes more and more significant. It should also be noted that self-oscillation occurs with a lower P_{in} (less than -2 dBm) when $V_{DS\text{-}Stress}$ achieves 60 V, and it becomes more severe as $V_{DS\text{-}Stress}$ increases to 90 V. It may be explained by circuit mismatches caused by the degradation of the active devices and bias network [19]-[23]. Fig. 3(b) shows the RF performance degradation against $V_{DS\text{-}Stress}$ at P_{in}= 10 dBm. It is evidently observed that both P_{out} and gain significantly decrease by 4.5 dB and the power-added efficiency (PAE) is reduced by 10% under $V_{DS\text{-}Stress}$ = 90 V.

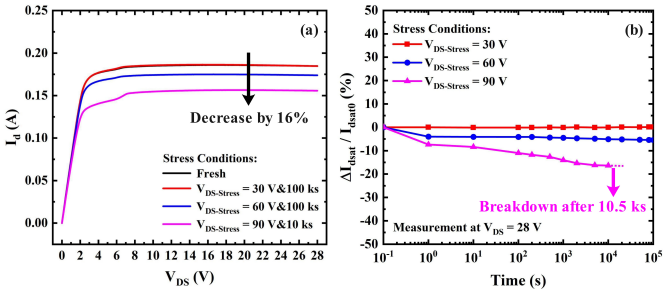

Fig. 2. The DC performance under on-state stress with different drain bias: (a) I_d-V_{DS} characteristics. (b) The normalized saturation drain current variation versus stress time.

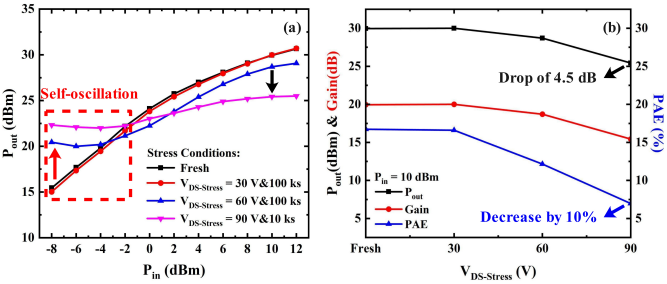

Fig. 3. The RF performances under on-state stress with different drain bias: (a) The output power vs. the input power at 10 GHz. (b) The output power, gain, and power-added efficiency (PAE) at P_{in} = 10 dBm as a function of $V_{DS\text{-}Stress}$.

B. Analysis of Current Leakage Paths

In order to gain more information about the possible physical degradation, PEM analysis was carried out on fresh and stressed GaN MMIC PAs to localize the leakage paths that were produced during the stress. Fig. 4(a) shows that the photoemission signature of the fresh device over the entire structure is insignificant, indicating the absence of leakage paths. Compared to the reference fresh device, Fig. 4(b) shows

a slight photoemission signature, indicating that insignificant damages were generated under $V_{DS\text{-}Stress}$ = 30 V. In Fig. 4(c), the hotspots start to be well visible, in agreement with the onset of electrical degradation under $V_{DS\text{-}Stress}$ = 60 V. In Fig. 4(d), stronger light emission intensities and more extensive light distributions are observed under $V_{DS\text{-}Stress}$ = 90 V. It reveals a significant rise in leakage current, which is considered one of the reasons for the degradation of electrical performance [8], [9], [16]. Two aspects should be noted in this work. First, nearly all hotspots are observed in the power-stage HEMTs instead of driver-stage ones in GaN MMIC PAs. It is because that the power-stage HEMTs suffered the worst damage due to the presence of the highest power output during stress. Second, the strongest hotspot signal appears at the drain edge (DE) of the HEMTs, as illustrated by the insets in Fig. 4(c) and (d). The above results suggest that the drain edge of the power-stage HEMTs in GaN MMIC PAs may be the most sensitive and vulnerable area under on-state with high drain bias.

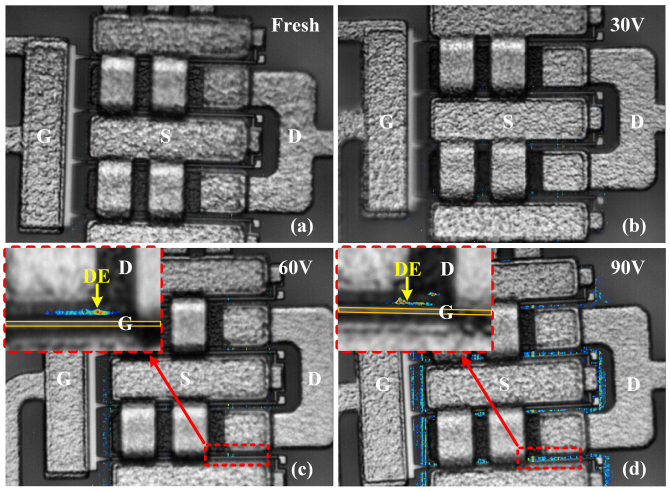

Fig. 4. PEM images of HEMTs in the power stage in on-state mode (V_{DS} =28 V) after different stress. (a) Fresh, (b) $V_{DS\text{-}Stress}$ = 30 V, (c) $V_{DS\text{-}Stress}$ = 60 V, and (d) $V_{DS\text{-}Stress}$ = 90 V. The insets show a higher magnification (×100) of the marked hotspots.

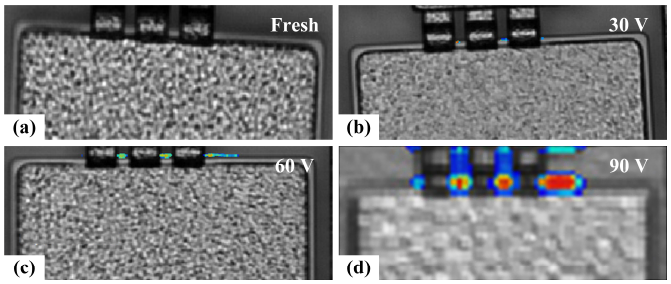

Fig. 5. PEM images of MIM capacitors in the power stage in on-state mode (V_{DS}= 28 V) after different stress. (a) Fresh, (b) $V_{DS\text{-}Stress}$ = 30 V, (c) $V_{DS\text{-}Stress}$ = 60 V, and (d) $V_{DS\text{-}Stress}$ = 90 V.

In addition to the leakage current in GaN HEMTs, failures were also observed in MIM capacitors in the power stage, as illustrated by Fig. 5. Fig. 5(a) shows the initial state of MIM capacitors. It is almost free of any leakage paths. Compared to the reference fresh capacitor, slight emission intensity was observed in Fig. 5(b), indicating that insignificant damages were generated under $V_{DS\text{-}Stress}$ = 30 V. In Fig. 5(c), the hotspots start to be well visible, in agreement with the onset of self-oscillation under $V_{DS\text{-}Stress}$ = 60 V. In Fig. 5(d), a stronger photoemission signature is observed under $V_{DS\text{-}Stress}$ = 90 V. It indicates that a significant leakage path is formed in the capacitor, which can seriously affect the stability of the bias network, leading to more severe self-oscillation even burnout. It should be noted that nearly all leakage paths are observed at the edge of MIM capacitors. This is because the electric field peak at the edge of the capacitor is denser than that in the bulk of the capacitor due to the electric field concentration effect, which will lead to dielectric breakdown at the edge. In addition, the local temperature near the power stage is higher, which can accelerate the degradation of capacitors here. The above results suggest that the failure of MIM capacitors also plays an important role in circuit deterioration, which should also be considered during the MMIC circuits assessment.

C. Defects Induced by Hot Electrons

In order to further investigate the physical origin of these leakage paths, the SEM analysis was performed on the degraded GaN MMIC PAs, which are shown in Fig. 6. The images were collected from the hotspots observed by PEM and the failure points in the burned GaN MMIC PAs. Fig. 6(a) shows the initial state of the device structure. It is clear that there is almost free of any intrinsic visible crystal defects. In Fig. 6(b), it is obviously observed that the cracks and pits start to appear around the drain edge, which is consistent with the result observed in Fig. 4. Furthermore, Fig. 6(c) and (d) show the evolution process of cracks and pits traveling from the drain edge toward the gate during the stress.

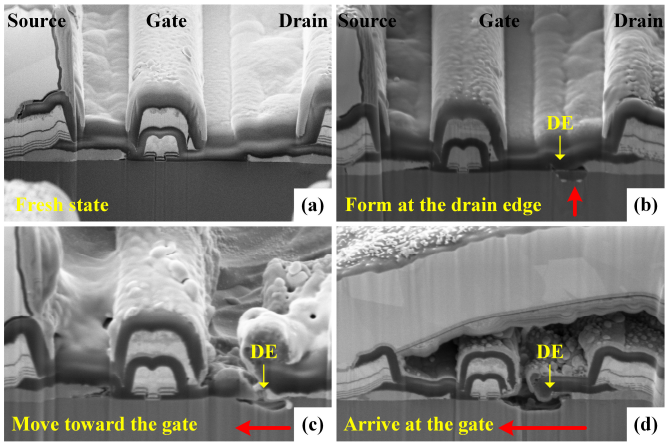

Fig. 6. FIB-SEM images show the evolution process of catastrophic failure under $V_{DS\text{-}Stress}$ = 90 V. (a) Fresh state. (b) Cracks and pits form at the drain edge (DE), (c) traveling from the drain edge toward the gate, (d) arriving at the gate. Traces of cracks and pits are marked with red arrows and explained with yellow texts.

One may suspect that the degradation and catastrophic burnout under high drain bias may be attributed to the inverse piezoelectric effect. In order to verify it, off-state stress with identical drain bias was performed on discrete GaN HEMTs fabricated in the same wafer with the identical process. In Fig. 7(a), it can be seen that the DC output performance degrades slightly as $V_{DS\text{-}Stress}$ increases. Even under $V_{DS\text{-}Stress}$ = 90 V, the maximum reduction of the saturation drain current is just 2.6%. Fig. 7(b) depicts the HEMT's RF performance degradation. It is observed that the P_{out} degradation is insignificant and only decreases by 0.4 dB even at $V_{DS\text{-}Stress}$= 90 V, which is much

lower than that in GaN MMIC PAs. The above results suggest that the electrical performance degradation caused by the off-state high drain bias is insignificant. It confirmed that the origin of electrical degradation of GaN MMIC PAs under on-state with high drain bias is not due to the inverse piezoelectric effect but rather closely related to the channel hot electrons.

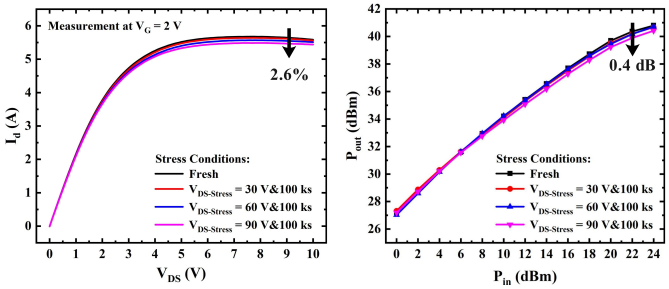

Fig. 7. The electrical performances of discrete GaN HEMTs under off-state stress with different drain bias: (a) The DC output characteristics. (d) The output power vs. the input power at 10 GHz. The static operating point is V_{DS} = 28 V, I_{dq}= 180 mA.

D. Degradation Mechanism Based on on-state Hot Electrons

In order to obtain an in-depth insight into this degradation, a hot electrons-based mechanism is proposed in this work. In Fig. 8, the schematic cross sections of HEMTs in GaN MMIC PAs are presented to understand the dynamic behavior during the stress. As shown in Fig. 8(a), when the GaN MMIC PA is biased at low $V_{DS-Stress}$ with on-state, electrons in the channel are accelerated by the transverse high electric field and then gain energy to become hot electrons accordingly. Especially, when the drain bias increases, more hot electrons with higher energy will be formed near the drain electrode, as illustrated in Fig. 8(b). Most of hot electrons can be collected by the drain electrode and form drain current. The other hot electrons are divided into two parts. One part of hot electrons with enough energy can surmount the AlGaN/GaN interface barrier and pass through the AlGaN layer. It then causes damage and induces leakage paths across it, which induces hotspots as that can be observed by PEM in Fig. 4. The other part of hot electrons will collide with the lattice in GaN buffer layer, especially near the drain edge and generate new defects. Meanwhile, these electrons can get trapped within the newly generated defects and cause significant electron trapping.

Based on the above procedure, the following side effects will be induced: 1) The density and mobility of electrons within the 2DEG channel will be reduced due to the depletion and the coulomb scattering effect of electron trapping within the buffer layer, which will decrease the DC and RF output performance. 2) With the stress time increasing, the electron trapping within the GaN layer will increase, which induces a higher electric field. The simulation results in Fig. 9 verified it. Fig. 9 shows the electric field for the devices with different amounts of buffer acceptor trap concentrations under $V_{DS-Stress}$= 90 V. It is clearly observed that the electric field near the drain electrode increases dramatically with the increasing electron trapping within the GaN buffer layer. When a critical longitudinal electric field (E_{Cr}) is achieved, a catastrophic burnout occurs near the drain edge, which can be observed as that in Fig. 6.

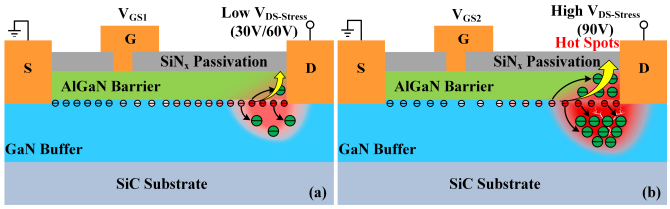

Fig. 8. Schematic cross sections of the HEMTs in the GaN MMIC PAs show channel electrons, electron trapping (Green symbols), and current leakage path (Yellow arrow) under (a) Low $V_{DS-Stress}$ and (b) High $V_{DS-Stress}$, respectively.

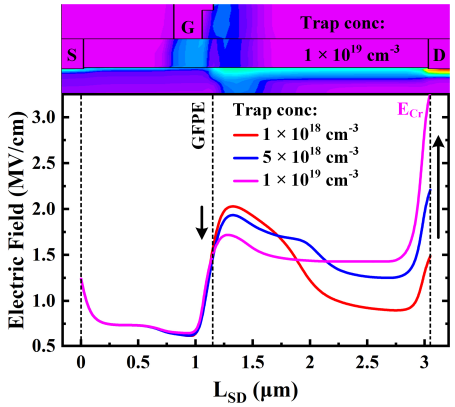

Fig. 9. The simulated electric field from the source edge to the drain edge with different acceptor trap concentrations in the buffer at $V_{DS-Stress}$ = 90 V.

IV. Conclusion

In conclusion, this work has studied the degradation mechanism of GaN MMIC PAs under on-state with high drain bias. It is found that the saturation drain current and RF output power drop significantly after the stress. Utilizing PEM, it is found that the leakage current of the MMICs significantly increases. When the drain bias increases to 90 V, a catastrophic burnout is observed on the power-stage HEMTs and MIM capacitors. With the aid of SEM and TCAD simulation, it is found that the destructive damage happens near the drain edge of the power-stage HEMTs, which is explained by the hot-electron effects and the corresponding electron trapping. With the drain bias increasing, the electrons in the channel can gain enough energy and then collide with the lattice in the buffer layer, especially near the drain edge, and generate new traps. The sequential electron trapping within these traps leads to a critical breakdown electric field. The leakage paths and burnout in MIM capacitors is observed at the edge of the capacitor, which is attributed to the electric field concentration effect. The results in this work can provide valuable information on the understanding of degradation mechanisms of GaN MMICs, which plays an instrumental role in their performance evaluation and reliability improvement.

REFERENCES

[1] K. J. Chen, O. Häberlen, A. Lidow, C. L. Tsai, T. Ueda, Y. Uemoto, and Y. Wu, "GaN-on-Si Power Technology: Devices and Applications," *IEEE Trans. Electron Devices.*, vol. 64, no. 3, pp. 779-795, March. 2017, doi: 10.1109/TED.2017.2657579.

[2] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, and W. L. Pribble, "A Review of GaN on SiC High Electron-Mobility Power Transistors and MMICs," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1764-1783, June. 2012, doi: 10.1109/TMTT.2012.2187535.

[3] W. R. Fang, W. H. Huang, W. H. Huang, J. W. Li, C. Fu, L. L. Wang, T. W. He, and Y. Cao, "X-Band High-Efficiency High-Power GaN Power Amplifier Based on Edge-Triggered Gate Modulation," *IEEE Microw. Wirel. Compon. Lett.*, vol. 30, no. 9, pp. 884-887, Sept. 2020, doi: 10.1109/LMWC.2020.3013146.

[4] D. Koyama, A. Barsegyan, and J. Walker, "Implications of Using kW-level GaN Transistors in Radar and Avionic Systems," in *Proc. IEEE Int. Conf. Microw., Commun., Antennas Electron. Syst.*, Nov. 2015, pp. 1-4.

[5] J. Custer, G. Formicone, and J. L. B. Walker, "Recent advances in kW-level pulsed GaN transistors with very high efficiency," in *Proc. 21st Int. Conf. Microw., Radar Wireless Commun. (MIKON)*, May. 2016, pp. 1–4.

[6] J. Chen, X. Du, Q. Luo, X. Y. Zhang, P. J. Sun, and L. Zhou, "A Review of Switching Oscillations of Wide Bandgap Semiconductor Devices," *IEEE Trans. Power Electron.*, vol. 35, no. 12, pp. 13182-13199, Dec. 2020, doi: 10.1109/TPEL.2020.2995778.

[7] I. Rossetto, M. Meneghini, A. Tajalli, S. Dalcanale, C. D. Santi, P. Moens, A. Banerjee, E. Zanoni, and G. Meneghesso, "Evidence of Hot-Electron Effects During Hard Switching of AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices.*, vol. 64, no. 9, pp. 3734-3739, Sept. 2017, doi: 10.1109/TED.2017.2728785.

[8] N. Moultif, O. Latry, E. Joubert, M. Ndiaye, C. Moreau, J. F. Goupy, and P. Carton, "Reliability Assessment Of AlGaN/GaN HEMTs on the SiC Substrate Under the RF Stress," *IEEE Trans. Power Electron.*, vol. 36, no. 7, pp. 7442-7450, July. 2021, doi: 10.1109/TPEL.2020.3042133.

[9] S. D. Burnham, R. Bowen, J. Tai, D. Brown, R. Grabar, D. Santos, J. Magadia, I. Khalaf, and M. Micovic, "Reliability Characteristics and Mechanisms of HRL's T3 GaN Technology," *IEEE Trans. Semicond Manuf.*, vol. 30, no. 4, pp. 480-485, Nov. 2017, doi: 10.1109/TSM.2017.2748921.

[10] R. R. Chaudhuri, V. Joshi, S. D. Gupta, and M. Shrivastava, "On the Channel Hot-Electron's Interaction With C-Doped GaN Buffer and Resultant Gate Degradation in AlGaN/GaN HEMTs," *IEEE Trans. Electron Devices.*, vol. 68, no. 10, pp. 4869-4876, Oct. 2021, doi: 10.1109/TED.2021.3102469.

[11] M. Meneghini, N. Ronchi, A. Stocco, G. Meneghesso, U. K. Mishra, Y. Pei, and E. Zanoni, "Investigation of Trapping and Hot-Electron Effects in GaN HEMTs by Means of a Combined Electrooptical Method," *IEEE Trans. Electron Devices.*, vol. 58, no. 9, pp. 2996-3003, Sept. 2011, doi: 10.1109/TED.2011.2160547.

[12] N. Braga, R. Mickevicius, R. Gaska, M. S. Shur, M. Asif Khan, and G. Simin, "Simulation of gate lag and current collapse in gallium nitride field-effect transistors," *Appl. Phys. Lett.*, vol. 85, no. 20, pp. 4780-4782, Nov. 2004, doi: 10.1063/1.1823018.

[13] X. Niu, X. H. Ma, B. Hou, L. Yang, Y. S. Lin, Q. Zhu, F. M. Ciou, K. H. Chen, Y. L. Chen, J. L. Du, M. Wu, M. Zhang, C. Wang, T. C. Chuang, and Y. Hao, "Electrical Degradation of In Situ SiN/AlGaN/GaN MIS-HEMTs Caused by Dehydrogenation and Trap Effect Under Hot Carrier Stress," *IEEE Trans. Electron Devices.*, vol. 68, no. 9, pp. 4283-4288, Sept. 2021, doi: 10.1109/TED.2021.3096929.

[14] Y. Puzyrev, S. Mukherjee, J. Chen, T. Roy, M. Silvestri, R. D. Schrimpf, D. M. Fleetwood, J. Singh, J. M. Hinckley, A. Paccagnella, and S. T. Pantelides, "Gate Bias Dependence of Defect-Mediated Hot-Carrier Degradation in GaN HEMTs," *IEEE Trans. Electron Devices.*, vol. 61, no. 5, pp. 1316-1320, May. 2014, doi: 10.1109/TED.2014.2309278.

[15] M. Rudolph, R. Behtash, R. Doerner, K. Hirvhe, J. Würfl, W. Heinrich, and G. Tränkle, "Analysis of the Survivability of GaN Low-Noise Amplifiers," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 1, pp. 37-43, Jan. 2007, doi: 10.1109/TMTT.2006.886907.

[16] X. Tong, R. Wang, S. Zhang, J. Xu, P. Zheng, and F. Chen, "Degradation of Ka-Band GaN LNA Under High-Input Power Stress: Experimental and Theoretical Insights," *IEEE Trans. Electron Devices.*, vol. 66, no. 12, pp. 5091-5096, Dec. 2019, doi: 10.1109/TED.2019.2947311.

[17] V. Sangwan, C. M. Tan, D. Kapoor, and H. C. Chiu, "Electromagnetic Induced Failure in GaN-HEMT High-Frequency Power Amplifier," *IEEE Trans on Ind Electron.*, vol. 67, no. 7, pp. 5708-5716, July. 2020, doi: 10.1109/TIE.2019.2931233.

[18] D. A. Gajewski, S. Ganguly, S. Sheppard, S. Wood, J. B. Barner, J. Milligan, and J. Palmour, "Reliability comparison of 28 V-50 V GaN-on-SiC S-band and X-band technologies," *Microelectron. Rel.*, vol. 84, pp. 1-6, May. 2018, doi: 10.1016/j.microrel.2018.02.018.

[19] G. Z. Wang, D. L. Su, Y. X. Xiao, and Y. Zhou, "The methods applied to eliminate self-oscillation of one integrated LNA," in *Proc. Asia-Pac. Conf. Environ. Electromagn.*, Nov. 2003, pp. 108-110.

[20] J. Vidkjaer, "Instabilities in RF-power amplifiers caused by a self-oscillation in the transistor bias network," *IEEE J Solid State Circuits.*, vol. 11, no. 5, pp. 703-712, Oct. 1976, doi: 10.1109/JSSC.1976.1050801.

[21] F. Zhao, Y. Li, Z. Chen, S. Yang, and J. Chen, "Negative Conductance Modeling and Stability Analysis of High-Frequency Oscillation Based on Cascode GaN Circuits," *IEEE Access*., vol. 8, pp. 114100-114111, May. 2020, doi: 10.1109/ACCESS.2020.2995726.12

[22] P. Xue, and F. Iannuzzo, "Self-Sustained Turn-OFF Oscillation of Cascode GaN HEMTs: Occurrence Mechanism, Instability Analysis, and Oscillation Suppression," *IEEE Trans. Power Electron.*, vol. 37, no. 5, pp. 5491-5500, May. 2022, doi: 10.1109/TPEL.2021.3131535.

[23] S. Imail, S. Watanabe, Y. Komatsuzaki, H. Okazaki, S. Shinjo, K. Yamanaka, Y. Sasaki, H. Katayama, and A. Inoue, "A 2.6-GHz-Band 78-W Doherty Power Amplifier with GaN HEMT Unit-Cell Structure Robust for Layout-Dependent Loop Oscillation," in *Proc. 11th Eur. Microw. Integr. Circuit Conf. (EuMIC)*, Oct. 2016, pp. 512–515.

[24] Wolfspeed Application Note, "Thermal Performance Guide for High Power SiC MESFET and GaN HEMT Transistors," [Online]. Available: http://www.wolfspeed.com/index.php/downloads/dl/file/id/195/product/0/thermal_performance_guide_for_high_power_sic_mesfet_and_gan_hemt_transistors.pdf.

[25] N. Moultif, A. Echeverri, D. Carisetti, O. Latry, and E. Joubert, "Thermal Analysis of AlGaN/GaN High-Electron Mobility Transistors Using I–V Pulsed Characterizations and Infra Red Microscopy," *IEEE Trans. Device Mater. Reliab.*, vol. 19, no. 4, pp. 704-710, Dec. 2019, doi: 10.1109/TDMR.2019.2950091.