Cu Protrusion of Different Through-Silicon Via Shapes under Annealing Process

Alireza Eslami Majd[1*], Il Ho Jeong[1,2], Jae Pil Jung[2], Nduka Nnamdi Ekere[1]
[1] School of Engineering, Faculty of Science and Engineering, University of Wolverhampton, TF2 9NN, UK
[2]Dept. of Materials Science and Engineering University of Seoul, Seoul 130-743, Republic of Korea
[*] **Corresponding author**

Contact e-mail: a.e.majd@wlv.ac.uk
Submitted: 11 September 2020 / Revised: 20 March 2021 / Accepted: 26 March 2021 / Published online:
Modeling and Simulation
JMEP-20-12-22630

Abstract
The through-silicon via (TSV) 3D integration method has become one of the most widely used techniques for achieving system-level integration for applications that require smaller package sizes, higher interconnection density, and high performance. This is because the TSV fabrication technology provides the mechanism for facilitating communications between various layers of the 3D integration system and for interconnecting stacked devices at wafer-level. Although there are several reported studies on TSV 3D integration R&D, with most of these studies focused on the improvement of TSV fabrication process, there are very limited in-depth studies associated with the TSV reliability issues and challenges. In this paper, we investigate the effect of TSV geometries on the associated TSV reliability factors. Different TSV geometries including I-type, tapered, elliptical, triangular, quadrangular and circular shapes (with same volume) are investigated to find the most reliable structure under annealing process. The results show that the tapered TSV shape releases thermo-mechanical stress more uniformly than other shapes and larger top surface shows better reliability.

Keywords: TSV, reliability, shape, annealing, simulation

1. Introduction

The very rapid developments in the electronics industry over the last decade, and the growing demand for consumer electronics are the key drivers for the migration from the traditional 2D integrated circuit to the new 3D IC integration [1-3]. As electronic devices become smarter and more multifunctional, portable devices such as mobile phones and notebooks now require that more chips be stacked together within smaller spaces, without increasing the package size [4-5]. The conventional 2D Integrated circuits usually have only one layer of electronic devices, which limits their performance and functionality; whilst the 3D integrated circuit that incorporates multiple device layers can facilitate the further miniaturization of the interconnection and packaging for different applications. The through silicon via (TSV) technology is fast becoming the most widely adopted 3D integration solution for achieving the shortest interconnections, minimum chip-to-chip bonding pad sizes and high integration densities and systems performance [6-9]. For these reasons, TSVs have now become the preferred interconnection choice for high-end memory, and they are also an enabling technology for the heterogeneous integration of logic circuits with sensors, MEMS and RF filters.

The steps in the TSV manufacturing process includes via formation, filling, annealing and wafer thinning.

Copper (Cu) is used to fill the via, as it is the preferred filling material due to its high electrical conductivity, relatively well-developed deposition process and its good resistance to electro-migration [6, 10, 11]. However, the annealing of the silicon device with copper TSVs causes high stresses in the copper and is known to lead to the "pumping" phenomenon in which copper is forced out of the blind TSV to form a protrusion [12]. Indeed, TSV protrusion (pumping) occurs due to the coefficient of thermal expansion (CTE) mismatch between Cu (17ppm/°C) and silicon (2.8ppm/°C). Releasing the induced stress causes formation of an irreversible Cu protrusion in the vertical direction, which results in many reliability problems such as crack or delamination [7-9, 13, 14-16]. The Cu protrusion is a potential threat to the IC interconnection layer, particularly for low-k (dielectric) materials [17]. Leakage current resulting from micro-cracks in scallop shaped dielectric layer, which are initiated by thermal stress during the annealing process, is known to be another major TSV reliability issue [20]; and it is recommended that the TSV leakage current should be less than l0nA on a l0V voltage system [18-19]. However, annealing treatment can help to increase the Cu grain size, which may the subsequently lead to a reduction in the Cu resistivity [21].

In the previous study, a comparison between different TSV geometries (cylindrical, quadrangular (square), elliptical, and triangular) showed that the quadrangular shape had the best electrical performance due to good characteristic impedance [22].

To deal with the reliability challenges associated with Cu-filled TSVs; several thermomechanical studies have been reported, including the study of the plastic behavior of the Cu [23], delamination and the interfacial sliding between Cu and Si [24, 25], and thermal cracks in the Cu and the wafer (Si) [26, 27]. For example, Jiang et. al. [28], showed that the high level of stress concentration in the Cu (up to 300MPa) can lead to mechanical reliability issue in the TSVs. Also other reliability studies have shown that long cracks are initiated in the wafer during the TSV high temperature annealing process [29, 30].

This paper reports on the study of the protrusion and the induced stress distribution in the wafer (Si) and the Cu for different TSV geometries including I-type, tapered, elliptical, triangular, quadrangular and circular shapes to find the most reliable TSV structure. The results of the study provide fundamental understanding of the effect of TSV geometry on the reliability of annealed TSV filled with the Cu.

2. Main Parameters for TSV Protrusion

Important annealing parameters such as heating rate, annealing temperature and annealing time have been investigated for the typical TSV protrusion with diameters ranging from 5µm to 50µm and depths ranging from 50µm to 150µm [31]. Q. Deng et al. [13], found that the Cu protrusion decreases with increasing heating rate for the range 1(°C/min) to 10(°C/min) and for heating rates over 10(°C/min), the associated larger thermal shock generates higher stress levels in the TSV [13]. Figure 1 shows the plot of the Cu protrusion versus the heating rates for 200°C, 400°C annealing temperatures.

The results show that under the same heating rate, the Cu protrusion increases sharply with increasing temperature particularly for temperatures higher than 300°C [13], [17] and [18]. Indeed, the critical temperature for the Cu plastic yield is about 240°C and for higher temperatures, Cu expands much more quickly. However, for temperatures higher than 400°C the Cu protrusion remains almost constant [10]. Besides, for very high annealing temperatures above 500°C, wafer breakage has been reported due to the high thermal stress levels induced in the wafer. This means that the annealing temperature in the range between 300°C and 400°C can be used for the effective control of the Cu protrusion levels, and thus can be used to improve TSV reliability. R. Can et al. [12] observed that if annealing time is long enough, then the annealing process is adequate and there is therefore no need for post-CMP (Chemical Mechanical Polish) annealing. H. Jin et al. [18] have also investigated the leakage current for different annealing temperatures and annealing times. They found that for the TSV annealed at 400°C, the leakage current increases sharply with increasing annealing time (and that the leakage current at 400°C for 20min, 60min and 180min are

0.055nA, 0.16nA and 22.7nA, respectively). Hence, annealing times longer than 180 min is not recommended since the leakage current exceeds the threshold current of 10nA [18].

3. Modelling and Simulation

As stated earlier in section #2 above, the annealing temperature has been shown to be one of the important parameters that affects the TSV Cu protrusion level. The TSV Cu protrusion can be subdivided into two main types namely; the elastic TSV protrusion and the plastic TSV protrusion. The Elastic TSV protrusion can be calculated using equation (1) [32], where ΔH_e is the elastic TSV height increase, ε_z is the thermal strain in z-direction, α is coefficient of thermal expansion, v is Poisson's ratio and E_{cu}, E_{si} are Young's modulus for Cu and Si.

$$\frac{\Delta H_e}{H} = \varepsilon_{z,Cu} - \varepsilon_{z,Si} = \Delta T(\alpha_{Cu} - \alpha_{Si})\left(1 + \frac{2v_{Cu}}{E_{Cu}}\left(\frac{1 - v_{Cu}}{E_{Cu}} + \frac{1 + v_{Si}}{E_{Si}}\right)^{-1}\right) \quad (1)$$

However, the TSV Cu protrusion is known to be mainly due to the plasticity and irreversible deformation that occurs when the material yields [24]. Therefore, analytical formulations such as that given in equation (1) above are only able to calculate the elastic deformation and does not provide a complete representation of the plasticity component. This is particularly true for the more complex geometries, hence there is an urgent need for the use of numerical approaches to the study of TSV Cu protrusion; to help provide better understanding of the response of TSV Cu protrusion to the annealing process.

In this study, the Finite Element Method in ABAQUS 6.14 software is used for the simulation of different TSV geometries (including I-type, tapered, elliptical, triangular, quadrangular and circular shapes), to evaluate the thermo-mechanical response of the TSV models and then to determine the most reliable TSV shape. Two symmetrical boundary conditions have been applied to the whole models where the bottom surface of each model is pinned. Three-dimensional continuum elements "C3D8R1" with a fine mesh density in Cu area are used to find good convergence and accuracy in results. Table 1 shows the mechanical properties of the materials (Cu and Si) used in the simulation. It is assumed that the Cu has homogenous isotropic material properties and the orientation of Cu TSVs with respect to Si is not considered.

To help with the validation of the simulation study, the results from ABAQUS have been compared with the published results from experiment [18]. In this case, the annealing temperature is between 250°C and 450°C and the heating rate is 5(°C/min). The diameter of the TSV is considered as 20µm and the TSV is partially penetrated to the depth of 120µm in 160µm silicon layer. Also, to clarify the influence of considering the temperature dependency of Cu on the Cu protrusion, the FEM models in ABAQUS are based on both Cu temperature dependent /and independent properties. Table 2 shows the temperature dependent properties of Cu.

Figure 2 shows that there is a good agreement between the results from ABAQUS and the experimental results [18]. The results also show that there is less than 11% difference in Cu protrusion at 450 °C between states with consideration of temperature dependency of Cu properties and without consideration of the temperature dependent Cu properties (at low temperatures there are same Cu protrusions for both states).

The reason for the difference of Cu protrusion is the difference in Coefficient of Thermal Expansion at high temperatures. Indeed, for the constant material properties, the Cu CTE is considered 17.3e-6 and for the temperature dependent properties, the Cu CTE is 19.5e-6 at 700 K (427 °C) (% 12 difference of the CTE values). This trend is found for other geometries and it means that for different geometries we have almost same difference between the results with and without considering the temperature dependency.

In this study, the temperature independent material properties are considered for all geometries as the aim

of this study is a comparative study of different TSV geometries with a same condition.

Figure 3 shows different TSV geometries used in the study, which they are fully penetrated in the interposer Si material with the width of 100µm. In order to ensure that same conditions are used to investigate the effect of the annealing process on the plastic and the elastic deformation, the TSV geometries have been adjusted to ensure that all the different shapes have the same volume. For instance, to have the same volume of the circular TSV shape (7853µm^3), the radius and mid part height of the I-type TSV shape are considered as 4.88µm and 80µm, respectively. Table 3 shows the details of the different geometries of the simulated TSV samples used in this study.

4. Results and Discussion

Figure 4 shows the vertical displacement in mid cross section of the tapered TSV shape for the temperature range, from 250°C to 450°C and under the same heating rate as 5(°C/min). The results show that the Cu protrusion increases with increasing annealing temperature. To calculate the protrusion of TSVs, the maximum pumping of Si is deducted from the maximum pumping of Cu. For example, the maximum pumping of Cu and Si at 450 °C annealing temperature are 0.36µm and 0.2µm, respectively, then the protrusion of TSV is calculated 0.16µm.

Figure 5 shows the protrusion of different TSV shapes for different temperatures during the annealing process. The results show that the tapered TSV shape has the largest protrusion compared to the other shapes due to having more Cu at the top surface. The largest Cu protrusion after annealing process means that the internal stress of TSV has been more released.

The FEM results show that the Si experiences high levels of stress in different directions at high annealing temperatures as in normal stress components have a very high stress concentration in the Si.

Figure 6 shows the value of different stress components in the Si for the tapered IV TSV shape at different annealing temperatures. As it is seen in Figure 6, there is a very linear change of stress values in terms of changing the temperatures. Also, Figure 6 shows that the 1st principal stress component has larger values rather than other stress components and it can affect the failure of the Si more than others. Hence, in this work, the 1st principal stress component is used to show the stress level in the Si.

Figure 7 depicts the maximum 1st principal stress in the Si for different TSV geometries at the various annealing temperatures. The results show that increasing the annealing temperature results in more expansion of Cu and this leads to an increase in the stress level. The results also show that the lowest magnitude of 1st principal stress are for the I-type shapes and the tapered shapes as at 450°C annealing temperature, the I-type I and the tapered IV shapes are experiencing 667 MPa and 643 MPa compressive stress, respectively.

Figure 8 shows 1st principal stress distribution in the mid cross section of Si at 450°C for different TSV shapes. Analysis of the results presented in Figure 7 and Figure 8 shows that for different TSV geometry designs used for the study, the induced thermal stresses in the Si has different values and distributions. For all TSV shapes, the compressive stress concentrations are located at the bottom and also they have larger magnitudes (about 2 times larger) compared to the tensile induced stress at top of the TSVs. Figure 8 shows that the Quadrangular shape is experiment a very high compressive stress at the bottom of TSV (1000 MPa) and this can result in failure at the interface at the connection of different wafer layers. The result therefore

shows that the use of the tapered geometry can guarantee more mechanical reliability for the TSV.

Figure 9 shows Von-Mises stress distribution in the mid-cross section of the Cu at 450°C for different TSV shapes. The results show that for all TSV shapes, the top area of Cu (in protrusion side) experiences high levels of plastic stress, that can adversely affect the reliability of the TSV, as it is thought to be associated with defects such as delamination and the interfacial sliding between Cu and Si [24, 25]. Figure 9 also shows that of the six TSV shapes investigated in this study, the Tapered and the I Type shapes experience the least amount of plastic stress (248 MPa) in Cu compared to four other shapes; and that the Triangular shape exhibited the highest level of plastic stress (274 MPa). This means that the Tapered and I Type shapes can provide higher reliability than other four TSV shapes investigated in this study due to the lower Cu plastic stress levels exhibited during the high temperature annealing process.

Figure 10 shows the Cu protrusion for different sizes of the tapered TSV shape. It should be noted that for theses tapered TSV shapes, in order to keep volume same, the diameter of top side is increased from 5.5µm to 7.0µm and simultaneously, the diameter of bottom side is decreased from 4.48µm to 2.68µm. The same trend of TSV protrusion is observed for all tapered sizes, however, the protrusion increases with the increase in the ratio of the top surface radius to the bottom surface radius. This means that the lager surface can be pumped easier due to having more filled Cu material to expand at the area near to the top free surface.

Figure 11 shows the trend of TSV protrusion of the tapered shapes (Hp) in terms of radius ratio (R_1/R_2), where R_1 is the top surface radius, R_2 is the bottom surface radius of each tapered shape. A second order polynomial equation (Eq. 2) has been derived to analytically express the trend of tapered shape protrusion against radius ratio. As it is clear from Figure 10, TSV protrusion increases with the increase in radius ratio (R1/R2).

$$H_p = -0.0123(R_1/R_2)^2 + 0.0716(R_1/R_2) + 0.06 \qquad \text{(Eq. 2)}$$

5. Conclusions

A typical through silicon via (TSV) is filled by Cu electroplating in the fabrication process, as Cu is the most preferred filling material due to its high electrical conductivity. However, TSV experiences some inevitable reliability issues such as Cu protrusion due to CTE mismatch between Cu and Si (substrate material). To remove the protruded Cu, and also to improve the electrical performance characteristics of TSV, the annealing process is the most widely used approach; which induces more protrusion to make the removal process easier.

Although there are many parameters that are known to affect TSV Cu protrusion under the annealing process, previous studies show that annealing temperature and annealing time are most important factors in the TSV annealing process.

This study has employed the Finite Element Method to investigate the protrusion of different TSV geometries (including I-type, tapered, elliptical, triangular, quadrangular and circular shapes) to find the most reliable TSV design.

The results show that the tapered TSV shape is a more reliable structure when compared to the other TSV geometries used in this study; due to the higher protrusion, levels of Cu material. The results also show that, the tapered TSV shape can be more effective in uniformly releasing the thermally induced stress in the vertical direction. This means that there is less stress concentration at the bottom of the TSV; and this subsequently reduces the potential for failure the external contact areas between wafers.

The results also show that, the magnitude of internal stress in wafer (Si) and the Cu for the tapered shape is less than the internal stress for the other TSV geometries; which can be beneficial for improving the

mechanical reliability. The results of this study can be used for the development of a structural design guideline and toolbox for improving the TSV reliability.

Author Contributions: Alireza Eslami Majd undertook FEM simulations & Analysis and Il Ho Jeong, developed the idea for this paper. Jae Pil Jung and Nduka Nnamdi Ekere supervised the work and contributed to developing the outline of the paper.

Acknowledgments: The authors would also like to acknowledge the support of the Faculty of Science and Engineering, University of Wolverhampton for providing the sponsorship for the corresponding author's Ph.D. studies.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. W. S. Kwon, D. T. Alastair, K. H. Teo, et al. Stress evolution in surrounding silicon of Cu-filled through-silicon via undergoing thermal annealing by multiwavelength micro-Raman spectroscopy. Applied Physics Letters Vol. 98, Issue 23, 2011. DOI: 10.1063/1.3596443.

2. H. Roth, Z. He and T. Mayer. Inspection of through silicon vias (TSV) and other interconnections in IC packages by computed tomography. In Proceeding of the 11th Electronics Packaging Technology Conference, Singapore, 2009. DOI: 10.1109/EPTC.2009.5416506.

3. T. Chen, J. Sun and R. Van. A review about the filling of TSV, In Proceeding of the 16th International Conference on Electronic Packaging Technology, Changsha, China, 2015, pp. 860. DOI: 10.1109/ICEPT.2015.7236716.

4. P. Kumar, and I. Dutta. Influence of electric current on diffusionally accommodated sliding at hetero-interfaces. Acta Materialia, Vol. 63, Issue 1, 2011, pp. 2096-2108. DOI: 10.1016/j.actamat.2010.12.011.

5. I. Dutta, P. Kumar, and M.S. Bakir. Interface-related reliability challenges in 3-d Interconnect Systems with through-Silicon Vias. The Journal of the Minerals, Metals & Materials Society. Vol. 63, 2011, pp. 70-77. DOI: 10.1007/s11837-011-0179-y.

6. J. De Messemaeker, O. V. Pedreira, H. Philipsen, E. Beyne, T. De Wolf and T. Van der Donck, et al. Correlation between Cu microstructure and TSV Cu pumping. In Proceeding of the Electronic Components and Technology Conference (ECTC). IEEE 64th, 2014, pp. 613-619. DOI: 10.1109/ECTC.2014.6897349.

7. J. De Messemaeker, O. V. Pedreira, B. Vandevelde and H. Philipsen, I. De Wolf, E. Beyne, et al. Impact of post-plating anneal and throughsilicon via dimensions on Cu pumping. In Proceeding of the Electronic Components and Technology Conference (ECTC). IEEE 63rd, 2013, pp. 586-591. DOI: 10.1109/ECTC.2013.6575633.

8. C. Song, R. He, D. Yu, and L. Wan. Comprehensive analysis of thermal mechanical stress induced by Cu TSV and its impact on device performance. In Proceeding of the 13th International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2012, pp. 85-89. DOI: 10.1109/ICEPT-HDP.2012.6474575.

9. H. He, C. Song, C. Xu, L. Wang, and W. Zhang. Cu pumping effect under different annealing conditions. In Proceeding of the 14th International Conference on Electronic Packaging Technology (lCEPT), 2013, pp. 769-771. DOI: 10.1109/ICEPT.2013.6756578.

10. T. Jiang, C. Wu, L. Spinella, J. 1m, N. Tamura, M. Kunz, et al. Plasticity mechanism for copper extrusion in through-silicon vias for three-dimensional interconnects. Applied Physics Letters, Vol. 103, Issue 21, 2013, pp. 211906. DOI: 10.1063/1.4833020.

11. P.C. Andricacos, C.E. Uzoh, J. Dukovic et al. Damascene Copper electroplating for chip interconnections. Ibm Journal of Research & Development. Vol. 42, Issue 5, 1998, pp. 567-574. DOI: 10.1147/rd.425.0567.

12. Can Rao, Tongqing Wang, Jie Cheng, Yuhong Liu and Xinchun Lu. Investigations of Annealing Effect on TSV CMP. In Proceeding of the International Conference on Planarization/CMP Technology (CPT). 11-13, Leuven,

Belgium, 2017.

13. Qi Deng, Lingang Huang, Jing Shang and Ming Li. Study on TSV-Cu protrusion under different annealing conditions and optimization. In Proceeding of the 17th International Conference on Electronic Packaging Technology, 2016. DOI: 10.1109/ICEPT.2016.7583158.

14. X. Jing, H. He, L. Ji, C. Xu, K. Xue, M. Su, et al. Effect of thermal annealing on TSV Cu protrusion and local stress. In Proceeding of the Electronic Components and Technology Conference (ECTC), IEEE 64th, 2014, pp. 1116-1121. DOI: 10.1109/ECTC.2014.6897429

15. X. Jing, U.-H. Lee, C. Xu, Z. Niu, H. Hao, J.-Y. Bae and J. Won, W. Zhang. Effect of pre-CMP annealing on TSV pumping in thermal budget and reliability test. In Proceeding of the International Symposium on the Physical and Failure Analysis of Integrated Circuits (IPFA), IEEE 22nd. 2015. DOI: 10.1109/IPFA.2015.7224329

16. Sven Niese, Peter Krueger, Ehrenfrid Zscheh, NanoXCT-A High-Resolution Technique for TSV characterization. In Proceeding of the AIP Conference, Vol. 1378, Issue 1, 2011, pp. 168-173. DOI: 10.1063/1.3615703.

17. Hongwen He, Xiangmeng Jing, Liqiang Cao, Daquan Yu, Kai Xue and Wenqi Zhang. Influence of thermal annealing on the deformation of Cu-filled TSV. In Proceeding of the Electronics System-Integration Conference, 2014. DOI: 10.1109/ESTC.2014.6962763.

18. Hai JIN, Jian Cai, Qian Wang, Yang HU and ZiYu Liu. Effects of post-CMP annealing on TSV Cu protrusion and leakage current. In Proceeding of the 17th International Conference on Electronic Packaging Technology, 2016, pp.1064-1068. DOI: 10.1109/ESTC.2014.6962763

19. J.F. Hung, J.H. Lau, P.S. Chen, et al. Electrical testing of blind Through-Silicon Via (TSV) for 3D IC integration. In Proceeding of the Electronic Components and Technology Conference. 2012, pp. 564-570. DOI: 10.1109/ECTC.2012.6248886.

20. T. Nakamura, H. Kitada, Y. Mizushima, et al. Comparative study of side-wall roughness effects on leakage currents in through-silicon via interconnects. In Proceeding of the 3D Systems Integration Conference (3DIC), 2012, pp. 1-4. DOI: 10.1109/3DIC.2012.6262948.

.

21. J.M.E. Harper, C. Cabral Jr., P.C. Andricacos. et al. Mechanisms for microstructure evolution in electroplated copper thin films near room temperature. Journal of Applied Physics 86 (5), 1999, pp.2516-2525. DOI: 10.1063/1.371086.

22. I.H. Jeong, A. Eslami Majd, J.P. Jung and N.N. Ekere. Electrical and Mechanical Analysis of Different TSV Geometries. Metals 2020, 10(4), 467, DOI: 10.3390/met10040467

23. P. Bayat, D. Vogel, Raul D. Rodriguez, E. Sheremet, D. R.T. Zahn and S. Rzepka, B. Michel. Thermo-mechanical Characterization of Copper Through-Silicon Vias (Cu-TSVs) Using Micro-Raman Spectroscopy and Atomic Force Microscopy. Microelectronic Engineering, Vol. 137, 2015, pp. 101–104. http://dx.doi.org/10.1016/j.mee.2015.02.004

24. S.K. Ryu, K.H. Lu, J. Im, R. Huang, and P.S. Ho. Stress-Induced Delamination of Through Silicon Via Structures. AIP Conf. Proc. (153), 2011. http://dx.doi.org/10.1063/1.3615702

25. P. Kumar, I. Dutta and M.S. Bakir. Interfacial Effects During Thermal Cycling of Cu-Filled Through-Silicon Vias (TSV). Journal of Electronic Materials, Vol. 41, No. 2, 2012

26. C. Okoro, J. W. Lau, F. Golshany, K. Hummler, and Y. S. Obeng. A Detailed Failure Analysis Examination of the Effect of Thermal Cycling on Cu TSV Reliability. IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 61, NO. 1, 2014.

27. M. Dong, Q. Deng, Y. Zhang, T. Hang, Mi. Li. Study on the Relationship Between Cu Protrusion Behavior and Stresses Evolution in the Through-Silicon Via Characterized by In-situ μ-Raman Spectroscopy. Microelectronics Reliability, Vol. 115, 2020. https://doi.org/10.1016/j.microrel.2020.113949

28. T. Jiang, S.K. Ryu, Q. Zhao, J. Im, R. Huang, P.S. Ho. Measurement and Analysis of Thermal Stresses in 3D Integrated Structures Containing Through-Silicon-Vias. Microelectronics Reliability, Vol. 53, 2013, pp. 53–62. http://dx.doi.org/10.1016/j.microrel.2012.05.008

29. K.Lee, T. Fukushima, T. Tanaka, and M. Koyanagi. Thermomechanical Reliability Challenges Induced by High Density Cu TSVs and Metal Micro-Joining for 3-D ICs. International Reliability Physics Symposium (IRPS), IEEE, 2012.

30. M. Stiebing, E. Lortscher, W. Steller, D. Vogel, M.J.Wolf, T. Brunschwile, B. Wunderle. Stress Investigations in 3D-integrated Silicon Microstructures.17th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Microelectronics and Microsystem, IEEE

31. Chen Si, QIN Fei, An Tong, Chen Pei. Effect of Electroplating Parameter on the TSV-Cu Protrusion during Annealing. In Proceeding of the 3D Electronic Components and Technology Conference (ECTC), IEEE 66th, 2016, pp.1599-1604. DOI: 10.1109/ECTC.2016.62

32. T. Jiang, C. Wu, L. Spinella, J. Im, N.i Tamura, M. Kunz, H.Y. Son, B.G. Kim, R. Huang, and P. S. Ho. Plasticity mechanism for copper extrusion in through-silicon vias for three dimensional interconnects. Applied Physics Letters 103(21): pp.211906-211906, 2013.

33. Y.S. Taulaukian, V. S., R.K.Kirby, E.Taylar, R., & Desai. Thermal expansion, metallic elements and alloys. 1975.

34. W. Li, H. KO, X. Zhang, et al. Temperature-dependent elastic modulus model for metallic bulk materials. Mechanics of Materials (139), 2019.

Table 1 Mechanical properties of material used in the ABAQUS simulation

Mat.	**Poisson's Ratio**	**CTE (ppm/k)**	**Young Modulus (GPa)**	**Plastic Curve (stress, MPa, Vs strain)**
Cu	0.34	17.3	121	121 at 0.001 186 at 0.004 217 at 0.01 234 at 0.02 248 at 0.04
Si	ν_{yz}=0.36 ν_{zx}=0.28 ν_{xy}=0.064	2.8	Ex=Ey=169 Ez=130 Gyz=Gzx=79.6 Gxy=50.9	-

Table 2 Temperature dependent properties of Cu

Temp. (°C)	CTE (ppm/k) [33]	Young Modulus (GPa) [34]
27	16.5	120
127	17.6	-
237	18.3	-
337	18.9	-
437	19.5	-
537	20.3	100

Table 3 geometrical details of the TSV shapes used in the simulation (in μm)

Shape		large radius or edge length	small radius or edge length
I-type	I	6.00	4.88
	II	7.00	4.73
Tapper	I	5.50	4.48
	II	6.00	3.93
	III	6.50	3.33
	IV	7.00	2.68
Elliptical		6.00	4.17
Triangular		13.47	13.47
Quadrangular		8.86	8.86
Circular		5.00	5.00

Figure 1 Function of Cu protrusion versus heating rate [13]

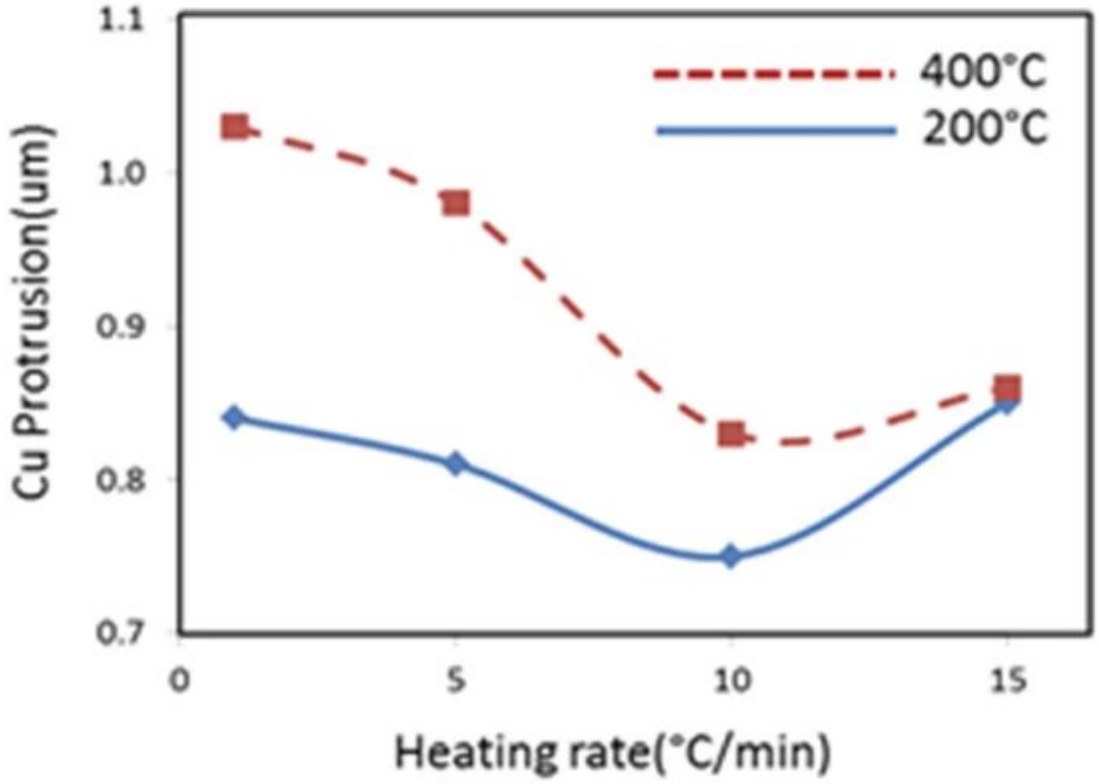

Figure 2 Comparison of the Cu protrusion results between ABAQUS and experiment [18]

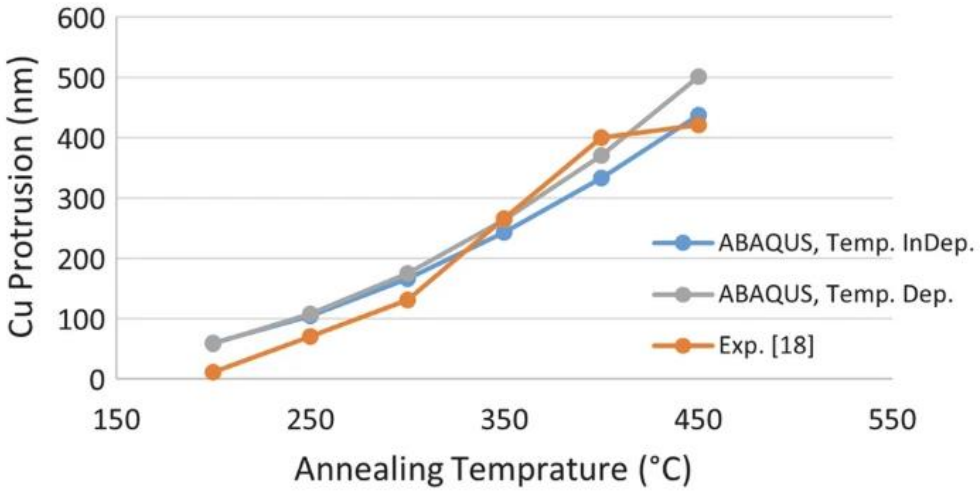

Figure 3 Different TSV shapes in the simulation

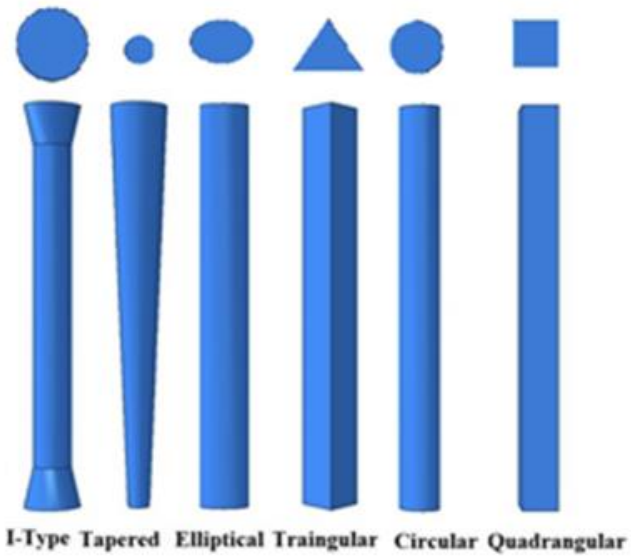

Figure 4 Vertical displacement (in mm) of tapered TSV shape

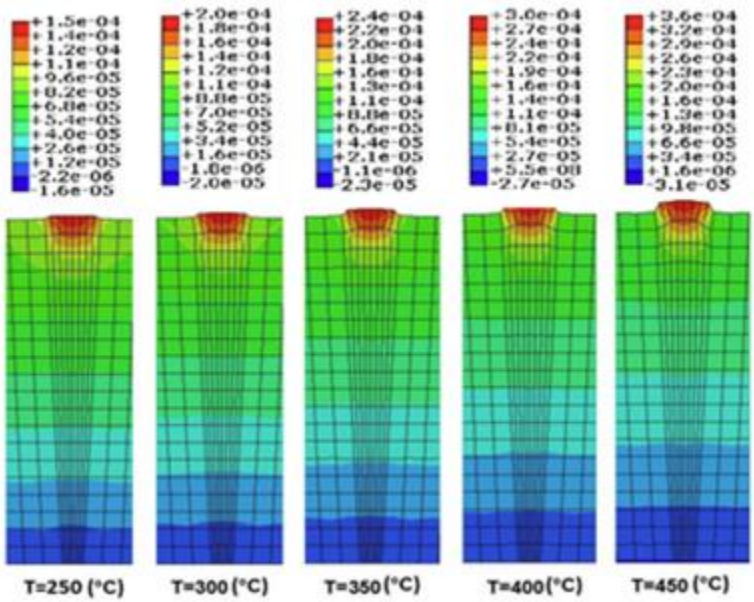

Figure 5 Cu protrusion for different TSV shapes according to annealing temperature

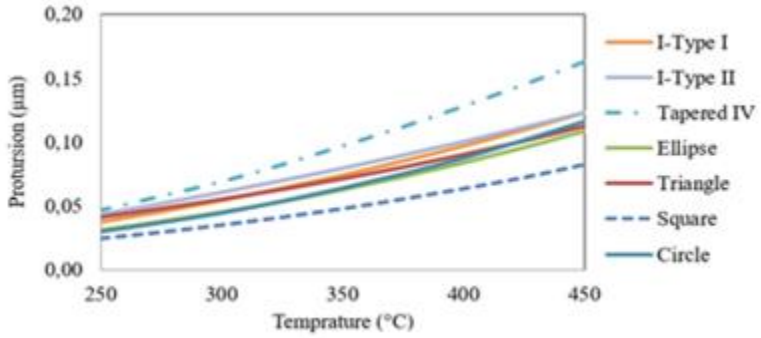

Figure 6 Maximum induced stress in different direction in Si for the tapered IV TSV at different annealing temperatures

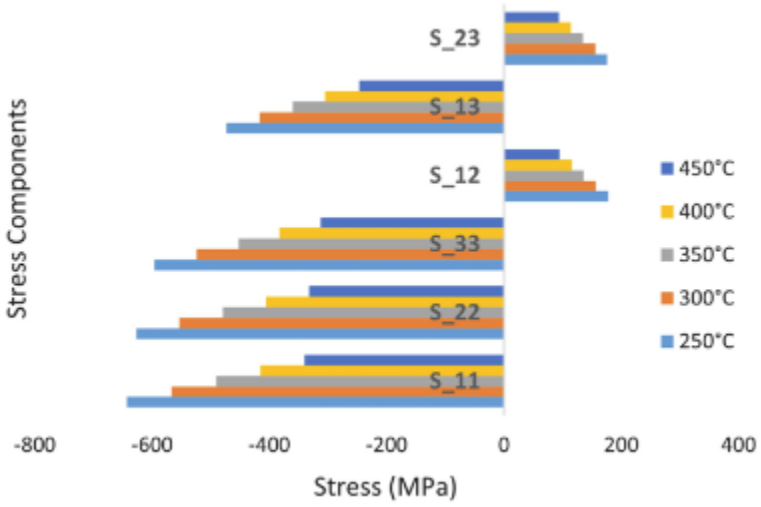

Figure 7 Maximum 1st principal stress component in the Si for different TSV shapes at different annealing temperatures

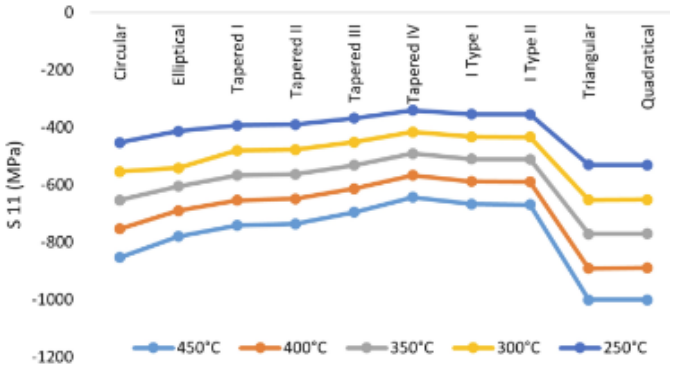

Figure 8 1st principal stress (in Pa) distribution in Si at 450°C for different TSV shapes

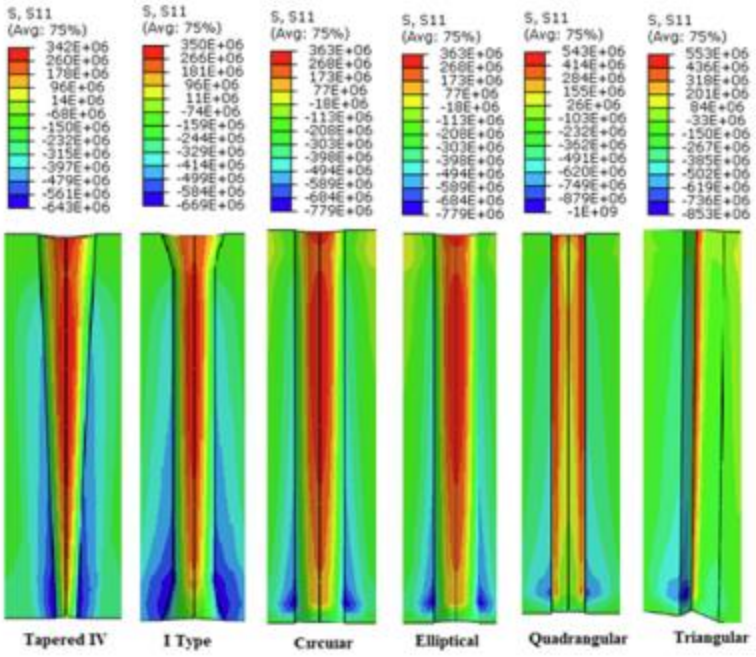

Figure 9 Von-Mises stress (in Pa) distribution in Cu at 450°C for different TSV shapes

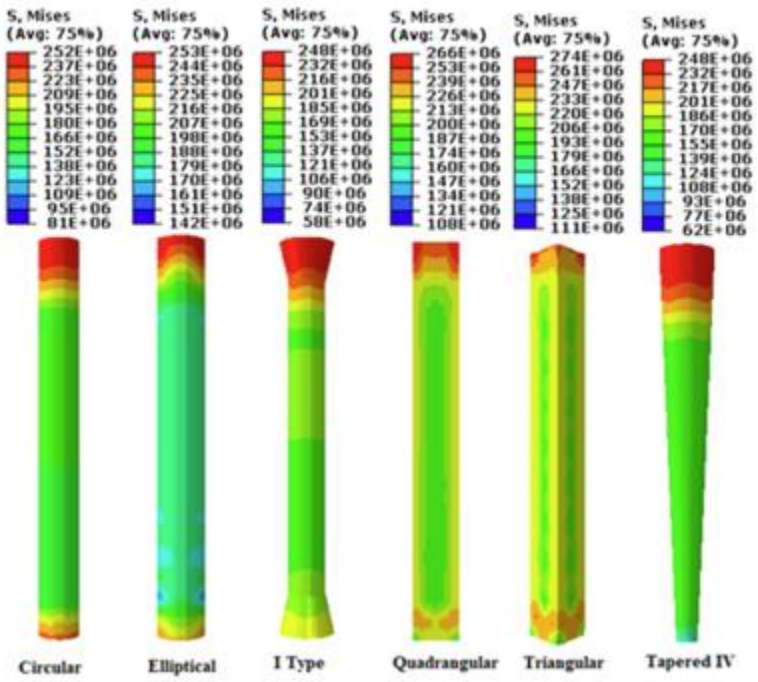

Figure 10 Cu protrusion for different tapered TSV size

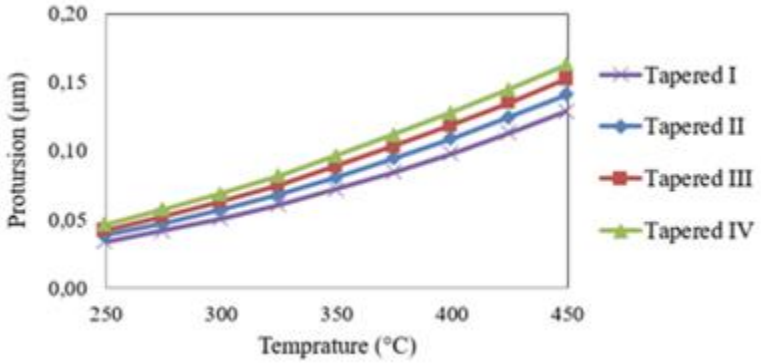

Figure 11 Tapered TSV shape protrusion via radius ratio