Characterization of Micro-Crack Propagation through Analysis of Edge Effect in Acoustic Micro Imaging of Microelectronic Packages

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Abstract

The miniaturization and three dimensional die stacking in advanced microelectronic packages poses a big challenge to their non-destructive evaluation by acoustic micro imaging. In particular, their complicated structures and multiple interfaces make the interpretation of acoustic data even more difficult. A common phenomenon observed in acoustic micro imaging of microelectronic packages is the edge effect phenomena, which obscures the detection of defects such as cracks and voids.

In this paper, two dimensional finite element modelling is firstly carried out to numerically simulate acoustic micro imaging of modern microelectronic packages. A flip-chip with a 140μm solder bump and a 230MHz virtual transducer with a spot size of 16μm are modelled. Crack propagation in the solder bump is further modelled, and B-scan images for different sizes of micro-cracks are obtained. C-line plots are then derived from the simulated B-scan images to quantitatively analyze the edge effect. Gradual progression of the crack is found to have a predictable influence on the edge effect profile. By exploiting this feature, a crack propagation characterization method is developed. Finally, an experiment based on the accelerated thermal cycling test is designed to verify the proposed method.

Keywords: Crack propagation; Acoustic micro imaging; Microelectronic package; Edge effect; Accelerated thermal cycling

1. Introduction

With the miniaturization of electronic devices, the solder bump pitches are increasingly dense with diameters as small as 30μm and decreasing. Moreover, many electronic devices are used in hostile environments. For example, in automobiles, electronic control units deal with vast temperature differences and constant vibrations. This brings into question the structural reliability of such devices [1]. According to Wunderle [2], up 65% of failures are thermo-mechanically related. Accelerated environment testing offers a way to evaluate the lifetime of such devices [3]. During thermal cycling, a crack will initiate in the solder bump and propagate through the solder bump structure, eventually resulting in an electrical discontinuity. It is observed that this particular failure mode usually occurs close to the silicon die to bump interface for the flip chip packages. To determine the crack size quantitatively in between thermally cycles, destructive evaluation on the sample often has to use in industry where a cross section will be cut, polished and optically examined.

Acoustic micro imaging (AMI) is effective at detecting discontinuities inside a test sample, which makes it ideal of non destructive evaluation of solder bump discontinuities [4-7]. Edge effect [8] is a physical phenomenon in acoustic imaging of microelectronic packages where sample edges scatter acoustic energy leading to dark annular regions around the solder bump. This is clearly seen from the ultrasonic C-scan images shown in Figure 1. The ultrasonic C-scan images in Figure 1 were produced from the detection of two flip-chip packages soldered on a PCB board [3] using a 230MHz focusing transducer and gating at the silicon die-solder bump interface. The images labelled as A_0 and B_0 were obtained before thermal cycling while A_{40} and B_{40} were obtained after thermal cycling for 40 thermal cycles. The flip-chip packages contained 109 solder joints. From Figure 1, it can be seen that the area and intensity the bright spot at a solder bump inner region increases after thermal cycling. This is due to that thermal cycling causes crack initiation and propagation at the silicon die-solder bump

interface. With a larger acoustic impedance mismatch caused by cracks, most of the incident signals are reflected back to the transducer and consequently produce higher intensities. However, how to non-destructively evaluate the crack size is a big challenge due to the limited resolution of acoustic imaging and the existing of edge effect. In this paper, a crack propagation characterization method is proposed, which is achieved through exploiting the relationship of the edge effect and the crack size.

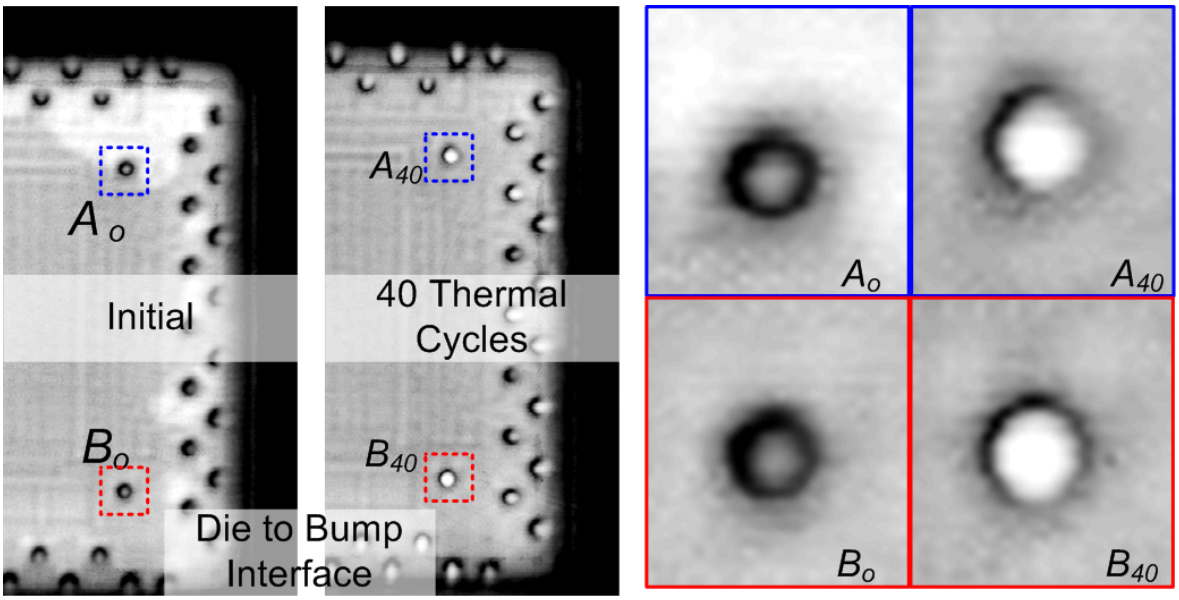


Figure 1: Edge effect in ultrasonic C-scan images of the silicon die-solder bump interface produced from the detection of two flip-chip packages soldered on a PCB board using a 230MHz focusing transducer. A_0 and B_0: before thermal cycling; A_{40} and B_{40}: after thermal cycling for 40 thermal cycles.

2. Finite element modelling for acoustic micro imaging of microelectronic packages

Finite element modelling for acoustic micro imaging of microelectronic packages was carried out in our previous research to investigate the acoustic wave propagation inside a package and the generation mechanism of edge effect [8, 9]. The numerical model was built

on the basis of acoustic micro imaging of the physical Flip Chip test sample used in our practical experiments. Two dimensional modelling was carried out using ANSYS APDL. The model schematic is shown in Figure 2. The numerical model consists of three parts: 1) the flip-chip modelled by a solder bump connecting to the silicon die through the Under Bump Metallization (UBM) structure. The composition of the UBM structure is based on [10]. 2) The water medium. The model is submerged in the water medium for simulation of immersion ultrasonic imaging. 3) A Virtual Transducer (VT) attached to the top of the model. The VT is modelled based on the 230MHz focused transducer used in our experiments. The displacement loads on the VT curve is vectored to mimic a travelling pulse ultrasonic waves very close to the sample. The same VT curve is used as a receiver to collect the reflected ultrasonic waves. In water, the VT produced a spot size of 16μm and a focal depth of 186μm which is in close agreement with the physical transducer with a spot size of 15μm and a focal depth of 192μm. The mechanical scanning in acoustic imaging of the flip chip package is implemented in the simulation by laterally moving the flip-chip at 1μm increment. Moving the flip-chip package is equivalent to scanning the transducer. At each scanning position, the entire model is solved to obtain an A-scan signal. The resultant A-scans at different scanning positions are assembled to create a B-scan image with a resolution of 1μm per pixel on the lateral X-axis. The B-Scan is a cross-sectional image of the flip chip. The deailed parameters of the FEM modeling undertaken to describe the contrast in the UT-imaging of solder bumps using an SAM can be found in [8].

To simulate crack propagation, a crack is modelled by the introduction of an air gap with a thickness of 2μm inside the solder bump. The crack length propagates at an increment of 2.5μm. The initial and end positions of the crack propagation are illustrated in

Figure 3.

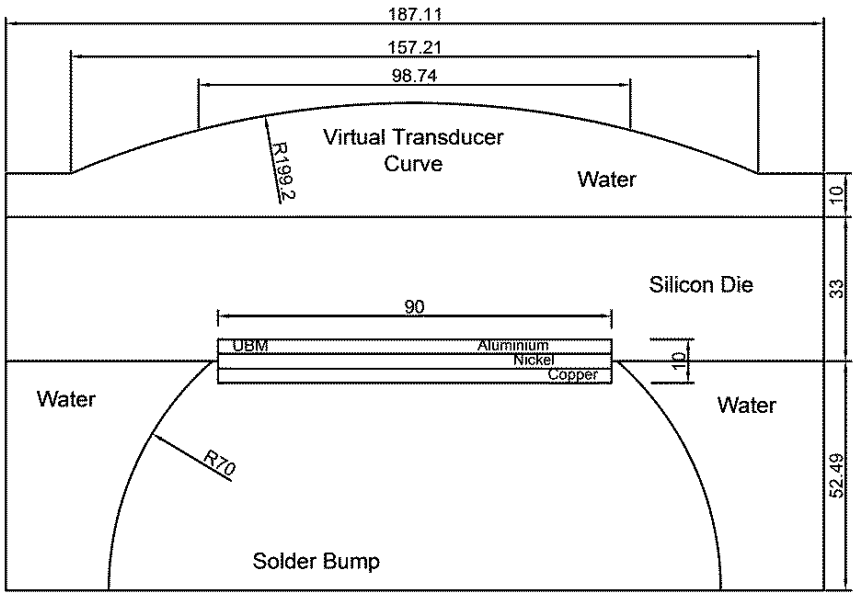


Figure 2: Numerical model schematic for acoustic imaging of a flip-chip package. Unit: µm.

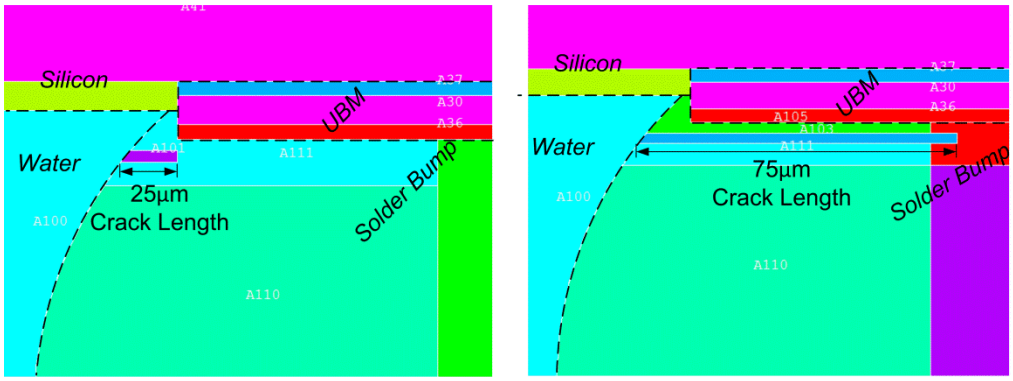
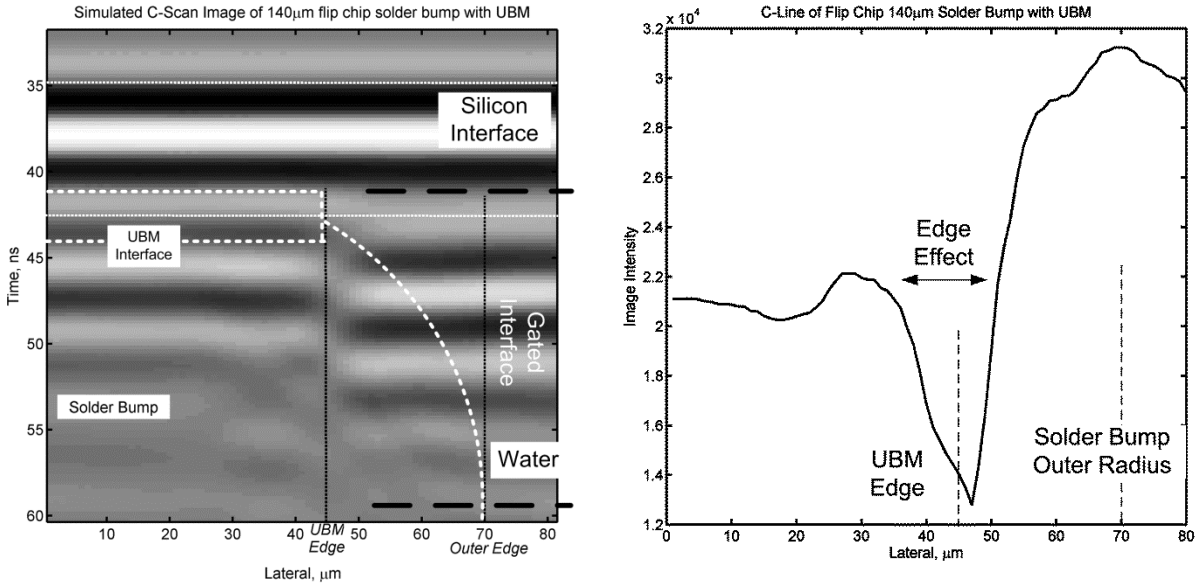


Figure 3: Crack propagation modelled by a crack with length from 25µm to 75µm at an increment of 2.5µm.

3. Characterization of crack propagation through analysis of edge effect

Error! Reference source not found.4(a) shows a simulated B-scan image. Since the solder bump structure is symmetrical, only half of the flip-chip show in Figure 2 is scanned and shown in Figure 4(a). The position of 0µm on the lateral X-axis in **Error! Reference source not found.**4(a) represents that the transducer located on the centre axis of the solder bump. Similar to the C-scan imaging, a C-Line plot can be obtained from the B-scan image

by gating the B-scan image at a desired interface. At each transducer position, the biggest amplitude in the gated A-scan signal is taken as the amplitude in that transducer position of the C-line plot. Figure 4(b) shows the C-line plot obtained from the B-scan shown in Figure 4(a) by gating interface between 40ns to 60ns.



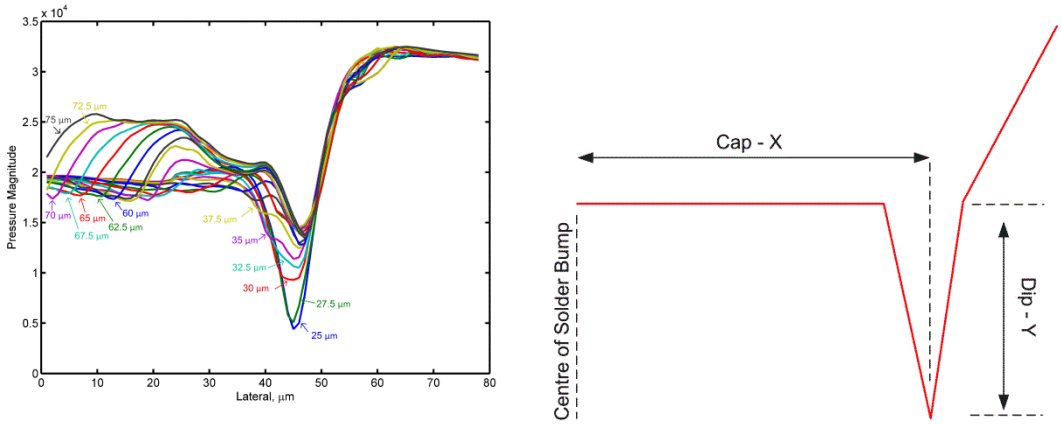
(a) (b)

Figure 4: (a) A simulated B-Scan image. (b) The C-Line plot produced by gating the B-scan in Figure 4(a) at the interface between 40ns to 60ns.

Using the finite elemental modelling described above, a number of simulations were carried out to monitor the crack propagation by the resultant B-scan images. C-Line plots were then obtained from these simulated B-scan images for the silicon die-solder bump interface. Figure 5 shows the C-Line plots for different size of cracks. The initial crack is set as 25μm as shown in Figure 3(a). The crack propagates into the centre of the solder bump underneath the UBM at an increment of 2.5μm.

To quantitatively characterise the severity of the edge effect from these C-Line plots, a key feature of Dip-Y is extracted from each C-Line plot. The Dip-Y is a feature used to

characterise the intensity of the dark ring of the solder joint C-scan image as shown in Figure 1. From Figure 5a, it can be seen that at the centre of the solder bump, the C-Line plot has a relatively flat profile. This flat region has been named as the cap as shown in Figure 5a. This was followed by a trough which is caused by the edge effect. The peak intensity of the trough, i.e., the minimum intensity in the C-line plot is defined as Dip-Y as illustrated in Figure 5b. From Figure 5a, it can be seen that as the crack becomes bigger, the Dip-Y value increases, i.e., the trough becomes shallower.



(a) (b)

Figure 5: (a) The C-Line plots obtained for different crack sizes by finite element modelling; (b) Illustration of Dip-Y and Cap-X definition.

Figure 6 plots the obtained Dip-Y against the crack size. From Figure 6, it can be seen that the Dip-Y reaches a quasi-saturation point beyond a crack of 55µm. This is due to the edge effect mainly occurring in regions at and close to the edge of the UBM structures [8]. Due to the transducer resolution limitation, current scanning acoustic microscopy cannot quantitatively evaluate small defects directly through C-scan images. The feature Dip-Y extracted from the edge effect seems to be an efficient way for defect sizing.

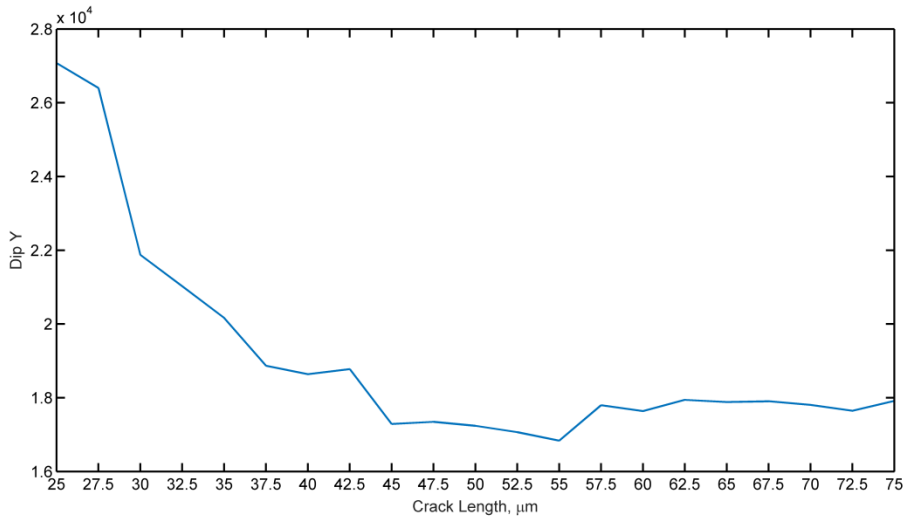


Figure 6: Crack sizes verse Dip-Y extracted from the simulated C-Lines.

4. Experimental verification

The experimental verification is based on our previous experimental data obtained in the study on through-life monitoring of solder joints using acoustic micro imaging [2]. A multipurpose test board was designed to enable reliability experiments to be undertaken to study the performance of various IC, PCB and solder configurations. An organic FR4 board containing 14 flip chips spread over both sides of the board was used in the tests. The flip chips contained 109 solder joints of 125μm height, 140μm diameter positioned in a staggered fashion at the periphery of the package. The silicon die thickness is 725μm and the die size is 3948μm × 8898μm. Accelerated thermal cycling (ATC) testing was carried out on these test samples.

Before the start of the ATC testing, AMI imaging and X-ray imaging were performed on the flip chips. The initial inspection confirmed that no cracks were generated during assembly and provided datum points for future comparison. Parameters obtained from this image were used as reference features to represent a healthy joint. Then, the board was subjected to thermal cycling testing. The testing was performed for a total period of 96 thermal cycles

after which time most of the solder joints had failed due to thermal fatigue loading. At each 8 cycle intervals, the board was removed from the chamber to investigate its integrity using acoustic imaging with a 230MHz focusing transducer and X-ray imaging. The ultrasonic C-scan images were acquired by gating to silicon die- solder joint interface. More details for sample preparation and experimental procedure can be found in ref.[2]. In [2] and [3], a few methods based on the image processing techniques were proposed to monitor the crack propagation for through-life monitoring of solder joints.

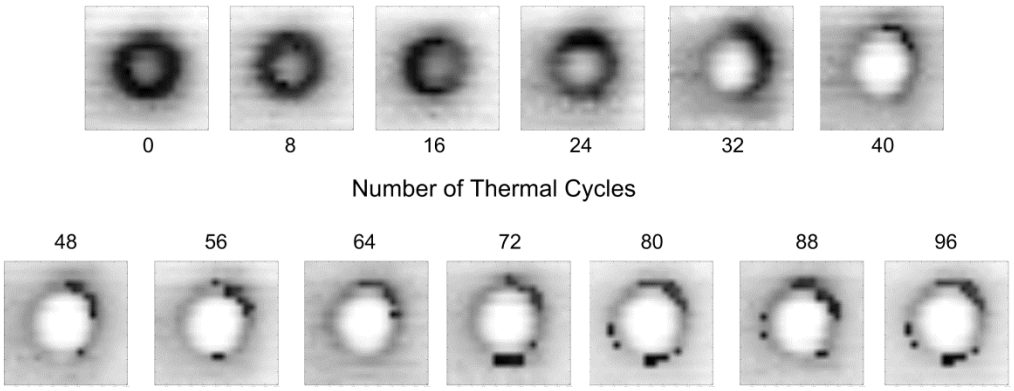
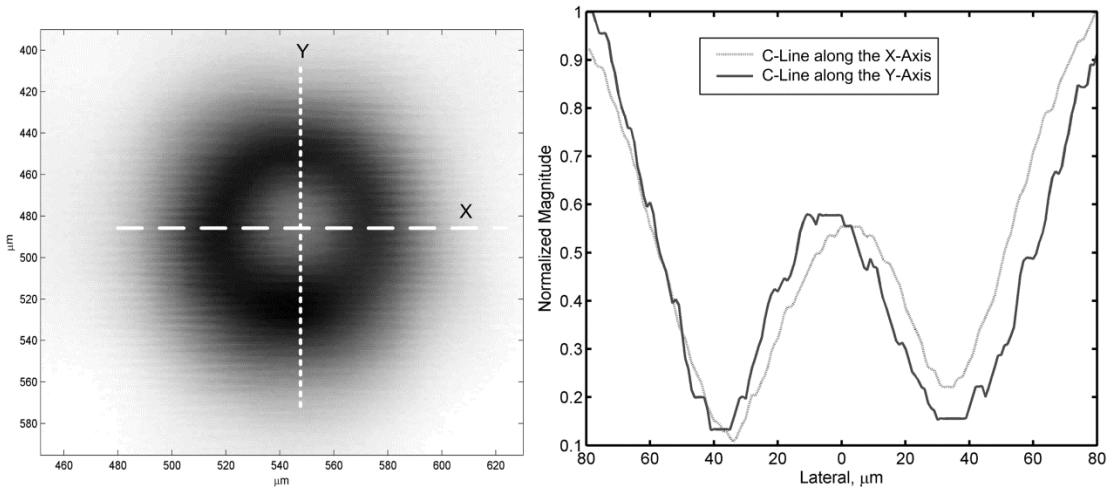


Figure 7: C-scan images of a solder bump before thermal cycling and after various number of thermal cycles.

Figure 7 shows the acquired C-scan image examples of a solder bump during the ATC testing after a certain number of thermal cycles. A number of C-Line plots can be obtained from an experimental C-scan image by directly extracting the cross-sectional profiles of the intensity (the pixel value) along various axes which pass through the centre point of the solder bump. Figure (b) shows two C-Line examples obtained from the C-scan image shown in Figure 7(a) along the two illustrated axes.



(a) (b)

Figure 8: (a) A measured C-scan image; (b) Two C-Line plot examples obtained from the image in (a) along the illustrated axes respectively.

Figure 9 shows the C-Line plots obtained from the C-scan images of a solder joint before and during the ATC testing. The C-Line plots were extracted along the X-axis as illustrated in Figure 8(a). Due to a lack of reference point in the image acquisition, the C-Line plots are unaligned. This is done in this paper by manually aligning the C-line plots along the rise transition. The rise transition describes the positive gradient caused by high reflections. This occurs when the transducer is positioned over the silicon die-water interface. In Figure , this is observed between 110µm and 150µm. Under the assumption that the solder bump is symmetrical, the C-Lines in Figure 9 are halved by discarding the left side of 0µm to 80µm for the purpose of comparison to the simulated results in Figure 5. Thus, the aligned C-Line plots are presented in Figure 10. Note that 0µm on the lateral axis in Figure 10 represents the centre of the solder bump.

Similar to the simulated C-Line plots, the Dip-Y feature can be directly obtained from the experimental C-Lines shown in Figure 10. The relationship of the Dip-Y against the number of thermal cycles is plotted in Figure 11. Notice that the number of thermal cycles is an

indicator to the crack size. A line obtained through curve fitting is plotted in Figure 11 as well. From Figures 6 and 11, it can be seen that the Dip-X is a suitable feature to characterize the crack size and crack propagation.

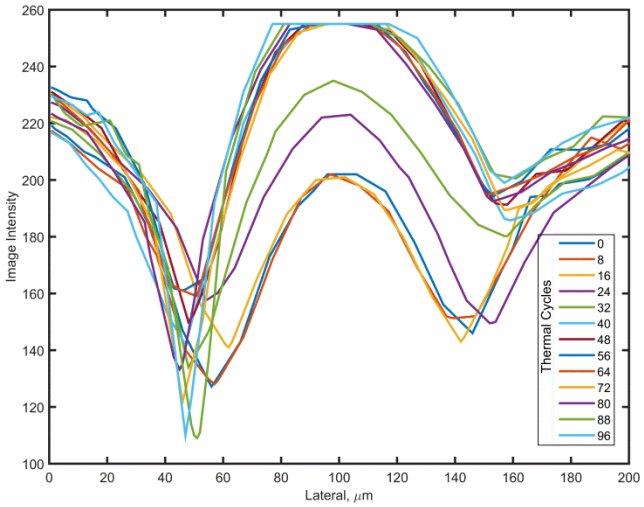


Figure 9: C-Line plots extracted from the experimental C-Scan images of a solder bump before and during the ATC testing.

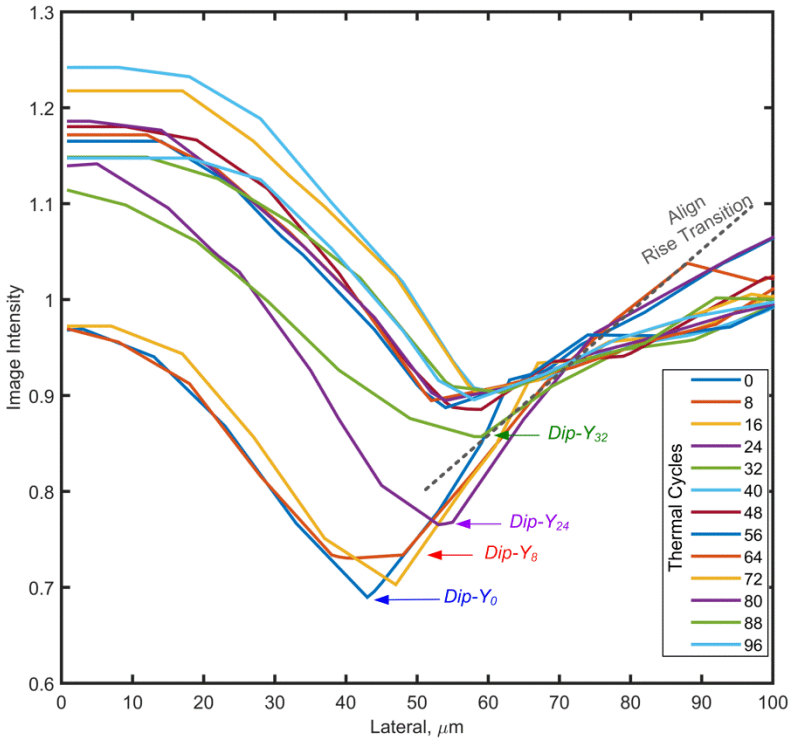


Figure 10: Aligned C-Line plots from Figure 9.

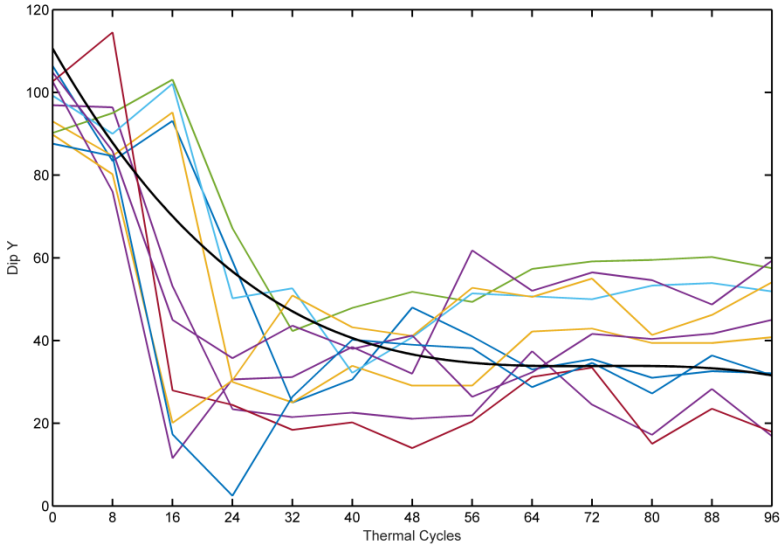


Figure 11: Dip-Y versus the number of thermal cycles.

5. Discussions

In this paper, a feature Dip-Y is extracted from the C-line plots to characterize crack propagation. Advanced techniques to compute the proposed the feature is expected. Moreover, more features could be extracted from the C-Line plots to detect defects and monitor crack propagation in the future, and fusion of all the extracted features could further improve the monitoring accuracy of crack propagation. For example, the Cap-X illustrated in Figure 5b is a potential feature to characterise the gradual expansion of the bright central region of the solder joint C-scan image as shown in Figure 1. The Cap-X value can be defined as the width from the centre of the solder bump, i.e., zero X-axis position in Figure 5a to the lateral position of the Dip point as illustrated in Figure 5b. Since significant acoustic energy being reflected by the crack as the crack propagates, the Cap-X should decrease across the crack propagation.

Due to the limited pixels of the solder joint in the both the simulated and experimental C-scan images, the extraction of the Cap-X feature is not accurate. Therefore, the results are not presented in this paper. This issue can be tackled by acquiring the solder joint C-scan images using a small scanning step size in future experiment and simulation.

For the extraction of C-Lines from the experimental C-scan images, averaging all the possible C-Lines rather than extracting the C-Line from a single cross-section of a C-scan image will improve the quality of the C-Lines. More advanced data processing techniques for alignment of the experimental C-Lines will also benefit the proposed crack propagation characterization technique.

Reducing the interval of acoustic micro imaging inspection during the ATC testing, for example carrying out an AMI inspection for every thermal cycle, will help us build a more accurate relationship between the extracted features and the crack size, particularly benefiting the monitoring of early crack propagation because of the non-linear effect of crack propagation versus the number of thermal cycles as seen in Figures 6 and 11.

From the destructive failure analysis experimental results in our previous study [2], it showed that crack initiations usually originate from the outer parameter of the solder bump [2] which is the focus of this study. Other types of defects like voids and on rare occasions, the cracks initiated from the centre of the solder bump needs further study in the future.

6. Conclusions

In this paper, a crack propagation characterization technique has been proposed for non-destructively through-life monitoring of solder joints. The proposed method is developed on the basis of edge effect observed in the C-scan image of a solder joint. Firstly, two dimensional finite element modelling is carried out to numerically monitor the crack propagation inside a solder joint by modelling acoustic imaging of a flip chip package. B-scan images for different size of cracks are obtained through the finite element modelling. C-Line plots which can be used to analyze the edge effect are then extracted from the simulated B-scan images. A feature called as Dip-Y is further developed to characterize the C-Line plots. The relationship between the feature and the crack sizes is investigated. Simulation results show that the feature Dip-Y can be used to characterise crack propagation.

An experiment is developed to verify the proposed crack characterization technique. A test board consisting of flip-chips is subject to ATC testing. The flip-chips were inspected using acoustic micro imaging before the ATC testing. During the ATC testing, the test boards were taken out from the thermal cycling chamber at an interval of 8 thermal cycles to be scanned by AMI. C-Line plots are extracted from the experimental C-scan images. The relationship between the Dip-Y versus the number of thermal cycles is presented. Experimental results confirmed the efficiency of the proposed technique.

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