Effect of p-NiO_x junction termination extension on interface states in NiO_x/β-Ga_2O_3 heterojunction diodes

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A B S T R A C T

Vertical p-n hetero-junction diodes (HJDs) were fabricated by employing NiO_x/β-Ga_2O_3 with p-NiO_x junction termination extension (JTE). It is found that NiO_x JTE leads to reduce interface states density in devices based on a smaller voltage hysteresis interval in I-V hysteresis analysis and a decrease in parasitic capacitance in C-V characteristics. It is due to the fact that JTE help to the retrain the activation of interface states. This study provides a basic understanding of interface states and lays the groundwork for the development of guiding principles for the design of Ga_2O_3 HJDs.

1. Introduction

The emerging The β-Gallium oxide (Ga_2O_3) has emerged as a promising ultra-wide bandgap semiconductor [1,2], demonstrating significant advancements in the field of power electronics [3,4], particularly in Schottky barrier diodes (SBDs) [5–7], p-n diodes [8,9], and field effect transistors (FETs) [10,11]. It is attributed to the high critical electric field (8 MV/cm) and superior Baliga's figure of merit (FOM), resulting from its 4.5–4.9 eV wide-bandgap [12–14]. In addition, n-type doping of Ga_2O_3 can be achieved through Si or Sn doping, thereby enabling the realization of easily controllable electron concentrations ranging from 10^{16}-10^{19} cm^{-3} [15]. Consequently, Ga_2O_3 holds tremendous potential to open new avenues for development of next-generation power electronics applications.

Currently, the p-NiO_x is frequently employed to integrate with β-Ga_2O_3 to achieve high performance devices due to the difficulty in achieving the p-type doping in β-Ga_2O_3 [16,17]. Typically, it is sputtered-NiO_x that is used in field plates and guard ring for SBDs [18,19], as well as p-region to be as hetero-junction for HJDs [20,21]. However, large density of interface states distributes at NiO_x/Ga_2O_3 interface [22, 23]. Note that the interface states degrade device performance and reliability [24,25]. Interface engineering related to minimize interface states density remains a challenge in the NiO_x/Ga_2O_3 heterostructures. Moreover, there has been little in-depth analysis on the interface states at NiO_x/Ga_2O_3. It is reported that the interface states density decreases sharply after annealing, resulting a much lower voltage hysteresis interval in NiO_x/Ga_2O_3 HJDs [26]. The improved interface quality through annealing contributes to the high temperature operation capability in NiO_x/Ga_2O_3 HJDs [18]. Annealing process was carried out to improve interface quality to achieve enhanced breakdown characteristics [27]. However, it should be noted that the annealing process causes a change unintentionally in hole concentration in NiO_x, which affects the devices performance accordingly [28].

In this work, NiO_x/β-Ga_2O_3 pn HJDs with JTE were fabricated and studied. The optimized I-V hysteresis and C-V characteristics demonstrate that the introduction of JTE contributes effectively to decrease in the detected interface states density.

2. Experiment

As shown in Fig. 1(a), (b), and (c), three types of vertical pn HJDs consisting of NiO_x/β-Ga_2O_3 with different device structures have been fabricated, respectively. For the purposes of discussion, these devices have been named S1, S2, and S3, which refer to HJDs without a JTE, HJDs with a 10 μm-extended JTE beyond the edge of the anode, and HJDs with a fully extended JTE, respectively. The devices were fabricated on a commercially obtained β-Ga_2O_3 wafer consisting of highly Sn-doped β-Ga_2O_3 (001) substrate and 10-μm-thick lightly Sn-doped Ga_2O_3 drift layer using halide vapor phase epitaxy (HVPE) technique. The doping concentration of the lightly doped Ga_2O_3 layer is determined to

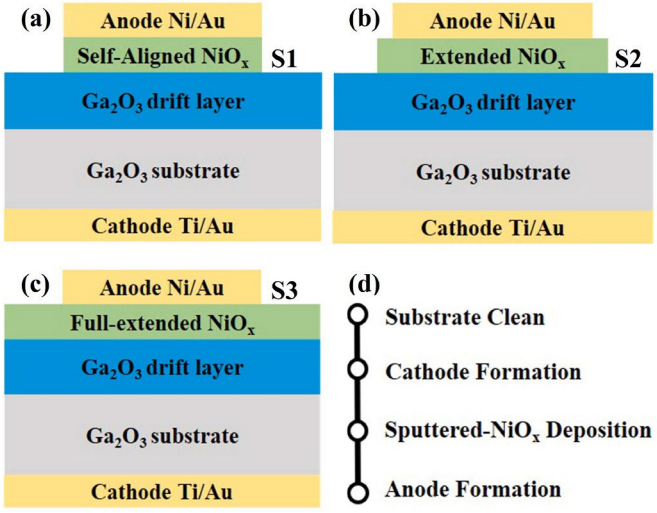

Fig. 1. Cross-sectional schematics of vertical NiO_x/β-Ga_2O_3 pn HJD with different device structures. (a) HJD without JTE, (b) HJD with 10 μm-extended JTE beyond the edge of anode and (c) HJD with full-extended JTE. (d) Key steps in fabrication of NiO_x/β-Ga_2O_3 HJD.

be ~3.6 × 10^{16} cm^{-3} from C-V measurement. Fig. 1(d) illustrates the key steps in the fabrication of devices. Prior to the fabrication of devices, the Ga_2O_3 wafer was initially cleaned with RCA critical cleaning technique [19]. The cathode Ti/Au (20/200 nm) was deposited on the back side of Ga_2O_3 wafer by E-beam evaporation (EBE), followed by Ohmic annealing in N_2 ambient at 440 °C for 1 min. Alignment mask and p-NiO_x layer areas were defined by photo-lithography on the front side of wafer for S1 and S2. Subsequently, a 60-nm thick p-NiO_x film was deposited by radio frequency (RF) magnetron sputtering at room temperature using a 150 W power and high purity (99.99 %) NiO ceramics target. The sputtering process was carried out in an O_2/Ar gas ambient, with flow rates of 4 sccm and 16 sccm for O_2 and Ar, respectively, resulting in a gas ratio of 1:4. The chamber pressure was maintained at 4 mTorr during deposition. Regarding the deposition rate, we measured it to be approximately 0.5 nm/min during the process. The hole mobility and concentration of NiO_x film were determined to be 0.36 $cm^2/V{\cdot}s$ and ~6.2 × 10^{19} cm^{-3}, from Hall measurement, respectively. The high hole concentration is consistent with several reports in the literature [29–31], particularly for NiO films deposited under oxygen-rich conditions [32]. Note that the NiO_x film was deposited entirely on the front of Ga_2O_3 wafer for S3. Finally, a circular anode Ni/Au (45/400 nm) with a radius of 50 μm was deposited by EBE. It should be noted that all three types of devices (S1, S2, and S3) were fabricated simultaneously with a meticulous control process to ensure uniformity and minimize variations. This approach aimed to eliminate potential differences arising from distinct fabrication processes. These devices were meticulously designed to represent varying extents of JTE coverage and serve as crucial benchmarks for comparison. S1 represents HJDs without a JTE, providing a baseline for understanding device behavior without the introduction of JTE. On the other hand, S2 features HJDs with a 10 μm-extended JTE beyond the edge of the anode, representing an intermediate configuration. Lastly, S3 comprises HJDs with a fully extended JTE, offering insight into the performance implications of a comprehensive JTE design. The comparison between S1 and S3 is particularly illuminating. S1 lacks a JTE entirely, while S3 boasts an infinitely large JTE. This deliberate contrast allows for a focused analysis of the influence of JTE size on device behavior.

The forward I-V characteristics and frequency dependences of C-V characteristics were measured using a B1500 semiconductor analyzer, while the B1505A semiconductor analyzer was used for high voltage to measure the breakdown characteristics.

3. Results and discussion

Fig. 2(a) exhibits the linear scale forward I-V forward characteristics of a conventional Ni/Ga_2O_3 Schottky diode and three types of HJDs on S1, S2, and S3. Current density is normalized to anode area. At 4 V, the peak current density (I_F) reaches 172, 201, and 239 A/cm^2 for S1, S2, and S3, respectively. The minimal differential specific On-resistance ($R_{on,sp}$) is extracted to be 5.2, 5.4, 5.3 and 4.0 mΩ cm^2, for S1, S2, S3, and Schottky diode respectively. Notably, it is observed that the on-resistance of HJDs with JTE shows little change compared with that without JTE. It indicates that the impact of the JTE on the on-resistance is comparatively negligible. It is due to the fact that the on-resistance is dominantly governed by the resistance intrinsic to lightly doped Ga_2O_3 drift layer [33]. In addition, the conductive area is almost confined to the region beneath the anode and current through JTE region is insignificant [34]. Fig. 2(b) exhibits the semilogarithmic forward I-V forward characteristics of three HJDs and Ni/Ga_2O_3 Schottky diode. The turn-on voltage (V_{on}) is extracted to be 2.50, 2.30, 1.90 V and 0.72 V for S1, S2, S3, and Schottky diode at I_F = 1 A/cm^2, respectively. It is identified that turn-on voltage exhibits negative shift upon the introduction of JTE. This phenomenon may involve the modification of interface states while utilizing JTE in devices. In order to investigate the interface states for three types of devices, the NiO_x/Ga_2O_3 interface trap density (D_{it}) were estimated. The value of D_{it} can be determined by [26,35].

$$D_{it} = q^{-1}\left(\frac{\varepsilon_i}{\delta}(n-1) - \frac{\varepsilon_s}{W}\right) \quad (1)$$

where q is electron charge, ε_i is the interface layer permittivity, δ is the thickness of the interface layer obtained from C-V (under the frequency of 1 MHz), n is the ideality factor, ε_s is the permittivity of semiconductor, and W is the width of the space charge layer. The density of interface states at NiO_x/Ga_2O_3 junction were determined to be 3.6 × 10^{12} eV^{-1} cm^{-2}, 3.2 × 10^{12} eV^{-1} cm^{-2}, and 2.9 × 10^{12} eV^{-1} cm^{-2} for devices S1, S2, and S3, respectively. It implies a correlation between the JTE and a reduction in interface states. However, the devices fabrication process was meticulously controlled to ensure uniformity and minimize variations across the devices. In theory, the number of interface states should remain constant per unit area. Further discussion on the varying interface states density will be provided in the following. The I_{off} of S1 and S2 reach as low as 1.00 × 10^{-8} and 1.20 × 10^{-8} A/cm^2, respectively. However, HJD on S3 shows degradative I of 1.41 × 10^{-6} A/cm^2. The full extended JTE extends up to the edge of devices, and causes high leakage accordingly [36]. The origin of this high leakage current in S3 can be attributed to the absence of mesa isolation. The extended NiO_x layer fully to the edge of Ga_2O_3 in S3 eliminates the mesa isolation, leading to increased edge leakage. In contrast, mesa isolation remains intact in S1 and S2 due to the unextended NiO_x layer, limiting the edge leakage.

Breakdown measurements were systematically conducted on a

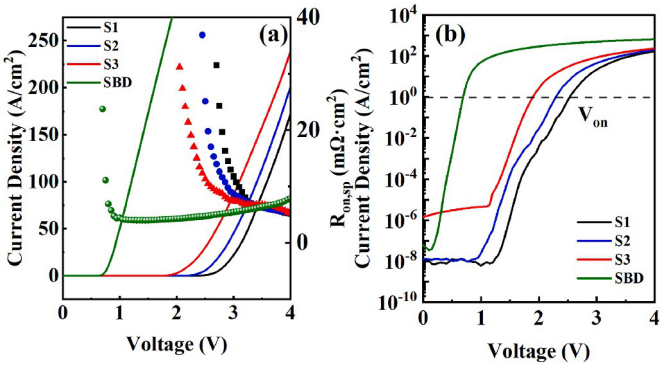

Fig. 2. Forward I-V characteristics of Ni/Ga_2O_3 Schottky diode and three types of devices for (a) linear and (b) semi-logarithmic I-V characteristics.

statistically significant number of samples to ensure the reliability and robustness of our findings. For statistical significance, breakdown measurements were performed on three separate wafers, each with an area size of 2 × 2 cm^2, across multiple fabrication runs. This comprehensive approach involved testing a total of 30 devices randomly selected from these three wafers. Fig. 3(a) illustrates the breakdown characteristics of HJDs for S1, S2, and S3, respectively. Fig. 3(b) displays box plot to represent the statistics of the breakdown voltages measured across the three types of devices. The breakdown voltage is yield to be 870 V for S1, but impressively enhanced breakdown voltages of 1043 V and 2065 V are achieved for S2 and S3, respectively. Therefore, it is interesting to be noted that the JTE can be identified to be an effective technique for improving and achieving superior breakdown voltage performance.

In order to further investigate and validate the impact of the JTE on the performance of our heterojunction diodes. The simulated 2-D electric field distributions for devices S1, S2, and S3 are shown in Fig. 4(a), (b), and (c), respectively, under a reverse bias of 1000 V. Notably, the simulations unveil a distinct electric field "hotspot" beneath the anode edge near NiO_x/Ga_2O_3 interface for all three devices, coinciding with the location of the peak electric field. Intriguingly, with the introduction of the JTE, the electric field distribution undergoes a notable transformation, becoming more uniform. To provide a closer examination of the electric field behavior, Fig. 4(d) depicts profiles along the cut-line below the NiO_x/Ga_2O_3 interface at 1 nm. Focusing on the NiO_x and Ga_2O_3 interface, the peak electric field in S1 reaches 6.1 MV/cm. However, a significant reduction is observed with the implementation of JTE, resulting in peak electric field values of 2.6 MV/cm in S2 and 2.2 MV/cm in S3. The observed reduction in the electric field, as attributed to the spreading and mitigating effects of the NiO_x JTE on the electric field distribution, aligns seamlessly with our experimental breakdown characteristics. This effect is crucial in preventing localized areas of high electric field, contributing to the overall improvement in device performance. Building on this insight, it is educible that the influence of the JTE on the electric field is not limited to reverse bias conditions. In the context of forward characteristics, the JTE is expected to exert a similar influence by spreading the electric field more uniformly. Further discussion on the JTE will be provided below.

In order to verify and analyze the interface states in NiO_x/Ga_2O_3 heterostructure, I-V hysteresis analysis was utilized. Note that during the sweeping process, charges are trapped by the interface states. The charge trapping alters the localized electric field within the devices, resulting in a change in current flow and occurrence of voltage hysteresis interval (ΔV) [37–39]. Fig. 5(a), (b), and (c) depict the I-V hysteresis characteristics of three device categories for S1, S2, and S3, respectively. This analysis involved subjecting all three types of devices to subsequent two voltage sweeps. In the first sweep, the ΔV is being extracted to be 0.50 V, 0.44 V, and 0.34 V for S1, S2, and S3, respectively. The hysteresis interval suggests that a multitude of interface states is presented at the junction of NiO_x/Ga_2O_3. However, there is a difference hysteresis interval among three devices. The impact of the JTE in devices S2 and S3 is clearly reflected in the observed reduction of ΔV. This effect can be attributed to two primary mechanisms. Firstly, the JTE lowers the electric field at the edge of anode by mitigating electric field strength and redistributing potential in the proximity of the junction, and operates as a charge blocking layer, thereby preventing augmented bulk fields [40,41]. It is crucial to note that the electric fields can stimulate interface states through thermal emission, and the excitation efficiency of defects can be enhanced by these electric fields [42,43]. Therefore, it can be inferred that the utilization of JTE results in a reduction in the detected interface states density by restraining the activation of interface states, ultimately leading to a reduction in ΔV. Secondly, as the electric field is mitigated by introducing the JTE, the strength of the driving force for electron injection is diminished, leading to a lower incidence of electrons being trapped by the interface states. In simpler terms, the introduction of the JTE causes fewer electrons to be trapped, resulting in weaker accumulation of localized electrons at the interface compared to devices without the JTE. Consequently, this leads to a reduced ΔV through the implementation of the JTE. In a word, the reduced ΔV by implementation of the JTE suggests a concurrent reduction in interface states density. This observation aligns consistently with the calculated D_{it}, reinforcing the connection between the JTE and the modulation of interface states density. Interestingly, the elimination of hysteresis was observed in the second sweep, highlighting the reversible nature of interface states. This phenomenon suggests a dynamic equilibrium between the trapping and release of electrons. The large number of electrons trapped during the first sweep effectively saturates the interface states, leading to a state where most of the traps are occupied and incapable of capturing additional charges. Consequently, in subsequent sweeps, these previously filled traps cease to actively participate in electrons trapping, resulting in the elimination of hysteresis. Furthermore, this observed behavior suggests that these states exhibit characteristics of slow traps. Slow traps are known for their extended capture and release times, aligning with the findings of persistent electrons occupation in these states throughout the second sweep. This intricacy adds a layer of depth to our understanding of the temporal dynamics of interface states. Notably, the elimination of hysteresis observed in the second sweep for S2 and S3 suggests that the majority of interface states become saturated with trapped electrons after the first sweep. This saturation reduces the capacity for further

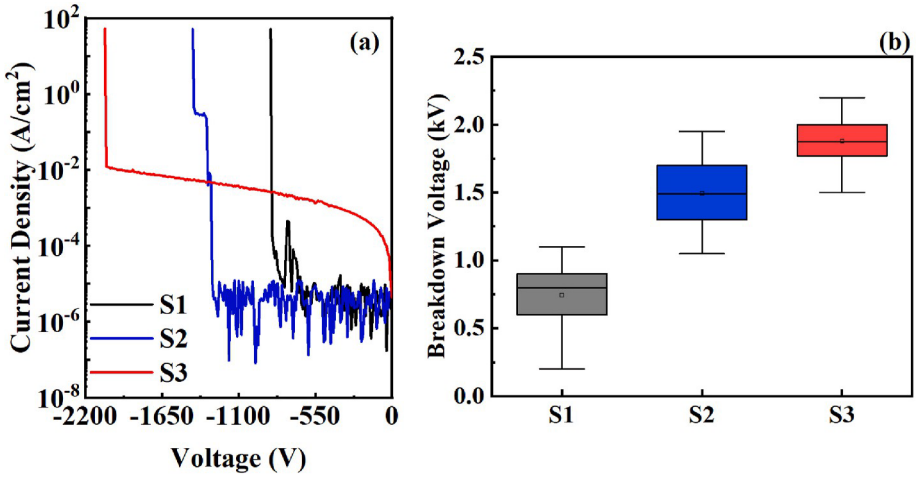

Fig. 3. (a) Breakdown characteristics of three types of devices. (b) Box plot to represent the statistics of the breakdown voltages measured across the three types of devices.

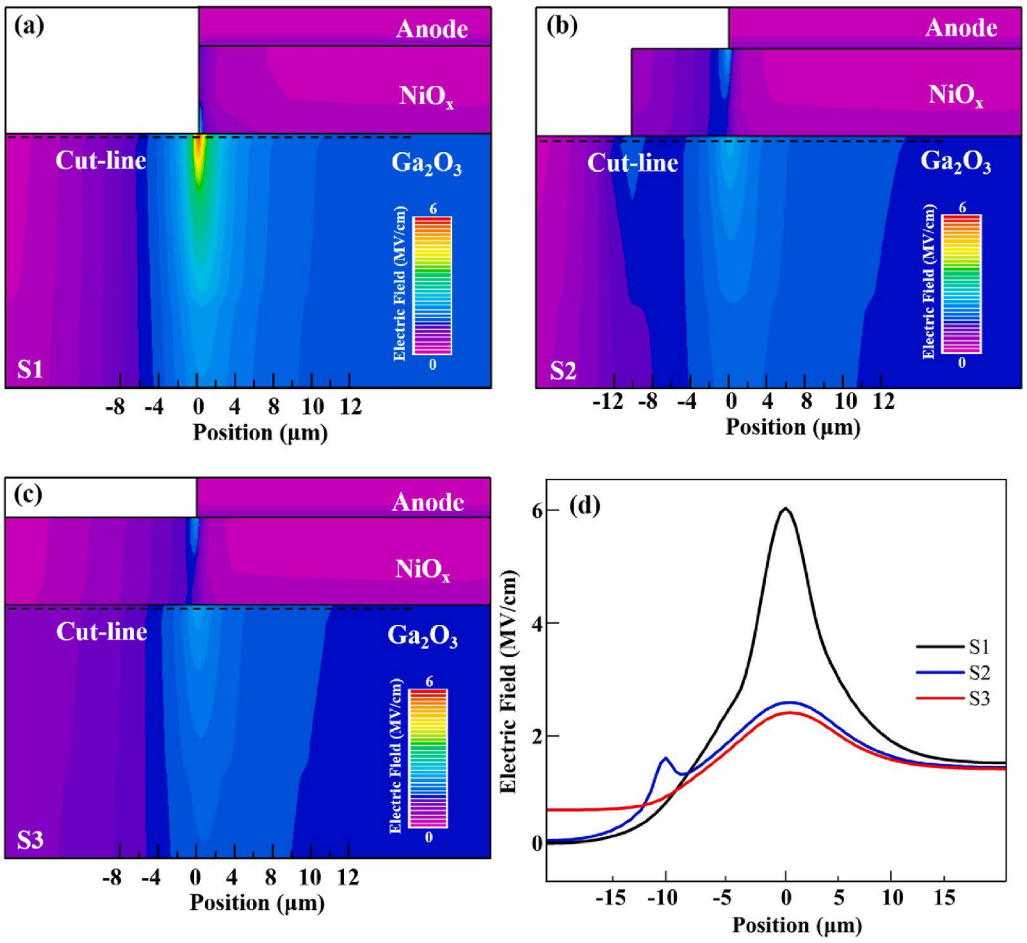

Fig. 4. Two-dimensional electric field distributions at reverse bias for all three types of devices. (a) HJD without JTE, (b) HJD with 10 μm-extended JTE and (c) HJD with full-extended JTE. (d) Simulated electric field profile at cut-line position below the NiO_x/Ga_2O_3 interface at 1 nm.

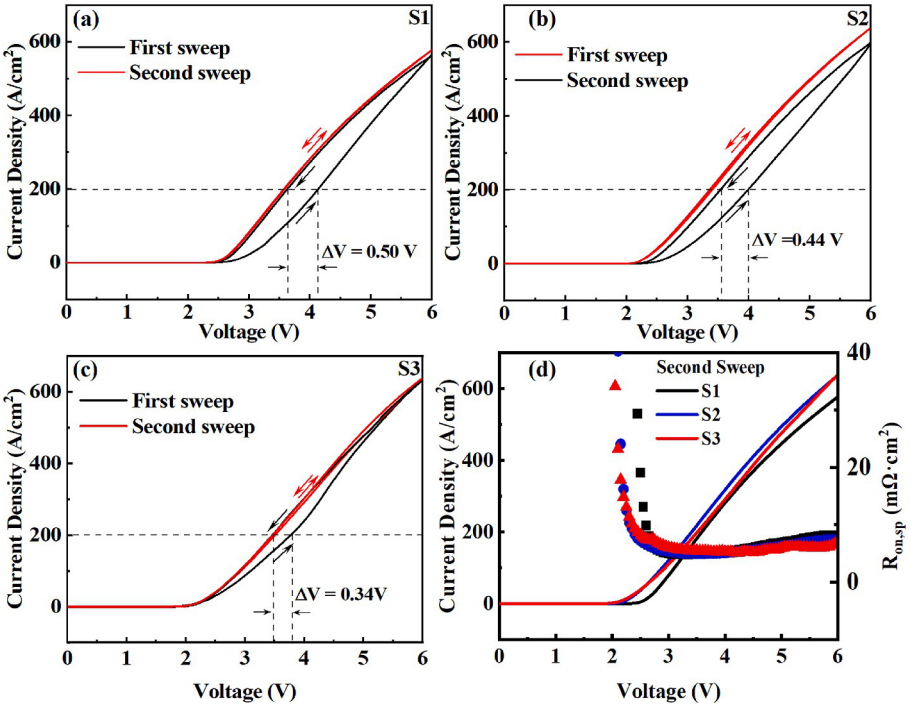

Fig. 5. I-V hysteresis characteristics of three types of devices. (a) HJD without JTE, (b) HJD with 10 μm-extended JTE and (c) HJD with full-extended JTE. (d) Forward I-V characteristics of three types of devices for the second sweep.

charge trapping, allowing the diodes to exhibit a more stable I-V response in subsequent sweeps in Fig. 5(d). In contrast, S1, with its higher density of interface states, continues to show hysteresis due to the persistent ability to trap additional electrons.

Note that hysteresis is primarily due to the NiO_x/Ga_2O_3 interface. On the other hand, in terms of other conditions associated with fixed charges, these charges are inherently immobile, they are not actively engaged in the charge dynamics that contribute to hysteresis. Shifting focus to the conditions related to mobile charges, these charges are typically electrons or holes that are free to move within the semiconductor material. Firstly, mobile charges can undergo trapping and release processes at interfaces and within the semiconductor bulk. Therefore, it implies that the presence of mobile charge can exert a significant influence on the I-V hysteresis characteristics. Secondly, the interface NiO_x/Ga_2O_3 junction can introduce localized states. Mobile charges interacting with these states can experience altered transport properties. Therefore, the conditions associated with mobile charges encompass a complex interplay of factors including charge trapping and interface states. At this stage, confirming these intricate details is challenging, and we commit to incorporating this aspect into our future studies.

It is noted that the conventional high (1 MHz)-low frequency technique can be used to detected interface states via C-V characteristics [44]. Therefore, in order to elucidate the mechanism of interface states, frequency dependences of C-V characteristics were investigated at frequencies of 10 kHz, 100 kHz, and 1 MHz. Fig. 6(a), (b), and (c) illustrate frequency dependences of C-V characteristics of S1, S2, and S3, respectively. Under strong-accumulation conditions, obvious frequency dispersion is observed in the C-V characteristics. Initially, the capacitance exhibits an increment with increasing the voltage due to the shrinkage of depletion width. Subsequently, the capacitance decreases and shows a peak near the turn-on voltage because of the switching on of devices. Moreover, the curve peak shifts to the larger capacitance with decreasing the frequency for the three types of devices. It indicates that the interface states are slow trap and can cause slow charging behavior, a phenomenon that consistently corresponds to the elimination of I-V hysteresis observed during the second sweep. The slow trap tends to accumulate more charges at low frequency. As a result, it yields an excess capacitance at low frequency. In order to investigate the interface slow trap furtherly, the capacitance under low frequency of 10 kHz is extracted for the three types of devices, as shown in Fig. 6(d). The depletion width is equivalent for the three types of devices due to the same configuration of NiO_x/Ga_2O_3 heterostructure. Thus, the assumption can be given that the C-V characteristics for those devices should be identical. However, it shows that the peak capacitance becomes smaller with inclusion of JTE. It is due to reduction of the parasitic capacitance through lowering interface states density with the help of JTE. It coordinates with result of voltage hysteresis interval discussed above.

4. Conclusion

In conclusion, various vertical NiO_x/β-Ga_2O_3 pn HJDs with different p-NiO_x JTE structures were fabricated and investigated. The findings indicated that the introduction of JTE resulted in a reduction of the voltage hysteresis interval and a decrease in parasitic capacitance. It suggests that the detected density of interface states can be effectively lowered through the implementation of JTE structures.

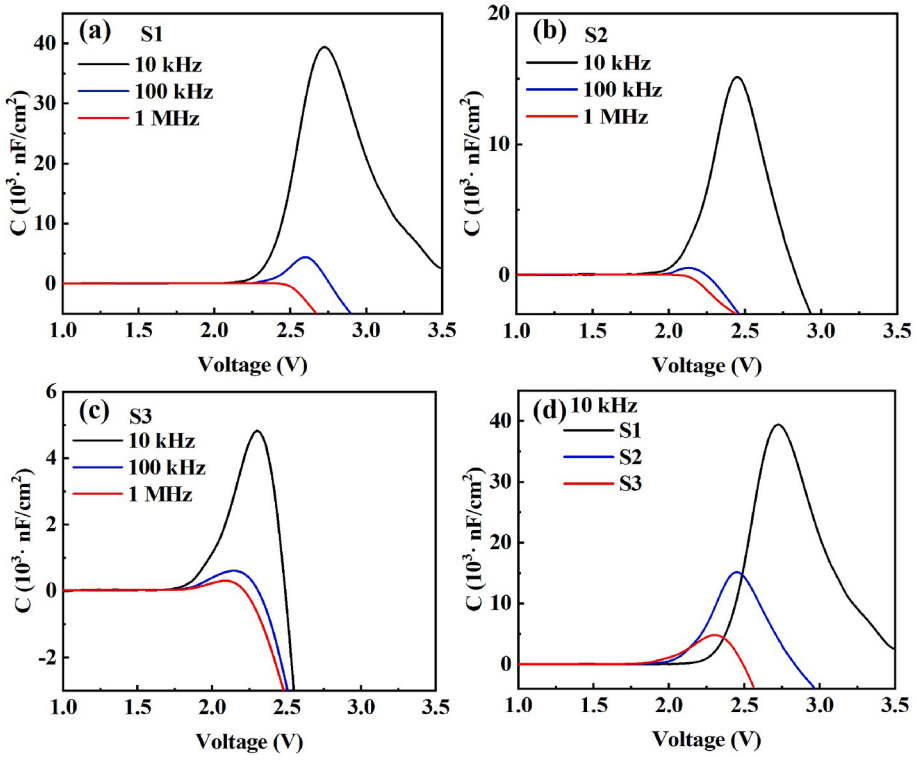

Fig. 6. Frequency dependences of C-V characteristics of three types of devices, (a) HJD without JTE, (b) HJD with 10 μm-extended JTE and (c) HJD with full-extended JTE. (d) Comparison of the C-V characteristics under 10 kHz among three types of devices.

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