BATTERY POWER ELECTRONICS INTEGRATION FOR MULTIPHASE EV DRIVETRAINS

MOHAMMAD UMAR KHAN

A thesis submitted in partial fulfilment of the requirements of
Liverpool John Moores University for the degree of
Doctor of Philosophy

April 2025

Abstract

The battery electric vehicle (EV) is the most prominent alternative to traditional fossil fuel powered cars. Most modern EVs use three-phase machines for propulsion supplied by a standard IGBT-based two-level voltage source converter connected to a single large battery pack. The two-level inverter is well-known to suffer from several disadvantages. Moreover, recent research has indicated that most driving takes place at low speeds and the two-level converter has been shown to be inefficient in such operating conditions.

Multilevel converters have been suggested for use in EV drivetrains due to their inherent benefits compared to the two-level converters. Specifically, the cascaded H-bridge (CHB) converter retains well-known benefits of multilevel converter topologies while offering unique benefits such as simplicity, modularity and redundancy, low device count, fault tolerance, reliability, and its suitability for applications where independent dc sources are readily available. This makes it particularly suitable for traction applications, especially in EV drivetrains with a distributed battery pack. Likewise, multiphase electric machines are prime candidates for propulsion in electric transportation. They offer improved reliability, natural fault tolerance, lower current per phase, and high power density. They have also been shown to be used as current filters in on-board fast and slow charging of EV batteries with minimal hardware reconfiguration leading to weight, space, and cost savings.

Therefore, this thesis examines an alternative EV drivetrain based on the combination of these two technologies to form a multilevel multiphase drive where a battery-supplied CHB multilevel inverter is used in conjunction with a six-phase induction machine. Initially, simulation and experimental results are presented for the three-phase multilevel CHB inverter, with equal dc-source voltages, connected to an RL load under different carrier-based modulation methods and min-max based offset voltage injections for the whole modulation index range. Issue of unequal dc-source and switching device utilisation in level-shifted PWM is addressed through the appropriate rotation of the reference waveforms. The operation of the three-phase CHB inverter is also investigated under the inevitable imbalance of the dc-source voltages. Improvement in the performance of a previously suggested method is made leading to better harmonic performance of resulting currents as well as achieving enhancement in dc-source energy management. The operation of the drive is verified with the open-loop control of a three-phase induction machine. High performance control of the multilevel multiphase drive is presented with experimental validation in equal dc-source voltage conditions. The previously presented method for the operation of the CHB inverter in unequal dc-source voltage conditions is further extended to a six-phase multiphase drive with multiple neutral points. The operation of the multilevel multiphase drive is verified in simulation with high performance speed control in unequal dc-source voltage conditions.

The drive benefits from modularity, inherent fault tolerance, low THD at low switching frequencies, fast dynamic performance, and the possibility to be used in both propulsion and battery charging modes with minimal hardware reconfiguration. Additionally, smaller per phase current would require smaller sized cables as well as facilitating the use of lower rated semiconductor devices. Likewise, the suggested multilevel multiphase converter requires much smaller dc-link capacitors, which translates to savings in terms of cost and space.

Acknowledgement

In the Name of Allah—the Most Compassionate, Most Merciful.

I would like to express sincere gratitude to my supervisor, Dr Obrad Dordevic, for his unwavering support and encouragement throughout the course of my doctoral studies, and most importantly for his friendship. He is a gem of a human being, always keen to offer help, educate, and engage in discussion. He sets an excellent example to follow. This would not have been possible without him.

Next, I am deeply grateful to my supervisor, Dr Martin Jones, for his continued support, supervision and guidance. I would also like to thank Prof Emil Levi for his words of encouragement and support over the years.

My heartfelt thanks to Dr Marko Slunjski and Dr Andrea Cervone for the brief but truly enjoyable time we spent together earlier on in my studies. I have also had the great opportunity to work with, learn from, and befriend Dr Angel González-Prieto and Mr Juan Carrillo Ríos during their short stay in Liverpool. I will fondly remember the time we spent engaged in truly enjoyable conversation.

Finally, I would like to thank my family, including my parents whose love and support has always been instrumental throughout my life. I would like to especially thank the pillar of my life, my beloved wife, Hina, for her continuous support and understanding, and my dear children, Noor and Ammaar, for bringing immense love and joy to my life.

Contents

List of Abbreviations

AC Alternating current
APOD Alternate phase opposition disposition
BESS Battery energy storage systems
BEV Battery electric vehicle
BMS Battery management system
CHB Cascaded H-bridge
CMV Common mode voltage
DC Direct current
DSP Digital signal processor
DTC Direct torque control
EMI Electromagnetic interference
EMF Electro-motive force
EV Electric vehicle
FC Flying capacitor
FOC Field-oriented control
FACTS Flexible ac transmission systems
FC Flying capacitor
FSHE Fundamental selective harmonic elimination
IGBT Insulated-gate bipolar transistor
IGCT Integrated gate-commutated thyristor
IM Induction machine
IPD In-phase disposition
IRFOC Indirect rotor flux-oriented control
LS Level-shifted
Li-ion Lithium-ion
MMF Magneto-motive force
MTPA Maximum torque per ampere
MV Medium voltage
MM Min-max
MMC Modular multilevel converter
MPC Model predictive control
MMC Modular multilevel converter
MMSP Modular multilevel series-parallel converter
MOSFET Metal-oxide-semiconductor field-effect transistor
MSIPD Multilevel sawtooth in-phase disposition
MSPOD Multilevel sawtooth phase opposition disposition
MTIPD Multilevel triangular in-phase disposition

MTPOD Multilevel triangular phase opposition disposition
MLI Multilevel inverter
NLM Nearest level modulation
NPC Neutral point clamped
NVM Neutral voltage modulation
NEDC New European Driving Cycle
NiMH Nickel metal hydride
NPC Neutral point clamped
OEM Original equipment manufacturer
OEW Open-end winding
PMSM Permanent magnet synchronous machine
POD Phase opposition disposition
PTC Predictive torque control
PI Proportional-integral
PR Proportional-resonant
PS Phase shifted
PWM Pulse width modulation
RFOC Rotor flux-oriented control
SHE Selective harmonic elimination
SiC Silicon carbide
SV Space-vector
SoC State-of-charge
STATCOM Static synchronous compensator
SRM Switched reluctance machine
THD Total harmonic distortion
THI Third harmonic injection
V2G Vehicle to grid
VSD Vector space decomposition
VSC Voltage source converter
VSI Voltage source inverter
WLTP Worldwide Harmonised Light Vehicle Test Procedure

List of Symbols

v Voltage in general (determined by index)

i Current (determined by index)

n Number of inverter or machine phases, or inverter neutral point

a, b, c Inverter, machine, or load phases

m, m_a Amplitude modulation index

h Harmonic number

k Number of H-bridge modules per phase leg

l Number of voltage levels of a waveform

T_m Fundamental period of the modulating wave

T_c Carrier wave fundamental period

T_s Switching time period

f_m Frequency of modulating wave

f_{sw} Switching frequency

f_{sd} Device switching frequency

$f_{sd,avg}$ Average device switching frequency

f_{si} Effective inverter switching frequency

f_c Carrier frequency

f_m Frequency of the modulating or reference waveform

f_{smc} Frequency of the sawtooth multilevel carrier waveform

f_{tmc} Frequency of the triangular multilevel carrier waveform

t_{cd} device conduction times

V_{dc} dc-link voltage

I_{dc} dc current of H-bridge module dc-source

g Number of winding sets

p Phases per winding set

θ, α, ϕ Angle in radians

$\alpha, \beta, x, y, z_+, z_-$ Indices denoting values after Clarke's transformation

d, q Indices denoting values after Park's transformation

ψ Flux-linkage

s In subscript denotes stator quantities, or star connected load neutral point

r In subscript denotes rotor quantities

ω Angular frequency in radians per second (unless stated otherwise)

ω_m Mechanical speed of rotation

ω_e Electrical speed of rotation

P Number of magnetic pole pairs

T_e Electromagnetic torque

T_l Load torque

J Inertia of the rotating mass

R Resistance (determined by index)

L Inductance (determined by index)

M Maximum value of the mutual magnetising inductance

Chapter 1
Introduction

1.1 Preliminary considerations

The transportation system contributes significantly to the emission of greenhouse gasses worldwide. In the UK, it is the largest contributor to the total greenhouse emissions as of 2017. With the sale of new petrol and diesel engine vehicles set to cease from 2030, the UK government's Road to Zero Strategy has outlined the transition to a more sustainable and environmentally friendly transportation system and aimed to achieve a planned target of 100% EV sales by 2035 (Dempsey and Hinson, 2020). Similar policy decisions globally have initiated a gradual shift towards the electrification of the transportation system. It is predicted that by 2030, 80% of all electrical energy will be processed by power electronics and electric vehicles are expected to play a major role in this transformation. Full or partially electric powertrains are growing significantly and by 2035 they will account for around 50% of the automotive market as projected in a report by the International Energy Agency (IEA, 2024).

The shift towards the electrification of the transportation system has stimulated significant research into finding optimum solutions for electric vehicle (EV) powertrain systems. Higher purchase price, lack of EV charging infrastructure, and battery charge time are all impediments to widespread EV adoption. However, one of the primary bottlenecks in the large-scale adoption of EVs is limited range. This issue needs to be addressed through research into improving storage density of the current battery technology at a reasonable cost. Concurrently, however, improvement in the function and efficiency of other drivetrain components also requires thorough investigation. Research into potential improvements that can be made in the design of the power electronic converter, energy storage system, and the selection of suitable electrical traction machines would contribute towards maximising the overall efficiency of the EV drivetrain and help alleviate range anxiety.

The internal combustion engine is notoriously inefficient with most cars achieving an overall efficiency in the range of 10%-20%, whereas current EVs are known to be at least three to five times more efficient (Bilgin et al., 2015). However, studies have shown that

although the inverters and electric motors operate at reasonably higher efficiencies at nominal loads, their efficiency drops considerably during partial load operation [(Agamloh, 2009); (Knischourek et al., 2012); (Chang et al., 2017); (Negahdari et al., 2019)]. Thus, there is considerable potential in terms of the savings from further optimising the performance of electric vehicle powertrain to achieve significantly higher efficiencies under all operating conditions, thereby increasing the range of an EV.

This research aims to improve the drawbacks of current EV drivetrains by introducing a novel design concept for increased overall drivetrain efficiency. It investigates an innovative approach for drivetrain design where the converter is integrated with the batteries to provide excitation to a multiphase electric machine for propulsion. Integration of the batteries with the power electronics will create a multilevel structure of the inverter output voltage with excellent output waveform quality, even at low switching frequency, while benefitting from higher multiphase machine efficiency and achieving space and weight reduction in an EV.

1.2 Potential benefits of the proposed solution

A three-phase machine primarily owes its existence to the adoption of the three-phase grid in the early twentieth century. An electric vehicle is battery powered and there is no requisite limitation on the number of phases of the propulsion machine. However, most current solutions for electric vehicle drivetrain primarily employ a single three-phase AC traction motor, a dc-ac power electronic converter and a single large battery pack, as shown in Figure 1.1. In addition, a battery management system (BMS) and an on-board (slow) battery charger are also provided for better reliability and practicality. This solution is expensive, inefficient and contains elements which are used occasionally, but constantly occupy extra space and represent extra load in an EV.

Integration of the batteries with the power electronics will simplify and improve the drivetrain because it can act as an active BMS, hence, eliminating the need for an additional BMS. The single battery pack will be broken down into multiple battery-converter modules making the system modular and distributed. In the case of a multiphase machine, these smaller battery-converter packs can then be used to individually supply each phase of the motor (see Figure 1.2). Splitting the power into smaller energy battery-converter packs would further improve the system and allow it to operate at lower voltages.

It is intended for the same system to be capable of being used in either of the two charging modes: single-phase – slow, or three-phase – fast AC charging. Consequently, usage of a multiphase machine can eliminate the need for additional charger commonly present in current EVs. A nine-phase machine albeit with a two-level inverter was shown to charge a single large battery by (Subotic et al., 2015). Lastly, the use of a multiphase machine enables the drive to have built-in fault tolerance capability (Duran and Barrero, 2016).

In addition to the above, with the battery-converter integration, the splitting of the battery pack into smaller units would result in the cables conducting much lower currents (e.g. 20-30 A) instead of the customary 300 A. Furthermore, the use of a cascaded battery structure will also significantly improve safety when an EV with modular battery packs is undergoing service or maintenance. This is because the maximum voltage in the car is equal to the battery pack voltage, which will be significantly reduced due to the splitting-up of the battery pack into multiple smaller units of lower total voltage (Chang et al., 2019). Furthermore, (Chang et al., 2019) have shown that the efficiency of the standard two-level inverter at partial loads is typically not very good, and it was shown to be considerably improved using a multilevel Si transistor-based inverter. Therefore, by splitting the battery and integrating it within a multilevel converter, the efficiency can be improved.

For propulsion, contemporary electric vehicles primarily employ either the three-phase permanent magnet or induction type motors in combination with a three-phase voltage source converter. While, for charging of the EV's battery bank, an additional charging unit is normally installed on the EV. However, since both the on-board charger and the power electronic components used during the propulsion mode are essentially similar, recent research has been directed towards the integration of the power electronics used for propulsion and charging. This would make a separate charging unit redundant and, consequently, offer potential savings in terms of cost, spare space, lesser weight, and associated savings on running fuel cost (Subotic et al., 2015). Although, not studied in this project, the designed topology is also potentially suitable to enable Vehicle-to-grid (V2G) mode of operation.

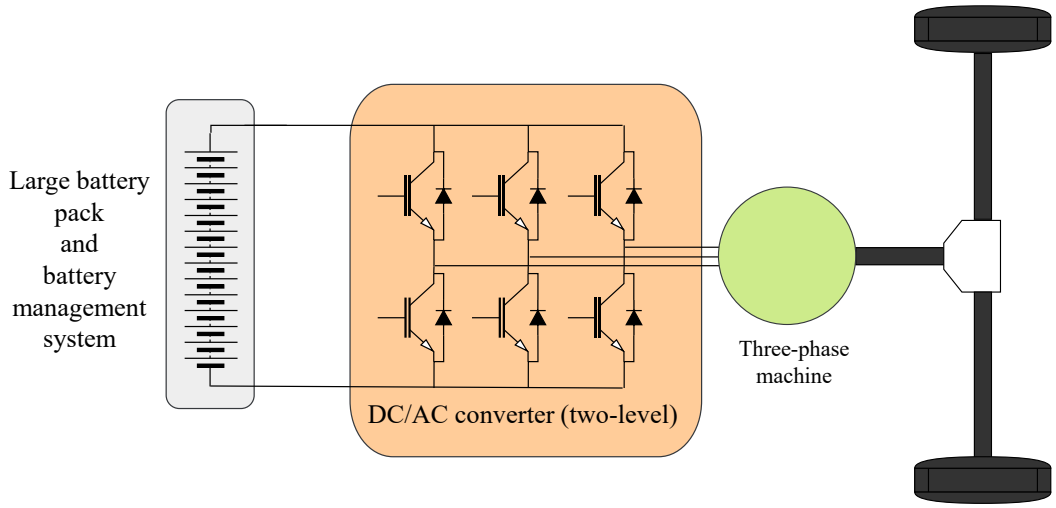


Figure 1.1: A typical EV drivetrain topology (simplified).

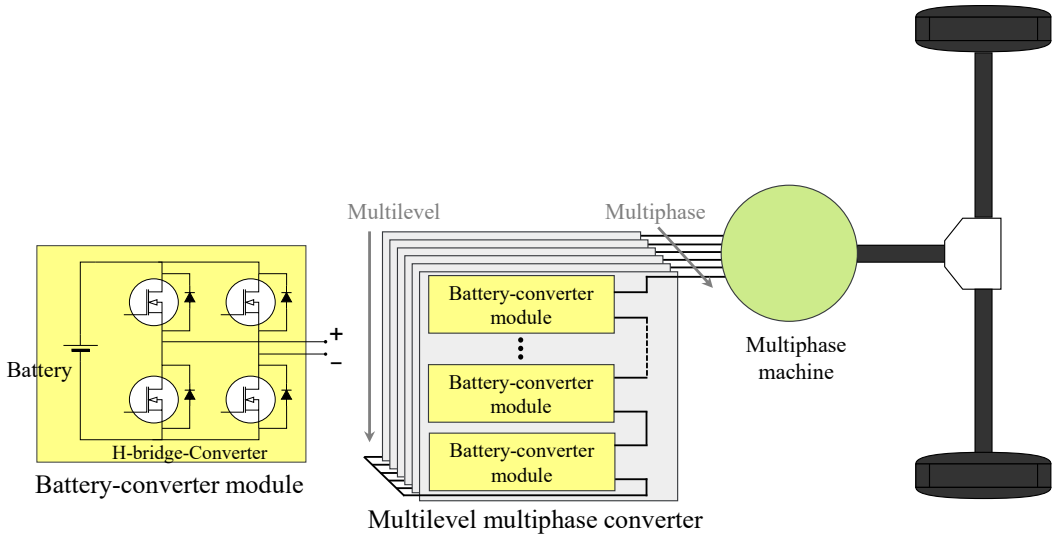


Figure 1.2: The proposed multilevel multiphase drivetrain topology (simplified).

1.3 Research objectives and novelty

This project is aimed at improving the drawbacks of currently used EV drivetrains which are primarily based on the two-level inverter drive with a three-phase machine for propulsion. An innovative approach for drivetrain design was investigated where a multilevel cascaded H-bridge converter with integrated batteries and a multiphase electric machine is used for propulsion. The following key objectives were formulated to meet the aim:

1. To investigate and compare different modulation methods applicable for a multilevel structure using a cascaded H-bridge (CHB) multilevel inverter (MLI) for the entire

modulation index range in terms of the harmonic performance of the phase voltages and currents.

2. To design appropriate battery state-of-charge balancing algorithm through the appropriate rotation of the reference or carrier waveforms to achieve balanced operation of the inverter (equalise dc-sources).

3. To develop a method that accounts for the naturally expected dc-source voltage/state-of-charge imbalance to achieve balanced operation of the machine (overcome unequal leg voltages).

4. To develop control algorithm for multiphase machine which includes the previously formulated algorithm, and which will enable propulsion.

5. To test the developed control algorithms by simulation, verify them experimentally in the laboratory conditions, and compare the performance.

The originality of the conducted research can be attributed to the achievement of the aforementioned objectives. The application and comparison of different min-max based offset voltage injections in a symmetric three-phase CHB inverter were studied in (Khan et al., 2022). It resulted in the conclusive determination of the second min-max offset injection and the double min-max offset voltage injection as the most optimal solutions among the tested injection methodologies in terms of the harmonic performance of the phase current in CHB inverters. The issue of unequal dc-source utilisation and equal power distribution in the level-shifted PWM was also discussed and a solution based on the cyclic rotation of the carriers and the resulting battery currents was presented.

Next, the performance of the so-called neutral voltage modulation (NVM) method, developed by (Kim and Cho, 2022) using the phase-shifted (PS) PWM for unbalanced dc-source voltage conditions, was improved with an appropriate modification of the level-shifted (LS) PWM in (Khan et al., 2024b). The operation of the CHB inverter under unbalanced dc-source voltages resulted in superior harmonic performance of the inverter phase currents while achieving extension of the modulation index range. The issue of the switching harmonic ripple at twice the carrier frequency associated with the PS-PWM in unequal dc-source voltage condition was successfully mitigated with the suggested adjustment of the LS-PWM method. The suggested solutions also showed enhanced energy

management of the dc-sources for extended operation, when compared to the originally proposed method.

After that, the implementation of a high-performance control of a six-phase induction machine (IM) for EV application using a battery-supplied five-level CHB-MLI was shown for the first time in (Khan et al., 2024a). The validity of the designed system for the operation of the drivetrain under different reference speeds was confirmed. The obtained results showed low harmonic distortion of the machine voltages and currents at a relatively low switching frequency.

Finally, the application of the methodology developed in (Khan et al., 2024b) for three-phase systems was applied (in simulation) for the first time to the high-performance control of an asymmetrical six-phase induction machine under unequal dc-source voltages (subsection 5.4.3). The obtained results confirmed the extension of the modulation index range under dc-source voltage imbalance where the balanced operation of the six-phase machine was shown for different speeds. In this way, the inevitable total dc-source (and inverter leg) voltage imbalance was countered successfully to achieve balanced machine operation with significantly lower total harmonic distortion of the machine currents, as well as the elimination of the first harmonic ripple (and its sideband harmonics) at double the carrier frequency, seen in the application of NVM under phase-shifted PWM. The list of papers, which are the outputs of the thesis, are given in Appendix D.

1.4 Organisation of the report

This thesis is organised into seven chapters. The first chapter introduces the topic and provides the necessary background and motivation for research. A simplified description of the proposed solution and its potential benefits are compared to contemporary EV drivetrain solutions. Next, the research objectives and originality are given.

Chapter 2 provides an extensive literature survey on topics relevant to this project. The literature survey begins with a description of multilevel converters and their topologies including classic and hybrid multilevel topologies. Next, relevant literature on multiphase machine modelling, features of multiphase machines and their suitability for EV applications, and various control strategies for multiphase machines are discussed. The following section provides a substantial review on modulation methods including various low and high frequency modulation methods and their features. Relevant literature

comparing converter losses under different modulation methods is also presented. Subsequently, literature on battery state-of-charge estimation and balancing is presented, which includes relevant literature on state-of-charge balancing in energy storage and electric vehicle applications. Lastly, a literature review covering current drivetrain solutions for battery electric vehicles (BEV) is presented. This includes relevant publications on converter topologies such as half-bridge, cascaded H-bridge, modular multilevel converters, and modular multilevel series-parallel converters. The literature focuses on converter efficiency comparison between different topologies under different modulation schemes and different drive cycles.

Chapter 3 describes the cascaded H-bridge (CHB) topology. Next, different low and high frequency modulation methods applicable to the CHB are described in considerable detail. Each method is implemented on a 9-level CHB converter connected to a single- and three-phase RL load. A comparison is made between the performance of the modulation methods in terms of the total harmonic distortion (THD) of the voltages and current waveforms over the complete modulation index range. Following that, the issue of equal power distribution in the level-shifted modulation method is discussed and appropriate carrier and reference rotation strategies are described and compared for the whole modulation index range in terms of the total harmonic distortion of the voltage and current waveforms.

Chapter 4 expands on the operation of the CHB-MLI under balanced and unbalanced dc-source voltage conditions. First, various min-max based offset voltage (zero-sequence) injections, under different carrier-based PWM methods, are described and tested in simulation and experimentally on an RL load, where the dc-source voltages of a CHB inverter are all considered to be equal. The described offset voltage injections are compared with each other in terms of the total harmonic distortion of the produced voltages and currents for different points of the modulation index range to determine the best choice. Next, the operation of a CHB inverter under unequal dc-source voltage conditions is investigated. Performance of the previously mentioned NVM method vis-à-vis the phase-shifted PWM method is examined for a nine-level three-phase CHB inverter. The described issues are resolved with the modification of the standard level-shifted PWM method to account for unbalanced dc-source voltage conditions and the application of the NVM for the

extension of the modulation index range. A comparison between the original and the suggested method is shown, and the improvements in the performance are highlighted.

Chapter 5 starts with a discussion on multiphase machine modelling followed by a description of the field-oriented control using the rotor-flux orientation principle. Next, the operation of the multilevel CHB inverter is verified experimentally with open-loop control of a three-phase induction machine for different operating frequencies corresponding to different points on the modulation index range. This is followed by the description and implementation of the high-performance control of a multilevel (>2) multiphase (>3) drive where a battery-supplied five-level six-phase CHB inverter feeds an asymmetrical six-phase induction machine. The operation of the system is confirmed in simulation and verified experimentally for different speeds of operation. The obtained waveforms are analysed to show significantly superior performance of the CHB inverter at relatively low switching frequency. Finally, the high-performance control of the same drive is investigated in unequal dc-source voltage conditions where the previously developed methodology is successfully employed (in simulation) to a multiphase machine. The obtained results demonstrate the correctness of the developed system along with the improvement over the originally proposed method.

Chapter 6 provides a summary of the completed work and offers different research directions for future work. This is followed by a list of references in Chapter 7. Finally, the end of the thesis contains appendices, where the vector space decomposition transformation, for symmetrical and asymmetrical machines with different neutral point configurations, is given in Appendix A. Next, the rotational transformation is given in Appendix B, followed by the presentation of the model of the asymmetrical six-phase induction machine in the rotational reference frame, which was used for simulation, in Appendix C. A list of the publications resulting from the thesis are provided in Appendix D.

Chapter 2
Literature survey

2.1 Introduction

In this chapter a detailed literature survey of the topics relevant to this project is given. The chapter begins with a general discussion and review of prominent multilevel inverter topologies in section 2.2. Next, the most prominent classic multilevel inverter topologies, i.e., the neutral point clamped (NPC) and the flying capacitor (FC) are reviewed. Thereafter, the cascaded H-bridge (CHB) topology is reviewed in depth, relevant literature is presented, and early important papers that propose the use of a CHB multilevel inverters (MLI) as traction inverters are reviewed. After that, other derivative and hybrid topologies for different applications are also presented and reviewed.

In section 2.3, a review of the modelling techniques of multiphase machines using vector space decomposition (VSD) and multiple d-q approach is provided. Prominent features of multiphase machines, their relevance and application to electric vehicles are examined. Next, multiphase machine control is addressed. A review of the most prominent control techniques such as field-oriented control (FOC), direct torque control (DTC), predictive torque control (PTC), model predictive control (MPC), and their respective strengths and drawbacks are reviewed.

In section 2.4, a discussion on different modulation techniques for multilevel inverters is presented. Modulation methods discussed include the phase-shifted (PS) and level-shifted (LS) pulse width modulation (PWM) strategies, and strategies focusing on the equal power distribution associated with LS-PWM modulation method. Next, a review on the selective harmonic elimination (SHE) technique, including the known methods for solving the SHE equations, is presented. The following subsection reviews literature related to the efficiency analysis of various modulation methods for the CHB inverter. After that, a literature survey on modulation techniques applicable for two-level and multilevel multiphase inverters is presented. The section concludes with a survey on space-vector PWM.

Section 2.5 provides a review of battery technology typically utilised for EV applications. A survey on battery state of charge (SoC) estimation methods and preferred

choices for EV applications are presented. Subsequently, a detailed review on battery SoC balancing is provided. The intrinsic structure of cascaded multilevel inverters makes them particularly suitable for integration with energy storage systems and EV batteries. Therefore, most literature surveyed here relates to multilevel inverter (MLI) application in the SoC balancing in battery energy storage systems (BESS) application which is closely related to the field of this research. Next, a survey of papers discussing battery SoC balancing methods related to EV applications is given. The section concludes with a discussion on other related aspects such as battery longevity and battery losses.

Section 2.6 begins with a general overview of the current EV drivetrain solutions. An overview of recent literature for current EV drivetrains in terms of inverter topologies and semiconductor devices is provided next. The literature surveyed here considers prominent topologies and the discussion is limited to modular and cascade topologies such as the cascaded H-bridge (CHB) multilevel inverter, modular multilevel converter (MMC), and the modular multilevel series-parallel converter (MMSP) supplying three-phase traction machines in an EV. The content of the literature survey chapter is summarised in section 2.7.

2.2 Multilevel inverters

The two-level voltage source converter is the most commonly used topology in variable speed drives and in most contemporary EVs because of its simplicity and reliability (Poorfakhraei et al., 2021a). However, it produces an output voltage waveform of a square shape with sudden periodic changes of peak voltage, i.e., a very high rate of change in the voltage. This is known to cause the issues such as leakage of current through the insulation in motor windings caused by the combination of the insulation and conductors acting as a capacitance. This is generally mitigated through the use of passive LC output filters which are large and expensive (Abu-Rub et al., 2010). A high $\mathrm{d}v/\mathrm{d}t$ is also responsible for causing electromagnetic interference with sensitive electronic equipment located around the motor-inverter connection.

An inverter that produces three or more voltage levels at the output terminals can be classified as a multilevel inverter. Multilevel converter development was initiated in response to the demand for converters capable of delivering higher power and voltages with minimal harmonic distortion in the output voltages and currents whilst operating at relatively low switching frequencies. In essence, an increase in the number of output voltage levels

causes the synthesised waveform to resemble a sinusoidal waveform, and as a natural consequence, amounts to lower harmonic distortion. Therefore, multilevel converters have been in development since late 1960s (Malinowski, 2017) and have since found use in various industrial applications, such as power distribution and interfacing between renewable energy sources and the utility grid.

First known patent of multilevel inverters is from (Baker and Bannister, 1975) where a staircase ac output waveform was produced using series connected multiple full-bridge cells using isolated dc sources. This came to be known as the cascaded H-bridge (CHB) multilevel converter (Rodriguez et al., 2002). Thereafter, the capacitor clamped multilevel converter was introduced where capacitors are neither connected to the positive nor to the negative dc rails – hence, named flying capacitor (FC) topology. In 1979, clever manipulation of the cascaded converter by blocking the sources using diodes to clamp the voltage resulted in the formation of a three-level neutral point converter (NPC), also known as the diode-clamped converter (Akagi, 2017). This type of converter has traditionally been used in industrial medium-voltage (MV) drives. Consequently, these three topologies came to be classified as the classic multilevel inverter topologies due to considerable research on these topologies and their extensions.

These classic multilevel topologies were together presented in an important paper by (Lai and Peng, 1996) where the authors describe the basic operating principles, salient features, limitations and potential applications of the three primary multilevel converter types, i.e. the NPC, FC and CHB inverters. Subsequently, operating principles and control techniques of these topologies have been comprehensively covered in several notable works [(Rodriguez et al., 2002); (Rodriguez et al., 2007); (Panagis et al., 2008); (Kouro et al., 2010); (Malinowski et al., 2010); (Abu-Rub et al., 2010); (Akagi, 2017); (Leon et al., 2017); (Wu and Narimani, 2017)]. In addition, these works provide a thorough discussion of other hybrid multilevel waveform generation topologies, classification and associated features, pertinent technical characteristics, relevant modulation and control schemes, common applications, and potential future applications and technological challenges. Specifically, recent developments and research in cascaded or series connected multilevel converters were covered by (Malinowski, 2017). The author describes the cascaded connection of the three major multilevel inverter topologies, and other hybrid topologies. Although many different topologies can be cascaded, a cascaded connection of full-bridge (H-bridge) modules in the

CHB converter and half-bridge modules in the modular multilevel converter (MMC) have proven to be the most popular option.

2.2.1 Classic multilevel topologies

Generally, the most commonly used multilevel converter in high power and medium voltage applications is the neutral point clamped (NPC) converter and its spin-off topologies. An early paper by (Choi et al., 1991) proposed a general circuit topology for a neutral point clamped (diode-clamped) multilevel inverter. It was shown that, in a diode-clamped topology, the inner capacitors discharge quicker than the outer capacitors that are connected to the dc-link bus. Additional voltage balancing circuitry (e.g., a buck-boost converter) can be used to facilitate transfer of energy from the outer capacitors to the inner capacitors. Alternatively, this problem can be addressed by the replacement of the capacitors with controlled constant dc voltage sources or batteries as noted by (Lai and Peng, 1996). Another important feature of the NPC MLI includes a higher rating requirement for reverse voltage blocking which necessitates the use of medium/high (higher) voltage devices such as IGCT and IGBTs (Kouro et al., 2010). In contrast, the CHB topology may use low voltage devices like low voltage MOSFETs as proposed by (Chang et al., 2017). Additionally, NPC MLI suffers from unequal conduction duration for devices that dictates the requirement for different current ratings for switching devices, resulting in loss of modularity.

The flying capacitor MLI topology was introduced initially for high voltage dc-dc conversion (Rodriguez et al., 2002). Although the FC topology has a modular structure, it requires an increasing number of energy storage capacitors, in addition to the dc-link capacitor, as the number of output levels increases. In addition to the requirement for a high number of clamping capacitors, a complicated capacitor voltage balancing control strategy is required to mitigate the problem of the voltage imbalance. For instance, the control of a five-level FC converter is noted to be much more complex than that of a four-level FC inverter (Akagi, 2017). The flying capacitors also need to be pre-charged prior to operation. Another significant issue for the FC topology is the inverse relationship between the switching frequency and the required capacitances (Abu-Rub et al., 2010). This invariably requires the operation of a flying capacitor inverter at relatively higher switching frequencies leading to increased switching losses. Alternatively, larger capacitances are needed to operate at lower frequencies to achieve proper voltage balancing.

2.2.2 Cascaded H-bridge topology

The cascaded H-bridge configuration is inherently well suited for use with multiple isolated dc sources. In the topology analysed in this thesis, the breakdown of the battery pack into separate smaller battery units can be used in conjunction with H-bridges to generate a multilevel waveform for the multiphase machine. This can be achieved by connecting each of the smaller battery unit to power each cell of the H-bridge inverter. Multiple phases can be generated by replicating the same structure to supply multiple phases of a multiphase machine.

Since a CHB-MLI is composed of multiple H-bridges, this leads to a reduction in manufacturing costs due to the modular design. A CHB structure intrinsically allows for the synthesis of a multilevel voltage waveform of higher ac voltage levels without having the issue of equal voltage sharing associated with series connected devices. Lower rated semiconductor devices can be used to form a modular structure which enables high voltage and high-power operation. A component requirement comparison between the three primary topologies (Lai and Peng, 1996) shows that CHB-MLI requires the least number of components from among the three primary MLI types for the same number of output levels. Furthermore, the structure of the CHB-MLI allows for a modular design with convenient packaging. And, as already mentioned, by virtue of having a multilevel structure of the output ac voltage, there is much lower $\mathrm{d}v/\mathrm{d}t$ stress and total harmonic distortion. A high transistor count and respective gating drivers do raise cost and reliability concerns.

A cascaded multilevel voltage source inverter (VSI) with separate dc sources (using capacitors) was proposed by (Peng et al., 1996) for use as a static VAr generator for power transmission systems. The authors argued that, practically, a diode-clamped inverter was limited to 7 or 9 levels due to the substantial increase in the requirement of clamping diodes. Similarly, flying capacitor inverters were known to be plagued by problems such as: large capacitance requirement, complicated control, and higher switching frequency for balancing capacitor voltages. Therefore, a multilevel inverter based on the CHB topology was a suitable alternative. Features such as lower switching frequency, no requirement for voltage balancing circuits, simple layout and structure, and decreased component count were cited as advantages. Simulation and experimental verification confirmed the viability of the proposed cascaded inverter, its suitability for flexible ac transmission systems (FACTS)

applications and its potential for other applications requiring isolated dc sources such as electric vehicles with several battery modules.

In (Tolbert et al., 1999), the authors anticipated the use of CHB multilevel converters as a suitable option for automotive electric drives as they generate near-sinusoidal voltage waveforms with low switching frequencies and produce minimal electro-magnetic interference (EMI) and common mode voltages. For an all-electric vehicle, the authors built a compelling case for the use of a CHB- MLI since it requires the use of multiple dc voltage sources, which could be obtained from a set of batteries, fuel cells, or super-capacitors. Subsequently, (Tolbert et al., 2002) proposed the use of a CHB-MLI for automotive electric drives. The basic structure and mode of operation of a MLI based on the CHB topology was described, where operation at high and low modulation indices was considered.

The CHB topology can be realised with either equal or unequal dc voltages as noted earlier. A generalised structure of an asymmetric CHB-MLI is presented by (Corzine and Familiant, 2002) where multiple H-bridges are connected in series to form an H-bridge module using unequal dc sources. The number of voltage levels achievable by the cascaded H-bridge inverter are maximised by setting the dc voltages in a certain ratio. In this way, power quality can be significantly improved with the use of different dc voltages (asymmetric CHB). An asymmetrical configuration of the CHB is useful in minimizing inverter losses and improved efficiency in certain applications. However, it suffers from drawbacks from loss of structural modularity such as the requirement for devices and components of different ratings and different thermal solution for each H-bridge module. Furthermore, dc sources of identical values are preferred for voltage isolation. Therefore, the asymmetric CHB is unsuitable for EV applications, as proposed in this thesis.

2.2.3 Hybrid multilevel topologies

Although not selected as a direct choice to be used in this thesis, due to mentioned complexity and non-modularity, it is worth stating that there are various other hybrid multilevel topologies. Some of these topologies are briefly reviewed in this subsection.

A dc-ac cascaded H-bridge multilevel boost inverter, without the use of inductors, for EV traction application was presented by (Du et al., 2009). The hybrid topology used a traditional three-phase two-level inverter where each leg of the inverter is connected in series

with an H-bridge using a capacitor as a dc power source. This type of converter is useful when high power is required by an EV motor; however, it requires several capacitors and a higher number of switches to realise. Similarly, an asymmetric CHB configuration (unequal dc sources) was proposed by (Tsang and Chan, 2014) with a three-phase multilevel inverter, using reduced number of switches, based on CHB topology with a single dc source and capacitors acting as the remaining dc sources. In this way, the requirement of multiple dc sources is mitigated and a better efficiency at nominal load compared to the standard two-level inverter is achieved. It was noted, however, that the voltage across the capacitors acting as dc sources, require proper regulation due to unequal current drawn from each capacitor. Additionally, since some of the inverter states do not support voltage regulation, larger capacitors were required to ensure acceptable voltage levels for inverter operation under these states.

Another MLI with a reduced component count was proposed by (Hota et al., 2017) where an optimised three-phase multilevel inverter topology is presented. This is achieved by splitting the inverter into a level generation part and a phase sequence generation part, which are cascaded together to form the MLI. In a symmetrical configuration, for a three-phase nine-level inverter output, the proposed topology requires 36 switches as compared to 48 for a conventional CHB-MLI. However, for the same number of output levels, the CHB-MLI requires only 12 voltage sources as compared to 14 required by the proposed topology. It is obvious that a reduction in the number of switches results in lower conduction and switching losses, but the requirement for a higher number of dc sources is problematic.

A paper by (Lee et al., 2018) extends the work of (Hota et al., 2017) for reducing the switching count in multilevel inverters. They have achieved this by modifying the voltage level generating basic units by replacing the half-bridge submodules with a four-level submodule with six switches. The proposed topology achieves reduction in the number of dc sources required as compared to the topology presented by (Hota et al., 2017) for both the three-phase and single-phase inverter cases. The paper shows graphically the number of switches and dc sources required. The topology requires an equal number of dc sources as that of CHB-MLI and significantly reduces number of power switches. However, a significant disadvantage of this topology for high voltage applications, and that of (Hota et al., 2017), when compared to CHB-MLI is that the maximum blocking voltage required for

each switch is equal to the sum of all dc sources. This would require switches with a significantly higher voltage rating thus increasing the price. However, this would not be a problem for low voltage applications.

In recent years, new topologies have emerged such as the modular multilevel converter (MMC), active neutral point clamped, neutral point piloted converter, several multilevel matrix converter topologies, various hybrid multilevel topologies based on the CHB and NPC topologies, which have been presented in (Kouro et al., 2010). An example of such a hybrid topology is presented in an interesting work by (Samadaei et al., 2018). The authors have introduced a topology with a reduced number of switching components using a square T-type module – a modified version of an H-bridge configuration – for an asymmetrical (unequal dc sources) multilevel inverter, for use in high power applications. Two T-type connections, each with two unidirectional and two bidirectional switches, are joined to form a square module which was shown to generate up to 17 voltage levels with 12 switches and 4 unequal dc sources. However, the use of unequal dc sources would not be a practically suitable solution for EV application due to loss of modularity and increased complexity, as the system would require batteries of different capacities and sizes.

2.3 Multiphase machines and their control

A machine with more than three phases on the stator is commonly referred to as a multiphase machine. Both the induction and synchronous type machines can be designed with multiple phase windings. The phase shift of the supply voltages in that case should match the angular shift between the individual phases. Multiphase machines can be broadly demarcated into either those that have a prime number of phases or those that have an even number of phases or a composite odd number of phases. Since three-phase machines are prevalent and their control is generally well analysed and understood, multiphase machines with phase number equal to an integer multiple of three are preferred for various applications due to similarities in their construction and control. One such machine will be analysed in this thesis. Therefore, references related to the modelling, various advanced features of multiphase machines, and their control, are reviewed in this section.

2.3.1 Modelling of multiphase machines

Multiphase machines can be modelled in the phase-variable domain using voltage equilibrium equations for the stator and the rotor windings, mechanical and torque equations, algebraic equations describing the relationship between the flux linkages and the machine currents, and the integral equation relating instantaneous rotor position with the angular electrical speed of rotation (Duran et al., 2017). In the case of a three-phase machine, transformation is carried out using the combined Clarke and Park transformation to obtain a model in a common reference frame rotating at an arbitrary angular speed. Similarly, multiphase machines may be described by transformation from a physical phase model into a dq model in the common reference frame using decoupling (or the vector space decomposition, VSD) and rotational transformation [(Zhao and Lipo, 1995); (Levi et al., 2007); (Rockhill and Lipo, 2009)]. Multiphase machine modelling has been covered in [(Levi, 2011a); (Duran et al., 2017); (Tessarolo, 2009); (Rockhill and Lipo, 2015)]. A simplified VSD transformation algorithm for any type of multiphase machine - symmetrical or asymmetrical - with a sinusoidally distributed magneto-motive force (MMF) was presented by (Zoric et al., 2017). A novel transformation technique was presented by (Rubino et al., 2021) for the modelling of a modular (multiple sets of three-phase stator windings) permanent magnet synchronous machine (PMSM) using a combination of the VSD transformation and the multiple d-q approach. This transformation allows for decoupled regulation and control of the torque developed by each of the winding sets of a modular multiphase machine.

2.3.2 Features of multiphase machines

A prominent feature of multiphase machines is the reduction in power per phase as the current is distributed over a larger number of phases. The inversely proportional relationship between the number of machine phases and per-phase current allows for the use of lower rated semiconductor devices in the power electronic converter. Another feature relates to the improvement in the distribution of the MMF in the machine airgap resulting in lower torque pulsations.

A comprehensive review paper by (Levi, 2016) reveals various innovative uses of the extra degrees of freedom enabled by the use of multiphase machines. These extra degrees of freedom stem from the requirement of only two independent currents for flux and torque

control of a machine irrespective of the total number of phases. The remaining variables can be utilised for numerous other useful purposes. For instance, the torque and power density of a multiphase machine with a concentrated winding can be enhanced by the injection of specific current harmonics, making use of the additional degrees of freedom.

Another important feature is the application of the multiphase machines in integrated on-board battery chargers in EVs. The combination of propulsion and charging components provides a positive economic benefit. This is achieved using the propulsion machine stator winding as a filter and the inverter as a rectifier during EV charging mode. An onboard integrated three-phase battery charger for EVs using only components necessary for propulsion was presented by (Subotic et al., 2015). The neutral points of the three isolated three-phase windings of an asymmetrical nine-phase machine were connected to the three-phase grid during the charging process with the current passing through a nine-phase half-bridge propulsion inverter operating as a rectifier to charge the EV batteries. The charging currents passing through each of the three-phase windings are equal and do not produce any flux or torque. The viability of the system in propulsion, charging and vehicle-to-grid (V2G) modes were investigated and confirmed. Similarly, a topology with the capability of operation both in propulsion mode and three-phase charging using the same powertrain components was presented by (Subotic et al., 2016) using a machine with a prime number of phases greater than three.

A key feature of multiphase drives is the fault tolerant capability. Fault tolerant operation is frequently a requirement in critical applications. Fault tolerant operation of a multiphase machine is made possible by the availability of additional degrees of freedom. Methodologies for the fault tolerant control of multiphase motor drives has been discussed in great detail by (Duran and Barrero, 2016). Different types of machine and inverter faults are surveyed, such as different open circuit and short circuit faults. Fault tolerant operation of a multiphase machine is achieved by the reconfiguration of the software upon fault detection and corrective post-fault control. A modification to the FOC scheme for post fault operation of the six-phase induction machine (IM) has been studied by (Che et al., 2014). Subsequently, it has been demonstrated that natural fault tolerance in a multiphase machine is possible through minimal adjustment to the FOC strategy through open-loop control of the x-y currents in case of open-phase fault conditions (Prieto et al., 2020). Although fault

tolerant operation of a multiphase machine is an important consideration for EVs, it is outside the scope of this thesis and will not be covered.

2.3.3 Control of multiphase machines

Ever growing industrial automation is primarily responsible for a continuous increase in the number of variable speed applications, and, as a consequence, an increase in the requirement for high performance applications such as robotics, machine tools, spindles, rolling mills, elevators. Multiphase machines, in particular, have found applications in high power compressors, electric ship propulsion, more-electric aircrafts, extruder pumps, high speed elevators, traction systems, electrical vehicles, and energy conversion systems (Levi, 2008).

The control system of a machine generally consists of an outer speed control loop, with a controller, generally of the proportional-integral (PI) type. The output of the speed controller is generally a reference current signal which is fed to the inner current control loop. The inner control can be realised using various control strategies. A common control technique employed in the industry for the control of ac machines is the open loop v/f control. This normally suffices for simple applications, but the dynamic speed and torque response is poor and consequently unsuitable for high performance variable-speed applications.

High performance applications require rapid, almost instantaneous, response from the motor in terms of acceleration, deceleration, and speed reversals and quick start/stop routines, all under abrupt variations in torque. Two popular high performance control methods are the direct torque control (DTC) and field-oriented control (FOC). DTC offers a fast dynamic response and low computational complexity due to simple implementation. An example of DTC scheme for EV application was presented by (Khoucha et al., 2010) where an asymmetrical CHB inverter was used to control a three-phase induction motor. However, implementation of direct torque control is rather challenging when it comes to control of multiphase drives. Additionally, DTC suffers from issues such as variable switching frequency, larger torque and current ripples, difficult control at low speed.

Field-oriented control of multiphase ac machines is prevalent and can be achieved in different ways but the most commonly used is the rotor flux-oriented control (RFOC)

methodology, which is covered in depth by (Levi, 2011b). The rotor flux-oriented control entails the use of inner current control loops and an outer speed control loop. A modified version of the RFOC scheme for the control of a five-phase induction motor drive (with sinusoidal magneto-motive force, MMF) is presented by (Jones et al., 2009). It shows that $n-1$ current controllers are required for the control of an n-phase drive to account for the low order current harmonics present due to inherent asymmetries and inverter dead time. Indirect RFOC is normally used, and various synchronization methods are applied to avoid the misalignment between the controller reference and motor reference coordinate systems. The misalignment would result in the loss of efficiency because of loss of torque and flux decoupling (Levi, 2011b).

With regard to the FOC in multilevel multiphase drives, most papers are focused on the neutral point clamped (NPC) three-level converter (Levi, 2016). For example, an FOC of a six-phase permanent magnet synchronous machine (PMSM) drive using a three-level NPC, based on space vector modulation (SVM) was presented by (Wang et al., 2016). FOC of other multilevel multiphase drives include an FOC of a fifteen-phase concentrated tooth winded PMSM (Gliese et al., 2022). Here each stator phase winding was connected to a single H-bridge module resulting in a three-level output voltage. A similar solution was suggested by (Bayati et al., 2023) but instead a reconfigurable battery is used. Each phase of a nine-phase IM was supplied by individual H-bridge modules and battery charging capability was demonstrated. In (Zaidi et al., 2019) a simulation comparison has been made between the performance of the sliding mode controller and the standard PI-based speed control of a multiphase drive with a hybrid cascaded multilevel converter with FOC applied separately to each three-phase winding set, with no x-y current control considered.

Limited literature is available on the combination of a CHB converter and a multiphase machine. An early study of a multilevel multiphase space vector pulse width modulation (PWM) of a five-level CHB converter was presented in (López et al., 2008) but an RL load was used. A simulation study showing a closed-loop v/f control of a five-phase IM drive based on a five-level CHB inverter under bipolar modulation for different load torque conditions was presented by (Rahman et al., 2019). A comprehensive study of the post fault operation of a medium voltage multiphase drive based on a CHB with a software-based x-y component voltage injection, for maximizing the dc-link voltage utilization in case of a bypassed H-bridge module, was presented in (López et al., 2024). However, none of these

papers are using FOC. On the other hand, FOC of a six-phase PMSM drive based on a five-level CHB converter was investigated for an electric aircraft powertrain in (Tedeschini et al., 2021), but the study was restricted to simulation only.

Other control methods include predictive torque control (PTC) and methods based on artificial neural networks, and other modified forms of v/f control methods. For example, the viability of predictive torque control application for the propulsion of an EV using a five-phase induction machine was established by (Riveros et al., 2010). Similarly, other alternatives using predictive current control have been proposed, as detailed in the survey by (Barrero and Duran, 2016), where inner current controllers are implemented using model predictive control (MPC) instead of classic PI controllers. MPC-based current control methodology requires no tuning for different operating points and features better dynamic performance as compared to PI controllers. However, PI controllers perform better in steady-state with a significantly smaller computational cost due to the presence of current components in non-torque/flux producing sub-planes in multiphase machines (Lim et al., 2014). Additionally, the computation cost of MPC increases with the number of output voltage levels. The reduction of computation cost of MPC has been addressed; for instance, a model predictive control method for a three-phase cascaded H-bridge multilevel converter was presented by (Chan et al., 2017) for fast dynamic applications with a reduced computation load compared to the standard MPC. Similarly for multiphase machines, efforts have been put in to achieve better quality and improved efficiency through the use of virtual voltage vectors in the finite control set model predictive control (Gonzalez-Prieto et al., 2018) or through the dynamic selection of appropriate voltage vectors due to switching state-redundancies under certain constraints (González-Prieto et al., 2019). However, these studies have been conducted for two-level multiphase converters and the implementation of model predictive control is quite challenging for multilevel multiphase systems.

Since it is an industry standard and is easily expandable to multiphase drives, rotor flux-oriented control will be used for the machine control in this thesis. Simplicity of vector control implementation will leave the microcontroller resources for implementation of other more complex algorithms related to battery monitoring, SoC and voltage balancing, etc.

2.4 Modulation methods

MPC and DTC do not require a modulation stage as gating signals for the inverter switches are directly created. But a modulation stage is needed for the implementation of scalar or field-oriented control. The inner-most control entails the generation of gating pulses with a modulator for the inverter switches to produce the inverter output voltage waveform.

Various modulation and control strategies have been devised for multilevel inverters, and they can be classified based on the switching frequency. For low/fundamental switching frequencies, the multilevel selective harmonic elimination (SHE) and nearest level modulation (NLM) are the primary modulation methods. For high switching frequencies, the classic carrier-based sinusoidal PWM including the phase- and level-shifted multicarrier PWM along with the space vector PWM (SV-PWM) are typically the preferred modulation methods (Franquelo et al., 2008). Although SV-PWM allows exploitation of additional degrees of freedom for several useful purposes, it generally requires more complex calculations as the number of levels and the number of phases increase. It is also preferable to use modulation methods which minimise switching losses by reducing the switching frequencies for high power applications. High dynamic range applications requiring enhanced output power quality are better served by a higher switching frequency algorithm [(Abu-Rub et al., 2010); (Kouro et al., 2010)].

The complexity of modulation methods usually increases with an increase in the number of the converter levels. Also, different modulation methods can significantly affect the losses of the converter, which is of considerable importance in battery powered EVs. Hence, various multilevel converter modulation methods are reviewed next.

2.4.1 Phase-shifted (PS) PWM

The standard phase-shifted carrier-based PWM (PS-PWM) is the modulation method of choice for industrial applications. The multicarrier phase-shifted PWM is an intrinsically suitable methodology for a CHB-MLI due to the modular structure of the topology (Townsend et al., 2015). Phase-shifted carrier-based PWM works by comparison of several phase-shifted carrier waveforms with a reference (modulating) signal to produce appropriate switching signals. An analytical solution of the carrier-based PWM was used by (Holmes and McGrath, 2001) to identify the opportunities for harmonic cancellation in carrier-based

PWM. The authors established the ideal phase shift required between the carrier waveforms to achieve best harmonic cancellation within each phase-leg of a cascaded MLI. For a cascade connection of k full-bridge modules, phase-shifted carrier signals with a phase shift angle of $180^{\circ}/k$ are required.

A major advantage of PS-PWM is that it shifts the spectrum to a higher frequency which can be filtered out using smaller filters. Moreover, PS-PWM features the equal distribution of power among all the CHB modules, equal losses between the devices within a module, and between different modules within a certain phase (Kouro et al., 2010). For these reasons, this modulation strategy finds use in most commercial applications of CHB based multilevel converters. The PS-PWM does produce some slight unwanted voltage distortion at the inverter output due to the phase-shift between different carriers (McGrath and Holmes, 2002). In the case of slight imbalances between dc-link voltages of different CHB modules, which is quite likely, increased lower order harmonic distortion is seen in the synthesised voltage waveform of CHB-MLI operating under PS-PWM. This could be reduced by making use of variable-shift angle PS-PWM as shown by (Marquez et al., 2017) but at the cost of increased complexity, especially for a higher number of CHBs.

2.4.2 Level-shifted (LS) PWM

The other popular PWM methodology is the level-shifted PWM (LS-PWM), also sometimes referred to as the phase-disposition PWM, and it has several variants depending on the phase difference between each of the carrier signals (Carrara et al., 1990). In the case of a level-shifted PWM scheme known as the in-phase disposition (IPD) or simply phase disposition (PD) PWM, multiple carrier signals of the same frequency, phase, and amplitude — but vertically shifted — are compared with a modulating reference to produce a multilevel phase voltage waveform. For the phase-opposition disposition (POD), the carriers above the zero reference are in phase-opposition with those below the zero reference. Finally, for the alternative phase-opposition disposition (APOD), adjacent carriers are in phase-opposition. It has been noted (McGrath and Holmes, 2002) that the THD for the line-to-line voltages is better for the level-shifted modulation scheme as compared to the phase-shifted modulation technique. However, the level-shifted modulation methods cause an uneven distribution of device conduction times and causes unbalanced power distribution among CHB modules (Rodriguez et al., 2007). This causes a variation in the switching frequency of different

devices in different H-bridge cells. Hence, there is a need to ensure that the switching pattern cyclically rotates between different H-bridge cells in order to provide balanced device switching and conduction times, which adds to the complexity of the scheme.

The issue of unequal power sharing between CHB converter cells under IPD-PWM was addressed by (Angulo et al., 2007). The authors proposed a modification to the IPD-PWM by alternating the amplitudes of the carrier waveforms related to each CHB module after a full modulation cycle to achieve a discontinuous modulation. In this way practically equal power flow from all cells within a phase is achieved, provided a sufficiently high switching frequency is utilised. The usefulness of the proposed method is confirmed with a simulation of a five-level inverter at 2 kHz switching frequency by comparing IPD-PWM and the proposed scheme with carrier rotation after every other carrier cycle. The discontinuous modulation scheme with carrier rotation is clearly shown to achieve identical switching cycles for both CHB modules compared to dissimilar switching patterns in the case of IPD-PWM. As mentioned previously, PS-PWM technique produces unwanted voltage distortion which can be avoided by means of the IPD-PWM. As the carrier rotation has been derived from the IPD-PWM, it achieves a better THD at the inverter output compared to the PS-PWM. The technique, however, does allow some higher order harmonics to appear in the input current waveform when compared to the PS-PWM. A similar methodology of discontinuous PWM using LS carrier rotation was patented by (Nondahl et al., 2015) for a multilevel cascaded H-bridge inverter. This was done to mitigate unequal power distribution between series connected H-bridge modules and achieve a better harmonic profile of the output voltage as compared to the PS-PWM.

An alternative modulation strategy for the equalisation of the power distribution between H-bridge modules has been presented by (Gupta et al., 2016). It utilises a manipulated output (double the number of levels) of the POD-PWM for the selection of appropriate switching states at specific time instants in a fundamental cycle to ensure balanced distribution of power between H-bridge modules is achieved over a single period of the modulating waveform. The method improves on the carrier rotation strategy (Angulo et al., 2007) by achieving CHB module source charge balance over a single fundamental period (T) of the output voltage instead of (nT) for the carrier rotation method. However, the methodology requires additional manipulation of the PWM signal and supplementary comparators to implement. The benefit of implementing such a technique is insignificant in

the case of a relatively small number of inverter levels where balancing occurs at a reasonable speed with the carrier rotation method.

2.4.3 Low switching frequency modulation

Among the low switching frequency modulation methods, the selective harmonic elimination (SHE) modulation is the most common choice for CHB inverter. SHE modulation at fundamental frequency is known as staircase modulation or fundamental selective harmonic elimination (FSHE). The main advantage of SHE over conventional pulse width modulation methods is that a comparable output waveform can be synthesised at a much lower switching frequency which leads to a reduction in switching losses associated with high frequency switching. Elimination of certain lower order harmonics from the output waveform thus requiring smaller filtering requirements and ease of implementation are the primary reasons for its popularity.

Elimination and control of specific lower order harmonics is achieved by solving non-linear transcendental equations resulting from the formulation of the required output voltage waveform using Fourier series to find the conduction angles for the modulation of the CHB semiconductor switches. Generally, the multilevel SHE problem is formulated using either the convenient quarter-wave symmetric (Fei et al., 2009) or half-wave symmetric (Fei et al., 2010) definition of the required stepped waveform for equal (Chiasson et al., 2003) and unequal dc voltage amplitude levels [(Tolbert et al., 2005); (Dahidah and Agelidis, 2009)].

The primary challenge for SHE modulation methods is the complexity arising from the formulation of non-linear transcendental equations for varying input conditions and required modulation indices. Several different approaches to finding optimal solutions to these equations have been suggested in the literature. These include the numerical iterative methods such as the Newton-Raphson, which typically requires reasonably close initial values for the swift convergence of the iteration towards the solution. Some methods include transformation of the non-linear SHE equations into differential equations (Guan et al., 2005) or into polynomials which are solved to find a wide range of solutions (Chiasson et al., 2005). However, these approaches get resource heavy with an increase in the number of levels. Other SHE formulations include optimisation based approaches such as genetic algorithms, particle swarm optimisation, and differential evolution (Dahidah et al., 2015). For real-time implementation, certain methods rely on interpolation to find approximate

solutions to the SHE equations using pre-calculated solution sets obtained using classic offline methods. Still others make use of curve fitting methods (Aleenejad et al., 2014) or use linear or nonlinear functions to achieve computation reduction (Liu et al., 2009).

However, an issue often encountered in the case of multilevel inverters is the discontinuous nature of the solution set and no solution for certain modulation indices which requires mitigation through alternative measures that increase complexity. Additionally, the switching angles are pre-calculated under the assumption of sinusoidal output voltage waveforms which is true only in steady state operation (Leon et al., 2017). For variable speed operation in a high dynamic performance system such as an EV traction motor, lower order harmonics are not fully cancelled, which results in poor performance during transients. There is also the risk of amplification of such harmonics due to the feedback controller [(Rodriguez et al., 2007); (Kouro et al., 2010)].

For a higher number of output levels, nearest level modulation (NLM) is a suitable modulation technique especially for applications requiring high dynamic performance with easy implementation. The functional equivalence between NLM with suitable common-mode voltage injection and that of space vector modulation has been shown by (Deng and Harley, 2015). However, the NLM method does not eliminate specific lower order harmonics like SHE and is also not particularly suitable for converters with a reduced number of output voltage levels as the approximation error becomes large with decrease in the number of output voltage levels, leading to higher THD of the waveform. Additionally, compared to PS-PWM, NLM does not lead to equal power distribution among the semiconductor switches of different CHB modules (Li et al., 2016) and consequently could lead to decreased converter reliability unless a reference rotation scheme is employed.

2.4.4 Loss comparison between modulation methods

Modification of the classical PWM techniques for addressing issues such as the reduction of switching losses has also been studied. A sequential switching hybrid technique for switching loss reduction with good harmonic performance for cascaded H-bridge multilevel multiphase inverters was presented by (Govindaraju, 2011). The basic principle involves operating four switches of an H-bridge at two different (fundamental and high) frequencies and using a sequential switching pattern to achieve equal power distribution.

A simulation study of switching losses for IGBT based CHB-MLIs under most popular modulation methods was provided by (Kouro et al., 2008). The switching loss model was developed using experimental measurements and manufacturer datasheets for a single CHB module; IGBT turn-on and turn-off losses were considered in addition to diode turn-off losses, while diode turn-on losses were not considered due to their relative insignificance. A generalised algorithm was presented for the performance and efficiency evaluation of inverter switching losses under different modulating methods. The modulation methods considered included PS-PWM, IPD-PWM, SV-PWM, NLM, and the SHE for both symmetrical and asymmetrical 11-level CHB-MLI inverter topologies for an identical *RL* load power factor. In the case of symmetrical CHB-MLI, the switching losses for the high frequency methods (i.e., PS-PWM, IPD-PWM, and SV-PWM) were found to grow linearly with the modulation index, reaching 0.25% of the total energy at unity modulation index. Low frequency methods like the NLM and SHE were found to exhibit lower switching losses as expected, with losses reaching only 0.035% of the total input energy at unity modulation index. Low frequency modulation methods also exhibited better performance at the lower end of the modulation index range. The PS-PWM method was shown to achieve a balanced power distribution between the modules in contrast to the IPD-PWM and SV-PWM as anticipated.

Application of a three-phase CHB-MLI for EV applications was presented in (Kersten et al., 2020). A seven-level CHB was formed using multiple battery-converter units, each comprising of a single H-bridge and a battery. The paper compares the output current THD, inverter and battery efficiency for converter operating under IPD-PWM and FSHE, for a wide operating range. Modelling and simulation results show high current harmonics and THD, at low modulation indices (low speed) when using FSHE. Similarly, at low speed, inverter efficiency suffers under FSHE, whereas IPD-PWM is shown to attain better efficiency due to reduced conduction losses. In contrast, at higher speeds, FSHE is shown to be much more efficient due to reduced switching losses. It must be noted, however, that the difference between inverter efficiencies is minor due to comparatively higher conduction losses of MOSFETs as compared to the switching losses. As for the efficiency of the battery, higher switching frequency of IPD-PWM causes increased battery losses when compared to FSHE, which achieves better efficiency for the whole operating range. An optimum boundary between the two modulation schemes, with respect to THD and battery efficiency, is roughly defined. Consequently, it has been suggested to operate the inverter under a hybrid

operating scheme where IPD-PWM is used for low driving speeds (modulation index < 0.25) and FSHE is used for medium and high driving speeds (modulation index > 0.25). The modulation index for a multilevel CHB converter with k modules per leg has been defined as the ratio of the peak voltage to kV_{dc}, where V_{dc} is the dc-source voltage connected to each H-bridge module. The same definition of the modulation index will be used in Chapter 3.

2.4.5 Multilevel multiphase modulation methods

A multiphase power electronic converter can be formed by having the same number of converter legs as the number of phases of the multiphase machine's stator windings (Lu and Corzine, 2005). Distribution of current to a higher number of phases is achieved with the use of multiphase machines, whereas the distribution of the supply voltage to a larger number of switches is offered by MLIs. The merger of the two concepts effectuates a reduction in voltage and current harmonic distortion which brings forth benefits such as lower torque ripple and higher power quality while utilising lower rated semiconductor devices (Levi et al., 2013).

Two-level power electronic converters are typically used to provide excitation for multiphase machines. However, among MLIs, the three-level inverters for multiphase machines have been the focus of most research. For multiphase systems, carrier-based modulation is the primary method of choice as it is naturally and easily extendable from three to more phases. Indeed, it has been shown by (Halasz, 2008) that the standard PS-PWM method is the most suitable modulation method due to its ease of implementation and harmonics losses for phase numbers greater than seven. Similarly, PS-PWM and LS-PWM methods have also been successfully implemented on a five-phase open-end winding induction machine with sinusoidal MMF distribution supplied by dual two-level inverters (Bodo et al., 2013). Note that open-end winding is an alternative way to obtain multilevel operation.

An extension of the PWM with third-harmonic injection (for a three-phase VSI) is also possible for a multiphase converter with injection of appropriate zero-sequence harmonic to achieve higher modulation indices. A generalised case for a carrier-based sinusoidal PWM method with a continuous sinusoidal harmonic injection for a multiphase VSI was presented by (Iqbal et al., 2006) to accomplish extension of the linear modulation range by increasing the dc-bus voltage utilisation to that achievable with the SV-PWM. It is also shown that

higher modulation indices are achievable with the injection of other lower order harmonics but at the cost of worse output voltage THD.

Although plenty of work on the modulation techniques for various topologies - including the CHB - has been carried out for the multilevel single- and three-phase converters, a comprehensive comparison of modulation methods for multilevel multiphase inverters based on the CHB topology has not been conducted. However, other multilevel multiphase topologies have been given due consideration. For example, a five-phase induction motor supplied by a three-level NPC inverter was used to test and compare different phase-disposition and space vector modulation methods in terms of load voltage and current THD, common mode voltage, and complexity of implementation by (Dordevic et al., 2013). The output voltage quality was found to be almost identical for the tested modulation techniques with some differences in the side-band harmonic profile around multiples of the switching frequency. The mapping of the sideband voltage harmonics into different planes and their effect on the harmonic distortion of the current waveform is established. The IPD-PWM with double min-max injection was found to be the most suitable method for three-level multiphase NPC inverters for real world applications. Nevertheless, even the simplest sinusoidal carrier-based IPD-PWM was shown to produce the cleanest voltage spectrum with slightly higher level of current harmonics, comparable harmonic distortion of the common mode voltage, and minimal fifth harmonic component over the full modulation range. An interesting outcome of the study shows that appropriate voltage injection for the carrier-based PWM can lead to performance equivalent to that achievable with the SV-PWM at a significantly lower computational cost. A similar conclusion was reached by (López et al., 2020) where it was analytically shown that most commonly used SV-PWM techniques for the multilevel multiphase inverter have an equivalent carrier-based counterpart which can be achieved with the injection of suitable zero sequence components with the IPD-PWM.

2.4.6 Space vector PWM

SV-PWM technique is utilised for the generation of inverter switching signals due to its intrinsic suitability and ease of implementation in digital controllers. The PWM waveform is generated using inverter states where the average variation in each of the phases is sinusoidal. SV-PWM features improved harmonic performance and improved utilisation of the dc-bus voltage. However, for multilevel multiphase inverters, the total number of inverter

switching states is governed by the formula l^n where l is the number of inverter levels and n is the number of phases. The exponential increase in the number of switching states with a rise in the number of phases and output levels makes the process of choosing appropriate vectors and their application times rather daunting. Additionally, the presence of $\frac{n-1}{2}$ two-dimensional planes (assuming odd n) in multiphase systems contributes significantly to the complexity of modulation as different unwanted voltage and current harmonics are mapped into these planes [(Levi, 2008); (Duran et al., 2017)].

In SV-PWM, a certain number of vectors are selected depending on the ultimate objective. For instance, (Dujic et al., 2007) have made a selection of appropriate voltage vectors in order to achieve generation of a purely sinusoidal output voltage waveform in a symmetrically distributed nine-phase load with negligible lower order current harmonics using standard digital signal processor (DSP) PWM hardware. On the other hand, (Grandi et al., 2007) have focused on the reduction of the complexity associated with SV-PWM by selecting only 72 out of 512 voltage vectors, for a nine-phase two-level inverter, in order to attain maximization of the modulation index while minimizing harmonics in the other planes. Alternatively, to achieve a reduction in the number of switching actions, a reduced switching modulation technique was proposed by (Bastos et al., 2019) for drive operation close to the rated frequency.

The authors (Bastos et al., 2019) argue that although the injection of the third harmonic with SV-PWM in multiphase machines can be used for the improvement of torque density and increasing output voltage, it can also lead to lower utilisation of the dc-bus voltage and the saturation of the machine core. The methodology works in the case of machines with multiple three-phases, where third harmonic injection is utilised for maximizing the dc-bus voltage utilisation by keeping the neutral point of each of the individual three-phase windings disconnected, thereby leaving no path for the flow of the third harmonic currents. A drawback of the modulation methodology is that it can only be used at higher modulation indices. Operation at lower modulation indices requires the use of other techniques such as SV-PWM. There is also no possibility to control the voltage harmonics in other planes because only four switching vectors are used for each case.

It is clear that SV-PWM is complex for higher numbers of levels and phases and the simplification of SV-PWM has been attempted by several researchers. For example, a

general approach for the formation of a simplified and computationally efficient SV-PWM for multilevel three-phase inverters was proposed by (Deng et al., 2016). The authors have also provided a methodology for extending the proposed scheme to multilevel multiphase inverters but have only provided experimental verification for a three-phase system. Similarly, a paper by (Ahmed et al., 2016) provides simplified SV-PWM techniques for multilevel CHB inverters where the primary objective is the reduction of SV-PWM complexity by reducing the number of multilevel space vector diagrams into two-level hexagons and identification of appropriate reference voltage vectors. A paper on SV-PWM in CHB based multilevel multiphase drives for the reduction of common-mode voltage was presented by (Lopez et al., 2016).

Due to the complexity of implementation, and due to the fact that SV-PWM can be obtained by carrier-based PWM method with an adequate injection (e.g., min-max injection in two-level case), space vector modulation methods will not be considered for practical implementations in this thesis. However, the concept of space vectors is crucial and has to be well understood in order to properly understand the concept of VSD and existence of subspaces (planes).

2.5 Batteries – state-of-charge balancing

A battery is the primary source of stored energy in a pure electric vehicle, akin to the fuel tank for the traditional internal combustion engine. It is therefore a critical component of the electric powertrain and the prime driving range determinant of an EV. Slow development in battery technology had consequently been one of the crucial factors for the delayed adoption of the EVs.

Rechargeable batteries are typically used for electric automotive applications. The lead-acid battery technology was mostly prevalent in the last century. In more recent times, nickel metal hydride (NiMH) and lithium-ion (Li-ion) battery technologies have been used for energy storage systems. Li-ion battery cells are the most prevalent battery types today powering mobile phones, computer laptops, and newer electric vehicles (Sarlioglu et al., 2017). The popularity of the Li-ion battery can be attributed to a longer lifetime, increased power rating, and energy density compared to other battery technologies. The first mass-produced EV to use the Li-ion based battery cells was the Tesla roadster in 2008.

Multiple cells are usually arranged in a series-parallel configuration to form a battery pack. A series connection of batteries allows for the generation of higher voltages and higher power delivery, whereas a parallel connection of batteries allows for an increased current output and power. Also, parallel connection leads to better lifetime of individual cells as each cell delivers a lower current. Higher battery discharge rate results in an inefficient utilisation of the battery capacity. Therefore, arrangement of individual cells in a series-parallel configuration leads to better battery lifespan, higher voltage levels, increased current, power and energy.

The series connected cells in a large battery pack pose certain challenges. None of the cells present in a battery are identical due to certain factors such as manufacturing tolerances and general age-related degradation. This results in inefficiencies during charging or discharging cycles. A cell with the highest charge-up voltage stops the charging process, and similarly, a cell with the lowest discharge-voltage level stops the discharge process. Thus, capacities of the remaining cells are not fully utilised. Consequently, a battery management system (BMS) is used for the passive balancing of the cells which is an inefficient solution. Breaking up the battery into smaller units improves battery utilisation because all the different battery units are controlled individually during the charge and discharge process.

The issue of charge and voltage balance between different battery cells is critical and must be resolved through the incorporation of a charge balancing scheme. Individual cell balancing is achieved either through cell terminal voltage or through cell SoC. Various charge balancing schemes have been proposed in the literature for series connected battery cells [(Cao et al., 2008); (Daowd et al., 2011); (Einhorn et al., 2011); (Lee et al., 2017); (Zhang et al., 2017); (Huang and Qahouq, 2015)].

As this thesis considers application of the batteries in EVs (with a CHB multiphase drive), detailed review and understanding of battery related terms such as, battery voltage balancing, SoC, etc. is necessary. Hence, relevant references are reviewed in the following subsections.

2.5.1 State-of-charge estimation

The SoC of a battery can be described as the amount (in percentage) of usable energy remaining in a battery. Knowledge of the SoC of a battery is required for communicating the

battery status to the end-user and is essential in the management of the battery to ensure optimum battery life. The impedance of a Li-ion battery stays approximately constant for most of the SoC range and can be reasonably used for SoC estimation. However, battery impedance rises rapidly when the battery SoC falls below a certain threshold value. Therefore, other variables, in addition to battery impedance, such as battery terminal voltage and load current were used by (Coleman et al., 2007) to better approximate the value of the battery electro-motive force (EMF), and therefore, the battery SoC.

The Ampere hour counting (Coulomb counting) methods is known to be the most common method for SoC determination due to its ease of implementation, online computational capacity, and reasonable cost. But the method is known to be sensitive to current measurement errors, high current variation, parasitic reactions, increased battery temperature, and requires regular calibration [(Piller et al., 2001); (Coleman et al., 2007)]. A paper by (Cheng et al., 2011) presents a technique for improving on a disadvantage of measurement error accumulation of the Coulomb counting method by using a Kalman filter approach, using open circuit voltage prediction to estimate battery SoC.

2.5.2 Battery SoC balancing in energy storage applications

The cascaded connection of multiple battery-converter integrated units to power the traction machine in an EV is the primary objective of this project. A closely related application using the cascaded modular multilevel converters with integrated batteries is the battery energy storage system (BESS). As a result of increased integration of renewable energy sources into the grid, sudden inevitable power disruption requires another power generation system to take over. This is usually handled by conventional back-up generators, which take a few minutes to start-up. Consequently, a battery energy storage system built using large battery banks, reduces the downtime and provides power until the back-up generators kick in. BESS systems based on modular multilevel converters have been proposed (Qian and Crow, 2002). Battery SoC balancing is an important issue for BESS applications and several papers have addressed it [(Maharjan et al., 2009); (Maharjan et al., 2010); (Chen et al., 2014); (Vasiladiotis and Rufer, 2013)].

An interesting paper by (Baruschka and Mertens, 2011) compares the performance of CHB multilevel converter, the MMC, and their variants, for BESS application. A need for the presence of a frequency filter for the CHB was highlighted to reduce battery current

harmonics. For the CHB converter, a dc-dc conversion stage connecting the batteries to the dc links was recommended in order to reduce the flow of a second current harmonic through the batteries which is harmful for battery performance. In addition to achieving a power-decoupling, this stage achieves a voltage decoupling between the battery and the dc-link. The CHB based converter was found to be much more suitable than MMC and its variants for BESS application in terms of efficiency, ease of control, lower energy variance between modules, and better opportunities for SoC and voltage balancing on the batteries. Importantly, the CHB converter was found to be better suited for applications with a low voltage variation between battery-converter modules. In addition, for applications requiring more real power than reactive power, a standard CHB converter system was found to be more efficient than a CHB converter with an additional dc-dc converter.

A control methodology for the SoC balancing of an energy storage system consisting of nine NiMH batteries using a PS-PWM controlled symmetrical cascaded H-bridge converter was proposed by (Maharjan et al., 2009). It focuses on the application of storing energy from a three-phase grid. The SoC balancing control was achieved by balancing the three clusters of converter cells in each phase by zero-sequence voltage injection in order to enable a control which has no effect on the line currents and the total power of the system. Additionally, the control algorithm individually controls the SoC across each cell of the cluster separately to complete the SoC balancing control. The scheme does not include voltage balancing control, which may be required in the practical implementation of the system. The control system was shown to balance the SoC values of the nine batteries in around 15 minutes to less than 2% average difference. However, it must be noted that the experiment was conducted on a mean battery SoC of between 25-75% while in practical application, this is likely to be in the region of 10-90%.

The relationship between the battery terminal voltages and SoC is exploited by (Young et al., 2013) to achieve balanced state of discharge with a single-phase multilevel CHB inverter with battery integrated modules. The battery voltages are measured and sorted as per their terminal voltages. Although the proposed battery voltage sorting technique was tested on a prototype built using lead-acid batteries, battery terminal voltage is a reasonably good indicator of battery SoC for Li-ion batteries (Coleman et al., 2007), and may be considered for EV application. However, accurate measurement of battery terminal voltage

is essential as it does not vary significantly with the battery SoC and small measurement errors could potentially result in the system unable to achieve proper balancing.

Another approach to achieve charge balancing in battery cells, in a BESS application, is adopted by (Chatzinikolaou and Rogers, 2016). Instead of connecting multilevel converters to small battery packs to form a cascaded structure, the authors have connected the multilevel converters to individual battery cells to achieve SoC balancing, individual cell monitoring and control. However, such a technique would be unsuitable for the battery-integrated power electronic converter proposed in this thesis. A disproportionally high number of H-bridges would be required to achieve the power level for a multiphase traction machine. As a result, such a system would be cost prohibitive and voluminous.

2.5.3 Battery SoC balancing in EV applications

A switching pattern swapping technique is used by (Tolbert et al., 1999) to address the battery SoC balancing issue in CHB inverters operating under FSHE. The FSHE modulation scheme requires certain dc voltage sources to contribute more than the others for certain periods of time causing unbalanced battery utilisation. Therefore, a cyclical swapping algorithm is used to equalise the total conduction times of the inverter devices as well as the energy contribution by the batteries. For low modulation indices, [(Tolbert et al., 2000); (Tolbert et al., 2002)] proposed making use of regular carrier-based PWM but with sequential rotation of the pulses or the reference waveforms to make sure all H-bridges contribute equally to generation of the phase voltage with a lower number of voltage levels.

A SoC balancing control scheme, based on the principle defined by (Maharjan et al., 2009) for BESS application, is presented by (Wang et al., 2015) for an 11-level three-phase CHB inverter with integrated batteries in a symmetrical configuration (equal dc sources) using unipolar PS-PWM for an EV application. The authors have verified the validity of the proposed methodology under different operating conditions. During grid connected charging, battery SoC balancing is defined for phase and module levels and the cell-level SoC balancing control is left to the BMS. The phase-level SoC balancing is carried out using zero sequence voltage injection for the three phases (Maharjan et al., 2009) as it does not result in any real power transfer between the load and the battery system. Similarly, module-level SoC balancing is carried out using the deviation in SoC between each battery module and that of the phase value. In standby mode, the SoC balancing is carried out through the

switching of certain devices to allow for the power flow to occur between cells with the highest and the lowest SoCs through the machine windings. This could potentially damage the motor in case of a high current flow. Similarly, (Mathe et al., 2016) have proposed a SoC balancing scheme for a CHB with battery-converter modules with the NLM instead of PS-PWM with a reduction in the number of switching actions as well as a faster time to achieve battery SoC balance.

In (Altaf and Egardt, 2017), the authors have shown the viability of modular battery system with cascaded converters for SoC balancing due to the possibility of bidirectional flow of energy into and out of each module. The cascaded H-bridge based modular battery converter under bipolar PWM was shown to be more suitable for SoC balancing as compared to the half-bridge battery-converter module under unipolar PWM. The reason for this is that the half-bridge inverter does not allow the reversal of battery module polarity, whereas the full-bridge converter using two unipolar PWM signals achieves polarity reversal of the module allowing simultaneous charge and discharge of different battery units. However, the battery efficiency was shown to slightly suffer as a result of increased battery temperature resulting from negative actuation of the cells under bipolar modulation of the full-bridge cells. Additionally, the full-bridge inverter was shown to suffer from slightly reduced efficiency (0.42%) due to the presence of two extra switches per module, whereas the half-bridge based inverter under unipolar PWM exhibited relatively poor SoC balancing capability during high-speed motorway driving. Regardless, the performance of the full-bridge converter in terms of SoC balancing capability was superior to the half-bridge converter.

2.5.4 Other battery considerations

A paper by (Kersten et al., 2019b) discusses the addition of filter capacitors in parallel with the batteries of a CHB-MLI in order to mitigate battery losses. A large parallel capacitor is connected to reduce the rms current drawn from the batteries and to stabilise the dc-link and help reduce battery losses. The use of higher capacitance is beneficial for reducing the high current drawn from the battery. Additionally, the presence of extra capacitors helps with the reduction of low frequency EMI emission from dc-link rails. Without a paralleled filter capacitor, the frequency spectrum of the current drawn from the battery shows a second harmonic larger than the dc component. The lower order harmonics are filtered out by the parallel filter capacitor. The capacitor reduces the lower order battery current and voltage

harmonics between 5% and 80%. A drive cycle analysis confirmed significant battery loss reduction when capacitors are placed at the H-bridge input terminals. Addition of capacitors helps with the reduction of EMI filter size as well as significant reduction of battery losses at low operating temperatures due to increased battery impedance.

Battery longevity can suffer as a result of the presence of lower order current harmonics flowing through the battery. A method using zero-sequence voltage injection for balancing a grid connected BESS was presented by (Vasiladiotis and Rufer, 2013). The system is based on battery-integrated cascaded H-bridge converter modules, with a non-isolated dc-dc conversion stage (using half-bridge modules) in between the H-bridge converter and the battery to stop the flow of high second harmonic currents into the battery. A similar dc-dc conversion stage was proposed by (Baruschka and Mertens, 2011) for the same purpose. Likewise, (Wang et al., 2019) propose the injection of a second harmonic current component into the circulating current in order to cancel the harmful effects of the lower order current harmonics flowing through the battery to increase battery cell life. Although the methodology has been proposed for MMC based MLI for EV application, a similar approach has yet to be applied to a CHB-MLI as used in this work.

An accurate battery model is an essential requirement in the modelling and analysis of electric vehicle simulations. One such model has been developed by (Cao et al., 2016) for the dynamic drivetrain simulation of EVs over standard driving cycles for fast and accurate prediction of battery SoC and current-voltage characteristics. The developed battery model is built upon the Randles' equivalent circuit consisting of multiple series connected parallel RC elements to model battery cell dynamics at different time frames. In addition to the battery model, the paper also presents a methodology for parameter extraction from a Li-ion battery cell. On the other hand, (Theliander et al., 2020) also discuss modelling and parameter extraction of battery packs using dynamic battery models, time-domain parameter extraction, and electrochemical impedance spectroscopy. A simple resistive model of the battery is shown to overestimate the battery losses by up to 20%. Therefore, for an accurate and complete evaluation of energy losses for different driving conditions, a more complex battery model is preferred. However, the use of a simple battery model is generally justifiable unless very accurate loss data is required.

2.6 Current EV drivetrain solutions

A large single battery pack with a 400 V output voltage is the most common solution employed while some high performance EVs use 800 V batteries (Poorfakhraei et al., 2021a). A battery pack with such voltages requires a battery management system (BMS) to protect from cell overcharging and stopping discharge below a certain threshold. At the same time, the BMS also functions to keep a balanced SoC on all the cells in the battery pack.

The most prevalent dc-ac power electronic converter typically makes use of a two-level structure with IGBT modules for switching. This is also the case for inverters used in EVs presently on the market (Poorfakhraei et al., 2021a). Instead of using a single semiconductor device, multiple paralleled switches, such as IGBTs or MOSFETs are used, to distribute the high current to multiple paths with lower current.

Presently, the most commonly used machine for traction application is either the three-phase PMSM or the three-phase IM. For EVs, the PMSM is the more popular choice due to its higher power density and efficiency compared to the IM, although the IM is cheaper, more reliable, and much more rugged as it is not susceptible to reduced efficiency at higher temperatures. Recently, switched reluctance machines (SRM) have been proposed for propulsion applications due to their sturdiness, low cost, and better performance at high speeds and operating temperatures (Bilgin et al., 2015). Special machines such as the three-phase permanent-magnet synchronous reluctance motor is being used on the Tesla Model 3 with a SiC MOSFET based two-level inverter (Tesla, 2019).

This section provides an overview of the latest EV drivetrain solutions in the recent literature, sub-sectioned in terms of inverter topology. It should be noted that a multilevel multiphase solution for EV application is not found in the literature. However, general review papers for potential application of multiphase drives for EVs do exist. For instance, (Bojoi et al., 2016) have proposed modular (multiple three-phase) multiphase machines for transport electrification. Various multiphase topologies are reviewed and a generic modelling approach including the VSD and multiple d–q for modular multiphase machines is provided along with the potential control strategies. Similarly, (Salem and Narimani, 2019) have mostly focused on providing a review of multiphase drives for automotive applications. The characteristic features of multiphase drives are provided with special

emphasis on the six-phase machine including its modelling, supply, control, and modulation methods, as it is the most researched type of multiphase machine.

2.6.1 Half-bridge two-level inverter with a multiphase machine

As mentioned previously, the three-phase half-bridge two-level converter using IGBT modules is the industry standard inverter for EV applications. However, a 48 V drive topology, using low voltage MOSFETs in a half-bridge inverter, and a low voltage (48 V) battery for traction applications using an ISCAD (intelligent stator cage drive) which uses a sixty-phase machine was proposed by (Baumgardt et al., 2016). The stator is constructed using multiple aluminium bars, instead of wound copper wires, that are short-circuited using a ring at one end. The topology patented by Molabo GmbH uses half-bridge MOSFET switches to feed each stator phase of the multiphase machine. Doing so allows for precise control of the resulting air gap MMF and for the option to control the number of pole pairs for maximal efficiency as per load demand. Better efficiency for a wide range of operating conditions is accomplished by increasing the number of pole pairs in low-speed high-torque region and by reducing the number of pole pairs for high-speed low-torque operation.

The authors (Baumgardt et al., 2016) note that compared to IGBTs, which exhibit diode like loss behaviour independent of the load current, MOSFET losses rise with increasing load current ($I^2R_{DS(on)}$). Since the voltage level is low, low voltage MOSFETs can replace high voltage IGBTs to reap benefit of lower losses at partial loads. Additionally, the presence of a parasitic (internal) body diode in MOSFETs allows for reverse conduction of current, eliminating the requirement for a freewheeling diode and its associated losses. Moreover, being unipolar, MOSFET based switches can be operated at higher frequencies, leading to reduced passive filters requirements as compared to IGBTs. In terms of cost, a low voltage MOSFET based system costs substantially less compared to high voltage IGBT based one. The integration of power electronics and the electrical machine would help mitigate cable/wire conduction losses between them.

The authors (Baumgardt et al., 2016) call for a redesign of the battery system for extra low voltage traction applications. They argue that a 48 V battery requires packaging of a higher number of battery cells in a parallel configuration as compared to contemporary designs. Battery lifetime is shown to be slightly increased as a result of statistically lower capacity deviation when battery cells are connected in parallel. The presence of a cell with

significantly reduced capacity affects the overall battery pack capacity of a highly series cell packaging much more than it does in a highly parallel packaging of battery cells. It is reasoned that paralleled cells inherently self-balance due to the presence of small balancing currents. Lower balancing losses are expected as balancing currents in parallel cell configuration are insignificant in comparison with balancing currents occurring in series connected cells. Thus, minimal balancing effort would be required when a higher percentage of cells are connected in parallel. Parallel and serial configuration of battery cells do not affect the current magnitude at the cell level. However, a higher overall battery current is present due to a lower battery voltage (48 V) to satisfy energy conservation.

2.6.2 Cascaded H-bridge (CHB) multilevel inverter with three-phase machine

The viability of an integrated battery-converter based on the CHB topology for EV application was recognised by (Josefsson et al., 2012). A three-phase PMSM was controlled with maximum torque per ampere (MTPA) to obtain a machine operating profile for different speed and torque conditions. The rms current and phase voltages at these operating points provide a means to calculate battery and inverter losses for a standard driving cycle. A 7-level CHB inverter (using low voltage MOSFETS) was modulated using FSHE to minimise lower order harmonics and switching losses, whereas the two-level IGBT inverter was operated under PWM (10 kHz) with third harmonic injection. The performance of a CHB inverter with integrated batteries was compared with a standard two-level IGBT based inverter under different standard driving cycles. Efficiencies of batteries and the two inverters under investigation were obtained by calculating energy losses. The performance of the MLI (with capacitors), in terms of accumulated energy loss, was shown to be around 2-4% better than the two-level inverter. Without the filter capacitors, the performance was still better for 3 out of the 4 driving cycles by around 1-3%. The necessity for the presence of sufficiently large filter capacitors on the dc side of the H-bridges was highlighted by a slightly reduced efficiency (by 0.7%) at higher speeds and torques when capacitors were not used. This is because the battery must provide reactive power to the traction machine in the absence of these capacitors.

The efficiency of a conventional IGBT (three-phase) inverter is particularly high (over 97%) at nominal or peak loads. However, for a real-world drive cycle, especially in city driving conditions, a significant proportion of the driving takes place at low speeds, which equates to low partial loads. An efficiency analysis of a standard six-pack (three-phase)

IGBT two-level inverter was conducted by modelling the conduction, switching, and thermal losses by (Chang et al., 2017). The model was validated using simulation and compared with experimental results. The efficiency of the inverters was shown to suffer considerably at low partial loads (~80%) with the overall inverter efficiency around 85-90% in realistic driving conditions, i.e., stop-start traffic and low speed cruising. Efficiency around 96% was obtained for driving cycles with more emphasis on highway driving during which the motor is operating at full load. This leads to the conclusion that low inverter efficiency during partial load operation (urban driving) is primarily responsible for lower overall inverter efficiency. It is understood that for low torque (current), IGBTs encounter switching losses arising from turn-off losses like tail currents and switching transients, whereas, in low speed (voltage), considerable conduction losses from the ON state voltage drop across the IGBT account for a 3-5% loss of efficiency.

As the bipolar IGBT switches were shown to be inefficient at partial load operation, unipolar switches like MOSFETs in a multilevel topology were suggested for the design of automotive inverters by (Chang et al., 2017). To ascertain the feasibility of the proposal, energy consumption and efficiency were determined for different topologies and switching device combinations under different driving cycles. A standard three-phase IGBT inverter was compared to a low voltage cascaded Si-based H-bridge multilevel inverter, a silicon carbide (SiC) MOSFET inverter, super junction (SJ) MOSFET inverter, and hybrid inverter designs using a combination of high voltage MOSFETS and IGBTs. The low voltage Si MOSFET based CHB-MLI achieved the highest energy savings under different driving cycles. Low voltage MOSFETS were shown to exhibit a higher partial load efficiency due to lower conduction and switching losses. As expected, the largest benefit was seen in city driving cycles as compared to comprehensive driving cycles. Similarly, in terms of potential cost reduction, CHB-MLI topology proved to be most promising. Further cost reduction possibilities for the CHB-MLI topology include sourcing cheaper MOSFET specific driving circuitry and cost-effective communication system. Therefore, the adoption of low voltage MOSFET based multilevel inverter to replace the traditional two-level IGBT inverter for EV application was suggested by (Chang et al., 2017).

A subsequent paper by (Chang et al., 2019) also provided a similar comparison between a Si MOSFET based CHB-MLI to a six-pack (three-phase) Si IGBT based conventional inverter and a six-pack (three-phase) SiC MOSFET based inverter under

different driving load scenarios. A PS-PWM strategy is chosen to control the CHB-MLI. The conduction and switching losses of the CHB-MLI are assessed and loss models for the IGBT and SiC MOSFET based inverters are presented. Thermal models of the inverters are also taken into consideration for improved accuracy of the analysis. Efficiency maps for speed-torque variations are generated for comparison. Again, the conventional IGBT inverter is shown to exhibit a high efficiency in high-speed (full load) operation. However, under partial loads (low speeds), the efficiency deteriorates as expected. In comparison, the CHB-MLI and the SiC MOSFET inverter achieve higher efficiency under both full and partial load conditions which is an improvement of 2%-3% in full-load and 3%-10% in partial load conditions. This improvement in efficiency can be attributed to the intrinsically lower switching and conduction losses of the MOSFETs at partial loads. Efficiencies for both the CHB-MLI and the SiC MOSFET inverter are quite similar but the associated losses of each are distributed differently. A cost analysis and comparison of the three inverters confirms the SiC based inverter to be the costliest. In comparison, the CHB-MLI solution is found to have the lowest total cost because of its higher efficiency and thus lower battery capacity requirement.

The paper (Chang et al., 2019) also discusses important performance factors for the integration of such inverter solutions in EV technology from an engineering point of view such as: the weight, volume, reliability, electromagnetic interference (EMI) and complexity of control. The CHB-MLI is assessed to have an advantage in terms of lower EMI but a slight disadvantage in terms of the other factors. In terms of design, the CHB-MLI is not conducive to the use of multiple motors, as is the case with certain high-performance EVs on the market such as the Tesla Model S. Secondly, the battery current is highly sinusoidal in nature and its effect on battery performance and longevity requires further investigation for a CHB-MLI inverter. On the other hand, a CHB-MLI topology is favourable for easier expandability due to its inherent modular structure. It can be deduced that a multiphase multilevel inverter based on a CHB topology using MOSFETs would achieve even higher efficiency due to the lower current per phase of the inverter.

2.6.3 Modular multilevel converter (MMC) with three-phase machine

In addition to the CHB-MLI, the other popular topology under research for EV application is the modular multilevel converter (MMC) with embedded battery cells. A half-bridge converter is integrated with a battery to form a submodule. Several such submodules

are cascaded to form the upper and lower arms of a phase leg. Since there is a voltage difference between phase legs, buffer inductors are placed between the top and bottom converter arms to limit the resulting circulating currents. One such topology based on the MMC was presented by (Quraan et al., 2016). The converter structure consists of series connected submodules for each phase of the converter. A high-quality multilevel output voltage waveform is produced with low current THD. The disadvantages associated with passive and active BMS are circumvented by applying different control strategies to actively balance individual cells, eliminating the need for a BMS altogether.

Motoring and recharge operations are enabled using interlocked contactors (switches). Low voltage MOSFETs are used as switches in order to reduce the conduction and switching losses. The motor control is achieved using rotor flux-oriented vector control. The efficiency of the inverter is shown to increase with the increase in the number of converter levels and the THD at 5-level operation is 17.7%. A disadvantage is the use of two un-coupled buffer inductors (or a single coupled inductor) for each phase of the converter which are responsible for reducing the amount of current circulating between converter legs. Circulating currents are controlled to achieve SoC balancing between battery cells. This is realised by implementing separate arm balancing, phase cluster balancing, and individual cell balancing control loops. For an initial maximum SoC disparity of 15% between individual battery cells, simulation results show complete cell balancing in 160 s.

A similar paper on the integration of MMC using low voltage MOSFETs and battery cells for EV traction application by (Quraan et al., 2017) provides an evaluation of the converter power losses under different range of operations. The converter is modulated using a carrier disposition sinusoidal PWM with third harmonic injection (THI). This modulation method reduces the number of required submodules, which leads to the reduction of the converter size, cost, and losses. The traction motor is vector controlled. The circulating currents are controlled to realise energy balance between upper and lower arms of each phase as well as achieving energy balance across the phases. Battery module balancing control is achieved by recharging and discharging modules based on current polarity. Battery modules with low SoCs are recharged when the arm currents are positive and cells with high SoCs are discharged when arm currents are negative. SoCs are estimated using the Coulomb-counting method to determine priority.

A linear approximation of MOSFET voltage and current switching transient is used to determine switching losses. The efficiency of the MMC inverter is compared to a two-level IGBT inverter for EV operation under different driving cycles. The MMC inverter achieved better efficiency when operated at a higher switching frequency. Simulation results also show increased MMC inverter efficiency (3-5%) under partial load (i.e., half of rated current) whereas the IGBT inverter achieved better efficiency at full load (i.e., nominal current). This shows that MMC inverter experiences decreased efficiency with increasing load current due to higher conduction losses at higher currents. Conversely, MMC inverter exhibits lower switching losses compared to the IGBT inverter as MOSFETs have faster switching transients. The MMC inverter achieves low THD (with 4 submodules per arm) while not requiring a separate cell balancing inverter.

Although like the CHB, the MMC is modular in nature, it does have some disadvantages compared to the CHB. For instance, a pair of buffering inductors per inverter leg is a necessity. A reliability analysis of the CHB and MMC based drive systems was presented by (Farzamkia et al., 2020) where the two converters (both three-phase) were compared under the same operating conditions, phase voltage, number of output voltage levels, and with similar components. The superior reliability of the CHB based three-phase drive was confirmed under all operating conditions and similar redundancies. Without built-in redundancies, the CHB based converter was shown to have a lifetime expectancy of more than double than that of an MMC based converter. Furthermore, the efficiency of a CHB-MLI was found to be higher than that of a MMC and 5-level active NPC by (Marzoughi et al., 2018) for motor drive applications where IGBTs of different ratings were used as switching devices. It was found that the use of smaller rated semiconductor devices resulted in smaller conduction and switching losses. Similarly, a conduction and switching loss comparison between a three-phase CHB-MLI and MMC using IGBTs under PS-PWM showed higher efficiency of the CHB-MLI (Shen et al., 2018).

2.6.4 Modular multilevel series-parallel (MMSP) inverter with three-phase machine

A modular multilevel series-parallel (MMSP) inverter consists of an additional half-bridge in parallel with the H-bridge for each phase leg. A paper by (Korte et al., 2017) presents an efficiency evaluation of promising battery integrated multilevel converter

topologies for EVs. The classic CHB topology and the MMSP converter topology are compared with the classic two-level IGBT inverter in terms of drive cycle efficiency under New European Driving Cycle (NEDC) and Worldwide Harmonised Light Vehicle Test Procedure (WLTP) drive cycles. For both the multilevel topologies, a capacitor in parallel with the battery is utilised for filtration of high frequency currents. The topologies also make use of low voltage MOSFETs compared to the IGBTs used by the standard two-level inverter. A standard vector controlled PMSM based automotive vehicle was simulated. MTPA method was used for the generation of inverter currents.

The switching frequency of individual cells of the MLIs is reduced to 1/14th of the switching frequency of a two-level inverter in order to keep the same overall switching frequency. Both multilevel inverters are operated under IPD-PWM with 14 carriers. The switching and conduction losses are calculated based on parameters obtained from the device datasheets. It was observed that the multilevel converter systems have a profoundly different loss profile compared to the two-level inverter. The multilevel converters exhibit better efficiencies at partial load operation whereas the two-level inverter achieves high efficiencies at full load (high torque – high speed) operation. The two-level inverter suffers from significantly higher switching and conduction losses at partial loads when compared to the multilevel topologies. At higher loads, the multilevel inverters suffer from higher battery losses due to higher currents drawn from the battery.

Compared to the CHB, MMSP converter is shown to achieve higher efficiency in the low speed-high torque region. The overall inverter efficiency for the CHB is found to be 7%-8% lower than MMSP. However, MMSP topology has significantly increased gate driver requirements in addition to the increased complexity of the control system. The two-level inverter achieved a better performance under WLTP (high load cycle) compared to the CHB. As expected, the doubling of the switching frequency did not significantly affect multilevel inverter efficiencies in contrast with the two-level inverter. Consequently, higher quality voltage can be synthesised by increasing the switching frequency of the MLI for the improvement in motor efficiency and control at higher speeds. Battery SoC balancing was not considered in the comparison by the authors.

A similar study for the performance evaluation of different inverters in terms of battery and inverter losses under various standard EV driving cycles was presented by (Kersten et al., 2019a). The inverters compared included the standard two-level IGBT inverter, a two-

level MOSFET inverter, a three cell (seven-level) CHB (MOSFETs), and a three cell (seven-level) MOSFET-based MMSP. The battery is modelled using a three-time-constants model (Cao et al., 2016) suitable for dynamic EV simulation. The switching and conduction losses are modelled using a look-up table. An interior permanent magnet synchronous machine is considered for simulation of the system. All inverters are operated under space vector modulation at 10 kHz. Instead of simulating the system for the complete duration of the driving cycle, which would be too resource intensive if all switching events were to be accounted, the authors have determined an inverter and battery loss map by simulating the system for the entire operating range. Thereafter, a look-up table based on these loss maps is used to determine the battery and inverter losses for the entire drivetrain operating range.

Overall battery losses are found to be roughly three times that of the inverter losses. CHB and MMSP based inverters exhibit reduced battery efficiency below rated speed due to intermittent phase currents conducted through the batteries at these speeds. The two-level inverter is shown to be most efficient at all operating points in terms of battery losses. Whereas, in terms of inverter efficiency, the multilevel CHB and MMSP inverters show increased efficiency at low speed and partial loads. Additionally, CHB and MMSP multilevel inverters also achieve higher peak efficiencies compared to their two-level counterparts. A breakdown of the losses shows a slightly higher conduction loss for the CHB inverter (36.4 Wh) when compared to the MMSP inverter (25 Wh). Whereas, the CHB inverter had the lowest switching losses (5.3 Wh) compared to MMSP inverter with 11.9 Wh. In contrast to the study by (Korte et al., 2017), the overall inverter efficiency was comparable between the two multilevel inverters with CHB at 98.52% and MMSP at 98.68%.

Under WLTP drive cycle, which is the global standard for emission and fuel consumption evaluation, MMSP inverter achieved a slightly higher overall efficiency (battery & inverter) of 95.03% as compared to 94.22% for the CHB. Interestingly, the two-level IGBT inverter also achieved a 94.24% overall efficiency. This is attributable to the increased battery losses incurred by the CHB inverter. The two-level IGBT is found to have outperformed the CHB-MLI under FTP-75 (Federal Test Procedure) city driving test, which is again attributed to higher battery losses incurred by the CHB topology. Regardless, the result of this study cannot be conclusively projected to that of a multilevel multiphase CHB

inverter. Furthermore, the extension of a MMSP inverter to multiple phases would make the system significantly more complicated to control, especially for higher voltage levels.

2.7 Summary

This chapter gave a comprehensive literature review of all important topics related to this project and application of multiphase CHB topology in EV drivetrain. Therefore, the literature survey begins with a review of prominent multilevel topologies and their characteristics. A review of other multilevel hybrid topologies is also given. A classification of the prominent voltage source converter topologies for EV drivetrains in presented in Figure 2.1. The classic multilevel topologies are presented along with a special emphasis on the cascaded H-bridge topology (highlighted in Figure 2.1).

The next section focused on the modelling and features of multiphase machines, their control strategies such as FOC, DTC, PTC, MPC, and their respective attributes. The third section provided a treatise on the literature on various modulation methods including the PS and LS methods, discontinuous methods, SHE, and the SV-PWM. A discussion on the modulation methods for the equal power distribution between different modules of a

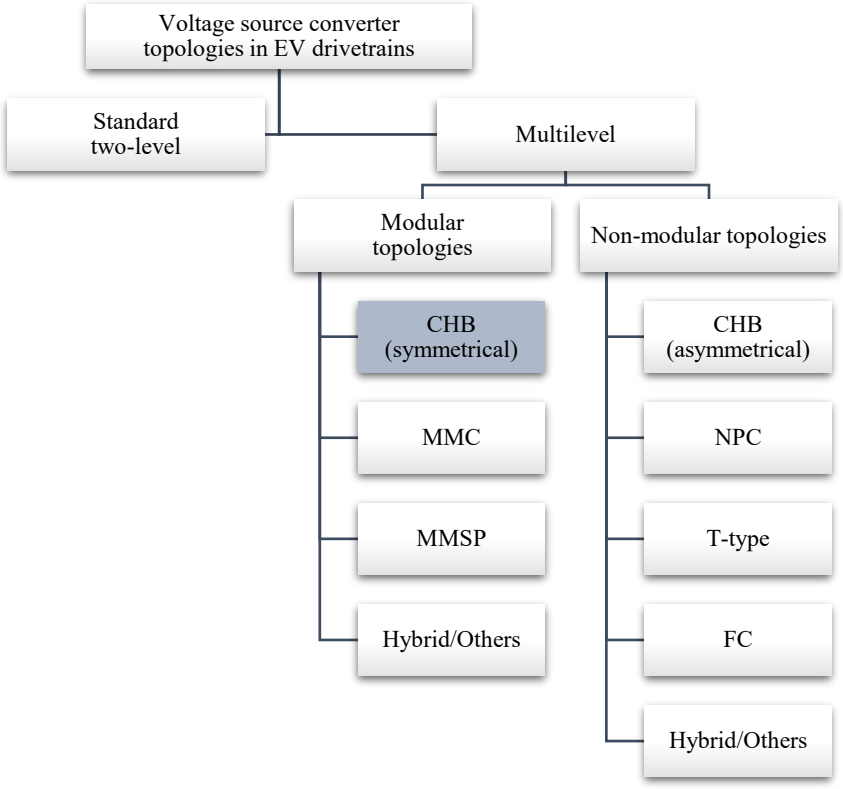


Figure 2.1: Classification of voltage source converter topologies in EV drivetrains.

cascaded multilevel inverter is also presented. The fourth section concentrated on battery technology and pertinent issues such as battery voltage, battery SoC estimation and balancing methods. Finally, contemporary solutions for EV drivetrain topology using cascaded and modular multilevel inverters such as half-bridge, CHB, MMC, MMSP are studied to assess current research on issues relevant to this project such as inverter efficiency and battery SoC balancing solutions under different driving conditions.

To conclude, a comparison between the features of the standard three-phase two-level converter and the CHB converter is presented in Table 2.1. Most literature on EV drives using the CHB converter is related to three-phase technology. Finally, prominent literature pertinent to the thesis has been summarised in Table 2.2 including the context and the topics addressed in this thesis highlighted with an asterisk (*). The list of publications from the thesis is given in Appendix D.1.

Table 2.1: Comparison between features of the standard two-level converter and the multilevel CHB converter.

	Standard two-level converter	**Multilevel CHB converter**
Structure	Simple structure	Medium complexity
Modularity	N/A	Highly modular
Control complexity	Low	Medium [1]
Switching device count	Low ($2n$, n: phases)	Medium (as compared to other multilevel topologies) ($4kn$, n: phases, k: CHB modules)
Switching device power rating	High	Low
Switching frequency	High	Low
Loss distribution (switch dependent)	Mostly switching losses if IGBTs used	• Mostly conduction losses if LV MOSFET used • Low switching losses [2]
Thermal performance	Concentrated (larger heat sink needed)	Better heat distribution [3]
Package size	Standard. Larger volume with dc-dc converter stage	Larger converter volume [4], [5]
Package mass	Standard	Higher [5]
Total harmonic distortion	High THD	Low THD
EMI	High EMI	Lower EMI
$\mathrm{d}v/\mathrm{d}t$	High $\mathrm{d}v/\mathrm{d}t$	Low $\mathrm{d}v/\mathrm{d}t$
Common mode voltage	Higher common mode voltage	Lower common mode voltage
Output filter requirement	Larger filtering requirements (large size, weight and cost)	Minimal / smaller filter requirement

	Standard two-level converter	**Multilevel CHB converter**
Battery pack design / BMS	Single large battery pack - Larger BMS necessary for SoC balance	Batteries distributed - Smaller BMS suffices (local BMS for battery pack) [6]
Safety	Low safety due to high battery pack voltages	Better safety due to lower isolated (distributed) battery voltages
DC-DC stage	Extra dc-dc stage preferred for higher motor voltage	Extra dc-dc stage not needed (but preferred [7])
DC-link capacitor size	Very large dc-link capacitance	Relatively smaller sized dc-link capacitors needed [8]
Efficiency (machine)	Higher motor losses due to higher $\mathrm{d}v/\mathrm{d}t$ especially at partial load operation	Better motor efficiency due to lower core losses (sinusoidal voltage) especially at partial load operation
Efficiency (converter)	High losses at partial loads	Higher efficiency at partial loads [1], [2], [3], [5], [9]
Efficiency (battery)	Higher	Lower [2]
Parallel switches (per switch position)	May be necessary for distribution of high currents	May or may not be needed (useful for reducing conduction losses) [5]
Fault tolerance	Possible with extra legs	With bypass switches [10]
Cost	Standard	Slightly lower [1], [5]
Reliability	Standard	• Lower than two-level but fault tolerance enhances reliability [5] • Increased reliability compared to other multilevel topologies [1], [11]

[1] (Poorfakhraei et al., 2021b)
[2] (Kersten et al., 2019a)
[3] (Ali and Khalid, 2023)
[4] (Sarrazin et al., 2011)
[5] (Chang et al., 2019)
[6] (Maharjan et al., 2009)
[7] (Vasiladiotis and Rufer, 2013)
[8] (Kersten et al., 2019b)
[9] (Marzoughi et al., 2018)
[10] (Leon et al., 2017)
[11] (Farzamkia et al., 2020)

Table 2.2: Summary of prominent literature on converter topologies for traction applications.

Converter	**Three-phase**	**Multiphase**
Standard two-level	Not surveyed directly (mature technology). Comparison provided in literature listed under **EV drive** heading (below) for NPC, CHB, MMSP, and MMC topologies.	(Jones et al., 2009) (Riveros et al., 2010) (Che et al., 2014) (Subotic et al., 2015) (Bojoi et al., 2016) (Subotic et al., 2016) (Baumgardt et al., 2016) (González-Prieto et al., 2019) (Salem and Narimani, 2019) (Prieto et al., 2020)

Converter	Three-phase	Multiphase
Single H-bridge	Not surveyed	**EV drive** (Gliese et al., 2022) (Bayati et al., 2023)
NPC	**EV drive** (Kersten et al., 2018) (Wang et al., 2021)	**EV drive** (Dordevic et al., 2013) (Wang et al., 2016)
MMSP	**EV drive** (Korte et al., 2017) (Kersten et al., 2019b) (Sorokina et al., 2021)	N/A
MMC	**EV drive** (Quraan et al., 2016) (Quraan et al., 2017) (Wang et al., 2019) **Related topics** (Shen et al., 2018) (Marzoughi et al., 2018) (Farzamkia et al., 2020)	N/A
CHB (symmetrical)	**EV drive** (Tolbert et al., 2002) (Josefsson et al., 2012) (Chang et al., 2017) (Korte et al., 2017) (Shen et al., 2018) (Kersten et al., 2019b) (Chang et al., 2019) (Ali and Khalid, 2023) **Unequal dc-source voltage** (Rodriguez et al., 2005) (Maharjan et al., 2010) (Carnielutti et al., 2012) (Lingom et al., 2022) (Cho et al., 2014) (Kim and Cho, 2022) **Related topics** (Angulo et al., 2007) (Kouro et al., 2008) (Marquez et al., 2017) (Kersten et al., 2020) **SoC Balancing** (Maharjan et al., 2009) (Wang et al., 2015) (Mathe et al., 2016) (Altaf and Egardt, 2017) (Kersten et al., 2019a)	**EV drive*** (Rahman et al., 2019) Closed loop *v/f* control only **Unequal dc-source voltage*** (López et al., 2024) **Electric aircraft drive** (Tedeschini et al., 2021) FOC of PMSM (simulation only) **Related topics** (López et al., 2008): SV-PWM (Lopez et al., 2016): SV-PWM method for CMV reduction (López et al., 2020): Analysis of carrier-based and SV-PWM methods
Hybrid/ Others	(Du et al., 2009) (Hota et al., 2017) (Samadaei et al., 2018) (Lee et al., 2018)	**EV drive** (Zaidi et al., 2019)
Note: * indicates the context and topics addressed in this thesis and the list of publications is given in Appendix D.1.		

Chapter 3
Cascaded H-bridge multilevel converter

3.1 Introduction

This chapter will introduce the single-phase (section 3.2) and three-phase CHB-MLI topology (section 3.3) and different modulation techniques applicable to it. Both low (subsection 3.4.1) and high (subsections 3.4.2 and 3.4.3) frequency modulation techniques will be presented and analysed in terms of the total harmonic distortion produced at different operating points (subsection 3.4.4) via simulation modelling. The problem related to the level-shifted multicarrier modulation schemes causing uneven power distribution between H-bridge modules will be addressed (section 3.5). Several equalisation methods will be explored to mitigate this drawback and ensure equal power distribution while retaining the performance advantage provided by level-shifted modulation. Part of the content of this chapter has been published in (Khan et al., 2022).

3.2 Cascaded H-bridge topology

A single-phase full-bridge voltage source converter forms the fundamental building block (module) for the CHB topology. A low power module consists of an isolated dc source connected in parallel with an H-bridge converter consisting of four switches - two switches per H-bridge leg. Antiparallel (freewheeling) diodes are always included with each switch for providing a return path to the current in the case of inductive loads (Rashid, 2018). A simplified structure of a single-phase H-bridge voltage source converter is shown in Figure 3.1.

The positive leg is assumed to include switches S1 and S2 whereas the negative leg is assumed to include switches S3 and S4, such that when the switches S1 and S4 are switched on, an output voltage of $+V_{dc}$ is seen at the output. Turning on switches S2 and S3 would lead to a load voltage of $-V_{dc}$. The other two possibilities result in an output voltage of zero where either switches S1 and S3 or switches S2 and S4 have been switched on (see Table 3.1). It must be noted that two switches in an H-bridge leg must not be switched on simultaneously to avoid a short circuit of the dc source. In similar vein, care must be taken to avoid a short circuit of the dc source during switching transients due to the dissimilarity

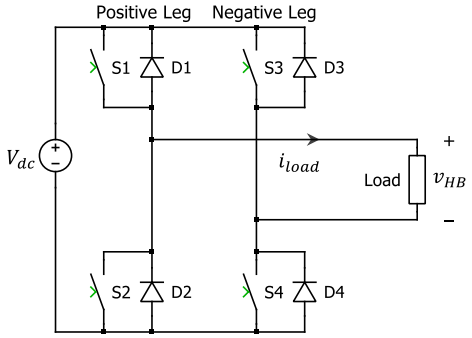


Figure 3.1: A single-phase H-bridge module with its dc source.

Table 3.1: Valid switching states and the resultant output voltage level.

S1	S2	S3	S4	v_{HB}
ON	OFF	OFF	ON	$+V_{dc}$
OFF	ON	ON	OFF	$-V_{dc}$
ON	OFF	ON	OFF	**0**
OFF	ON	OFF	ON	**0**

between the turn off and turn on times of the switching devices. This is achieved through the insertion of a small time-delay, known as dead time, to the device turn on signal. However, for the simulation results shown in this chapter, dead time has not been introduced, and the switches are considered to be ideal.

Two additional possibilities do exist for the flow of current into the dc source when all switches are turned off. This occurs in the case of regenerative mode of operation where active power is delivered from the load to the dc source through current flowing through the freewheeling diodes which are turned on and off automatically. In the first regenerative case, a negative load current flows from the load into the dc source through the freewheeling diodes D1 and D4, causing an output voltage equal to $+V_{dc}$ across the load. Similarly, in the second regenerative case, a positive load current flows from the load into the dc source through the freewheeling diodes D2 and D3, causing an output voltage of $-V_{dc}$ across the load.

A series connection of the output terminals of multiple H-bridge modules forms the CHB converter, which is illustrated in Figure 3.2a. Each module, as explained, can generate three voltage levels ($+V_{dc}$, 0, and $-V_{dc}$) depending on the switching state combination, as summarised in Table 3.1. A cascaded connection of the H-bridge modules results in the synthesis of an output voltage waveform, which is the sum of all the module output voltages. In the considered case, all dc sources have identical voltages (symmetrical configuration) leading to advantages that come from modularity. As the number of levels of the output voltage waveform increases, the more the synthesised waveform resembles a sinusoidal wave. It can be observed that two unique switching combinations produce the same output voltage (i.e., 0 V) and are thus known as redundant switching states. The redundant

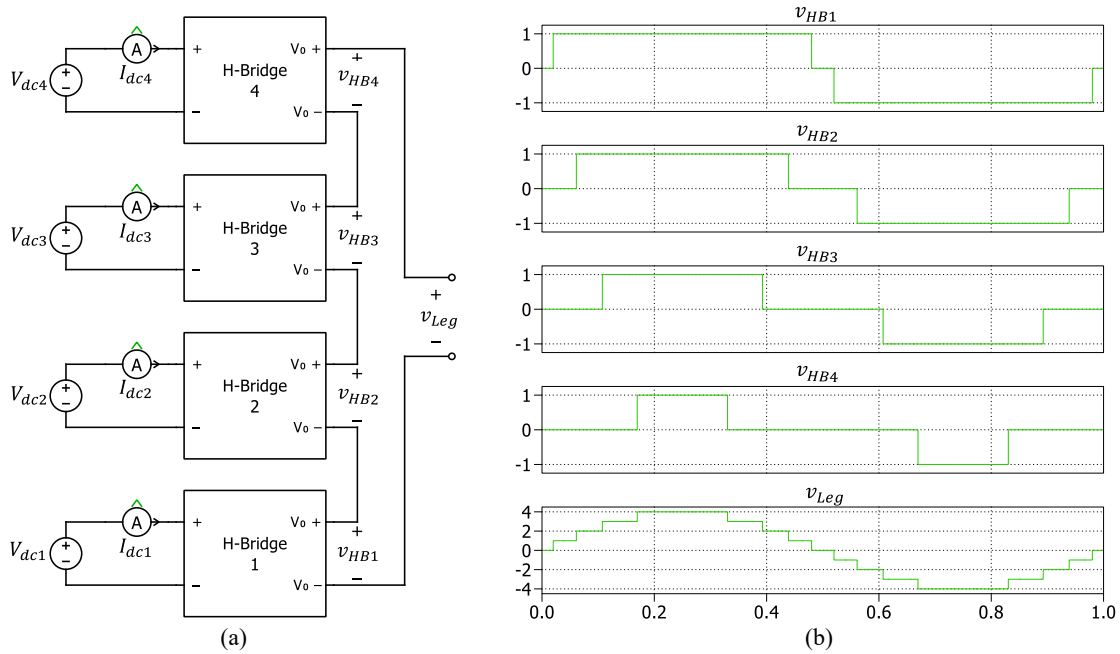


Figure 3.2: (a) A single-phase CHB consisting of 4 H-bridge modules in series (b) An example of the output voltage waveforms for each H-bridge and the resultant multilevel (9-level) inverter output leg voltage.

switching state number increases correspondingly with the increase in the number of levels. The output voltage waveform of the CHB-MLI is made up of $l = 2k + 1$ voltage levels, where k is the number of H-bridge modules per inverter phase leg, each with its own isolated dc source. The number of levels of the waveform is always an odd number for a CHB inverter. In the case of a cascade connection of four H-bridges, taken as an example for analysis in this chapter, a 9-level output leg voltage results from the sum of the output voltages of all individual H-bridges modules:

$$v_{Leg} = v_{HB1} + v_{HB2} + v_{HB3} + v_{HB4} \tag{3.1}$$

An example of a 9-level leg voltage waveform from a CHB with $k = 4$ is demonstrated in Figure 3.2b. The switching device in each H-bridge module must be operated in a manner that produces the desired output voltage waveform. This is done through an appropriate modulation strategy. A discussion on the modulation methods will follow in section 3.4.

3.3 Three-phase CHB inverter topology

A multiphase multilevel CHB inverter may be formed with multiple single-phase CHB legs connected in parallel to form individual phase legs. Each individual H-bridge is supplied by a constant dc voltage source, which would typically be a battery in an EV application. The topology of a three-phase multilevel CHB connected to a star-connected RL load can be

seen in Figure 3.3 where the dc sources are represented by a battery. The leg voltages of a three-phase CHB converter, consisting of k modules per converter leg, are obtained as:

$$v_{xn} = \sum_{i=1}^{k} v_{xi} \tag{3.2}$$

where x can be any of three phases (a, b, or c). Similarly, the total dc-link voltage in any of the three converter legs is defined by:

$$V_{dc\_x} = \sum_{i=1}^{k} V_{dc\_xi} \tag{3.3}$$

In a balanced three-phase system, the offset (also known as common-mode or zero sequence) voltage, between the floating load neutral point s and inverter neutral point n (see Figure 3.3), can be defined as the average of the converter leg voltages:

$$v_{sn} = (v_{an} + v_{bn} + v_{cn})/3 \tag{3.4}$$

Correspondingly, the load phase voltages sum up to zero in a balanced system and are described, in terms of the leg, common-mode and line voltages, by:

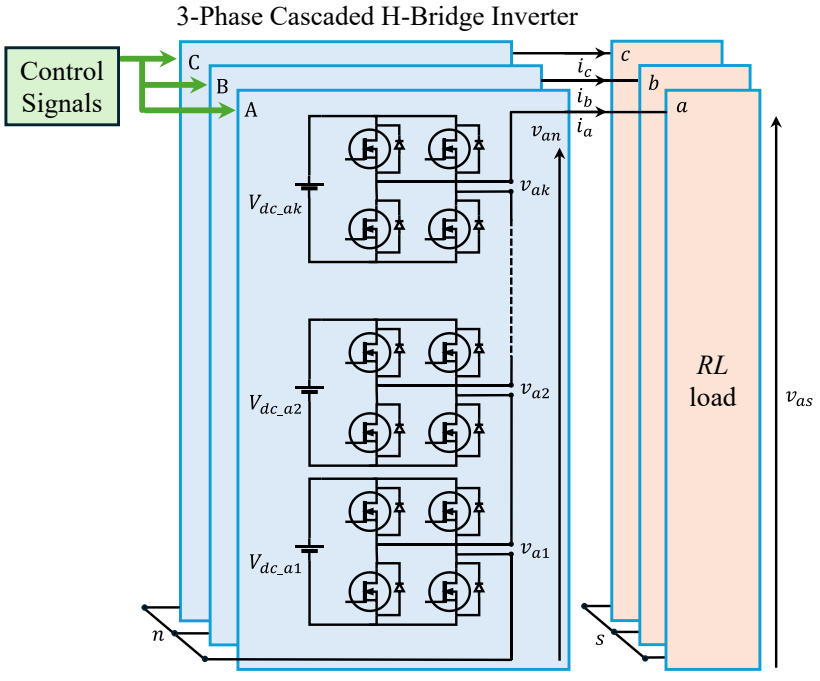


Figure 3.3: Three-phase k-module cascaded H-bridge inverter connected to an RL load.

$$\begin{cases} v_{as} = v_{an} - v_{sn} = (v_{ab} - v_{ca})/3 \\ v_{bs} = v_{bn} - v_{sn} = (v_{bc} - v_{ab})/3 \\ v_{cs} = v_{cn} - v_{sn} = (v_{ca} - v_{bc})/3 \end{cases} \quad (3.5)$$

In a balanced star-connected three-phase system with an RL load, the load phase currents sum up to zero and are related to the phase voltages for any of the three phases: $x = (a, b, \text{or } c)$, as:

$$v_{xs} = Ri_x + L\frac{\mathrm{d}i_x}{\mathrm{d}t} \quad (3.6)$$

3.4 Modulation methods

The objective of modulation is to control the switching of semiconductor devices in a power electronic converter from one condition to another. Typically, this involves conversion between dc to ac in the case of inverters and ac to dc in the case of rectifiers. The amplitude and/or frequency of the output voltage of a CHB inverter can be controlled using various modulation methods. However, each modulation method needs to be considered based on the satisfaction of certain requirements. Issues such as switching frequency, inverter losses, presence of harmonics and harmonic distortion are important factors that need to be taken into consideration. Specifically for traction applications, such as EV drives, factors such as dynamic response, torque ripple, equal switch utilisation, waveform quality, complexity of the modulation scheme and cost are important criteria for selection (Poorfakhraei et al., 2021a).

PWM is the most used modulation method with the sinusoidal PS- and LS-PWM being the most well-known among the carrier-based high frequency modulation methods. Among the low frequency modulation strategies, simple techniques - like the programmable multilevel SHE - are widely used. Another simple technique with easy implementation and low switching frequency is the nearest level modulation (NLM) which is the 'time domain' equivalent of space vector control. SV-PWM is also very popular for two- and three-level inverters but becomes computationally intensive for higher number of voltage levels. It has also been proven by (McGrath et al., 2003) that an equivalent performance can be achieved with an injection of appropriate zero-sequence voltage to the reference waveform using carrier-based PWM, hence, SV-PWM is not studied in this thesis, but instead appropriate

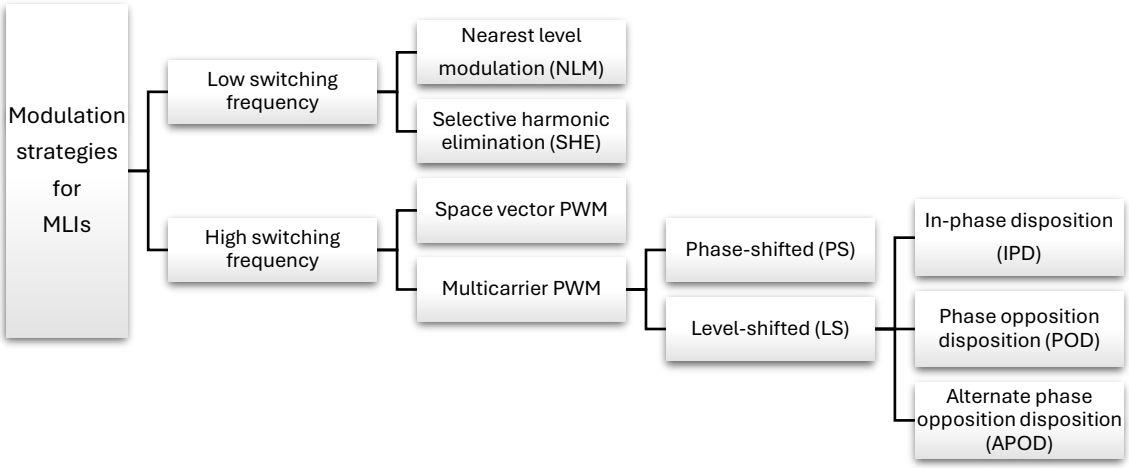


Figure 3.4: Classification of modulation strategies for multilevel inverters.

carrier-based implementations are used. A classification of well-known modulation strategies for multilevel inverters is shown in Figure 3.4.

In this section, two low frequency methods are described including the NLM and SHE. High frequency modulation methods based on multicarrier PWM are also studied and compared in greater detail. These include the multicarrier PS-PWM (most popular method for CHB-MLI (Leon et al., 2017)), and the LS-PWM methods i.e., the IPD-PWM, POD-PWM, and APOD-PWM. Multicarrier PWM schemes are implemented on a 9-level CHB connected to a single-phase RL load and a three-phase 9-level CHB connected to a star-connected RL load. The modulation methods are compared to each other in terms of the THD of the inverter leg voltage, line to line voltage, the load phase voltage, and phase current waveforms over the entire linear modulation index range.

Parameters used for obtaining simulation results in this chapter are specified in Table 3.2, unless otherwise stated. It is also apt to point out that the figures demonstrating the modulation methods were generated using a significantly lower switching frequency for illustrative purposes. Inverter switches are considered as ideal with V_{on} and R_{on} taken as zero. A sinusoidal modulating signal has been used throughout, although min-max injection for a multiphase system would be appropriate and will be considered in later work.

For comparison between different modulation methods discussed hereafter, it is necessary to define the total harmonic distortion (THD), in percentage, of a waveform:

Table 3.2: Simulation parameters for modulation method comparison

Parameter	Value
Load resistance	R = 15 Ω
Load inductance	L = 10 mH
DC source voltage	V_{dc} = 30 V
Frequency of modulating wave	f_m = 50 Hz

$$\mathrm{THD}_U = \sqrt{\frac{U_{rms}^2 - U_0^2 - U_1^2}{U_1^2}} \times 100\% \tag{3.7}$$

where U stands for either the leg voltage, phase voltage, or the phase current, U_0 and U_1 represent the dc component and the rms value of the fundamental harmonic respectively, and U_{rms} is the overall rms value (calculated from the time domain). Therefore, all harmonics are considered in the calculation of the THD in (3.7). In contrast, weighted total harmonic distortion (WTHD) is also sometimes used to describe the harmonic distortion in inductive loads where a scaling factor considers the impact of a certain number of higher order current harmonics to account for higher impedances associated with these harmonics. However, WTHD was not used in this thesis.

3.4.1 Low frequency modulation

Low frequency modulation methods are generally simpler to implement and offer an advantage over the high frequency modulation methods in terms of lower switching losses. However, operation at lower switching frequency results in a significantly higher amount of THD compared to the high frequency modulation methods. This section provides a discussion on two low frequency modulation methods, namely the NLM and SHE.

3.4.1.1 Nearest level modulation

A simple low frequency modulation method can be formulated by synthesising the desired multilevel output voltage waveform by switching at instants such that the modulating wave intersects each level of the stepped waveform at exactly half of its amplitude. The process for obtaining the voltage levels is illustrated in Figure 3.5a.

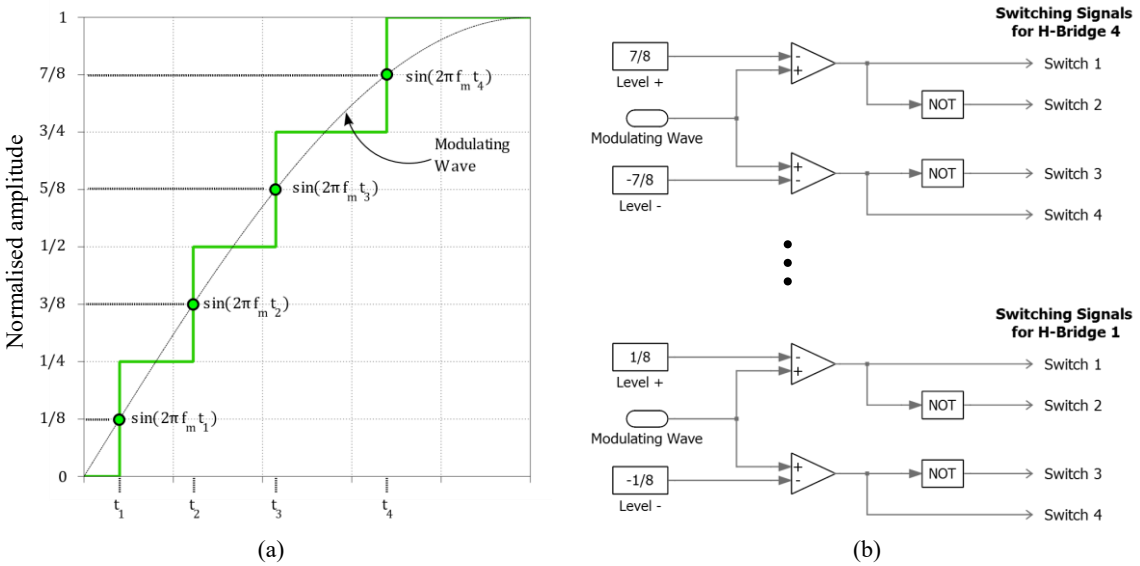


Figure 3.5: (a) Nearest level modulation (b) Schematic for the generation of gate signals for H-bridge modules in a CHB using NLM.

For an l level output waveform (l is odd), the number of switching angles is $\frac{l-1}{2}$, which is equal to the number of H-bridge modules in series. Thus, the synthesis of a 9-level output voltage waveform requires the calculation of four switching angles in the first quarter of the modulating wave, one for each of the four H-bridge modules. These can be calculated simply by solving for the respective time t by equating the amplitude at that angle with the value of the modulating sinusoidal signal as shown in Figure 3.5a. The general formula for the switching angles can be described as

$$\mathrm{t_i} = \frac{1}{2\pi f_m} \sin^{-1}\left(\frac{1}{k}\left(i - \frac{1}{2}\right)\right);\ i = 1, 2, \ldots, k \tag{3.8}$$

where k is the number of H-bridges modules per phase. The gate signals for the switches in the positive leg of each H-bridge module can be obtained by comparing a modulating sinusoidal waveform (positive half of the modulating wave) with the fixed amplitude values (nearest level, N) found with the general formula for an k number of switching angles as

$$N_i = \frac{1}{k}\left(i - \frac{1}{2}\right);\ i = 1, 2, \ldots, k \tag{3.9}$$

The nearest level amplitude values (N_i) obtained for the positive half of the modulating wave are multiplied by -1 to form the nearest levels required for comparison with the modulating

sinusoidal waveform (negative half of the modulating wave) to generate the gate signals for the negative leg of each H-bridge module (Figure 3.5b) to complete the modulation process.

Although the implementation of the NLM is very simple, it suffers from certain drawbacks. The quality of the resulting multilevel waveform highly depends on the number of levels of the output voltage. If a fewer number of H-bridges are used, then the resulting harmonic distortion of the output voltage waveform is more likely to be unacceptable for practical applications. Additionally, unequal utilisation of the H-bridge dc sources is an additional problem that needs to be addressed. The biggest drawback comes from the presence of lower order harmonics at the inverter output, and, consequently, in the line and phase voltages and currents as can be seen from the simulation results in Figure 3.6b shown for unity modulation index.

It can be observed (Figure 3.6b) that the fundamental harmonic magnitude at unity modulation index has not been accurately achieved with value slightly higher than the required 120 V ($4V_{dc}$). This imprecision is even more pronounced for other modulation indices. Even harmonics are not present due to leg voltage waveform symmetry as expected. The third harmonic is absent in the line and phase voltage waveforms due to the cancellation of the third harmonic (and other triples) in a balanced three-phase system. However, magnitude of odd non-triplen lower order harmonics (e.g., 5th, 7th, and 11th) is relatively large

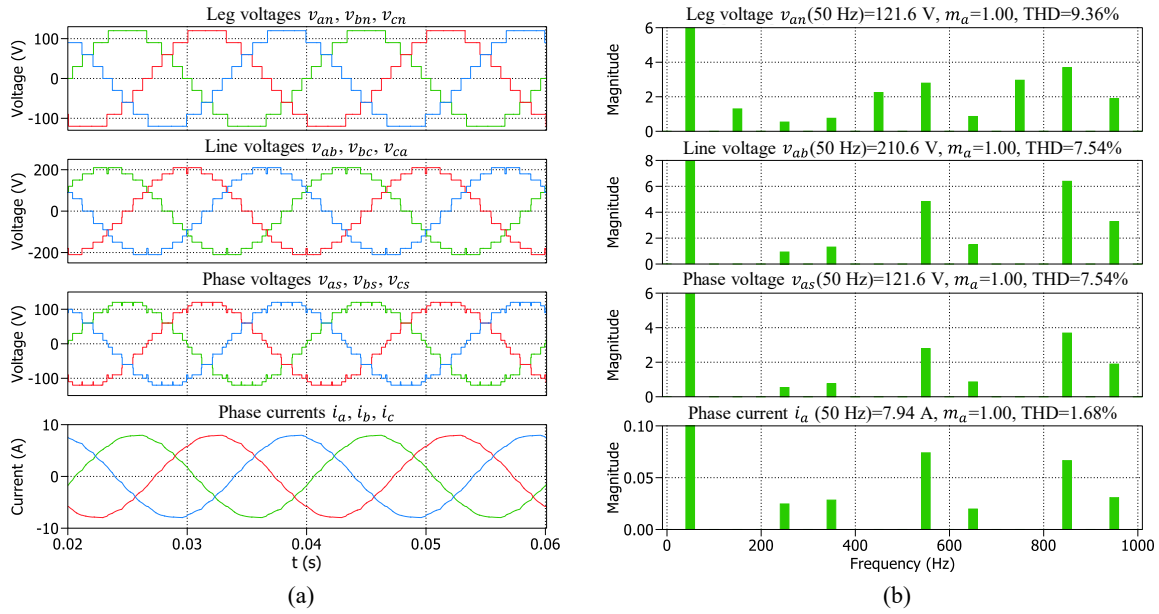


Figure 3.6: Simulation results for NLM implementation on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index (a) Leg, line and phase voltage, and phase current waveforms (b) associated spectra and THD.

for certain modulation indices. This issue can be addressed with low frequency modulation using the selective harmonic elimination method which follows next.

3.4.1.2Selective harmonic elimination

Selective harmonic elimination (SHE) is a low frequency modulation technique, in which each semiconductor device switches only once per fundamental cycle. The idea of SHE entails cancellation of certain lower order harmonics while keeping the fundamental harmonic at a specified value. In the case where this is not achievable for the complete modulation index range, the harmonics can be minimised to a certain level while maintaining the required fundamental output.

A periodic stepped waveform can be described using Fourier series as a sum of its composite harmonics, which are defined in terms of independent switching angles. The formulation of the Fourier series equations depends on waveform symmetry consideration. Generally, a quarter wave symmetrical formulation of the multilevel waveform is used for simplicity. An l-level leg voltage waveform can be expressed in terms of its Fourier series components as:

$$v_{xn} = \frac{4V_{dc}}{\pi}\sum_{h=1,3,5,\dots}^{\infty}\frac{\sin(h\omega t)}{h}\left(\cos(h\theta_1) + \cos(h\theta_2) + \cdots + \cos\left(h\theta_{\frac{l-1}{2}}\right)\right) \tag{3.10}$$

where h is the harmonic order, $\omega = 2\pi f$ (f is the fundamental frequency), $x = \{a, b, c, \dots\}$ denotes the phase, and the independent switching angles $\theta_1, \theta_2, \dots, \theta_{(l-1)/2}$ must satisfy the following constraint:

$$0 \le \theta_1 \le \theta_2 \le \cdots \le \theta_{\frac{l-1}{2}} \le \frac{\pi}{2} \tag{3.11}$$

A 9-level inverter leg voltage waveform, shown in Figure 3.7, can be expressed as:

$$v_{an} = \frac{4V_{dc}}{\pi}\sum_{h=1,3,5,\dots}^{\infty}\frac{\sin(h\omega t)}{h}(\cos(h\theta_1) + \cos(h\theta_2) + \cos(h\theta_3) + \cos(h\theta_4)) \tag{3.12}$$

where h is the harmonic order, and the independent switching angles $\theta_1, \theta_2, \theta_3$, and θ_4 must satisfy the following constraint:

Figure 3.7: A nine-level inverter output voltage waveform with 4 switching angles.

$$0 \leq \theta_1 \leq \theta_2 \leq \theta_3 \leq \theta_4 \leq \frac{\pi}{2} \tag{3.13}$$

From (3.12), the fundamental component of the stepped voltage waveform can be defined as:

$$v_{an,1} = \frac{4V_{dc}}{\pi}(\cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4) \tag{3.14}$$

The modulation index (m_a) can be defined as the ratio of the fundamental component to the maximum achievable peak which is kV_{dc}. In the case of a 9-level waveform, it is:

$$m_a = \frac{v_{an,1}}{4V_{dc}} \tag{3.15}$$

From (3.14) and (3.15), an expression for the fundamental leg voltage harmonic in terms of switching angles can be obtained as:

$$v_{h1} = \cos\theta_1 + \cos\theta_2 + \cos\theta_3 + \cos\theta_4 = \pi m_a \tag{3.16}$$

Note that v_{h1} represents the normalised fundamental leg voltage harmonic. The remaining three equations can be formed for the elimination of the 5th, 7th, and 11th harmonics for a 9-level waveform as:

$$v_{h5} = \cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) = 0 \tag{3.17}$$

$$v_{h7} = \cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) = 0 \tag{3.18}$$

$$v_{h11} = \cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) = 0 \tag{3.19}$$

The 3rd and 9th harmonic were not chosen for elimination as they naturally cancel out in the line and phase voltages in a balanced three-phase system. Numerous techniques have been proposed in the literature for the solution of these transcendental non-linear equations. Numerical approaches are generally the preferred method of choice to find the switching angles, the iterative Newton-Raphson method being the most widely used (Dahidah et al., 2015). Other methods resort to the reformulation of the transcendental trigonometric equations into equivalent polynomial functions or into an optimisation problem where a cost function is minimised subject to certain constraints.

First, the system of equations was solved using the iterative Newton-Raphson method to obtain solutions for the switching angles where the function converges and provides feasible solution to the SHE equations. The amplitude modulation index (m_a) was varied from 0 to 1 and the system of non-linear equations was solved iteratively to obtain solutions for the switching angles at each modulation index shown in Figure 3.8a. The solution to the SHE equations only exists for a certain range of modulation indices. Here, a solution does not exist for a modulation index below 0.42, which means that the fundamental harmonic cannot be controlled to the desired value while the 5th, 7th, and the 11th harmonics are eliminated.

Next, to obtain a solution of the SHE equations for the complete modulation index range, the 5th, 7th, and the 11th harmonics were instead minimised while the fundamental harmonic was controlled to the desired value. In this case, the set of nonlinear equations [(3.16) – (3.19)] was transformed into an optimisation problem and solved for the switching angles using the *fmincon* function in MATAB. The SHE angles were obtained using non-linear optimisation to minimise an objective function, subject to certain equality and non-equality constraints being met, defined as:

$$\underbrace{Minimise}_{\theta} \{(v_{h1} - \pi m_a)^2 + (v_{h5})^2 + (v_{h7})^2 + (v_{h11})^2\} \tag{3.20}$$

The equality constraint was taken to be the control of the fundamental component of the inverter output voltage ($v_{an,1}$) to exactly follow $4V_{dc}m_a$ (3.15) and the inequality constraints being the minimisation of the 5th, 7th, and 11th harmonics to a small tolerance value (instead of zero) to ensure convergence. The results for the switching angles obtained are plotted in Figure 3.8b.

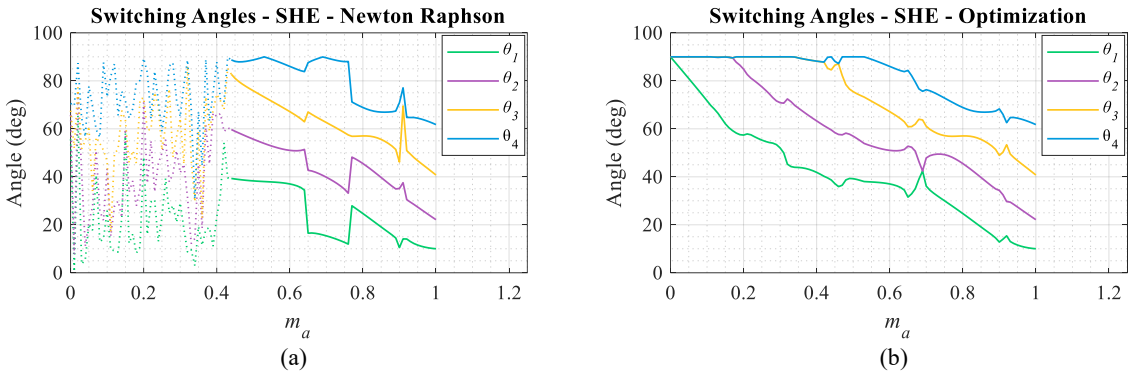
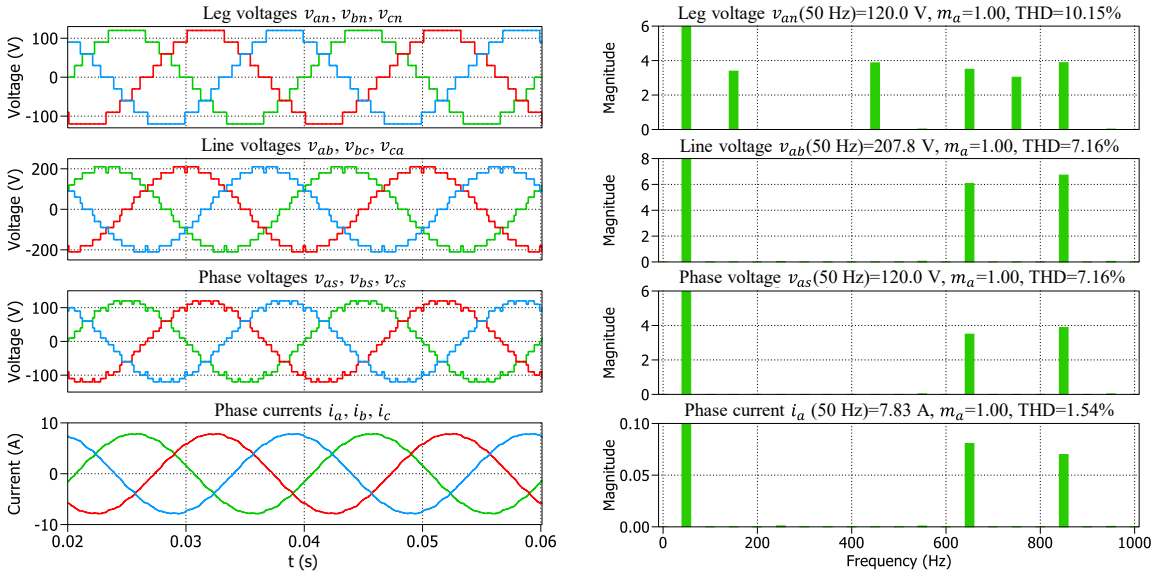


Figure 3.8: Switching angles versus modulation index for SHE equations with (a) Iterative Newton Raphson method (b) Optimisation function.

The switching angles obtained with both solution techniques were implemented in simulation on a balanced star-connected three-phase RL load connected to a 9-level CHB-MLI to obtain the waveforms for the leg, line and phase voltage and phase current as shown in Figure 3.9. As expected the triplen harmonics are absent from the line and phase voltage waveforms, as well as from the phase current waveform.

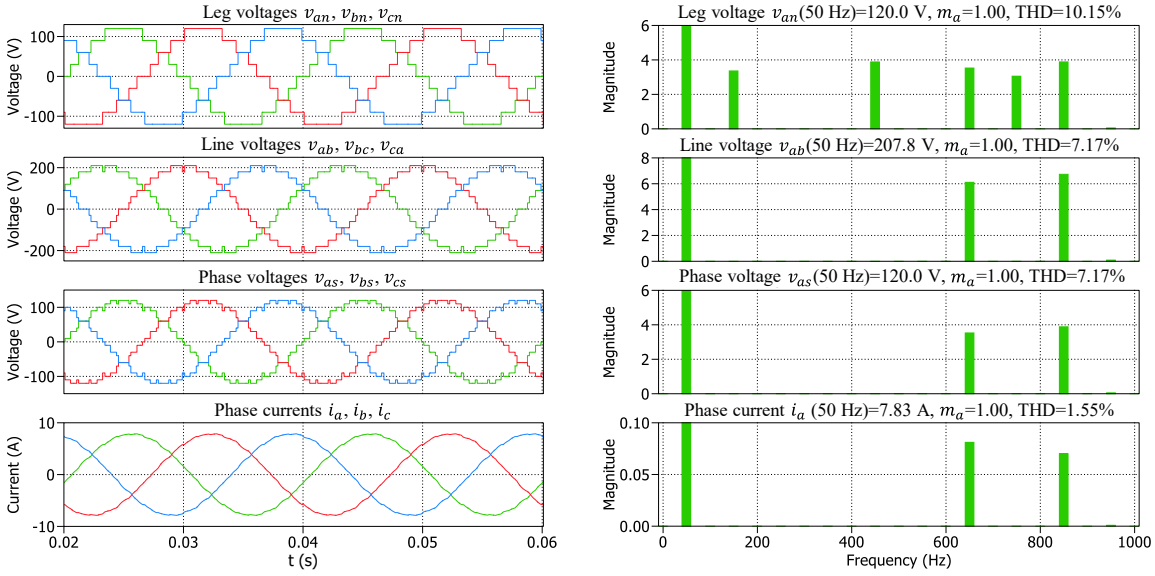
The waveforms generated using both methods (Figure 3.9 and Figure 3.10) are practically indistinguishable. This is because the same switching angles were obtained as solutions to the SHE equations by both methods at unity modulation index. Consequently, the THD for the voltage and current waveforms are practically the same. The primary objective of SHE has been achieved, i.e., the 5^{th}, 7^{th}, and 11^{th} harmonics have been eliminated, while the fundamental leg voltage magnitude of 120 V has been accomplished. The first dominant harmonic is the 13^{th} harmonic (@650 Hz) in the line and phase voltages and phase currents waveforms.

A sweep through the modulation index range was performed for each of the low frequency modulation methods. Figure 3.11a shows the magnitude of the fundamental phase voltage (v_{as}) harmonic plotted for the entire modulation index range for each method. For NLM, the fundamental harmonic produced does not precisely follow the desired amplitude ($4V_{dc}m_a$) for most of the modulation index range and the method does not work below modulation index of 0.125 as expected. This behaviour can be improved, and the range of operation over a larger range of modulation indices can be achieved, with the use of a greater number of H-bridge modules in series per phase. However, the lower order harmonics are not controlled using NLM (Figure 3.12) and its implementation would neccessitate larger filtering.



(a) (b)

Figure 3.9: Simulation results for SHE-Newton Raphson implemented on a 9-level CHB-MLI connected to a three-phase RL load at unity modulation index (a) Leg, line and phase voltage, and phase current waveforms (b) associated spectra and THD.



(a) (b)

Figure 3.10: Simulation results for SHE-Optimization implemented on a 9-level CHB-MLI connected to a three-phase RL load at unity modulation index (a) Leg, line and phase voltage, and phase current waveforms (b) associated spectra and THD.

It can be observed from Figure 3.11 that the solution set obtained with the SHE-Newton Raphson method was not implemented for $m_a < 0.42$ as no viable solution to the SHE equations was found. However, for the achievable range of modulation indices, the fundamental harmonic is seen to follow the desired amplitude ($4V_{dc}m_a$) linearly with minor divergence around $m_a = 0.45$ and $m_a = 0.65$. A similar profile for the phase current can be seen in Figure 3.11b.

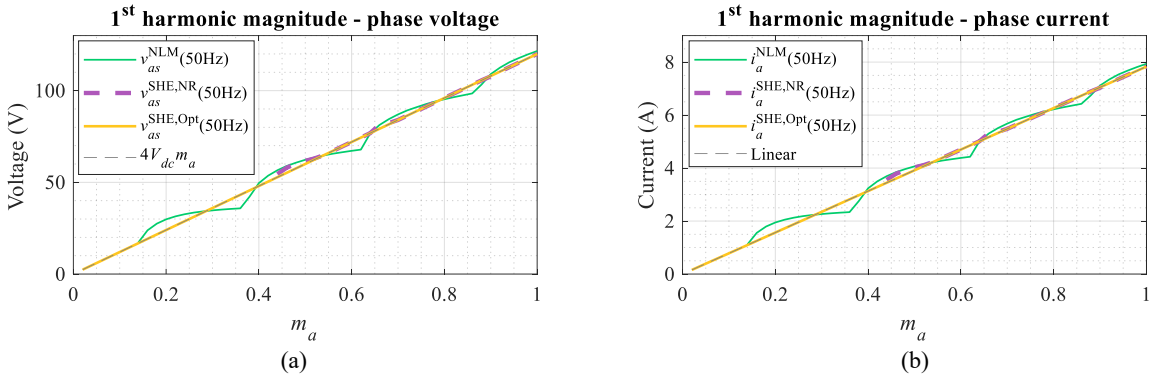


Figure 3.11: Magnitude of the fundamental (a) phase voltage and (b) phase current over the entire modulation index range for NLM, SHE-Newton Raphson (SHE,NR), and SHE-Optimisation (SHE,Opt).

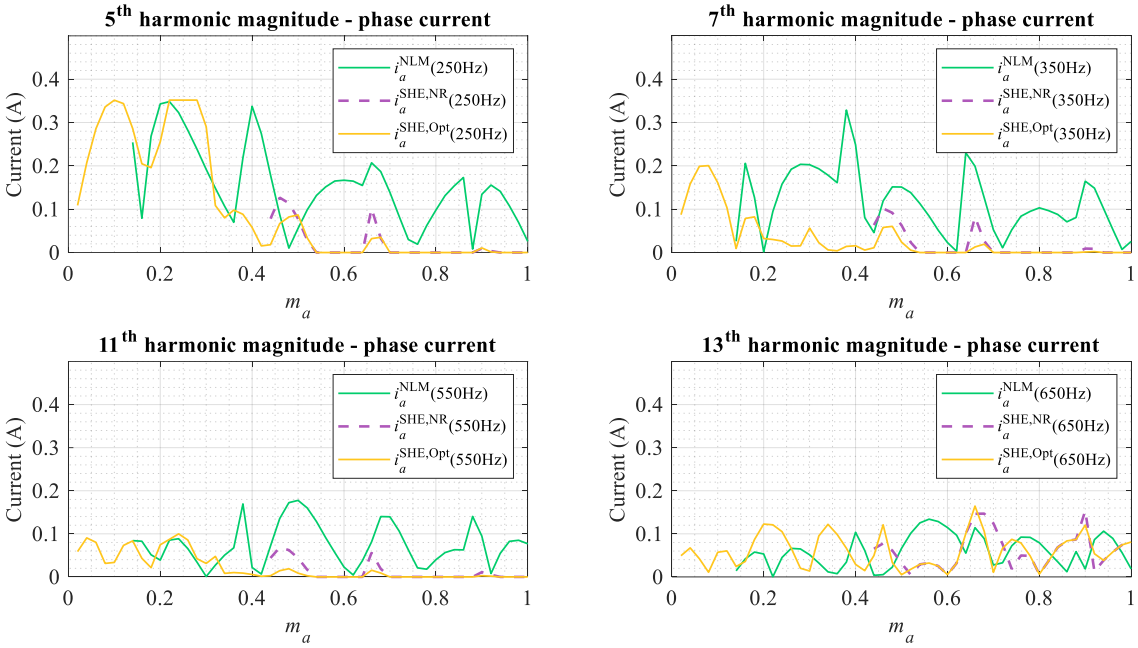


Figure 3.12: Magnitude of the 5th, 7th, 11th, and 13th harmonics of the phase current over entire modulation index range for NLM, SHE-Newton Raphson, and SHE-Optimisation.

In contrast, the solution of the SHE equations using optimisation produces a set of solutions for the entire range of modulation indices. The required fundamental harmonic amplitude can be seen to have been achieved for the entirety of the modulation index range with a small allowance of lower order harmonics where necessary as can be seen from Figure 3.12. The NLM method produces a poor quality waveform at low modulaton indices.

The primary lower order harmonics that were selected to be eliminated or minimised were the 5th, 7th, and 11th harmonics. These harmonics can be seen to have been practically eliminated by both SHE-Newton Raphson and SHE-Optimisation for higher modulation indices (Figure 3.12). However, for lower modulation indices, SHE-Newton Raphson method does not have a valid solution (see Figure 3.8a). Therefore, the magnitudes of the

lower order harmonics are instead minimised using the optimisation function (*fmincon* function in MATLAB) while keeping the magnitude of the fundamental at the desired value.

The THD of the leg, line, and phase voltages and phase currents for each of the modulation methods has been plotted for the modulation index range between 0.10 to 1.00 in Figure 3.13. It can be seen that the THD produced with the NLM method for the leg voltage is the lowest, but this comes at the cost of imprecise control of the fundamental harmonic which is obviously not desirable. Whereas SHE-Optimisation offers a much tighter control of the fundamental harmonic. It can be observed (Figure 3.13) that the leg voltage THD with the SHE-Optimisation method only increases above 100% for $m_a < 0.15$. A similar increase in the THD of the line and load phase voltages can be seen around the same region, when the line voltage THD is seen to jump above 50%. The load phase current THD profile shows that the SHE-Optimisation offers the lowest overall THD for the entire modulation index range. The phase current THD with SHE-Optimisation does however jump above 25% for $m_a < 0.15$. It is possible to reduce these harmonic distortion values using higher frequency modulation methods, which follow next.

3.4.2 Phase-shifted PWM

PS-PWM is a well-known technique where a modulating wave is compared with a high frequency carrier wave to generate switching pulses. Pulse widths are determined by

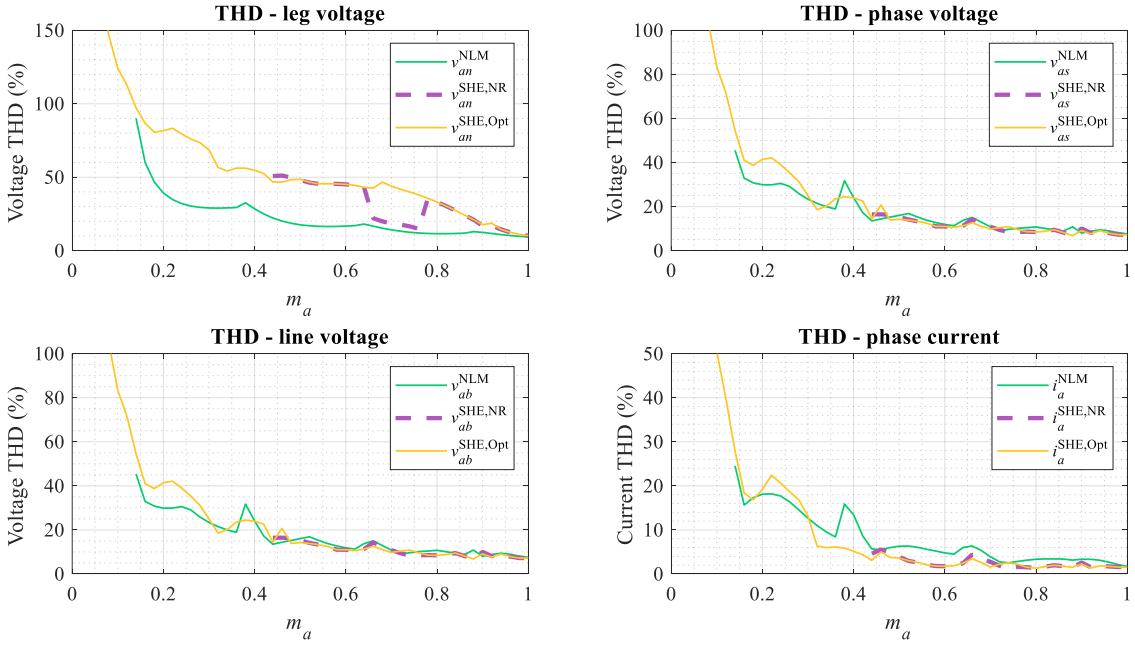


Figure 3.13: THD comparison between low frequency modulation methods for leg voltage, line voltage, phase voltage and phase current for the entire modulation index range.

the cross section of the modulating and carrier waves. Triangular carriers have been used as they tend to produce output waveforms with a lower total harmonic distortion as noted by (Hamman and Merwe, 1988).

Certain important definitions are necessary before proceeding with the following discussion on modulation methods. The amplitude or peak value of the modulating (reference) wave is defined as A_m whereas that of the carrier wave is defined as A_c. Similarly, the period of the modulating wave is defined as T_m and that of the carrier wave is defined as T_c. The periods are related to the frequency of the carrier and modulating waves respectively as:

$$f_c = {T_c}^{-1}$$
$$f_m = {T_m}^{-1} \tag{3.21}$$

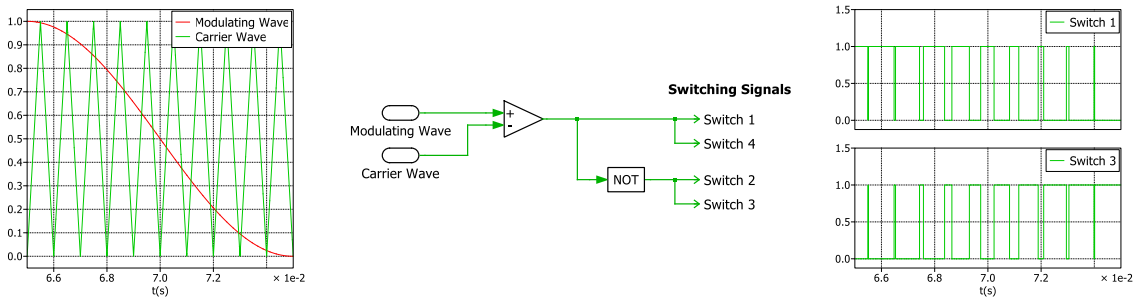
The amplitude modulation index is defined as the ratio between the amplitude of modulating waveform and that of the carrier wave:

$$m_a = \frac{A_m}{A_c} \tag{3.22}$$

The effective inverter switching frequency is designated as f_{si} which is where the dominant switching harmonic lies on the spectrum. Similarly, the device switching frequency (f_{sd}) is switching frequency of the active switches in the CHB. In what follows, the concept of bipolar and unipolar modulation methods applied on a single H-bridge will be explained. After that, the extension of the unipolar modulation method to multicarrier PS-PWM, applicable to the CHB-MLI, is revised.

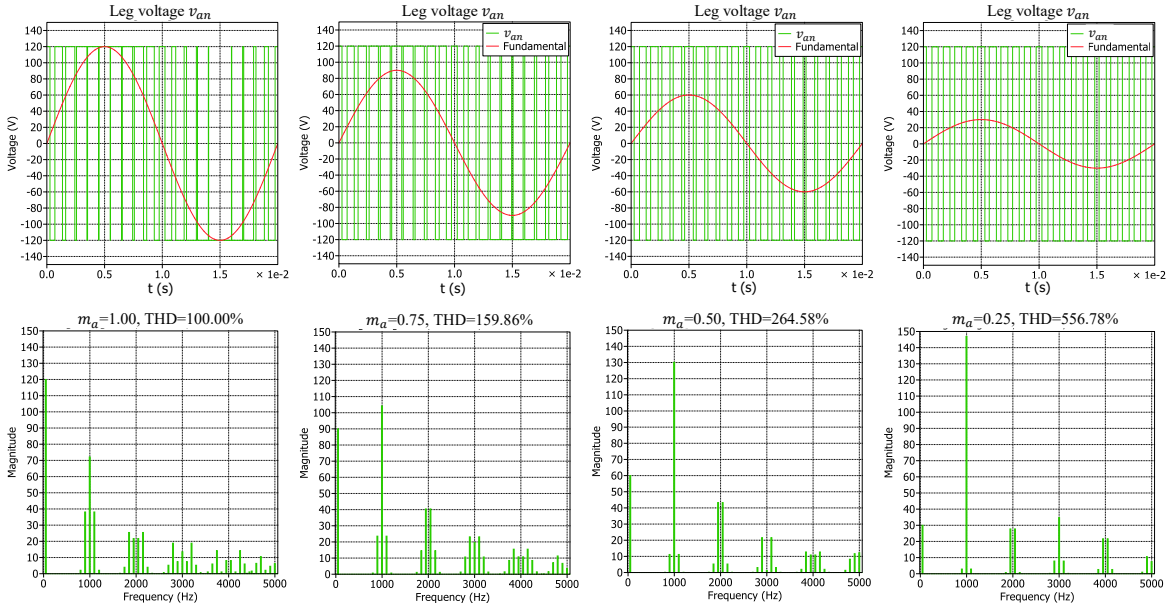
3.4.2.1 Bipolar modulation

A single-phase H-bridge inverter can be modulated using a modulation method where a single sinusoidal modulating wave is compared with a single triangular carrier to generate gating signals for one switch in each leg of the H-bridge inverter (Figure 3.14). Refer to Figure 3.1 for switch notation. This is known as bipolar modulation because the generated output voltage waveform switches between $+V_{dc}$ and $-V_{dc}$ (2 levels) as can be seen from the generated output voltage waveform in Figure 3.15.



(a) (b) (c)

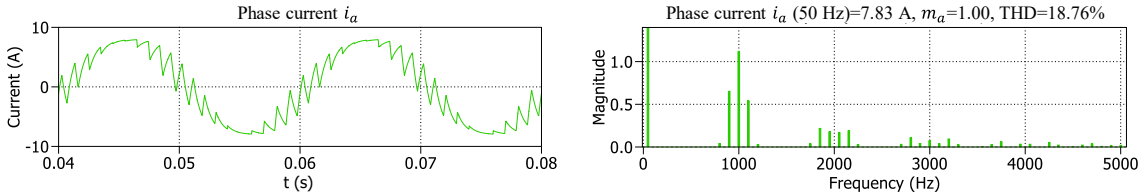
Figure 3.14: (a) Bipolar modulation with a single modulating wave and a single carrier wave (b) schematic (c) gate signals for the switches S1 and S3.



(a) (b) (c) (d)

Figure 3.15: Simulation results for bipolar modulation - leg voltage waveforms and their spectra at different modulation indices for a two-level H-bridge inverter (V_{dc} = 120 V, f_c = 1 kHz, f_{sd} = 1 kHz, f_{si} = 1 kHz).

The main problem with bipolar modulation is that the output voltage waveform is a two-level ($\pm V_{dc}$) square shaped waveform which causes a high $\frac{\mathrm{d}v}{\mathrm{d}t}$ stress on the load, which in the case of electric motors causes unwanted leakage currents through the insulation. Secondly, the harmonic spectrum of the waveform reveals a relatively high magnitude of the dominant harmonic which lies at the carrier frequency (f_c) as can be seen from the spectrum. The dominant harmonic magnitude becomes even greater than that of the fundamental at lower modulation indices as can be seen from Figure 3.15 where amplitude modulation index (m_a) has been reduced progressively in steps of 0.25. For bipolar modulation, harmonics are distributed at the carrier frequency (f_c) and its integer multiples and sidebands around these integer multiple frequencies. At a switching frequency of 1 kHz with an *RL*



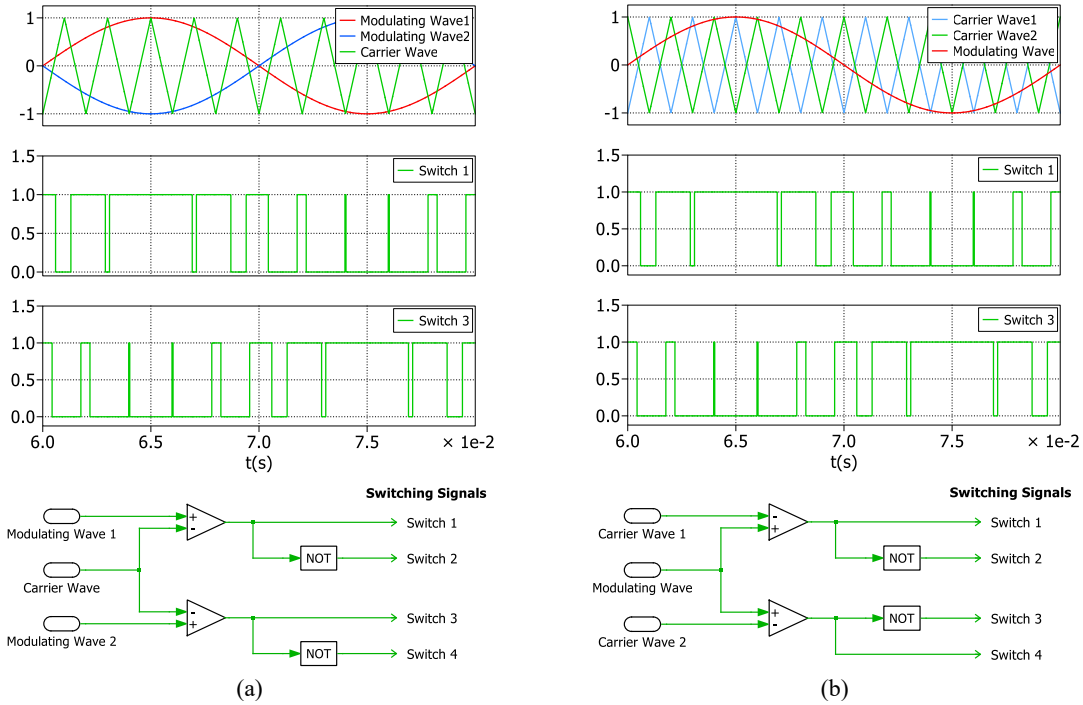
(a) (b)

Figure 3.16: Simulation results for bipolar modulation - phase current waveform and spectrum at unity modulation index for a two-level H-bridge inverter connected to a single-phase *RL* load (V_{dc} = 120 V, f_c = 1 kHz, f_{sd} = 1 kHz, f_{si} = 1 kHz).

load connected to a single H-bridge module under bipolar modulation, the total harmonic distortion at unity modulation index for the phase current is 18.76% (Figure 3.16).

3.4.2.2 Unipolar modulation

The presence of a dominant harmonic and its sidebands at carrier frequency (f_c) with bipolar modulation can be eradicated with unipolar modulation. In contrast to bipolar modulation, unipolar modulation needs two sinusoidal modulating waves which are 180° out-of-phase, one for each leg of the inverter. A common triangular carrier is compared with these two modulating waves to generate the gate signals for one switch in each leg of the H-bridge inverter (Figure 3.17a).



(a) (b)

Figure 3.17: Unipolar modulation: waveforms, switching signals, and schematic (a) two out-of-phase modulating waves with a single carrier wave (b) two out-of-phase carrier waves with a single modulating wave.

The output voltage waveform of the H-bridge inverter produces three voltage levels ($0, +V_{dc}$ and $-V_{dc}$) which reduces the $\frac{\mathrm{d}v}{\mathrm{d}t}$ stress on the load by half as compared to the two-level waveform produced with bipolar modulation. The output voltage waveform pulses step between zero and $+V_{dc}$ in the positive half of the fundamental frequency component and between zero and $-V_{dc}$ during the negative half of the fundamental frequency component (Figure 3.18). It should be noted that unipolar modulation scheme can alternatively be achieved by comparison of a single sinusoidal modulating wave with two $180°$ out-of-phase triangular carriers one for each leg of the inverter, to produce gate signals for the inverter switches (Figure 3.17b).

The frequency spectrum of the output voltage waveform under unipolar modulation can be seen in Figure 3.18. The dominant harmonic present at the carrier frequency (f_c) in the case of bipolar modulation and its sideband, have been eliminated under unipolar modulation. It can be observed from the spectra that the dominant harmonics are now present at $2f_c \pm f_m$, $2f_c \pm 3f_m$, $2f_c \pm 5f_m$ and so on, which were also present in the bipolar modulation method as the next significant harmonics. For unipolar modulation, harmonics are distributed at twice the carrier frequency ($2f_c$) and integer multiples and sidebands around these integer multiple frequencies.

At a switching frequency of 1 kHz with an RL load connected to the single H-bridge module under unipolar modulation, the total harmonic distortion at unity modulation index for the phase current is 5.05% which is significantly lower than that of the bipolar modulation (18.76%), as can be seen in Figure 3.19.

3.4.2.3 Multicarrier phase-shifted PWM

The multicarrier PS-PWM is well suited for a CHB converter. It is essentially an extension of the unipolar modulation method. As mentioned previously, unipolar modulation for a single H-bridge can be accomplished using two out-of-phase modulating waves compared with a single triangular carrier wave to produce gate signals for the switches in an H-bridge. Alternatively, a single modulating wave could be compared with two out-of-phase triangular carrier waves (one for each inverter leg) to generate identical gate signals. In a CHB, there are multiple H-bridge modules in series with each other, and each H-bridge inverter has two phase legs, positive and negative, two triangular carriers are required for each H-bridge. Therefore, for PS-PWM, the total number of triangular carriers required for

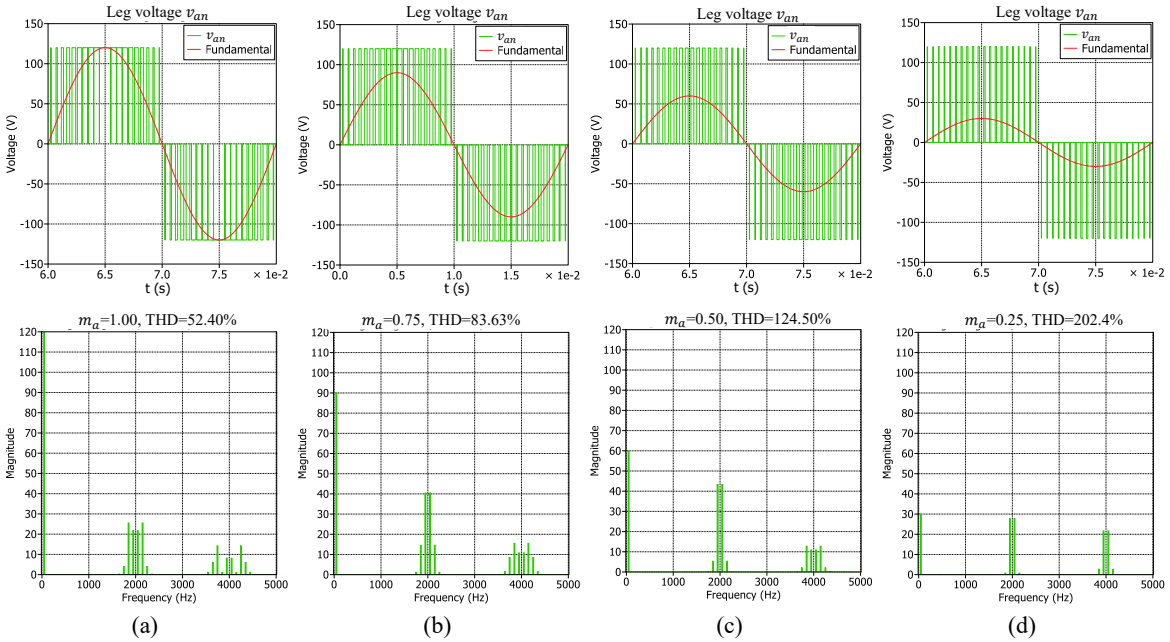


Figure 3.18: Simulation results for unipolar modulation - leg voltage waveforms and their spectra at different modulation indices for a two-level H-bridge inverter (V_{dc} = 120 V, f_c = 1 kHz, f_{sd} = 1 kHz, f_{si} = 2 kHz).

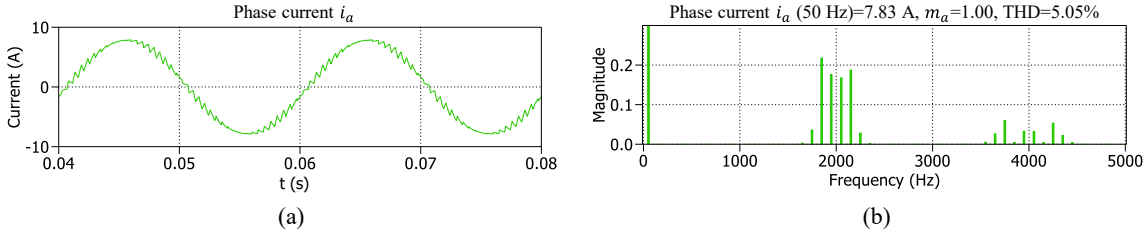


Figure 3.19: Simulation results for unipolar modulation - phase current waveform and spectrum at unity modulation index for a two-level H-bridge inverter connected to a single-phase *RL* load (V_{dc} = 120 V, f_c = 1 kHz, f_{sd} = 1 kHz, f_{si} = 2 kHz).

a CHB is $2k$. Half of the triangular carriers are for the positive phase leg of each H-bridge module and the other half for the negative phase leg of each H-bridge module, both halves being 180° out-of-phase with each other respectively. The phase shift between any two adjacent carriers can be described by:

$$\emptyset_{cr}^{\circ} = \frac{360°}{2k} \tag{3.23}$$

For example, a CHB with 4 H-bridge modules ($k = 4$) would require 8 triangular carriers with a phase shift of 45° between any two adjacent carriers, as shown in Figure 3.20a.

Four of these triangular carriers with a phase shift of 45° between them are compared with a common modulating wave to generate gate signals for the switches in the positive phase leg of each H-bridge module. The other four carriers, which are 180° out-of-phase with the

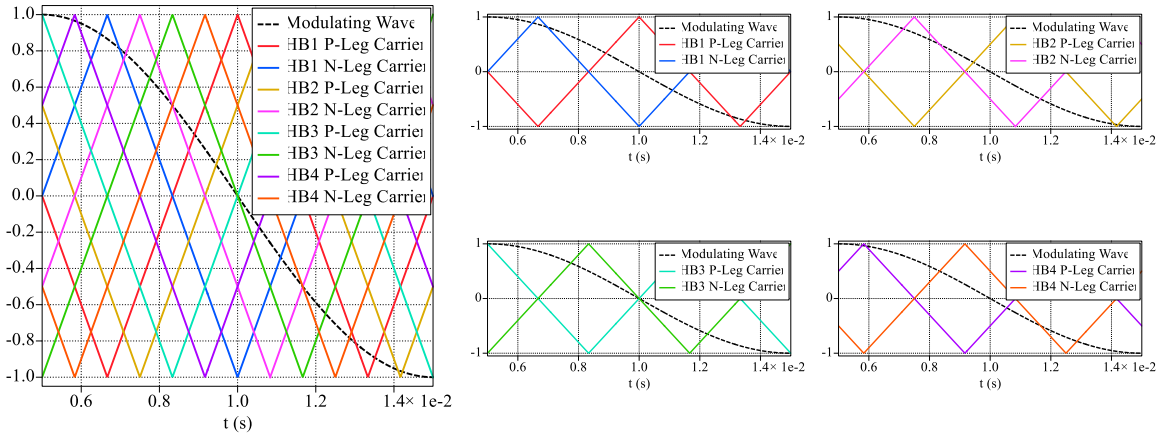


Figure 3.20: Multicarrier PS-PWM for a 9-level CHB-MLI – (a) modulating and carrier waveforms (b) waveforms for each cascaded H-bridge module.

first set, are compared with the same modulating wave to generate gate signals for switches in the negative phase leg of each H-bridge module. The pair of carrier waveforms used for the generation of gate signals for each H-bridge module to generate a 9-level waveform have been shown in Figure 3.20b.

Advantages of a multilevel waveform are lost when the modulation index drops below a certain point. These points vary depending on the type of reference waveform used. When a sinusoidal reference waveform is used (no offset injection), the leg voltage produced consists of only three levels (Figure 3.21a) for a 9-level CHB-MLI for $m_a \leq 0.25$. The number of output levels increases by two, as the modulation index is increased past certain modulation index values. For a 9-level CHB-MLI ($k = 4$) with no offset injection, these modulation index values are 0.25, 0.50, 0.75, and 1.00.

The simulation results of the leg voltage waveforms, with their respective spectra, generated by a CHB-MLI at modulation indices of 0.25, 0.50, 0.75, and 1.00 are shown in Figure 3.21. For $m_a > 0.75$, the output voltage waveform consists of all nine levels: $\pm 4V_{dc}, \pm 3V_{dc}, \pm 2V_{dc}, \pm V_{dc}$ and 0, as can be seen from the leg voltage waveform at unity modulation index in Figure 3.21a. Compared to a two-level waveform, a multilevel waveform imparts significantly lower $\frac{dv}{dt}$ stress on the load, which decreases proportionally with an increase in the number of levels. The output leg voltage waveform of the CHB-MLI is simply the sum of each H-bridge module output voltage as in (3.1). All H-bridges are utilised equally as the modulating wave is intersected by all the carrier waveforms. The only

difference between the output voltages of individual H-bridges is the phase shift between them.

At lower modulation indices, the decrease in the number of levels results in an increase in the total harmonic distortion of the output waveform, as can be seen in Figure 3.21b. Similarly, the phase current waveform spectra (Figure 3.22b) obtained for modulation indices of 0.25, 0.50, 0.75, and 1.00 also show an increase in the total harmonic distortion as the modulation index is reduced. However, phase current THD at $m_a = 0.25$ is still much better than that achievable with low frequency modulation methods such as SHE at unity modulation index. The dominant harmonics and their sidebands appear at the inverter switching frequency ($8f_c$) and its multiples.

The switching frequency of each semiconductor device (f_{sd}) can be calculated as the number of switching cycles per fundamental period times the fundamental frequency. The frequency of the carrier in a CHB inverter under multicarrier PS-PWM is always equal to that of the device switching frequency. Therefore, if a carrier frequency of 1 kHz is used, then the switching frequency of all the devices in the CHB will be 1 kHz. However, the switching frequency of the CHB-MLI (f_{si}) is $2k$ times that of the device switching frequency which is the dominant harmonic (position of the first sideband) in the inverter output voltage. This can be expressed as:

$$f_{sd} = f_c \tag{3.24}$$

$$f_{si} = 2kf_c \tag{3.25}$$

For a 9-level output voltage which is generated by 4 H-bridges in cascade, the switching frequency of the inverter would be $8f_c$ which is where the dominant harmonic of the inverter output voltage (and current) lies. This is beneficial because harmonics at smaller frequencies are eliminated when line-to-line voltages are considered in a three- or multi-phase load. Additionally, lower device switching frequencies are advantageous as switching losses are minimised.

The simulation results for the leg, line, and phase voltage, and phase current waveforms with their respective spectra can be seen in Figure 3.23 where multicarrier PS-PWM was implemented on a 9-level CHB-MLI on three-phase RL at unity modulation index. The carrier frequency was again chosen as 1 kHz, and as discussed earlier, the

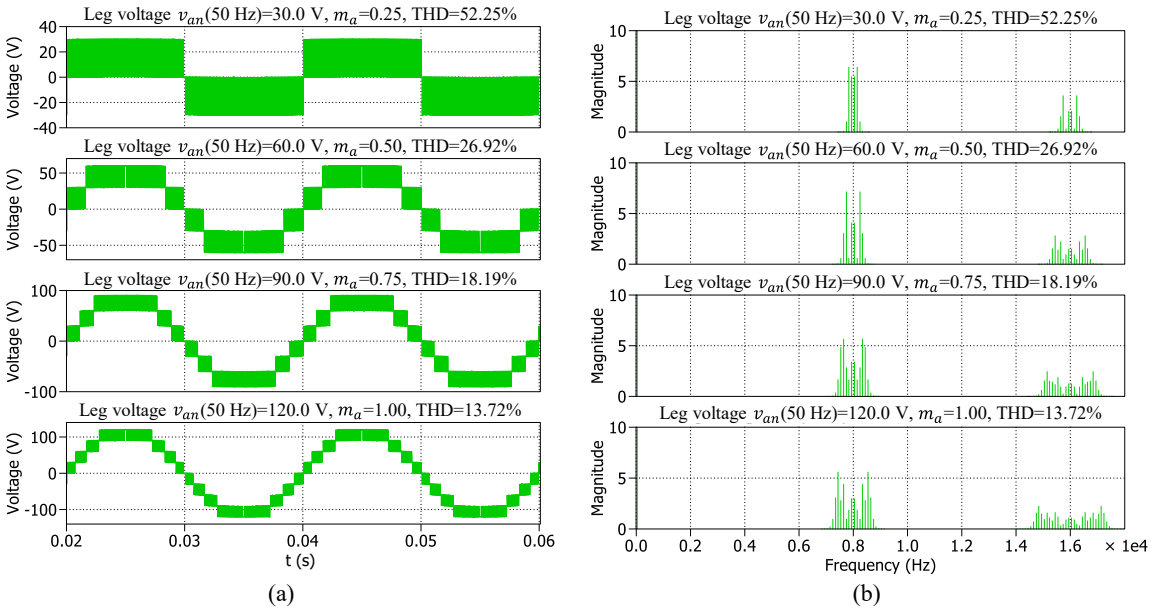


Figure 3.21: Simulation results for multicarrier PS-PWM implemented on a CHB-MLI connected to a single-phase *RL* load at different modulation indices (a) Leg voltage waveforms (b) associated spectra and THD ($f_c = 1$ kHz, $f_{sd} = 1$ kHz, $f_{si} = 8$ kHz).

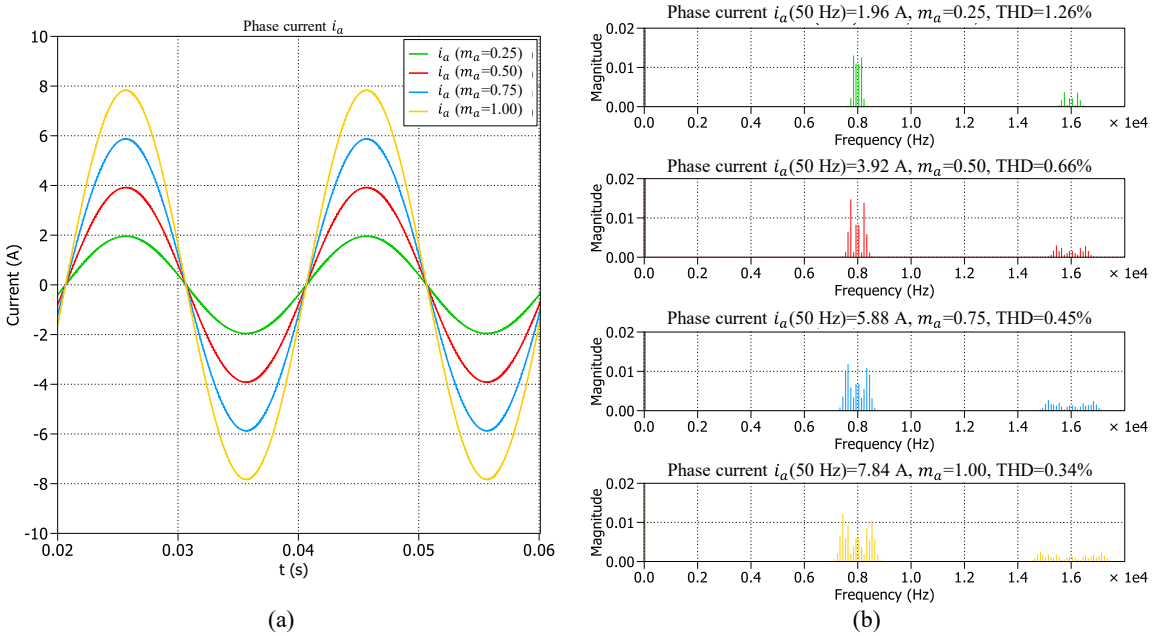


Figure 3.22: Simulation results for multicarrier PS-PWM implemented on a 9-level CHB-MLI connected to a single-phase *RL* load at different modulation indices (a) Phase current waveforms (b) associated spectra and THD ($f_c = 1$ kHz, $f_{sd} = 1$ kHz, $f_{si} = 8$ kHz).

CHB-MLI switching frequency (f_{si}) is eight times that of the carrier frequency (f_c). The line voltages lead the leg voltages by 30° electrical and the phase current lags the phase voltage as expected from an *RL* load. The phase current THD is only 0.31% at unity modulation index, which results in a very smooth current waveform. Triplen harmonics in the leg voltage are eliminated from the line and phase voltages and the THD is further reduced due to the

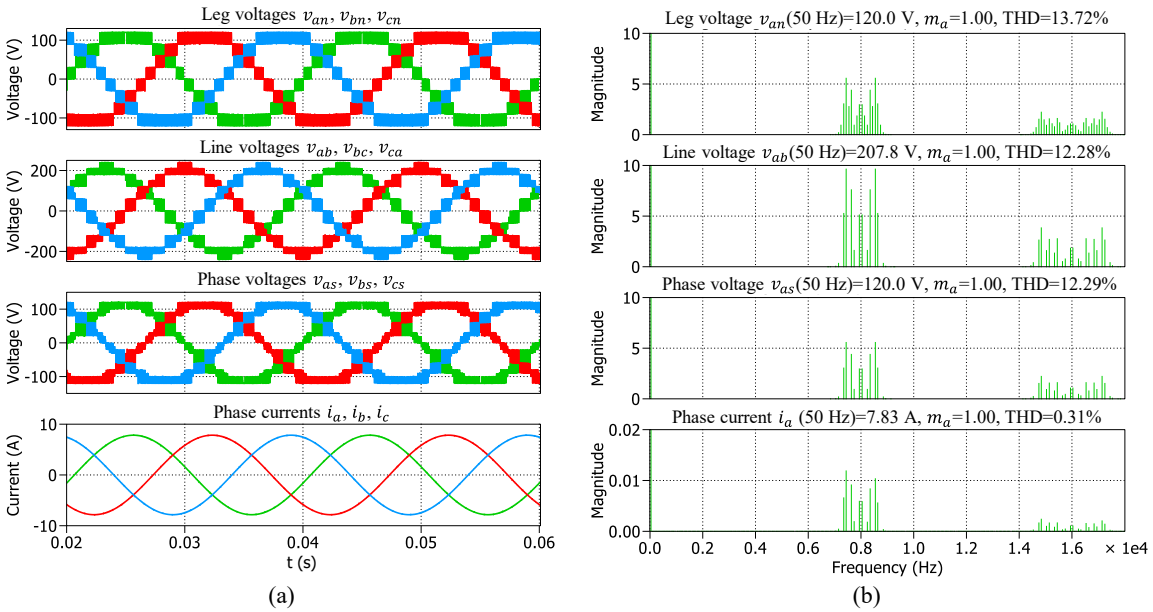


Figure 3.23: Simulation results for multicarrier PS-PWM implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index (a) Leg, line and phase voltages, and phase current waveforms (b) associated spectra and THD (f_c = 1 kHz, f_{sd} = 1 kHz, f_{si} = 8 kHz).

cancellation in a balanced three-phase system. In addition to the line and phase voltage harmonics, the phase current harmonics lie at $2kf_c \pm f_m$, $2kf_c \pm 5f_m$, $2kf_c \pm 7f_m$ and so on – while the triplen harmonics such as $2kf_c \pm 3f_m$, $2kf_c \pm 9f_m$, etc. do not exist as noted. The maximum harmonic magnitudes of the line and phase voltages, and phase currents occurs at $2kf_c \pm 11f_m$ [$v_{ab} = 9.6$ V, $v_{as} = 5.6$ V, $i_a = 10$ mA], the second largest harmonic at $2kf_c \pm 7f_m$ [$v_{ab} = 7.6$ V, $v_{as} = 4.4$ V, $i_a = 8$ mA], and the third largest harmonic at $2kf_c \pm 13f_m$ [$v_{ab} = 5.3$ V, $v_{as} = 3$ V, $i_a = 6$ mA]. Higher order harmonics at multiples of inverter switching frequency can be alleviated by filters and by high load impedances at higher frequencies in loads such as motors.

3.4.3 Multicarrier level-shifted PWM

LS-PWM is applicable for a CHB-MLI to generate the desired output voltage. Multicarrier LS-PWM schemes differ in the vertical disposition of the carrier waves and the phase relationship between adjacent carriers. The three possible LS-PWM schemes are the IPD, POD, and APOD, with the carrier arrangement for each shown in Figure 3.24.

The number of triangular carrier waveforms required for the multicarrier LS modulation is the same as that for the PS modulation, as two carrier waveforms of the same amplitude and frequency are required for each H-bridge. Therefore, the total number of

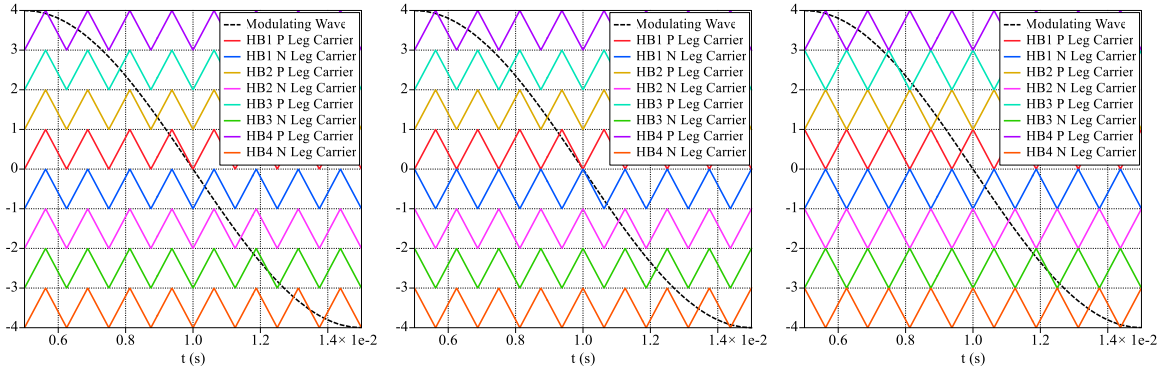


Figure 3.24: Multicarrier LS-PWM – modulating and carrier waveforms for a 9-level CHB-MLI (a) IPD-PWM (b) POD-PWM (c) APOD-PWM.

triangular carriers required for a CHB is $2k$, which equals $(l-1)$, with l being the number of levels of the output waveform. For each of the LS modulation methods, the amplitude modulation index is defined as:

$$m_a = \frac{A_m}{2kA_c} = \frac{A_m}{(l-1)A_c} \tag{3.26}$$

where A_m is the amplitude of the modulating wave and A_c is the amplitude of each carrier wave. For a 9-level waveform at unity modulation index, the amplitude of the modulating wave and that of the carrier waveform would be 4 and 0.5 respectively.

3.4.3.1 In-phase disposition (IPD)

Level-shifting of multiple carrier waveforms such that each carrier wave is in-phase with each other is known as IPD-PWM. Gate signals are required for switching devices in the positive and negative legs of each H-bridge in a cascaded H-bridge configuration. Therefore, two carrier waves - one for each leg of an H-bridge module - are compared with a modulating wave to produce the gate signals for devices in each H-bridge module. Vertical carrier wave disposition and the generated gating signals are shown in Figure 3.25 for each H-bridge module. Gating signals are only shown for the top switches (S1 and S3 in Figure 3.1) since bottom switches operate in a complementary manner to the top switches in each leg of an H-bridge module.

It can be observed that conduction time for the switches in each H-bridge module is different from each other which has implications in terms of the amount of power supplied by the dc source of each H-bridge module. It can also be observed that switches in different

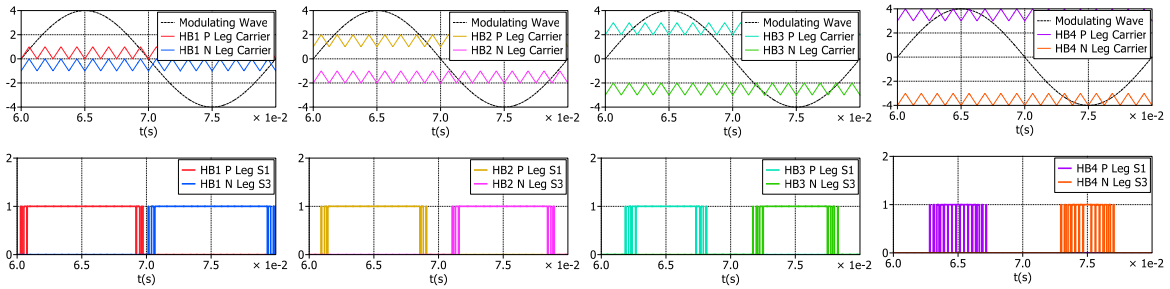


Figure 3.25: IPD-PWM for a 9-level CHB-MLI – modulating and carrier waveforms for each cascaded H-bridge module and respective switching signals.

H-bridge modules operate at different switching frequencies, in contrast to PS-PWM where the carrier frequency equals the device switching frequency for all H-bridge modules. The following relation holds for the average switching frequency of devices for all LS-PWM schemes for a 9-level CHB-MLI for a modulation index range of $0.75 < m_a \leq 1.00$:

$$f_{sd,HB1} < f_{sd,HB2} < f_{sd,HB3} < f_{sd,HB4} \tag{3.27}$$

where f_{sd} is device switching frequency. Similarly, device conduction times (t_{cd}) also follow the relationship:

$$t_{cd,HB1} > t_{cd,HB2} > t_{cd,HB3} > t_{cd,HB4} \tag{3.28}$$

For sinusoidal references, the switching frequency of devices in HB4 ($f_{sd,HB4}$) drops to zero (no conduction), i.e., the devices in HB4 are not utilised for $m_a \leq 0.75$. Switching devices in HB3 stop conducting for $m_a \leq 0.50$ until $m_a \leq 0.25$ when switching devices only in HB1 are utilised to generate the output voltage waveform, while all other H-bridge modules are not used. The issue of unequal device switching frequency and different conduction times for different H-bridges is discussed further in section 3.5.

The switching frequency for LS-PWM schemes equals the carrier frequency ($f_{si} = f_c$) while the switching devices in a CHB switch on average at a switching frequency of:

$$f_{sd,avg} = \frac{f_c}{l-1} = \frac{f_c}{2k} \tag{3.29}$$

The IPD-PWM scheme was implemented on a single-phase 9-level CHB-MLI connected to an RL load to obtain inverter leg voltage (Figure 3.26) and phase current waveforms (Figure 3.27) and their respective spectra at modulation indices of 0.25, 0.50,

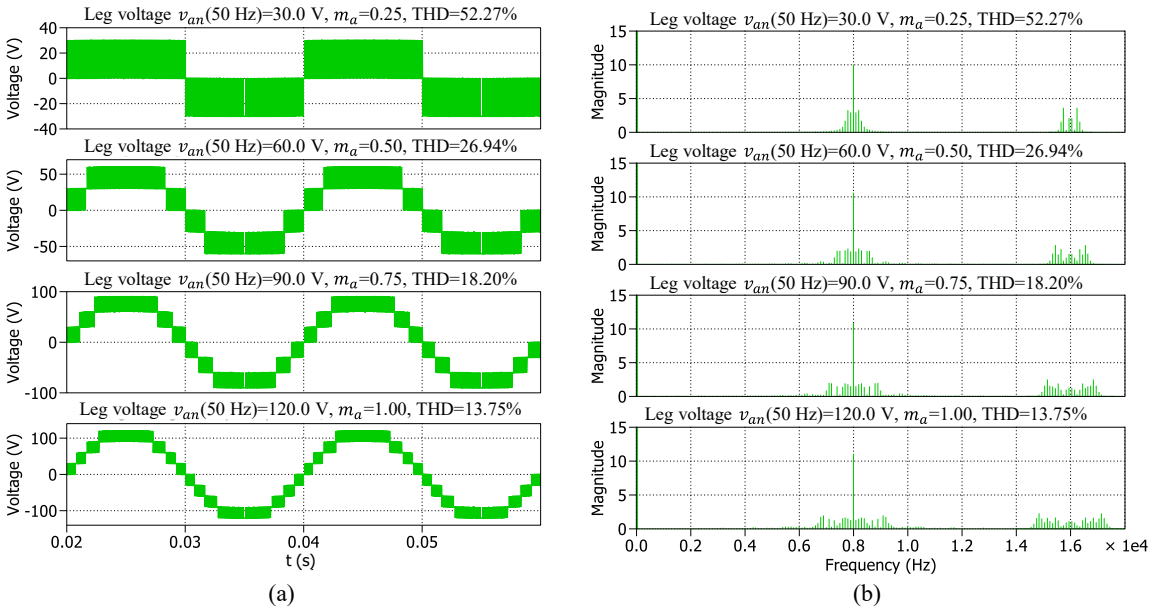


Figure 3.26: Simulation results for IPD-PWM implemented on a 9-level CHB-MLI connected to a single-phase *RL* load at different modulation indices (a) Leg voltage waveforms (b) associated spectra and THD (f_c = 8 kHz, $f_{sd,avg}$ = 1 kHz, f_{si} = 8 kHz).

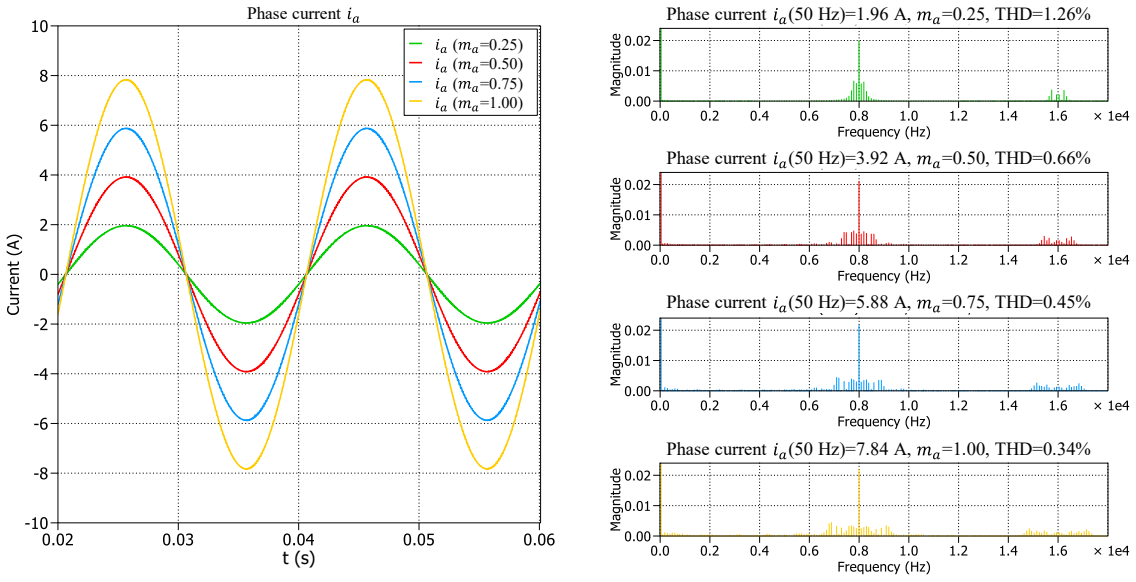


Figure 3.27: Simulation results for IPD-PWM implemented on a 9-level CHB-MLI connected to a single-phase *RL* load at different modulation indices (a) Phase current waveforms (b) associated spectra and THD (f_c = 8 kHz, $f_{sd,avg}$ = 1 kHz, f_{si} = 8 kHz).

0.75, and 1.00. The carrier switching frequency (f_c) is chosen such that the switching frequency of the CHB-MLI (f_{si}) under PS-PWM and IPD-PWM are equal for a fair comparison between the two modulation methods. Consequently, the simulations were conducted at the carrier frequency f_c = 8 kHz which gives an average device switching frequency ($f_{sd,avg}$) of 1 kHz for the level-shifted PWM schemes.

The leg voltage waveforms produced with IPD-PWM are very similar to those produced by PS-PWM (Figure 3.21) and the number of waveform levels (l) drops by two when the modulation index drops below 0.75, 0.50, and 0.25. The THD figures for the leg voltage at modulation indices of 0.25, 0.50, 0.75, and 1.00 are very similar to those obtained with the PS-PWM. At the same modulation indices, the spectral peaks of 9.89 V, 10.54 V, 10.83 V, 11.00 V lie at inverter switching frequency of 8 kHz. The next set of harmonics lie at twice the inverter switching frequency as expected. The difference between the phase- and level-shifted modulation methods is in the distribution of the harmonic content in the sidebands.

The IPD-PWM distributes the harmonic sidebands over a wider bandwidth but with a large harmonic at the carrier frequency. In contrast, the harmonic content is distributed over a narrower bandwidth but with several higher magnitude peaks for PS-PWM. For example, phase current carrier frequency harmonic amplitude is around 0.02 A for IPD-PWM at unity modulation index whereas several sideband harmonics of around 0.01 A magnitude are present for PS-PWM. Lower order harmonics of minimal magnitude (~1 mA) do appear near the fundamental phase current harmonic, which are negligible. For IPD-PWM, the dominant harmonic lies at carrier frequency f_c and the distribution of the sidebands occur at $f_c \pm 2f_m$, $f_c \pm 4f_m$, $f_c \pm 6f_m$ and so on.

The three-phase implementation of IPD-PWM at unity modulation index (Figure 3.28) shows a very similar THD value of the leg voltage as that obtained with PS-PWM. However, the line and phase voltage THD values are 4% lower for the IPD-PWM in comparison with PS-PWM. Similarly, phase current THD is reduced by half from 0.31% to 0.15% at unity modulation index. Magnitudes of the line and phase voltage harmonics as well as those of phase current around the carrier frequency are extremely low with harmonic frequencies lying at $f_c \pm 2f_m$, $f_c \pm 4f_m$, and so on - except for even triples such as $f_c \pm 6f_m$, $f_c \pm 12f_m$, etc., being absent from the spectra. The maximum harmonic magnitudes of the line and phase voltages, and phase currents occur at $f_c \pm 22f_m$ [$v_{ab} = 3.3$ V, $v_{as} = 1.9$ V, $i_a = 3$ mA], the second largest harmonic at $f_c \pm 8f_m$ [$v_{ab} = 2.6$ V, $v_{as} = 1.5$ V, $i_a = 2.8$ mA], and the third largest harmonic at $f_c \pm 4f_m$ [$v_{ab} = 2.5$ V, $v_{as} = 1.4$ V, $i_a = 2.7$ mA].

3.4.3.2 Phase opposition disposition (POD)

POD-PWM requires multiple carrier waveforms where the carrier waveforms that are above zero are in-phase with each other but are 180° out-of-phase with the ones below zero.

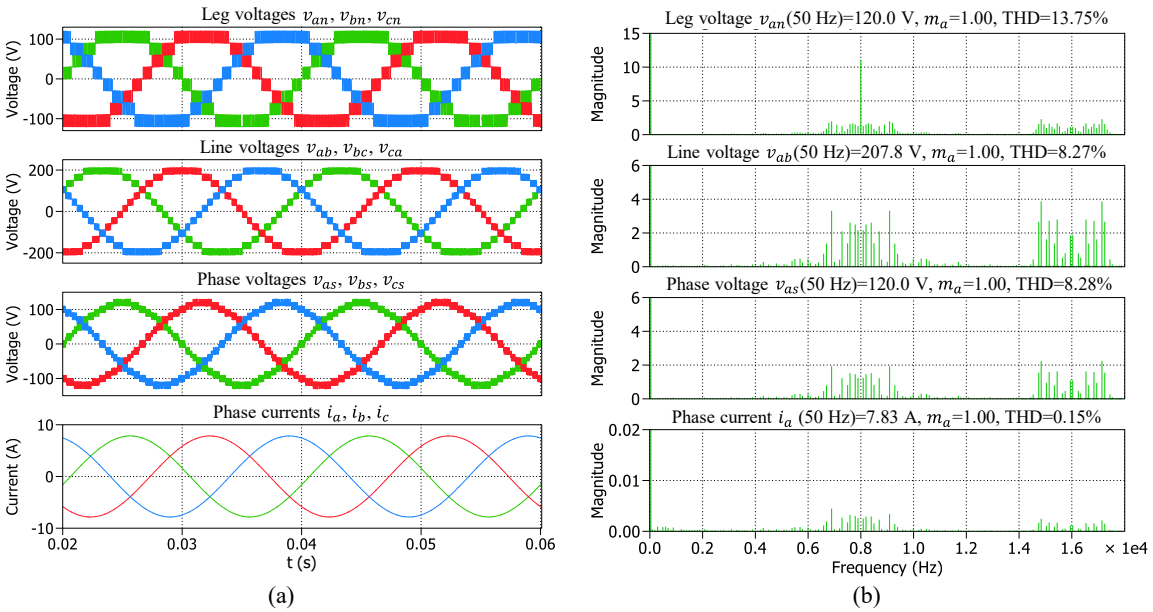


Figure 3.28: Simulation results for IPD-PWM implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index (a) Leg, line and phase voltage, and phase current waveforms (b) associated spectra and THD (f_c = 8 kHz, $f_{sd,avg}$ = 1 kHz, f_{si} = 8 kHz).

Consequently, the carrier waveforms that generate the gate signals for the positive legs are in phase opposition with those of the negative legs of each H-bridge. The carrier waveform along with the modulating wave can be seen in the Figure 3.29.

Simulated leg voltage waveforms (Figure 3.30) and phase current waveforms (Figure 3.31) and respective spectra were obtained for POD-PWM implemented on single-phase 9-level CHB-MLI connected to an *RL* load at modulation indices of 0.25, 0.50, 0.75, and 1.00.

A carrier frequency of 8 kHz was used to ensure the average device switching frequency is equal to that achieved by PS-PWM and IPD-PWM for comparison. The leg voltage THD is again very similar to that obtained with PS-PWM and IPD-PWM for the chosen modulation indices. The device conduction times and switching frequencies are not

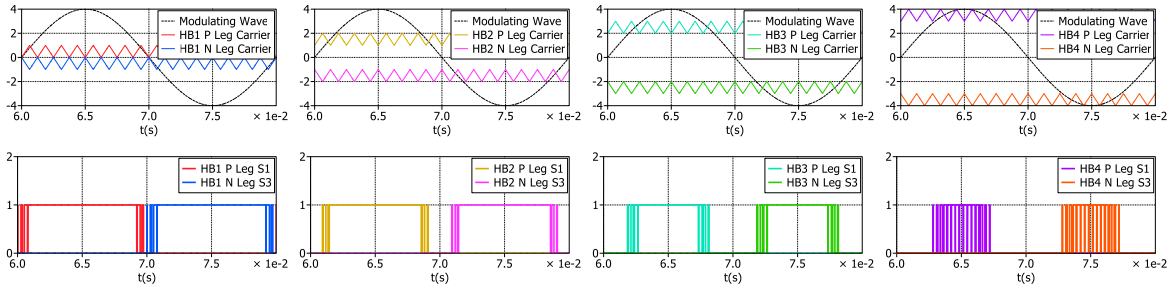


Figure 3.29: POD-PWM for a 9-level CHB-MLI – modulating and carrier waveforms for each CHB module and respective switching signals.

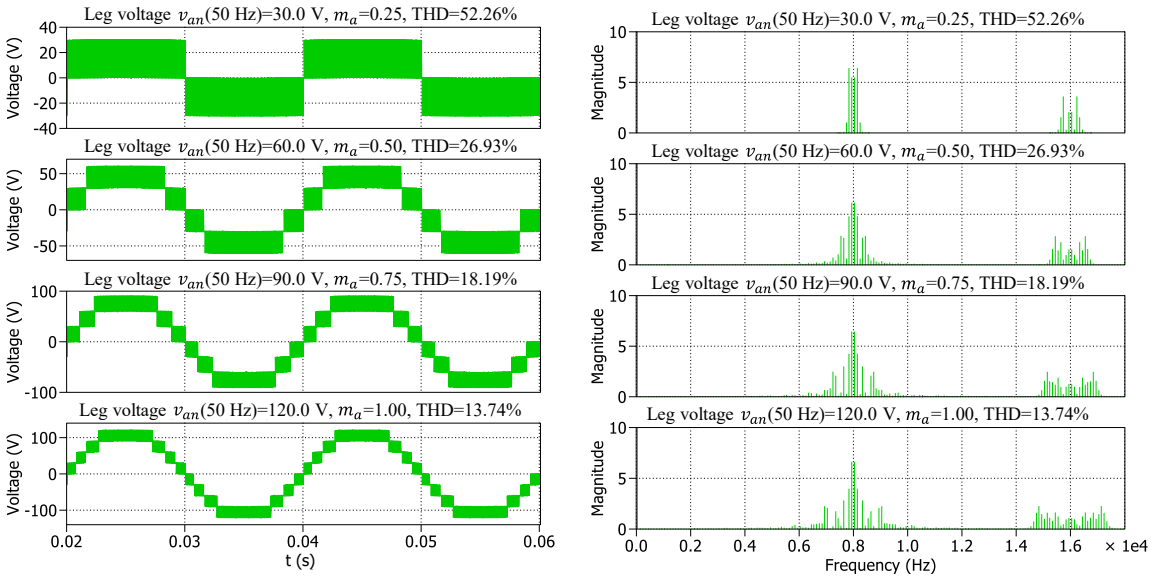


Figure 3.30: Simulation results for POD-PWM implemented on a 9-level CHB-MLI connected to a single-phase *RL* load at different modulation indices (a) Leg voltage waveforms (b) associated spectra and THD (f_c = 8 kHz, $f_{sd,avg}$ = 1 kHz, f_{si} = 8 kHz).

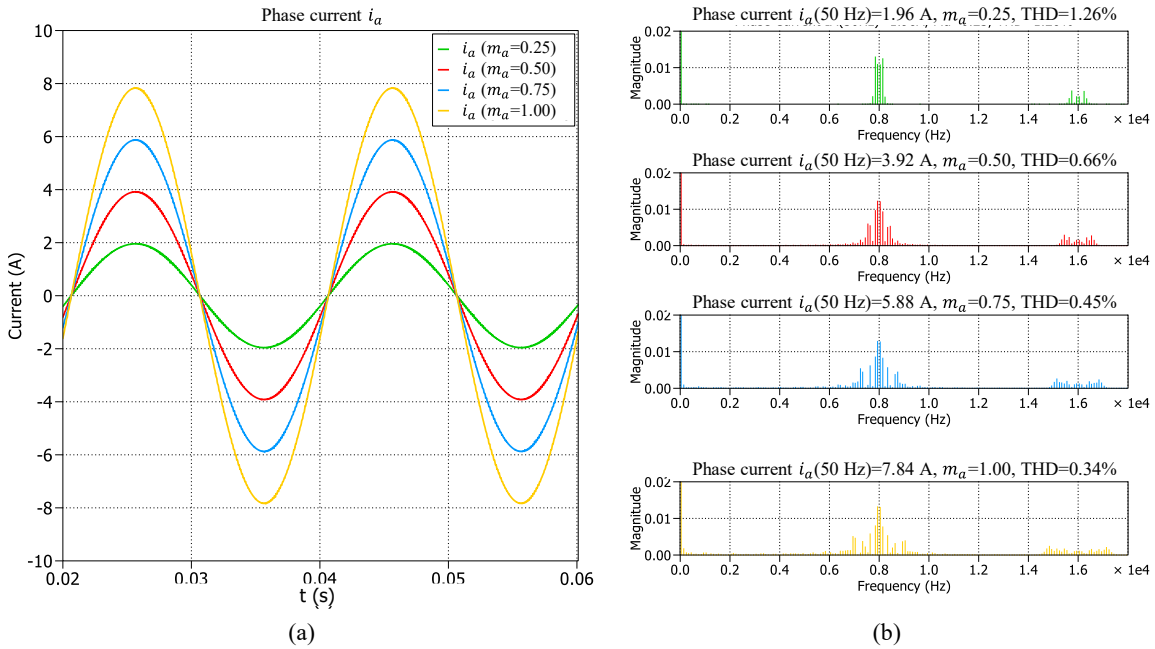


Figure 3.31: Simulation results for POD-PWM implemented on a 9-level CHB-MLI connected to a single-phase *RL* load at different modulation indices (a) Phase current waveforms (b) associated spectra and THD (f_c = 8 kHz, $f_{sd,avg}$ = 1 kHz, f_{si} = 8 kHz).

the same for all H-bridge modules as was the case with IPD-PWM. In contrast to IPD-PWM, the leg voltage and phase current spectra under POD-PWM reveal harmonics at $f_c \pm f_m$, $f_c \pm 3f_m$ and so on.

Implementation of POD-PWM at unity modulation index on a three-phase CHB-MLI connected to a star-connected *RL* load (Figure 3.32) shows a comparable THD value of the

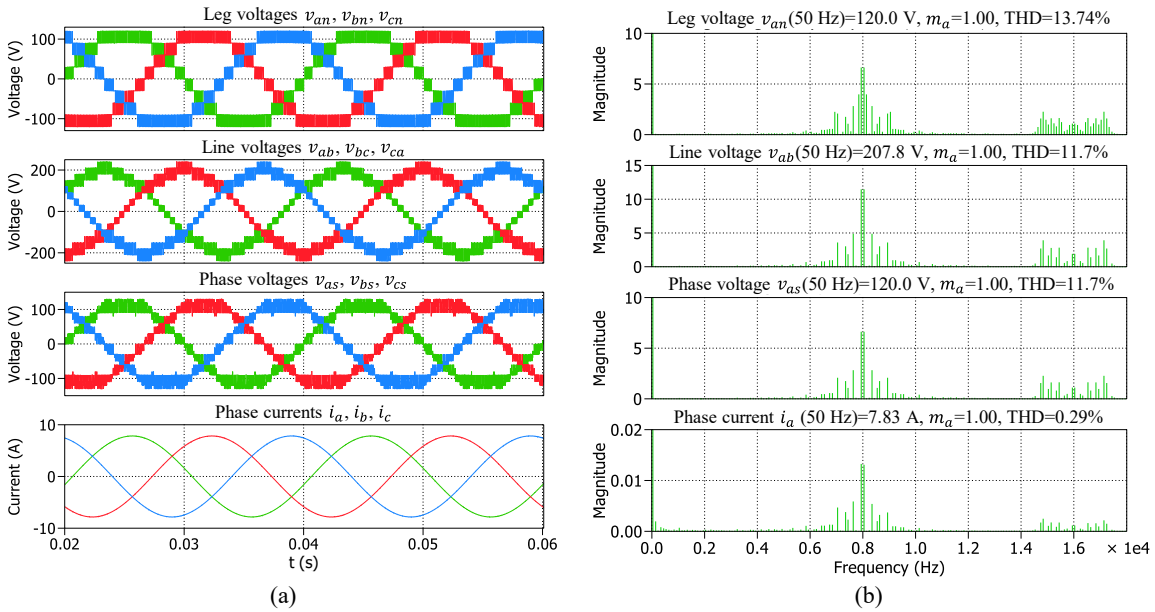


Figure 3.32: Simulation results for POD-PWM implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index (a) Leg, line and phase voltage, and phase current waveforms (b) associated spectra and THD (f_c = 8 kHz, $f_{sd,avg}$ = 1 kHz, f_{si} = 8 kHz).

leg voltage as that obtained with IPD-PWM and PS-PWM. However, the line and phase voltage THD values are 3.4% more than that obtained with IPD-PWM and 0.6% smaller than those obtained with PS-PWM. Likewise, phase current THD is almost the same as that obtained with PS-PWM at 0.29% which is almost double that of the 0.15% achieved by IPD-PWM at unity modulation index.

Line and phase voltage harmonics as well as those of the phase current lie at $f_c \pm f_m$, $f_c \pm 5f_m$, $f_c \pm 7f_m$ and so on – except for triples such as $f_c \pm 3f_m$, $f_c \pm 9f_m$, etc., being absent from the spectra. The maximum harmonic magnitudes of the line and phase voltages, and phase currents occur at $f_c \pm f_m$ [$v_{ab} = 11.4$ V, $v_{as} = 6.6$ V, $i_a = 13$ mA], the second largest harmonic at $f_c \pm 7f_m$ [$v_{ab} = 4.8$ V, $v_{as} = 2.8$ V, $i_a = 5$ mA], and the third largest harmonic at $f_c \pm 19f_m$ [$v_{ab} = 3.5$ V, $v_{as} = 2$ V, $i_a = 3$ mA].

3.4.3.3 Alternate phase opposition disposition (APOD)

In contrast to the carrier waveforms in the POD-PWM, adjacent carrier waves are phase-shifted by 180° and can be said to be alternatively in phase opposition. The process of APOD-PWM is shown in Figure 3.33 with the gate signals for the top switches being shown for each leg of all H-bridge modules in a 9-level CHB-MLI.

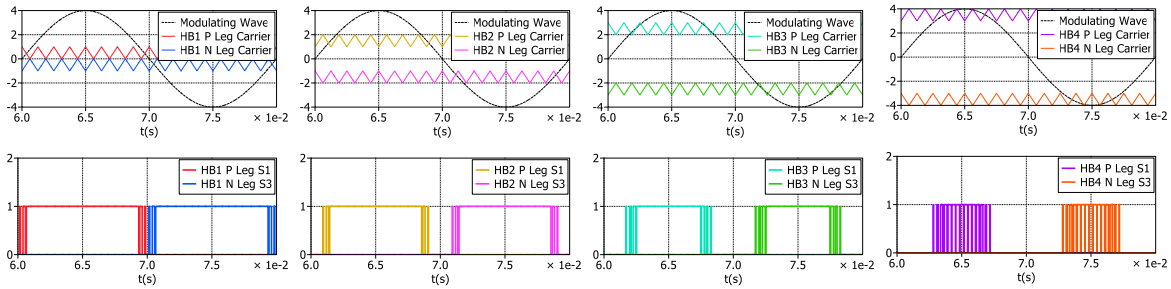


Figure 3.33: APOD-PWM for a 9-level CHB-MLI – Modulating and carrier waveforms for each CHB module and respective switching signals.

The APOD-PWM scheme was implemented on a single-phase 9-level CHB-MLI connected to an RL load to obtain inverter leg voltage (Figure 3.34) and phase current waveforms (Figure 3.35) and their respective spectra for modulation indices of 0.25, 0.50, 0.75, 1.00 at a carrier frequency of 8 kHz to ensure consistency. The THD of the leg voltage and the phase current waveforms at the chosen modulation indices are quite similar to those obtained with PS-PWM, IPD-PWM, and POD-PWM. The leg voltage and phase current spectra under APOD-PWM show a harmonic distribution like that of POD-PWM at $f_c \pm f_m$, $f_c \pm 3f_m$, $f_c \pm 5f_m$ and so on. The switching frequencies of devices and the conduction times vary from one H-bridge to the next as is the case for all level-shifted modulation strategies discussed.

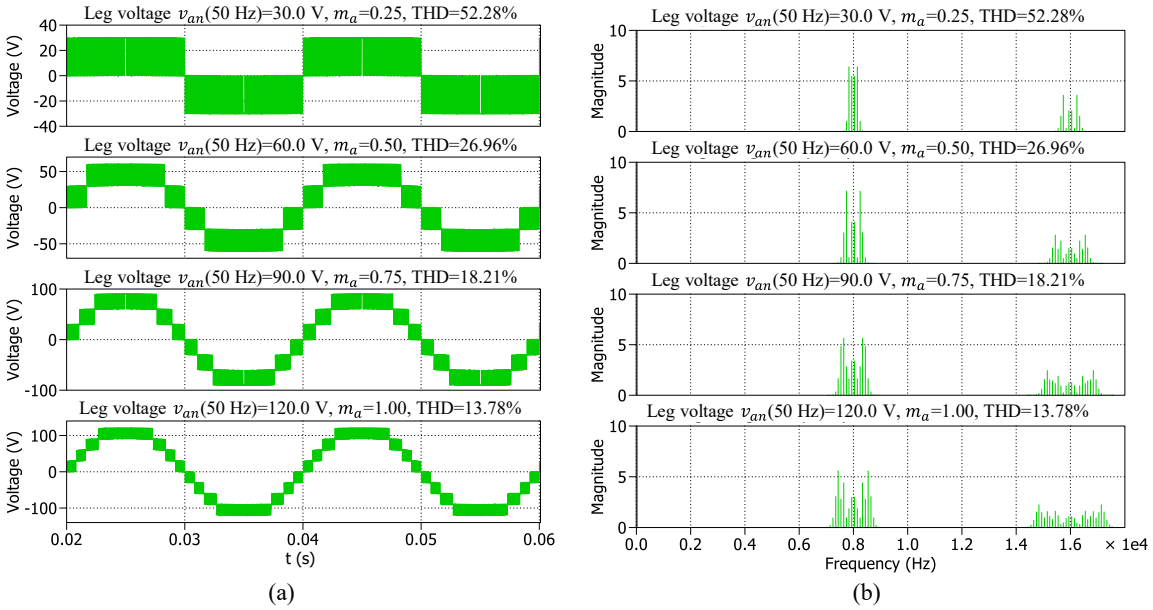
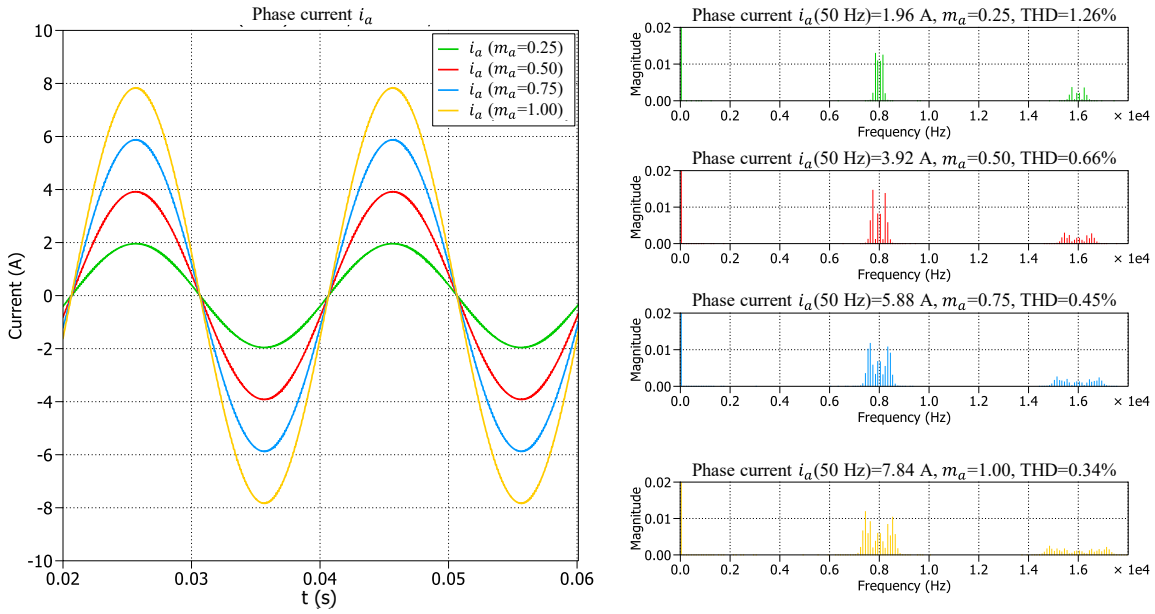


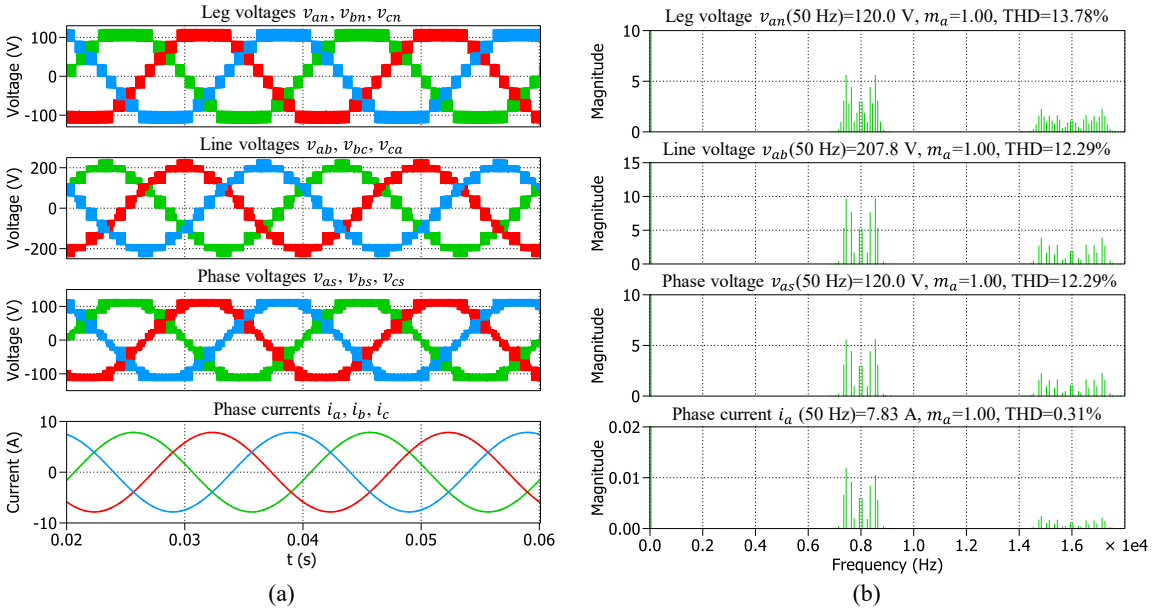
Figure 3.34: Simulation results for APOD-PWM implemented on a 9-level CHB-MLI connected to a single-phase RL load at different modulation indices (a) Leg voltage waveforms (b) associated spectra and THD ($f_c = 8$ kHz, $f_{sd,avg} = 1$ kHz, $f_{si} = 8$ kHz).



(a) (b)

Figure 3.35: Simulation results for APOD-PWM implemented on a 9-level CHB-MLI connected to a single-phase RL load at different modulation indices (a) Phase current waveforms (b) associated spectra and THD ($f_c = 8$ kHz, $M_f = 160$, $f_{sd,avg} = 1$ kHz, $f_{si} = 8$ kHz).

APOD-PWM was applied at unity modulation index on a three-phase CHB-MLI connected to a star-connected RL load (Figure 3.36). It shows very similar THD value of the leg voltage as that obtained with the PS-PWM scheme. The obtained THD values for the line and phase voltage as well as the phase current are very similar to those obtained under PS-PWM. It makes intuitive sense that PS-PWM and APOD-PWM are analogous because



(a) (b)

Figure 3.36: Simulation results for APOD-PWM implemented on a 9-level CHB-MLI connected to a three-phase RL load at unity modulation index (a) Leg, line and phase voltage, and phase current waveforms (b) associated spectra and THD ($f_c = 8$ kHz, $f_{sd,avg} = 1$ kHz, $f_{si} = 8$ kHz).

of the high resemblance between the carrier waveforms for the two schemes. Expectedly, like the PS-PWM, line and phase voltage harmonics, together with the phase current harmonics for APOD-PWM lie at $f_c \pm f_m$, $f_c \pm 5f_m$, $f_c \pm 7f_m$ and so on – while the triples such as $f_c \pm 3f_m$, $f_c \pm 9f_m$, etc. are zero. The maximum harmonic magnitudes of the line and phase voltages, and phase currents occur at $f_c \pm 11f_m$ [$v_{ab} = 9.6$ V, $v_{as} = 5.6$ V, $i_a = 10$ mA], the second largest harmonic at $f_c \pm 7f_m$ [$v_{ab} = 7.6$ V, $v_{as} = 4.4$ V, $i_a = 8$ mA], and the third largest harmonic at $f_c \pm 13f_m$ [$v_{ab} = 5.3$ V, $v_{as} = 3$ V, $i_a = 6$ mA] – all of which match the values obtained with PS-PWM.

3.4.4 Comparison between multicarrier modulation schemes

At this point, it is appropriate to consider the performance of multicarrier modulation schemes in terms of the THD of the leg, line, and phase voltage and phase current waveforms at different operating points. This was achieved via simulation through the implementation of PS-PWM, IPD-PWM, POD-PWM, and APOD-PWM on a three-phase star-connected *RL* load fed by a 9-level CHB-MLI for entire linear modulation index range from 0.01 to 1.00 in steps of 0.01.

The leg (v_{an}), line (v_{ab}), and phase (v_{as}) voltages and phase 'a' current (i_a) THD profiles are plotted in Figure 3.37 for each of the multicarrier PWM schemes for the entire

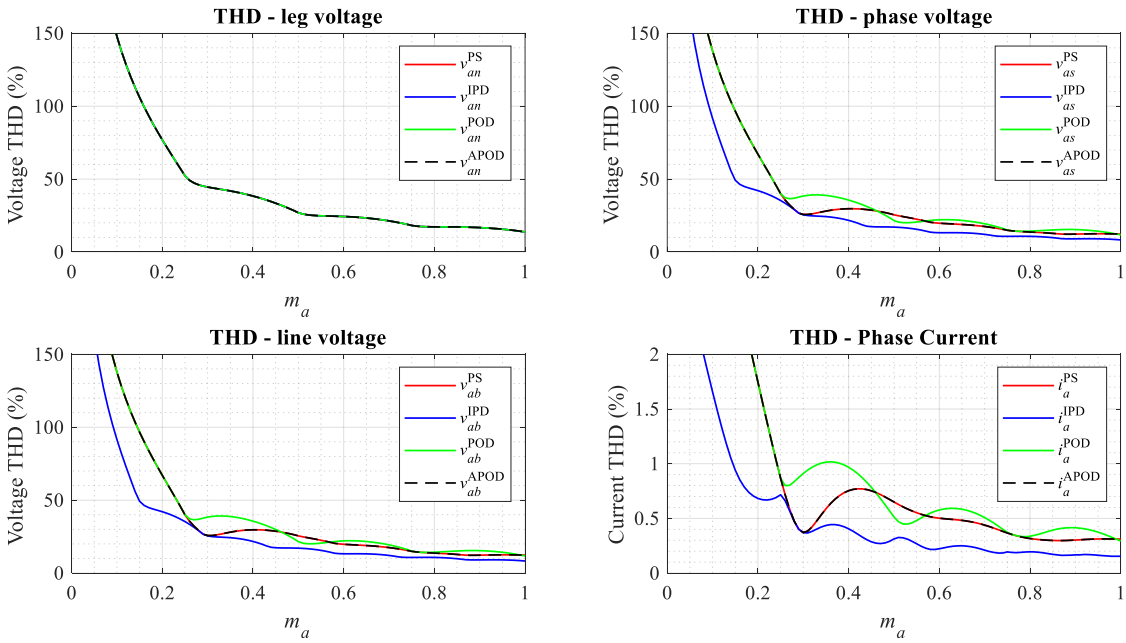


Figure 3.37: THD comparison between PS, IPD, POD, and APOD-PWM modulation methods for leg voltage, line voltage, phase voltage and phase current for the entire modulation index range ($f_{si} = 8$ kHz).

linear modulation index range. It was previously mentioned that PS-PWM and APOD-PWM were similar to each other in terms of the harmonic distortion of the waveforms as well as the location of the harmonics on the specturm at unity modulation index. Hence, it is not surprising to see that PS-PWM and APOD-PWM produce overlapping THD plots for each of the considered variables. It is interesting to note that the leg voltage (v_{an}) THD plots for all modulation methods overlap each other, i.e., they have a similar harmonic distortion profile. On the other hand, the line (v_{ab}) and phase (v_{as}) harmonic distortion plots are very similar to each other, as expected.

It is evident that IPD-PWM produces the best THD profile of the line and phase voltages, and the phase current over the entire modulation index range. The difference is more pronounced at lower modulation indices and especially for the phase current where the THD for IPD-PWM generally remains at half of that produced by other modulation schemes. POD-PWM produces the highest overall THD through the modulation index range for line and phase voltages and phase current. For $m_a < 0.25$, the THD profiles of PS-PWM, POD-PWM, and APOD-PWM overlap. PS-PWM and APOD-PWM perform better, in terms of lower THD, than POD-PWM for most of the modulation index range.

For the best performing IPD-PWM scheme, the THD of v_{an}^{IPD} stays below 50% when for $m_a > 0.25$. Similarly, the THD for the v_{ab}^{IPD} and v_{as}^{IPD} stay below 50% and the i_a^{IPD} stays below 1% for $m_a > 0.15$. Naturally, the THD is the lowest at unity modulation index and increases slowly with a decrease in the modulation index for all voltage and current THD plots. However, the greatest rate of change of the THD occurs for $m_a < 0.25$ when the benefits of the multilevel waveform are lost as a three-level waveform is produced at the inverter output. Further reduction in the modulation index sees significantly higher THD values. This point can be shifted further to the left with the use of a greater number of H-bridge modules per leg which will lead to even better THD profiles.

The effect of variation in carrier frequency on phase current THD for IPD-PWM for the linear modulation index range can be seen in Figure 3.38. A reduction in current THD is seen with an increase in the carrier frequency. For a carrier frequency of 16 kHz, the average device switching frequency ($f_{sd,avg}$) for a 9-level CHB-MLI is 2 kHz which would mean a phase current THD of less than 1% at $m_a = 0.1$. Though, the law of diminishing returns holds sway as the first doubling of the carrier frequency produces a significantly larger reduction in current THD compared to the next doubling where a lower benefit is attained.

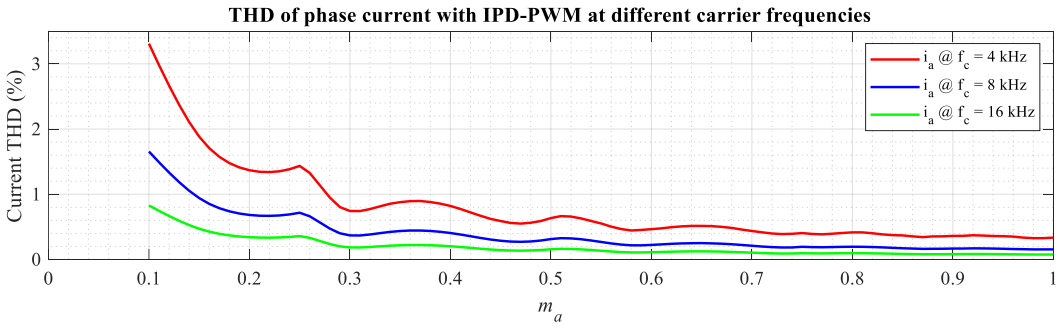


Figure 3.38: IPD-PWM - THD for phase current at different carrier frequencies.

However, as an increase in the carrier switching frequency produces higher switching losses in an inverter, it is best to utilise a switching frequency that meets the required performance specification though analysis and optimisation.

3.5 Power distribution and equalisation

3.5.1 DC source utilisation in PS- and LS-PWM

The advantage of the multicarrier PS-PWM is the equal utilisation of dc sources. This can be observed from the voltage pulse contribution of each H-bridge (Figure 3.39a) of the CHB to the synthesis of the inverter output leg voltage. It can also be noticed from the corresponding dc current contribution of each of the input dc sources connected to these H-bridge modules (Figure 3.39b). The contribution of each H-bridge is always equal, for all modulation indices.

The primary issue with LS-PWM is the unequal utilisation of the dc sources which occurs regardless of the chosen LS-PWM scheme. In the case of IPD-PWM, the switching frequency of the CHB inverter is the same as that of the frequency of the carrier wave. However, since carriers are distributed vertically at different voltage levels, switching devices in each H-bridge operate at different frequencies and with different device conduction times. This leads to an uneven distribution of switching and conduction losses between different H-bridge modules.

Figure 3.40a shows the individual H-bridge voltages and synthesised pole/leg voltages for a 4-module CHB under IPD-PWM. Disproportionate power distribution between different H-bridge modules can be observed where individual H-bridge voltage waveforms are shown. In the case of a CHB-MLI where multiple batteries are used as dc sources, it

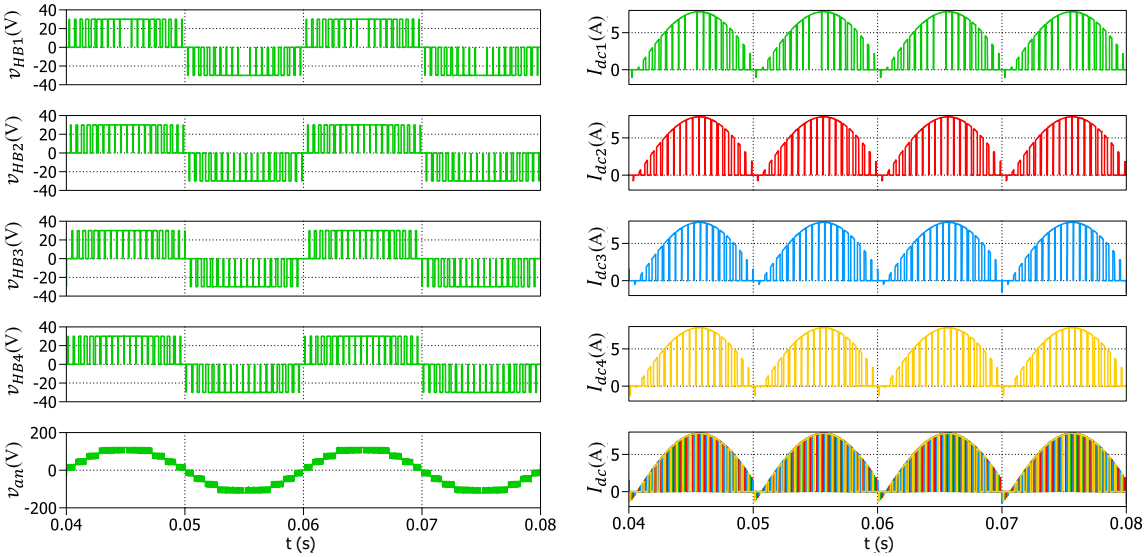


Figure 3.39: Simulation results for PS-PWM implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index - Inverter phase leg A (a) individual H-bridge output voltages and inverter leg voltage (b) dc current waveforms of corresponding dc sources and overall dc current profile (f_{si} = 8 kHz).

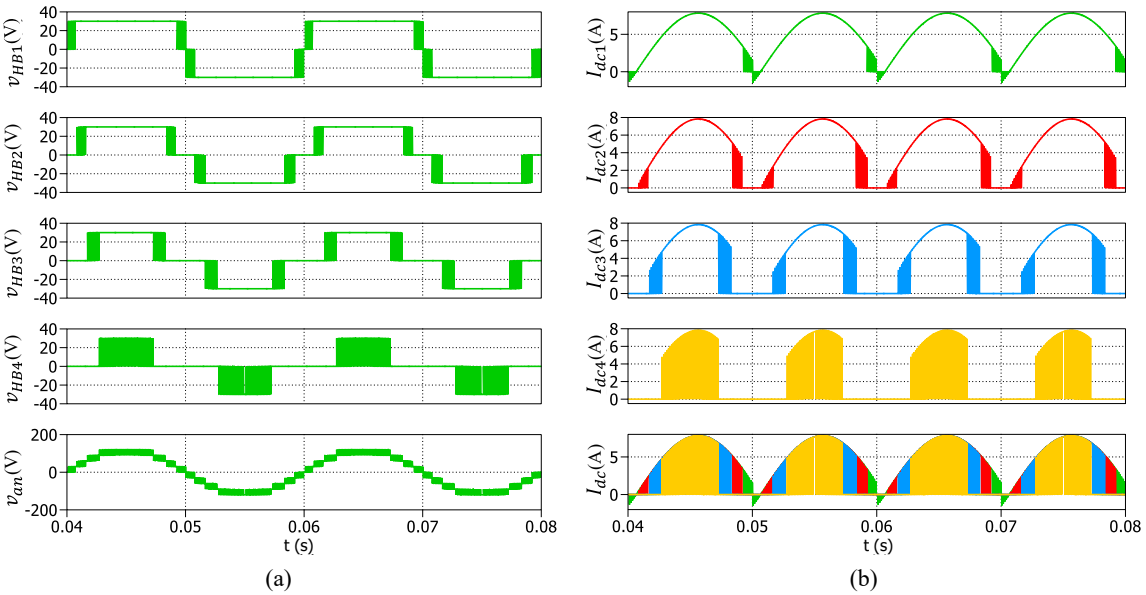


Figure 3.40: Simulation results for IPD-PWM implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index - Inverter phase leg A (a) individual H-bridge output voltages and inverter leg voltage (b) dc current waveforms of corresponding dc sources and overall dc current profile (f_{si} = 8 kHz).

leads to uneven energy consumption and over time significant SoC imbalances occur unless a SoC balancing methodology is adopted.

It can be observed that the contribution of each H-bridge varies in decreasing order from the most in the case of the first H-bridge (HB1) to the least for the last (HB4) in the synthesis of the output voltage waveform. Accordingly, the highest battery current is drawn

from the dc source connected to HB1 (I_{dc1}) to the least for the dc source connected to HB4 (I_{dc4}) as can be seen from Figure 3.40b. An identical imbalance occurs under POD-PWM and APOD-PWM schemes with comparable output voltage and battery current profiles which are not presented here to avoid redundancy.

3.5.2 Fundamental frequency level-shifting

The discussion in the previous subsection (3.5.1) focused on the uneven utilisation of power between different H-bridge modules which are powered with identical isolated dc sources. The issue of unequal charge/discharge cycles can be resolved to ensure equal distribution of power by the rotation of the carrier waveforms to occupy different voltage levels (Angulo et al., 2007). In the simplest case, the carrier waveforms are shifted by one voltage level in a circular manner after each fundamental cycle. Thus, four H-bridges are ultimately utilised equally over four fundamental cycles as shown in Figure 3.41a. In this manner, a CHB with k modules ($k \geq 2$) would require k fundamental cycles to equalise power distribution. Similarly, equal dc-source utilisation can be achieved in just 2 fundamental cycles (CR2P) by halving the time each carrier spends at each voltage level as shown by carrier disposition in Figure 3.41b. In this case, power can be equalised in $\frac{k}{2}$ fundamental cycles.

The implementation of the described equalisation methods on a single-phase 9-level CHB-MLI produces the leg voltage waveforms and corresponding dc current waveforms. It can be noted from Figure 3.42a that the voltage contribution of each H-bridge in the CHB is sequentially equalised over four fundamental cycles, while it takes only two fundamental cycles (CR2P) to achieve equalisation (Figure 3.43a). Similarly, the dc current withdrawn by each dc source (battery) is equalised over four fundamental cycles in the first case (Figure 3.42b) while it takes only two fundamental cycles to achieve the same result in the second case (Figure 3.43b).

3.5.3 Carrier frequency level-shifting

Balanced device switching and conduction times are achieved on average when the switching pattern is altered sequentially to ensure each H-bridge module's output voltage is equally utilised. This was realised with carrier rotation at fundamental frequency and in the second case at half the fundamental frequency. The process of equalisation can be further

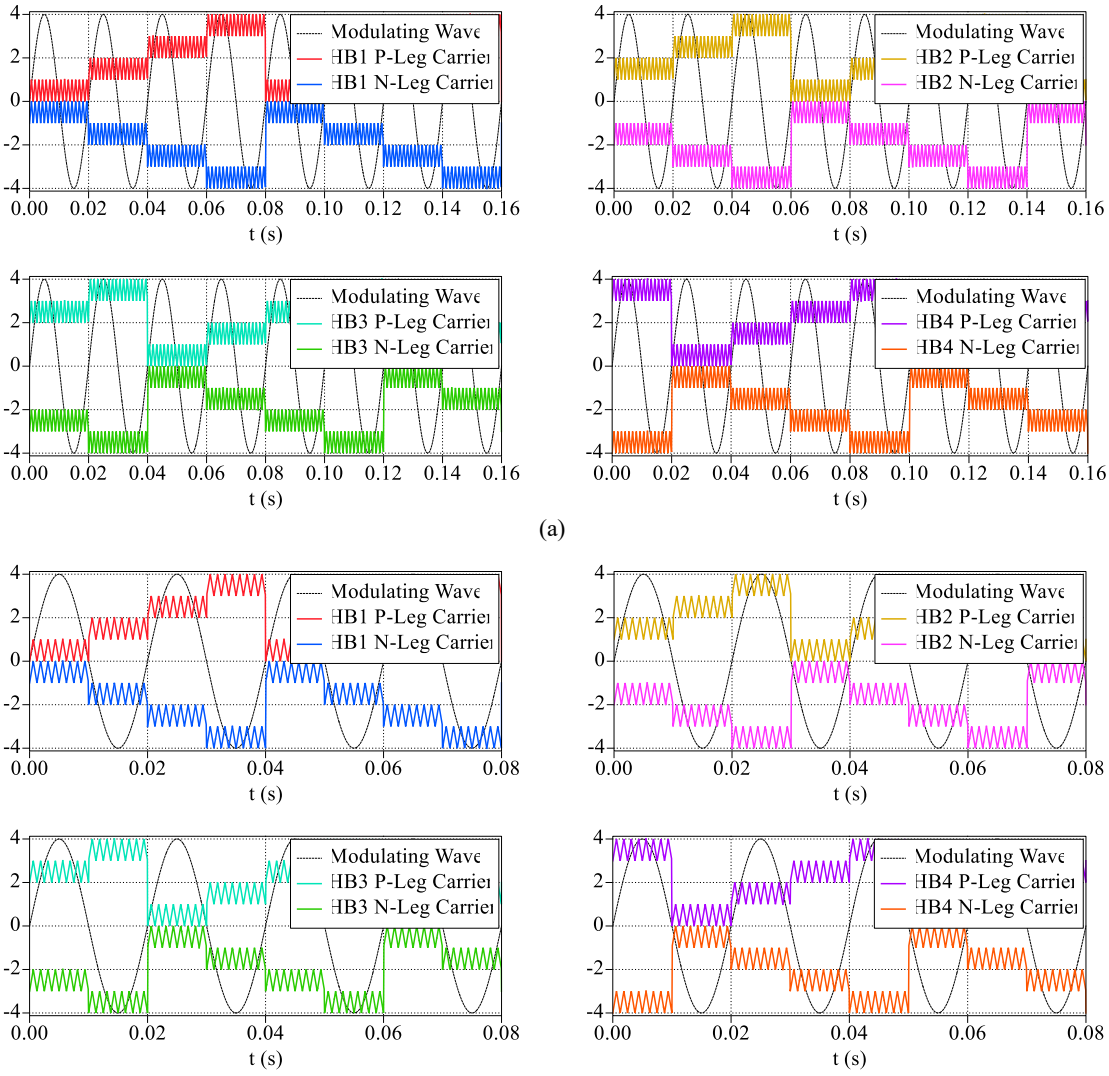
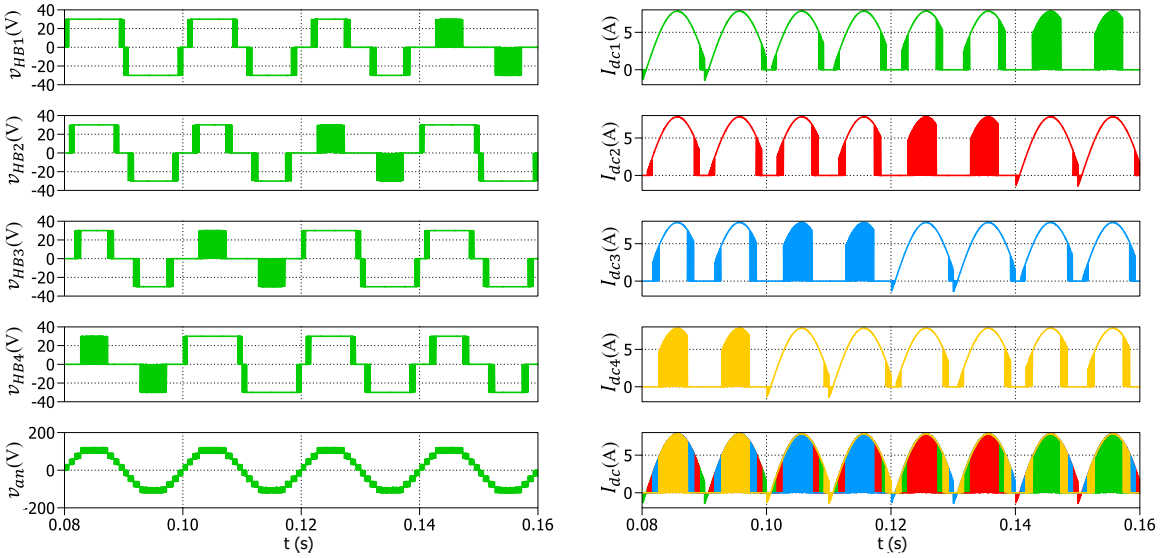


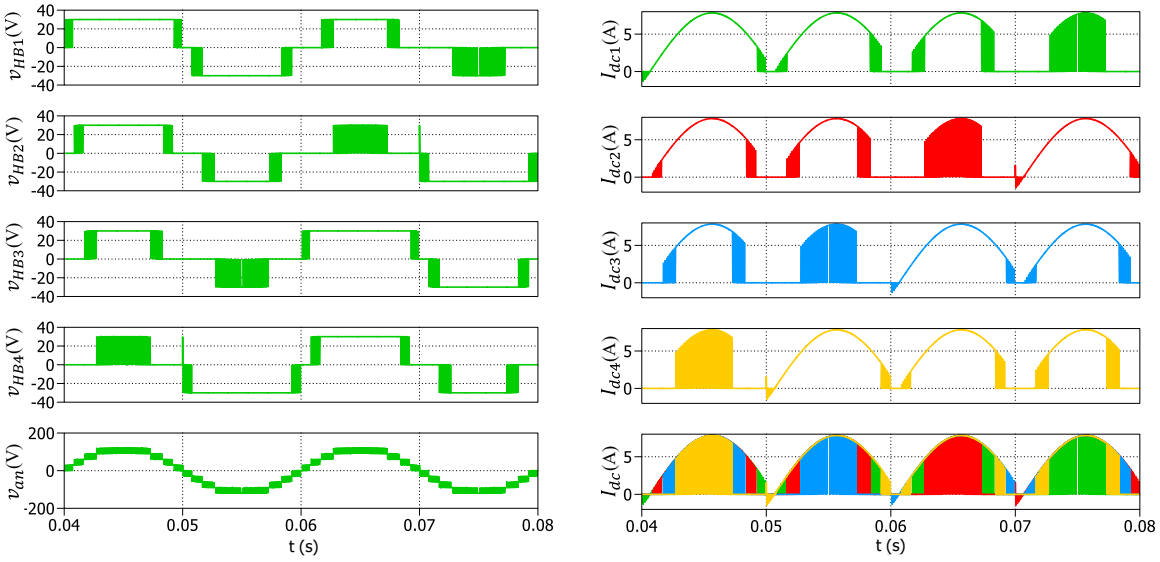
Figure 3.41: Carrier rotation for a 9-level CHB-MLI with modulating and carrier waveforms for each cascaded H-bridge module (a) Equalisation in 4 fundamental cycles (b) Equalisation in 2 fundamental cycles (CR2P).

accelerated through the reduction in time each triangular carrier occupies a certain voltage level. In the case of a CHB with 4 H-bridge modules, there are 4 positive and 4 negative levels that need to be occupied. The carrier waves can be made to occupy the next voltage level by level-shifting the triangular carrier waves at the frequency of the carrier wave (f_c). This forms a multilevel carrier waveform which moves through each contiguous voltage level. Although several configurations are possible, two basic multilevel carrier waveform shapes can be formed in shape of the traditional sawtooth and triangular carrier waveforms.



(a) (b)

Figure 3.42: Simulation results for fundamental frequency level-shifting with equalisation in four fundamental cycles implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index - Inverter phase leg A (a) individual H-bridge output voltages and inverter leg voltage (b) dc current waveforms of corresponding dc sources and overall dc current profile (f_{si} = 8 kHz).



(a) (b)

Figure 3.43: Simulation results for fundamental frequency level-shifting with equalisation in two fundamental cycles (CR2P) implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index - Inverter phase leg A (a) individual H-bridge output voltages and inverter leg voltage (b) dc current waveforms of corresponding dc sources and overall dc current profile (f_{si} = 8 kHz).

Figure 3.44 shows the sawtooth and triangular multicarrier waveforms formed using level-shifted triangular waveforms. In the case of a CHB with k modules per phase, the multilevel sawtooth waveform period would be kT_c. Therefore, the frequency of the sawtooth multilevel carrier waveform can be defined as:

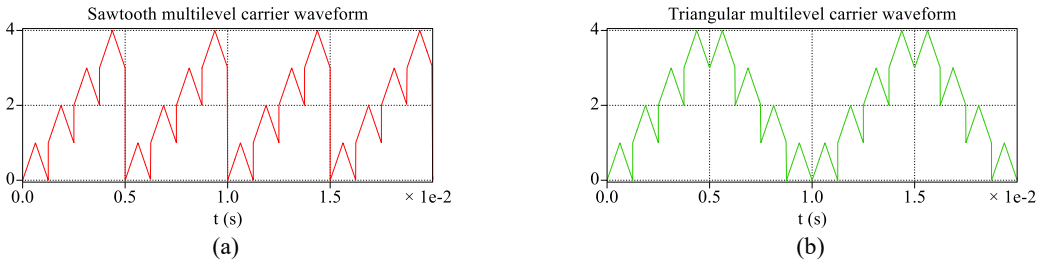


Figure 3.44: (a) Sawtooth and (b) triangular multilevel carrier waveforms (negative half not shown) ($f_c = 800$ Hz, $f_{smc} = 200$ Hz, $f_{tmc} = 100$ Hz).

$$f_{smc} = \frac{1}{kT_c} = \frac{f_c}{k} \tag{3.30}$$

Comparably, the period of the triangular multilevel carrier waveform is double that of the sawtooth multilevel carrier waveform. Therefore, the frequency of the triangular multilevel carrier waveform for a CHB-MLI with k modules per phase can be defined as:

$$f_{tmc} = \frac{1}{2kT_c} = \frac{f_c}{2k} \tag{3.31}$$

Carrier frequency level-shifting is possible for a CHB with a minimum of 3 H-bridge modules (7-level output voltage). As mentioned earlier, multilevel carrier wave disposition is achievable through several different configurations. Hence, only four basic configurations of interest were tried and tested for performance in terms of the harmonic distortion of the leg, phase and line voltages and the load phase current. All the proposed carrier frequency level-shifting modulation methods make use of triangular carrier waveforms which remain in phase with each other within a carrier period (T_c).

3.5.3.1 Multilevel sawtooth IPD (MSIPD)

The first configuration involves sequential carrier disposition in the shape of a sawtooth wave, for both the positive and negative legs of each H-bridge, to form multilevel carrier waveforms which are in phase with each other, as illustrated in Figure 3.45. This is called the multilevel sawtooth in-phase disposition (MSIPD). The period of each multilevel sawtooth waveform is $4T_c$ and there is a phase shift of T_c between the multilevel sawtooth waveforms modulating successive H-bridges.

3.5.3.2 Multilevel sawtooth POD (MSPOD)

This carrier rotation strategy also makes use of sequential carrier disposition in the shape of sawtooth waves, one for each leg of an H-bridge, which are in phase opposition

with each other (Figure 3.46), thus named multilevel sawtooth POD (MSPOD). Like the MSIPD, the period of each saw-toothed multilevel carrier waveform is four times the carrier period ($4T_c$) with a phase shift of T_c between multilevel sawtooth waveforms controlling two consecutive H-bridges.

3.5.3.3 Multilevel triangular IPD (MTIPD)

If the carrier waveforms are rotated sequentially to occupy different voltage levels at the carrier frequency, but, in the shape of a multilevel triangular carrier waveform, then each pair of the resulting multilevel carrier waves, for each of the positive and negative H-bridge legs, are in phase disposition with each other (Figure 3.47) with a period of $8T_c$. This method

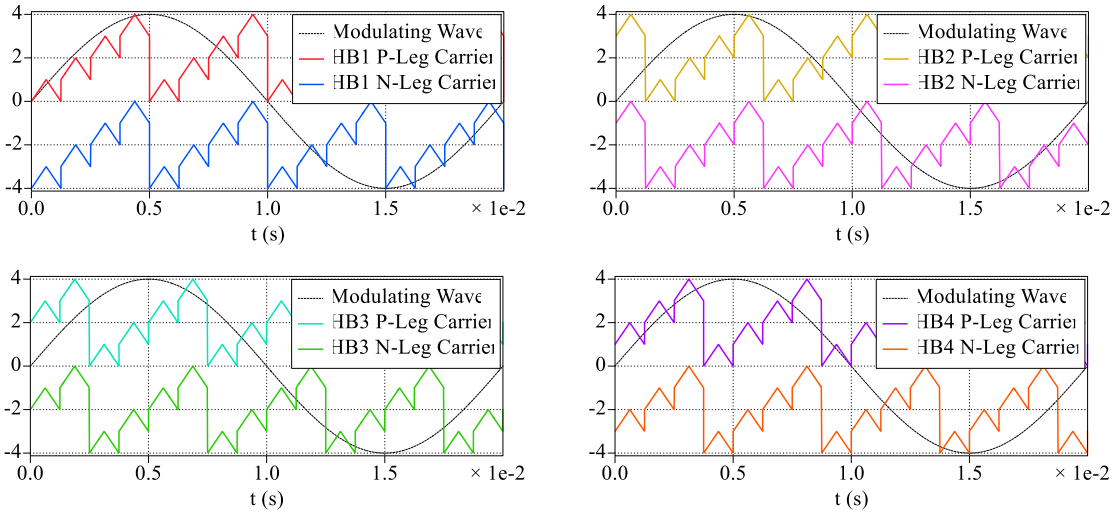


Figure 3.45: Carrier frequency level-shifting – MSIPD-PWM for a 9-level CHB-MLI – Modulating and carrier waveforms for each cascaded H-bridge module (very low carrier frequency for illustration).

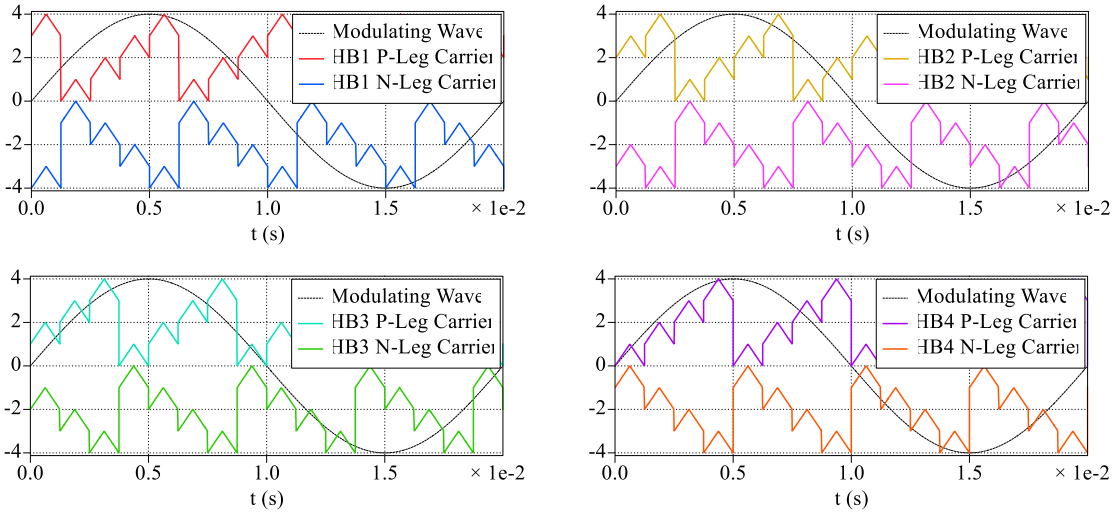


Figure 3.46: Carrier frequency level-shifting – MSPOD-PWM for a 9-level CHB-MLI – Modulating and carrier waveforms for each cascaded H-bridge module (very low carrier frequency for illustration).

is hence called multilevel triangular IPD (MTIPD). Here, there is a phase shift of $2T_c$ between the multilevel carrier waveforms controlling the gating signals of each succeeding H-bridge to achieve full coverage of the modulation range.

3.5.3.4 Multilevel triangular POD (MTPOD)

In contrast to the MTIPD scheme, the other possibility is to have a multilevel carrier disposition strategy where the multilevel carrier waveforms are in phase opposition with one another (Figure 3.48). This is called the multilevel triangular POD (MTPOD). Like the MTIPD, carrier waves are level-shifted in succession every carrier period T_c to form a triangular multilevel carrier wave, one for each leg of an H-bridge module, while being in

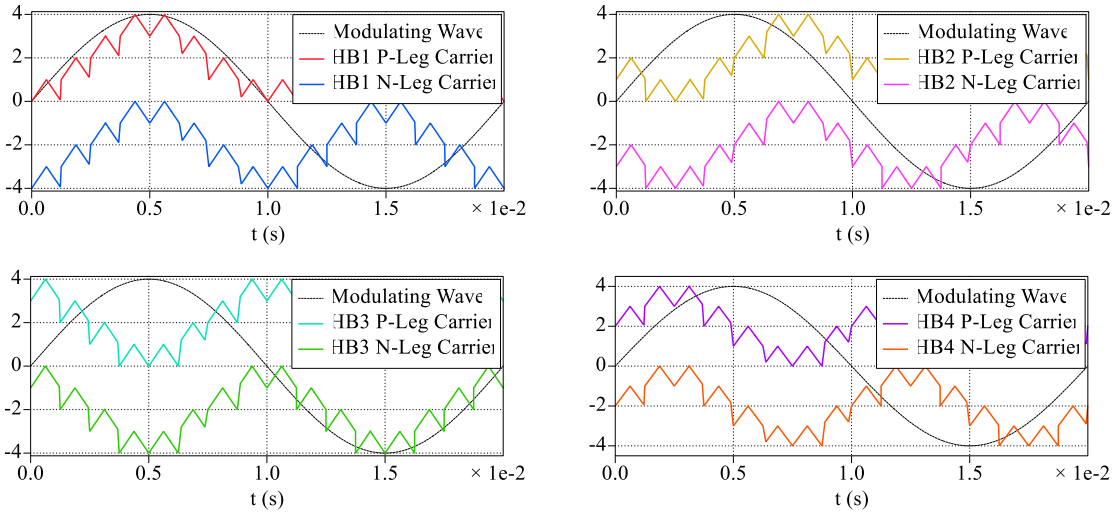


Figure 3.47: Carrier frequency level-shifting – MTIPD-PWM for a 9-level CHB-MLI – Modulating and carrier waveforms for each cascaded H-bridge module (very low carrier frequency for illustration).

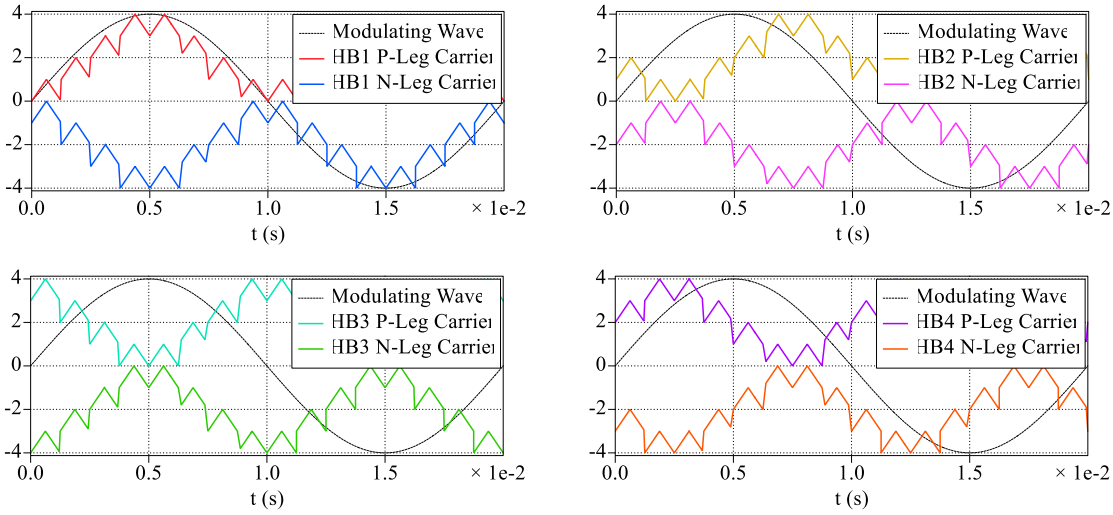


Figure 3.48: Carrier frequency level-shifting – MTPOD-PWM for a 9-level CHB-MLI – Modulating and carrier waveforms for each cascaded H-bridge module (very low carrier frequency for illustration).

phase opposition with each other. As was the case with MTIPD, the period of each resulting multilevel carrier waveform is $8T_c$ with a phase shift of $2T_c$ between subsequent carrier waveforms regulating the gate signals for the following succession of H-bridges.

3.5.3.5Simulation results and comparison

The carrier rotation modulation methods were implemented on a 9-level three-phase CHB-MLI connected to a balanced three-phase star-connected RL load. As mentioned previously, the triangular carrier waveforms, of all the discussed multilevel carrier rotation strategies, remain in phase with each other within a carrier period (T_c). Therefore, the THD values of the load phase voltage and current are identical to those obtained with the classical IPD-PWM method, for all modulation index points (Figure 3.49). Naturally, the leg, line, and phase voltages and phase current waveforms produced with MSIPD, MSPOD, MTIPD, and MTPOD PWM are all indistinguishable, as shown in Figure 3.50.

However, the difference between the multilevel sawtooth carrier (MSIPD and MSPOD) and multilevel triangular carrier (MTIPD and MTPOD) is clearly noticeable in Figure 3.51. Although the inverter leg voltage waveforms produced by all four of these carrier rotation techniques are identical, individual H-bridge module output voltage waveforms are very different from each other. The rotation period of the multilevel triangular carrier waveform (MTIPD and MTPOD) is double that of the multilevel sawtooth carrier (MSIPD and MSPOD) waveform. This causes visibly different H-bridge output voltage waveforms although the average device switching frequency is determined by the carrier frequency and remains the same for each method. Consequently, evaluation of the switching and conduction losses as well as thermal analysis of the switching devices needs to be carried out to conclusively agree on the merits and demerits of each carrier rotation modulation method.

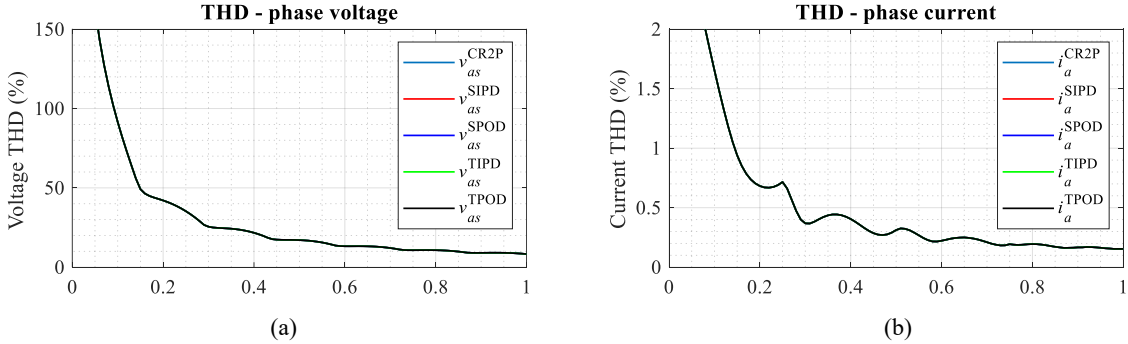


Figure 3.49: Multilevel carrier rotations schemes - THD comparison for phase voltage and current for the entire modulation index range (f_{si} = 8 kHz).

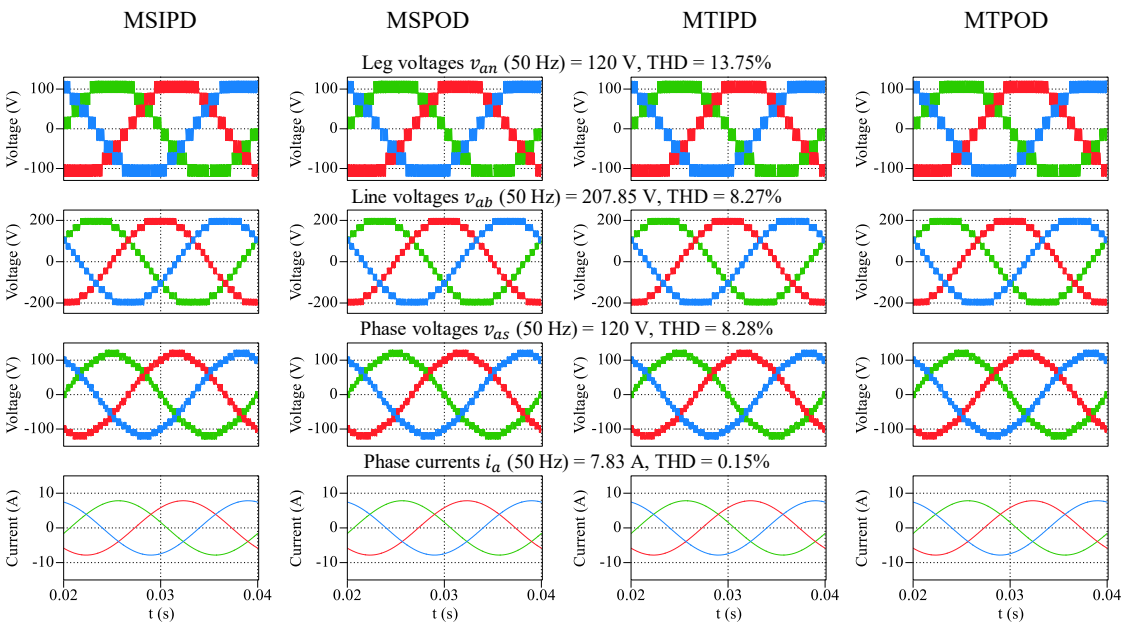


Figure 3.50: Simulation results - Leg, line and phase voltages, and phase current waveforms for multilevel MSIPD, MSPOD, MTIPD, and MTPOD PWM methods implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index ($m_a = 1.00$, $f_c = 8$ kHz, $f_{sd,avg} = 1$ kHz, $f_{si} = 8$ kHz).

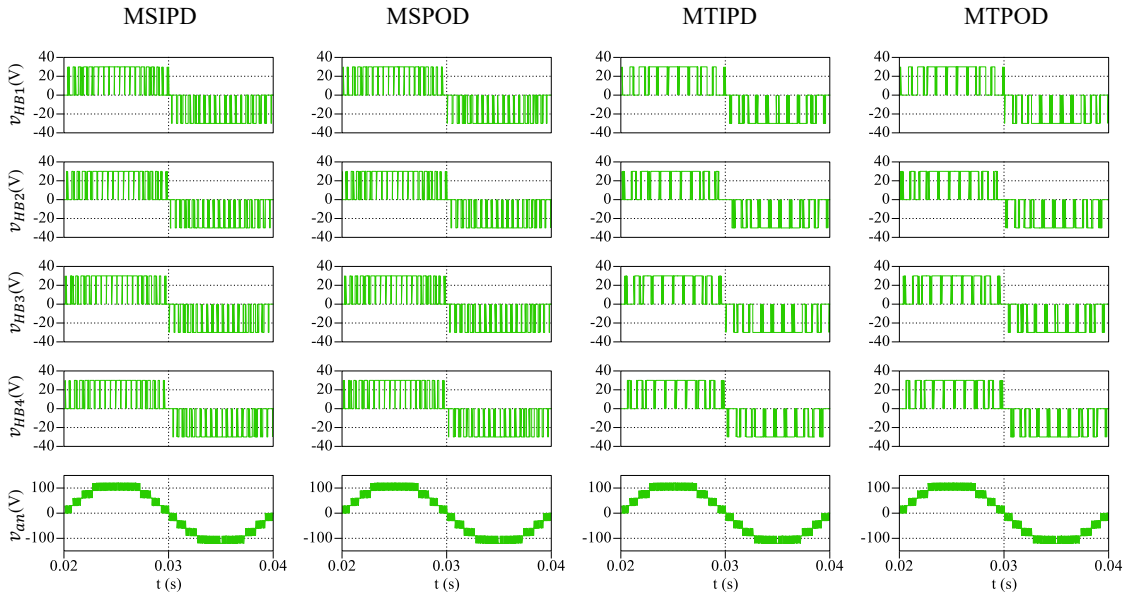


Figure 3.51: Simulation results - Individual H-bridge output voltages and the inverter phase leg A voltage for multilevel MSIPD, MSPOD, MTIPD, and MTPOD PWM methods implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index ($f_c = 8$ kHz, $f_{sd,avg} = 1$ kHz, $f_{si} = 8$ kHz).

A similar phenomenon can be noticed in Figure 3.52 where dc current profiles for each dc source show equal power distribution but multilevel triangular carrier rotation schemes (MTIPD and MTPOD) draw dc current with more overall continuity. In contrast, multilevel sawtooth carrier-based schemes (MSIPD and MSPOD) draw current with a higher number of pulsations because of a carrier rotation frequency that is double that of multilevel triangular carrier rotation schemes. Therefore, the effect of the modulation techniques on the performance of the battery also requires consideration before arriving at a conclusion.

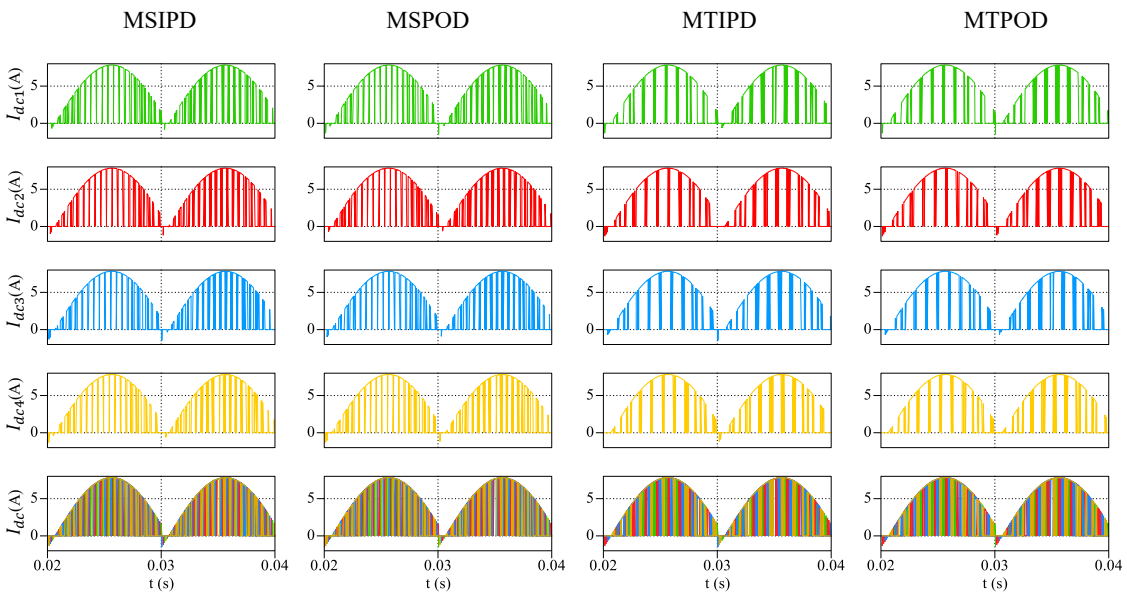


Figure 3.52: Simulation results - Inverter phase leg A - dc current profiles for each dc source and overall dc current profile for multilevel MSIPD, MSPOD, MTIPD, and MTPOD PWM methods implemented on a 9-level CHB-MLI connected to a three-phase RL load at unity modulation index ($f_c = 8$ kHz, $f_{sd,avg} = 1$ kHz, $f_{si} = 8$ kHz).

3.5.4 Fundamental frequency reference rotation

The discussion in the previous subsections 3.5.2 and 3.5.3 revolved around the cyclic rotation of the carrier waveforms over different voltage levels to achieve balanced dc-source and switching device utilisation. The other option available to achieve a similar outcome is with the periodic rotation of the reference waveforms. This can be useful when implementation of the modulation method relies on the manipulation of the dc-source voltages instead of the carrier waveforms. In certain practical applications/situations, limited access to the PWM generation system is available with an original equipment manufacturer specified implementation of the carrier waveforms in a microcontroller device. Therefore, through careful manipulation of the reference waveforms and appropriate phase-shift timing of the carrier waveforms, the same modulation objectives can be achieved.

An alternative method to achieve any of the LS-PWM method involves splitting the sinusoidal modulating wave into multiple voltage levels depending on the desired number of H-bridges. For example, in the case of a CHB with four H-bridge modules, the sinusoidal reference waveform is sectioned into 8 parts with 4 positive and 4 negative parts, as shown in Figure 3.53. Parts sectioned in the positive half-cycle and those in the negative half-cycle of the fundamental are brought to a common range [0-1] and compared with carrier waveforms which are appropriately assigned to achieve the desired modulation result. For instance, when a single carrier waveform is compared with the positive and negative parts

of the reference waveform to generate gate signals for the top switch in the positive leg and negative leg of each H-bridge respectively, one gets the equivalent implementation of the POD-PWM, as shown in Figure 3.54. Therefore, only one carrier waveform can be used to generate the gating signals for POD-PWM implementation. On the other hand, a pair of carrier waveforms (out-of-phase with each other by 180°) are needed to implement the IPD-PWM. This is equivalent to a phase-shift of $1/(2f_c)$ between the two carrier waveforms. Thus, one carrier waveform is compared with the positive half-cycle reference waveforms associated with each H-bridge [0-1] to produce gating signals for the positive legs of each H-bridge. The same process is applied but the other carrier waveform (which is out-of-phase with the first one) is compared with the negative half-cycle of the reference waveforms after the detection of reference zero-crossing. Thus, the equivalent implementation of IPD-PWM

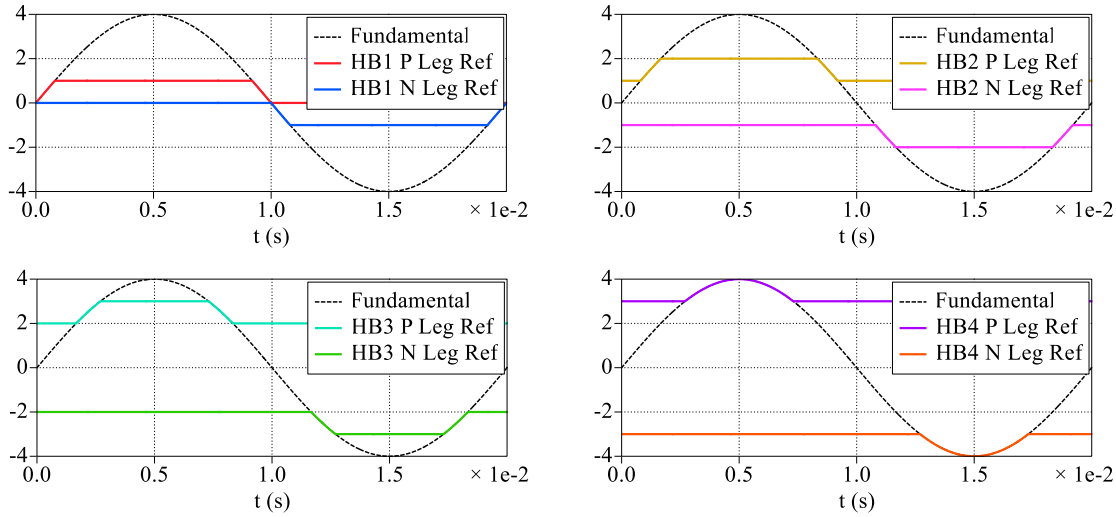


Figure 3.53: Alternative mechanism to achieve LS-PWM for a 9-level CHB inverter – modulating reference splitting.

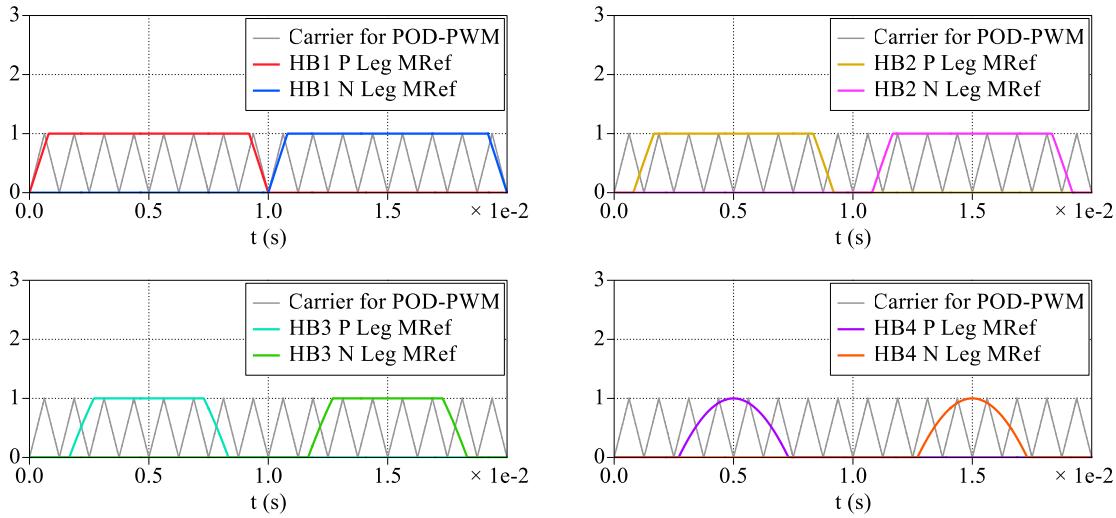


Figure 3.54: Alternative mechanism to achieve LS-PWM for a 9-level CHB inverter – assignment of reference and carrier waveforms to each CHB module for switching signal generation in POD-PWM.

is achieved, as shown in Figure 3.55. Likewise, for APOD-PWM, two out-of-phase carriers are again needed. However, an appropriate alternating carrier distribution for even and odd numbered H-bridge modules results in the equivalent implementation of the APOD-PWM, as seen in Figure 3.56.

The different parts of the reference waveforms can be attributed to different dc sources of the H-bridge battery modules. In this way, through periodic rotation or cycling of the dc sources, balanced power distribution can be achieved. Additionally, if the terminal voltage of each dc-source is known (measured), then each H-bridge battery module can be appropriately placed in the modulation index range to generate the desired leg voltages while maximizing the time of operation. Placement of the dc-source with the highest terminal

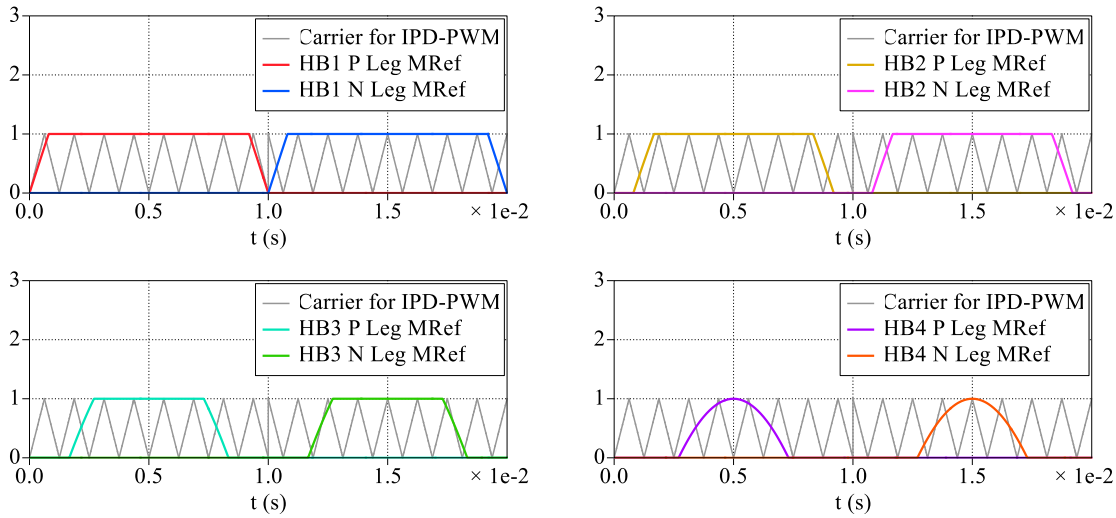


Figure 3.55: Alternative mechanism to achieve LS-PWM for a 9-level CHB inverter – assignment of reference and carrier waveforms to each CHB module for switching signal generation in IPD-PWM.

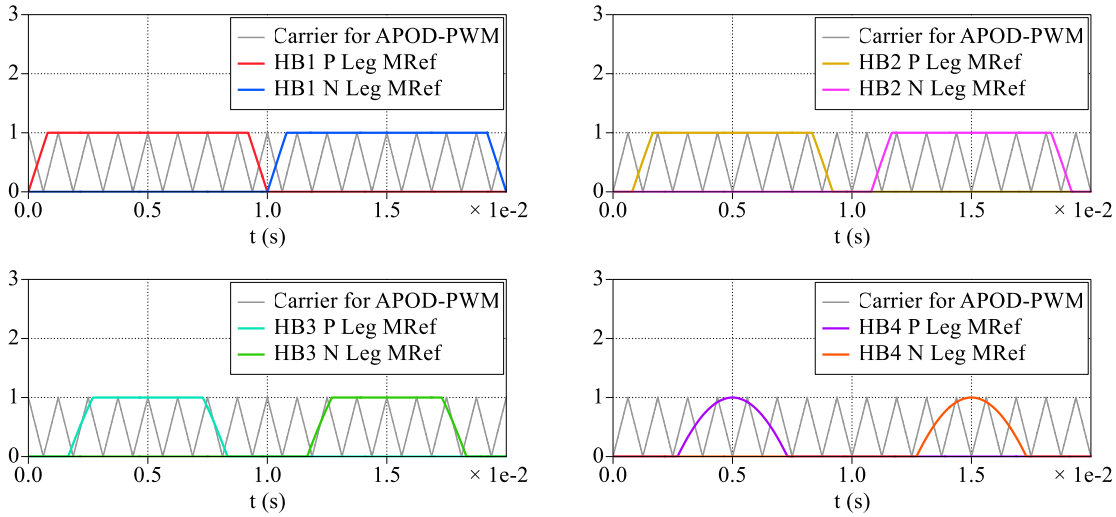


Figure 3.56: Alternative mechanism to achieve LS-PWM for a 9-level CHB inverter – assignment of reference and carrier waveforms to each CHB module for switching signal generation in APOD-PWM.

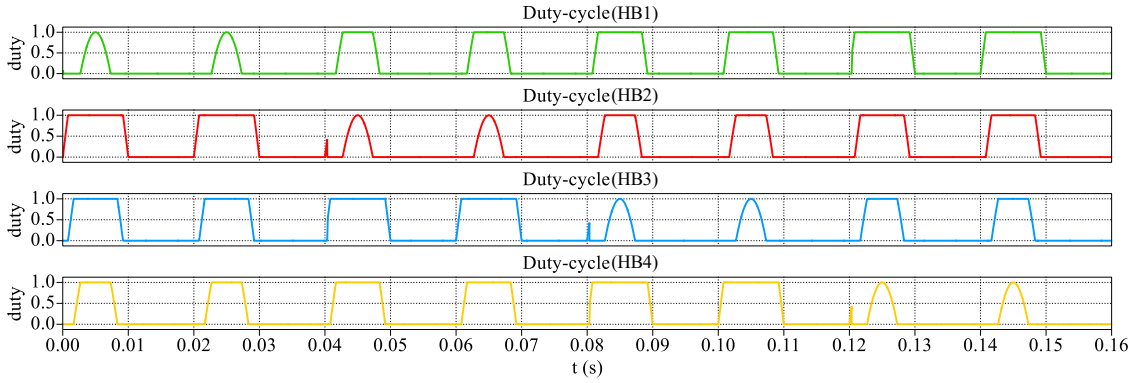
voltage (SoC) in the lowest part of the modulation index range will prolong the time of operation.

The simulation results obtained after the implementation of the reference rotation strategy are shown in Figure 3.57. All four dc-source voltages are taken to be equal (30 V). The duty-cycle references for each of the four H-bridges to obtain the desired voltage level at unity modulation index are shown in Figure 3.57a where the reference rotation is triggered after every two fundamental cycles (fundamental of 50 Hz). It can be noticed that in this way average equal dc-source utilisation is achieved in eight fundamental cycles. The respective individual output voltages of each H-bridge as well as the inverter output leg voltage can be seen in Figure 3.57b. The respective dc-source currents are also shown (Figure 3.57c) where the dc-source current supplied by each battery is equalised over eight fundamental cycles.

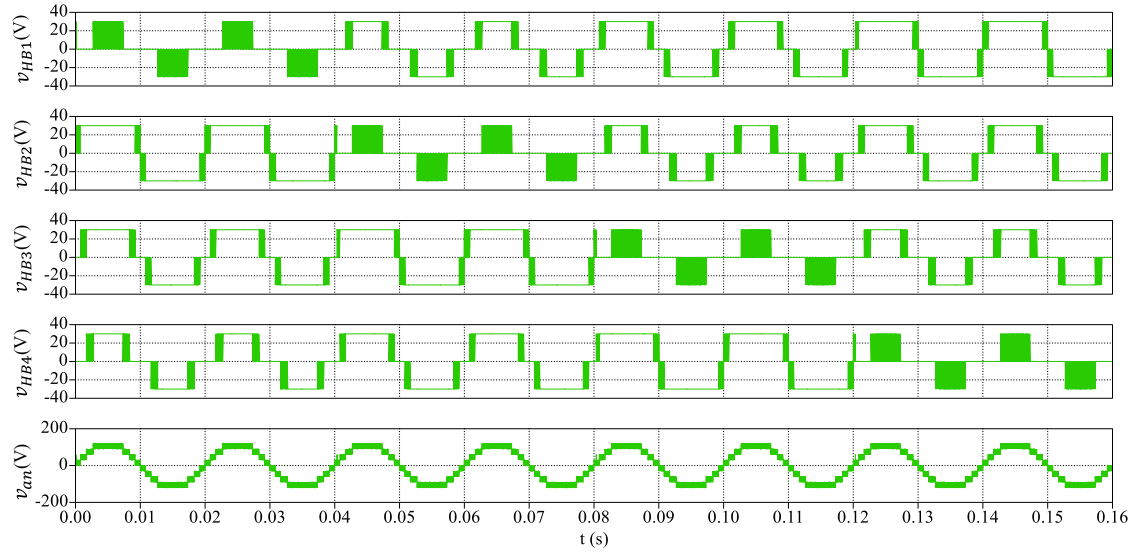
Although the results shown are for the scenario where all dc-source voltages are taken to be equal, the described reference rotation method is later applied to unequal dc-source voltage conditions, which is further discussed in subsection 4.3.2.

3.6 Summary

This chapter serves as a foundation for the rest of the chapters in the thesis. It began with a description of the CHB topology. Both the single-phase and three-phase CHB-MLI consisting of four H-bridge modules per phase were used as an example. Then, different modulation methods applicable to the CHB-MLI were presented. Included were the low frequency methods like the NLM and the SHE. Their implementation via simulation on a three-phase multilevel converter through the entire linear modulation index range was done. The primary issue with the implementation of these low frequency modulation methods is the relatively high magnitude (up to 0.35 A in the considered case – subsection 3.4.1) of lower order harmonics especially at low modulation indices. The harmonic distortion figures for the current at low modulation index are also unacceptably high (10-20% in the considered case – subsection 3.4.1). The other issue is of poor dynamic performance which is an essential performance criterion in EV drives. This is due to the dependence on pre-calculated switching angles in SHE for certain operating conditions which may not deliver sufficiently acceptable performance in dynamic conditions.



(a)



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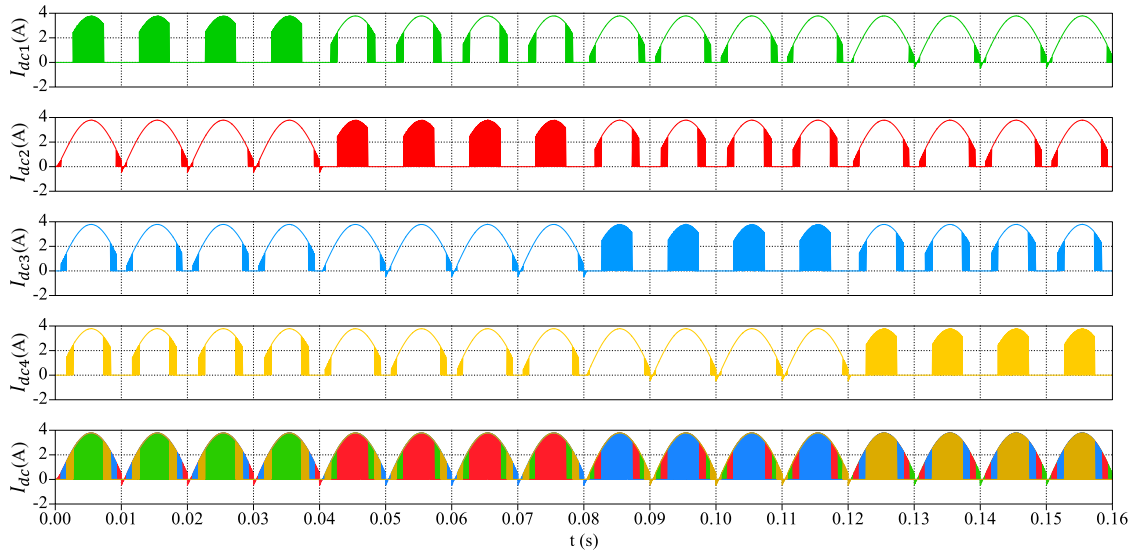


(c)

Figure 3.57: Simulation results for reference rotation with equalisation in eight fundamental cycles implemented on a 9-level CHB-MLI connected to a three-phase *RL* load at unity modulation index - Inverter phase leg A (a) positive half duty-cycles for H-bridges (b) individual H-bridge output voltages and inverter leg voltage (c) dc current waveforms of corresponding dc sources and overall dc current profile.

Next, high frequency modulation methods including the multicarrier PS-PWM and LS-PWM were described and implemented in simulation on a single- and three-phase CHB-MLI. A comparison between the LS modulation methods including the IPD-PWM, POD-PWM, and APOD-PWM along with the PS-PWM in terms of the THD of the leg, line, and phase voltages and phase current waveforms for the entire linear modulation index range was presented. It was conclusively shown that the IPD-PWM performs best in terms of THD produced over the linear modulation index range. The difference in the current THD is most pronounced at lower modulation indices ranging (0.5% to more than 1%, under the considered case – subsection 3.4.4).

Although IPD-PWM performs best in terms of the THD produced, it was shown that it suffers from the issue of unequal power distribution between H-bridge modules. It was shown that even power distribution through carrier wave disposition at different voltage levels can be achieved with the circular rotation of the carrier waves. Different carrier rotation modulation strategies including the carrier rotation at fundamental frequency and four different carrier rotation schemes at carrier frequency were presented. This included carrier rotation in two periods (CR2P) and through carrier rotation with multilevel sawtooth waveforms (MSIPD and MSPOD) and multilevel triangular waveforms (MTIPD and MTPOD). For each of the described carrier rotation techniques, the average device switching frequency and conduction times were equalised between different H-bridge modules. A comparison between the carrier rotation techniques was presented in terms of the harmonic distortion profile over the linear modulation index range which shows performance identical to that achieved with the IPD-PWM. Consequently, no loss would be incurred from utilizing one of these techniques over the other in terms of potential gain in harmonic performance. However, the dc-current drawn under MTIPD and MTPOD at a lower frequency as compared to MSIPD and MSPOD may prove beneficial in terms of the battery losses. However, further investigation is needed for each of the described equalisation schemes in terms of the switching and conduction loss distribution and thermal performance to conclusively establish superiority.

A novel technique to realise LS-PWM methods based on the splitting of the reference waveforms was presented. It should be noted that the alternative mechanism to achieve LS-PWM allows for the appropriate scaling of the reference waveform in both equal and unequal dc-source voltage conditions, as will be further shown in Chapter 4 (subsection

4.3.2). This contrasts with the standard LS-PWM implementation which cannot deal with the dc-source voltage unbalance. The described methodology permits attribution of difference dc-sources of the CHB modules to different parts of the reference waveform. This allows better energy management of the dc-sources (batteries) with appropriately timed rotation of the reference waveforms to achieve controlled dc-source utilisation.

Chapter 4
CHB operation with offset voltage injections

4.1 Introduction

This chapter discusses the operation of the CHB inverter under balanced and unbalanced dc-source voltage conditions. The role of different offset injections is investigated in achieving different objectives. This includes improvement in the harmonic performance of the phase voltages and currents for the entire modulation index range as well as the extension of the modulation index range. Better harmonic performance of the converter means a reduction in filtering requirements which positively impacts space and cost considerations. The focus of the chapter is only on multicarrier phase- and level-shifted modulation methods because the dynamic performance requirements in EV application are better served by high frequency modulation methods.

Generally, inverters are operated at high modulation indices for better harmonic performance and dc-source utilisation. However, unlike these applications, when such a converter is employed in EV applications the inverter would have to be operated at lower modulation indices. For example, for operation of the machine at partial loads/reduced speeds, the operation of the machine is directly related to the frequency of operation and thus the voltage modulation index. Therefore, the performance of different phase and level shifted modulation methods under different min-max based offset voltage injections is investigated for the whole modulation index range in section 4.2 where all dc-source voltages are considered equal. A comparison, in terms of the harmonic performance of the phase current, between the investigated methods shows superiority of the second and double min-max offset injections.

In applications where the H-bridges in a CHB converter are supplied by batteries, there can be a natural variation in the individual battery voltages. This imbalanced dc-link condition causes a deviation in the total leg voltage that can be synthesised by each of the three converter legs causing asymmetries in the output. Therefore, section 4.3 provides a discussion on the consequences of the CHB inverter under dc-source voltage imbalance as well as methods to achieve balanced operation through different min-max based offset

injections. Extension of the modulation index range under unbalanced dc-source voltage conditions is shown through the standard min-max as well as the recently improved neutral voltage modulation method (NVM) presented by (Kim and Cho, 2022). Further performance enhancement of the method suggested in (Kim and Cho, 2022), through the modification of the standard level-shifted modulation method, is presented in 4.3.2.

The simulation and experimental results are obtained using a nine-level three-phase CHB connected to an RL load, as in previous Chapter 3. The results and conclusions drawn from this chapter are used for the application of appropriate methodologies to the three-phase machine and further extended to multiphase machines, in Chapter 5. The work presented in this chapter has been published in (Khan et al., 2022) and (Khan et al., 2024b).

4.2 Equal dc-source voltage conditions

This section provides a discussion of different min-max based offset voltage injections under the assumption that all the dc-source voltages in the CHB are equal. The maximum linear modulation index for sinusoidal PWM can be extended from unity to $2/\sqrt{3}$ for a three-phase system through an appropriate offset voltage injection. The most well-known offset voltage injection is the third harmonic injection (THI) of one-sixth amplitude. The THI of one-quarter magnitude has also been suggested for further reduction in the current THD at the cost of slightly reduced maximum linear modulation index range (Holmes, 1996) for the two-level converter. The CHB converter can also make use of the THI for the extension of the modulation index range (Figure 4.1).

Various offset injections have been applied in a diverse range of applications to achieve different objectives. The carrier-based first min-max injection for balanced utilisation of switching devices was introduced in diode-clamped multilevel inverters (Tolbert and Habetler, 1999). Others have made use of zero-sequence voltage injection of fundamental frequency to the state-of-charge balancing of the three phases of a CHB converter for battery energy storage application (Maharjan et al., 2009). Similarly, balancing of the dc-link capacitor voltages and power flow among the phase legs in a CHB multilevel converter for static synchronous compensation was achieved by zero sequence voltage injection (Chen et al., 2015). Likewise, an offset voltage injection was applied for the reduction of the ripple current (battery/capacitor) in battery-converter systems in a cascaded double H-bridge converter (Li et al., 2020).

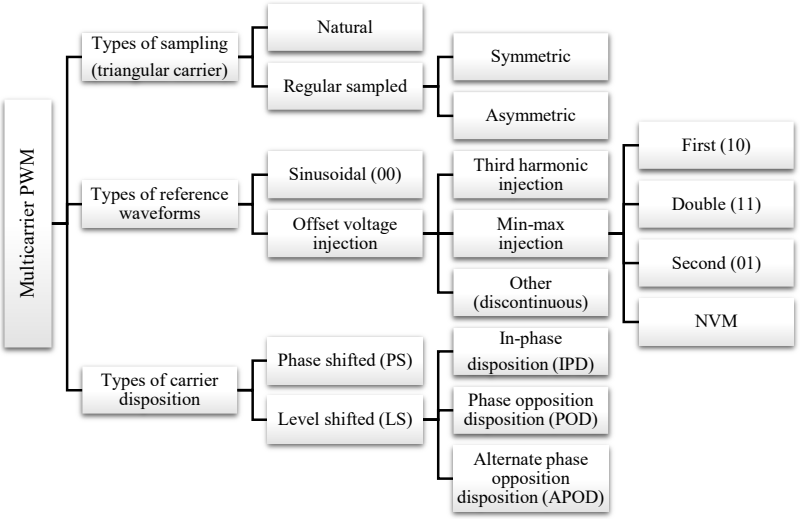


Figure 4.1: Multicarrier PWM: Type of carriers, injections, and carrier dispositions.

A study comparing harmonic performance of the load current, in different carrier-based modulation methods under different min-max injections, for the whole modulation index range in CHB multilevel converters is presented in this section. This includes the sinusoidal references (00), the first min-max (10), the second min-max (01) and the double min-max injections (11), see Figure 4.1. Experimental verification is made considering the full modulation index range, and a simplified implementation scheme of different offset voltage injections is posed for the carrier-based phase-shifted and level-shifted modulation methods.

It is essential to point out that it is necessary to ensure an appropriate and fair comparison between the phase- and level-shifted modulation methods as the effective converter switching frequency should be the same. Therefore, the carrier frequency has been adjusted to satisfy the above-mentioned point and ensure an equivalence between the average device switching frequency for both the PS- and LS-PWM methods.

The modulation index for the considered CHB multilevel converter, with k modules per leg, is defined as:

$$m = \frac{\hat{V}_{xs}^{*}}{kV_{\mathrm{dc}}} \tag{4.1}$$

where V_{dc} is the dc-link voltage across one H-bridge module and $\hat{V}_{xs}^{*}$ is the reference phase voltage amplitude for phase a, b, or c, which is defined as:

$$v_{xs}^{*} = \hat{V}_{xs}^{*} \cdot \sin(\omega_r t + \phi) = m \cdot\ k \cdot V_{dc} \cdot \sin(\omega_r t + \phi) \tag{4.2}$$

where ϕ is 0, $-2\pi/3$, and $-4\pi/3$ for the three phases a, b, and c respectively, and $\omega_r = 2\pi f_r$ is the fundamental angular frequency of the reference waveforms. For simplification, the phase reference voltages are normalised with respect to V_{dc} prior to the application of different offset voltage injections:

$$u_{xs} = m\ \cdot k \cdot \sin(\omega_r t + \phi) \tag{4.3}$$

Normalised voltages are denoted with u, and for simplicity the asterisk (*), denoting reference values, is omitted further on. The cancellation of the offset voltage in the line and phase voltages of a three-phase system allows the injection of an appropriate common-mode voltage. The fundamental relationship between the leg voltage (u_{xn}), the desired phase voltage (u_{xs}) and the offset voltage (u_{sn}), using normalised notation, can be given as:

$$u_{xn} = u_{xs} + u_{sn} \tag{4.4}$$

Therefore, the reference phase voltages are set as the desired sinusoid and a suitable offset voltage, within linear modulation range, is added to obtain the required leg voltage waveform that is compared with the carrier signals for PWM operation of the converter. Note that normalised notation is used which scales each CHB voltage to unity allowing usage of the *floor* and *modulus* functions later. The following subsections provide a discussion of the different min-max based zero-sequence injections applicable to the CHB converter, as shown in Figure 4.1.

4.2.1 Sinusoidal reference (00)

For sinusoidal PWM, the desired phase voltage reference is taken as the converter leg voltage reference (See Figure 4.2). Therefore, no offset voltage injection to the phase voltage is needed, thus:

$$u_{sn} = 0 \tag{4.5}$$

Consequently, from (4.4), the leg voltage is equal to the required phase voltage:

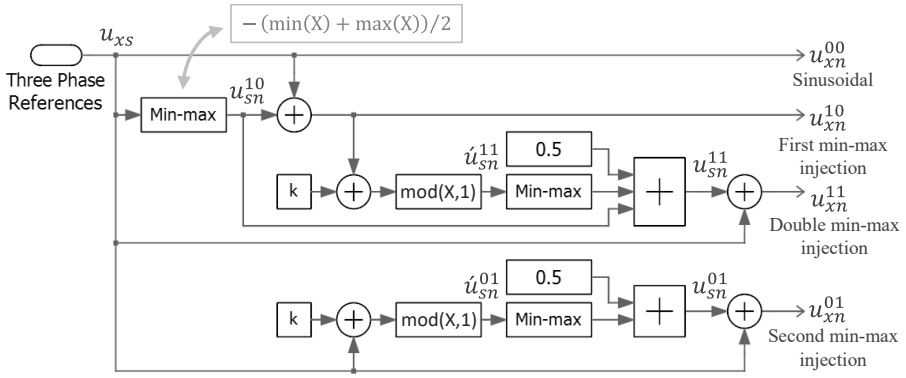


Figure 4.2: Block diagram implementation of the min-max injections.

$$u_{xn}^{00} = u_{xs} \tag{4.6}$$

4.2.2 First min-max injection (10)

The addition of an offset voltage based on the negative instantaneous average of the maximum and minimum values of the reference phase voltage from each reference phase voltage results in the centring of each reference leg voltage within the modulation period in two-level inverters (Wang, 2002). The offset voltage for the first min-max injection can thus be defined as:

$$u_{sn}^{10} = -(\min(u_{xs}) + \max(u_{xs}))/2 \tag{4.7}$$

where $x = (a, b, \text{and } c)$. The resulting leg voltage after the first min-max injection (Figure 4.2) becomes:

$$u_{xn}^{10} = u_{xs} + u_{sn}^{10} \tag{4.8}$$

For two-level converters, the centring of active space vectors within a switching period is achieved with the first offset injection to the three-phase references (Holmes and Lipo, 2003), (Holmes, 1996). The first min-max injection also lowers the total harmonic distortion of the phase current while leading to an increase in the dc-bus voltage utilisation (Holmes and Lipo, 2003). However, this is not the most effective strategy for the reduction of the total harmonic distortion of the phase current for multilevel converters, as will be shown later.

4.2.3 Double min-max injection (11)

The equivalence between SV-PWM and IPD-PWM was proven through the double min-max offset voltage injection for the multilevel CHB (McGrath et al., 2003). The centring of the active space vectors achieved by the first injection was shown to be inadequate for multilevel converters. It was shown that only the vectors of odd redundancy are centred on either side of the half switching period (McGrath et al., 2003) when subjected to the first min-max injection. As references in a multilevel waveform lie at different voltage levels which are occupied by different carrier waveforms, the active voltage vector sequence cannot be determined in this scenario. The first and last switching transitions cannot be guaranteed to have been produced by reference waveforms at their minimum and maximum points. Therefore, normalised reference leg voltage waveforms, after the application of the first min-max injection, are brought to a common voltage level within the same carrier level, using the *modulus* function, as:

$$\acute{u}_{sn}^{11} = \mathrm{mod}(k + u_{xn}^{10}, 1) \tag{4.9}$$

A dc offset of k is added to avoid erroneous results from the *modulus* operation on negative values. The min-max calculation of a new offset voltage and subsequent reapplication of min-max injection achieves the double min-max injection (u_{sn}^{11}):

$$u_{sn}^{11} = u_{sn}^{10} + 0.5 - 0.5\big((\min(\acute{u}_{sn}^{11}) + \max(\acute{u}_{sn}^{11}))\big) \tag{4.10}$$

The leg voltage reference from double min-max injection is thus completed as:

$$u_{xn}^{11} = u_{xs} + u_{sn}^{11} \tag{4.11}$$

which is shown in Figure 4.2. Equalisation of the dwell times of the first and the last voltage vector is achieved and the active space vectors within the half carrier period are centred (Holmes, 1996).

4.2.4 Second min-max injection (01)

For certain regions of the modulation index range, application of the double min-max injection (11) does not produce the lowest current THD. In multilevel inverters, the centring of the active space vectors is actually done through the application of the second min-max

injection after bringing the three-phase reference voltage waveforms into a common carrier interval. Thus, the first min-max injection can be omitted, and the second min-max operation can be applied on the desired phase reference waveforms (brought into common carrier range by *modulus* function) to obtain a different offset voltage (see Figure 4.2). Hence, the normalised offset voltage for the second min-max injection (u_{sn}^{10}) is described by:

$$\acute{u}_{sn}^{01} = \mathrm{mod}(k + u_{xs}\,, 1) \tag{4.12}$$

$$u_{sn}^{01} = 0.5 - 0.5\big((\min(\acute{u}_{sn}^{01}) + \max(\acute{u}_{sn}^{01}))\big) \tag{4.13}$$

Similarly, the reference leg voltage after the application of the second min-max injection becomes:

$$u_{xn}^{01} = u_{xs} + u_{sn}^{01} \tag{4.14}$$

It must be pointed out that in contrast to the first min-max injection, the second min-max injection does not lead to an increase in the modulation index range. This can be attributed to the application of the *modulus* function.

The block diagram implementation of all the injections is shown in Figure 4.2. An alternative simplified implementation is shown in Figure 4.3 where the *floor* function is used instead of the *modulus* function. Note that the diagram shown is in fact a universal implementation for all analysed injections, as any of the injections can be achieved by changing the relevant switches.

4.2.5 Simulation and experimental results

A MOSFET based symmetrical three-phase cascaded H-bridge converter with 4 modules per converter leg ($k = 4$) was used for the experiment (Figure 4.4). A dc-link voltage of $V_{\mathrm{dc}} = 30\ \mathrm{V}$ for each module of the converter was obtained with two serially

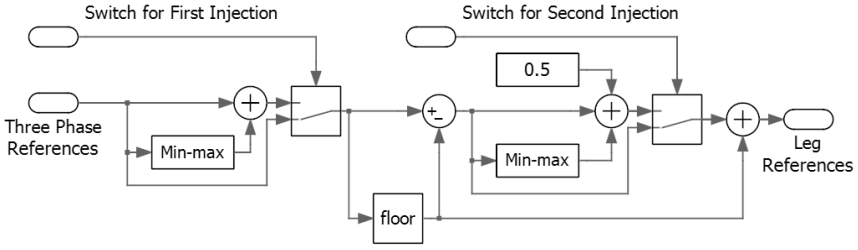


Figure 4.3: Alternative implementation of the min-max injections in PLECS.

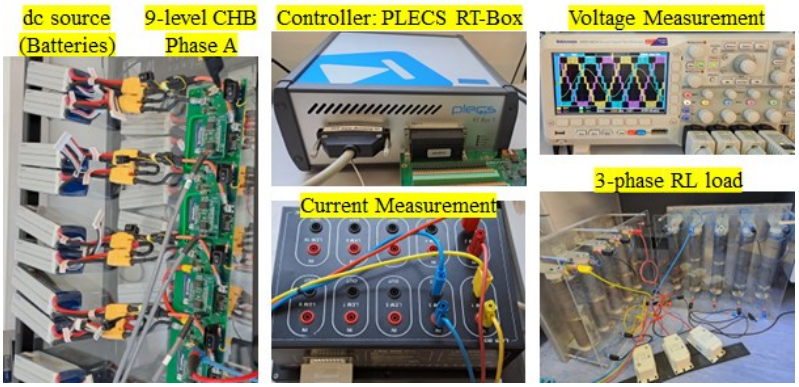


Figure 4.4: Experimental setup of the nine-level CHB inverter.

connected 14.8 V LiPo-batteries. A leg voltage amplitude of 120 V is thus obtained at unity modulation index. The three-phase converter was connected to a Y-connected balanced three-phase RL load with $\mathrm{R} = 31.5\ \Omega$ and $\mathrm{L} = 13.2$ mH. Converter control was done using Plexim RT-Box 1. The CHB converter produces high quality currents. Therefore, a lower value of inductance was intentionally chosen to increase the resulting current ripple, which also minimises the effect of the measurement noise, and emphasises the current THD difference between different modulation methods.

Balanced three-phase sinusoidal phase voltage reference waveforms with a fundamental frequency of 50 Hz were asymmetrically sampled and subjected to min-max strategies from the previous subsections. The amplitude of the reference waveforms was varied as per definition of modulation index in (4.1). Each resulting leg voltage was compared with carriers in PS, IPD, POD, and APOD (see Table 4.1). The carrier frequency was chosen to be 250 Hz for the PS-PWM and 2 kHz for the LS-PWM methods to ensure an effective converter switching frequency of 2 kHz. Measured leg, phase, and current waveforms data was acquired with an 8-bit oscilloscope with a horizontal resolution of 125k samples. Both the simulation and experimental waveforms were obtained during steady state conditions for calculation of the total harmonic distortion (THD) of the waveforms using the formula described in (3.7).

Table 4.1: Nomenclature of investigated methods.

	Sinusoidal (00)	**First Min-Max (10)**	**Double Min-Max (11)**	**Second Min-Max (01)**
PS	PS00	PS10	PS11	PS01
IPD	IPD00	IPD10	IPD11	IPD01
POD	POD00	POD10	POD11	POD01
APOD	APOD00	APOD10	APOD11	APOD01

The same system was modelled and simulated in PLECS. The simulated model used ideal switches with V_{on} and R_{on} taken as zero. A dead time of 0.5 µs was considered for simulation to match the actual experimental value and no dead time compensation was implemented as the effect of the dead time is negligible due to the discretization step size being 250 µs.

For the digital implementation of carrier-based PWM methods, the desired leg voltage references are regularly sampled either at the carrier minimum, maximum or at both points. The latter sampling method is called asymmetric sampling whereas sampling at either the carrier minimum or maximum points is known as symmetric sampling (see Figure 4.1). Symmetric sampling is suboptimal as it produces a large second harmonic component with only a partial cancellation of the sideband harmonics around odd multiples of the carrier frequency in the output, and worse harmonic performance than asymmetric sampling (Holmes and Lipo, 2003). Therefore, asymmetric sampling has been considered for implementation.

An important consideration for a fair comparison between the LS-PWM and PS-PWM schemes (which in fact have different carrier frequencies) lies in the sampling of the reference waveform and the discretization step size. For LS-PWM, the reference waveform sample is updated on carrier minimum and maximum points (asymmetric regular sampling of the reference waveform). The sampled value is held at a frequency of 4 kHz (every 250 µs) when the carrier frequency is 2 kHz (Figure 4.5 left). However, in the case of PS-PWM, if a sample and hold is performed at carrier minimum and maximum with a carrier frequency of 250 Hz – the equivalent effective converter switching frequency for equivalence between PS- and LS- methods – then the resulting reference sampling frequency of 500 Hz leads to an unfair comparison with LS-PWM. A fair comparison, therefore, requires the sampling of the reference to be conducted at the same frequency as that of

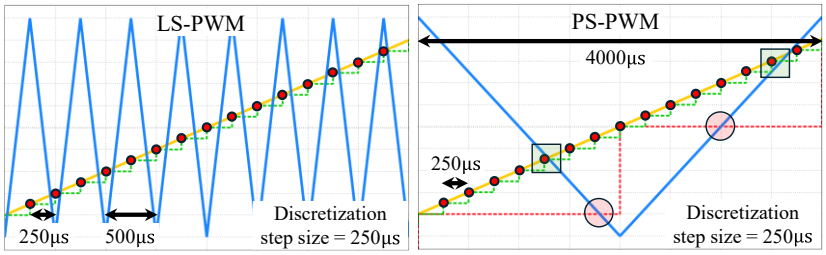


Figure 4.5: Comparison between sampling of the modulation index for a fair comparison between PS- and LS-PWM modulation schemes.

LS-PWM, i.e. every 250 μs to match the sample and hold value of LS reference (Figure 4.5 right). If all eight carrier waveforms of the PS-PWM are considered, then this would naturally match the abovementioned discretisation step size of the LS-PWM.

A comparison between the multicarrier PS- and LS-PWM methods under the offset injections (Table 4.1) is made via simulation and confirmed experimentally. The total harmonic distortion of the phase current waveforms over the entire modulation index range can be seen in Figure 4.6. The figures on the left show simulation results whereas those on the right are experimental. The vertical scaling has not been preserved for comparison between the simulation and experimental results to demonstrate similarity in the trend.

The difference between the simulation and experimental results can be primarily attributed to an error in the measurement of the inductance values of the inductors during the experiment, and to a somewhat lesser degree, to the limitation in the vertical resolution of the oscilloscope, the digitization process and from other measurement noise. From Figure 4.6, it is clear that among all the multicarrier modulation methods compared, IPD-PWM produces the lowest phase current THD for all the analysed injections. Likewise, a similar comparison between the tested methods for the phase voltage THD confirms IPD-PWM to lead to the best harmonic performance and is therefore not shown to avoid repetition. Hence, further on only the IPD-PWM is analysed.

A comparison of the phase voltage THD profiles under different offset injections for the IPD-PWM exhibits practically identical THD profiles over the entire modulation index range, as shown in Figure 4.7. However, the difference becomes apparent when the harmonic distortion of the phase currents is analysed. The phase current THD profiles of the best performing IPD-PWM under different offset injections from Figure 4.6 are plotted once again in Figure 4.8 for a direct comparison. Figure 4.8 shows that the second min-max injection produces the best current THD profile for $m \leq 1$ in both simulation and experiment. Additionally, a similarity in trend between the THD profiles of the phase current is obvious for both simulation and experiment. For $m \leq 0.25$, both the second and double injections produce practically identical current THD. In this region, only one battery-converter module is activated which corresponds to a three-level waveform operation. It can be noted that other such regions of comparable distortion are also present at higher modulation indices. However, it is evident that the second min-max injection consistently produces the lowest current THD for modulation indices below unity, barring a

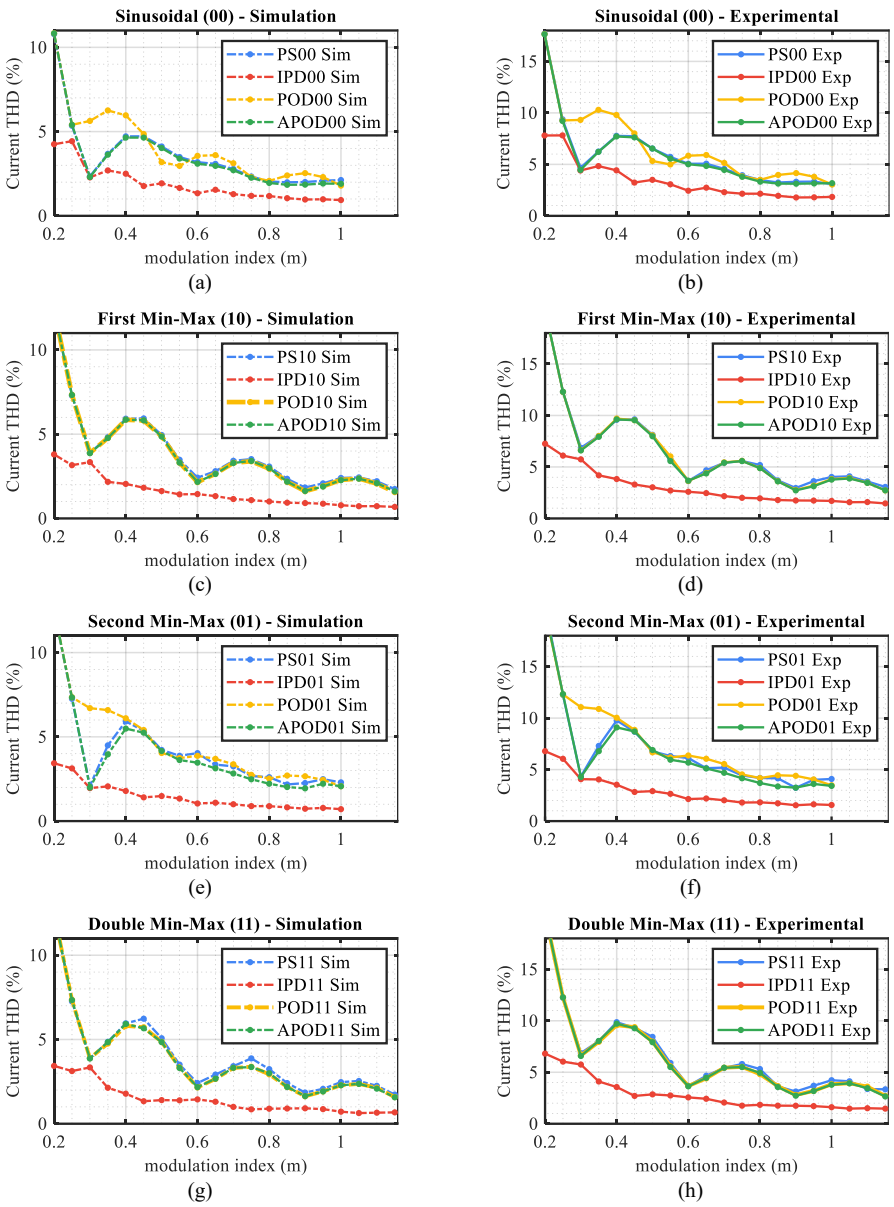


Figure 4.6: Simulation and experimental phase current THD (%) profiles for phase- and level-shifted modulation methods for different offset injections: sinusoidal (00) (a) simulation and (b) experiment, first min-max (10) (c) simulation and (d) experiment, second min-max (01) (e) simulation and (f) experiment, and double min-max (11) (g) simulation and (h) experiment.

few points where the double min-max is marginally better. The second min-max injection is not valid for modulation indices beyond unity ($m > 1$). Here, the double min-max injection produces slightly lower current THD in comparison to the first min-max injection.

The waveforms of the first (10), double (11), and the second (01) offset voltage injections are shown in Figure 4.9a and Figure 4.10a for different modulation index points. The injection of these offset voltages into each of the three desired sinusoidal phase references, respectively, produces the reference leg voltages which are shown in Figure 4.9b

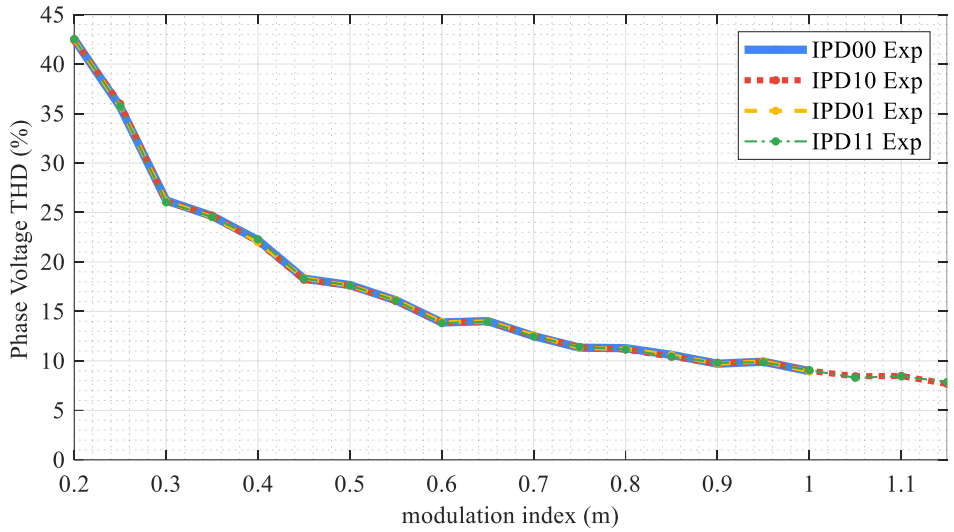


Figure 4.7: Phase voltage THD (%) profiles for IPD-PWM method for different injections – experimental results.

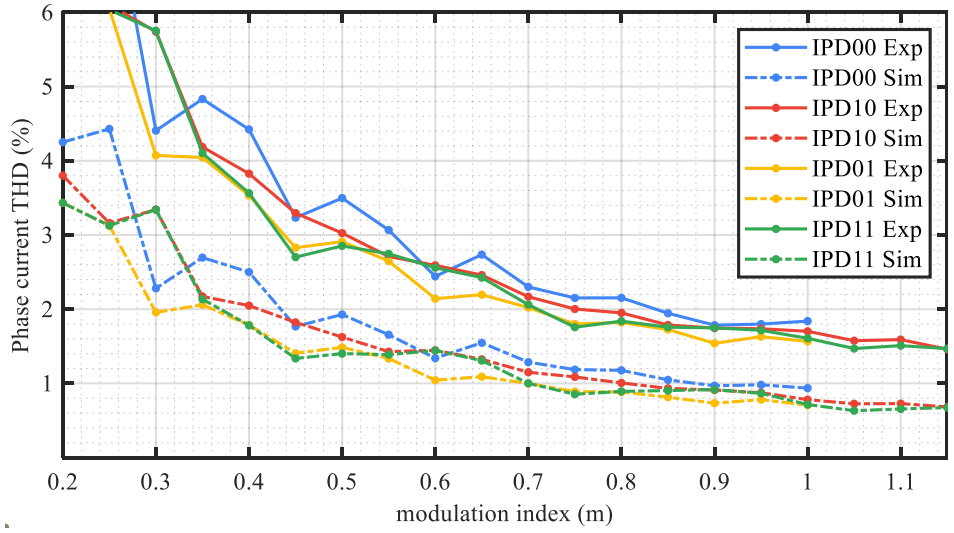


Figure 4.8: Phase current THD (%) profiles for IPD-PWM method for different injections – simulation and experimental results.

and Figure 4.10b. The offset voltage for the sinusoidal reference (00) is not shown as it is always zero [see (4.5)], leading to the reference leg voltages being equal to the desired phase references. These reference leg voltage waveforms are then compared with appropriate carriers to produce the switching signals for the H-bridge modules. It is interesting to note that the first (10) and double (11) injections produce similar offset voltage waveforms at modulation indices of $m = 0.3$, $m = 0.6$, and $m = 0.9$ (Figure 4.9a and Figure 4.10a) and produce approximately the same amount of harmonic distortion (Figure 4.8).

The leg voltage and phase 'a' current waveforms, obtained experimentally, at modulation indices of $m = 0.3$, $m = 0.6$, and $m = 0.9$ are presented in Figure 4.11 for the injections under discussion. As expected, the number of converter levels of the leg voltage

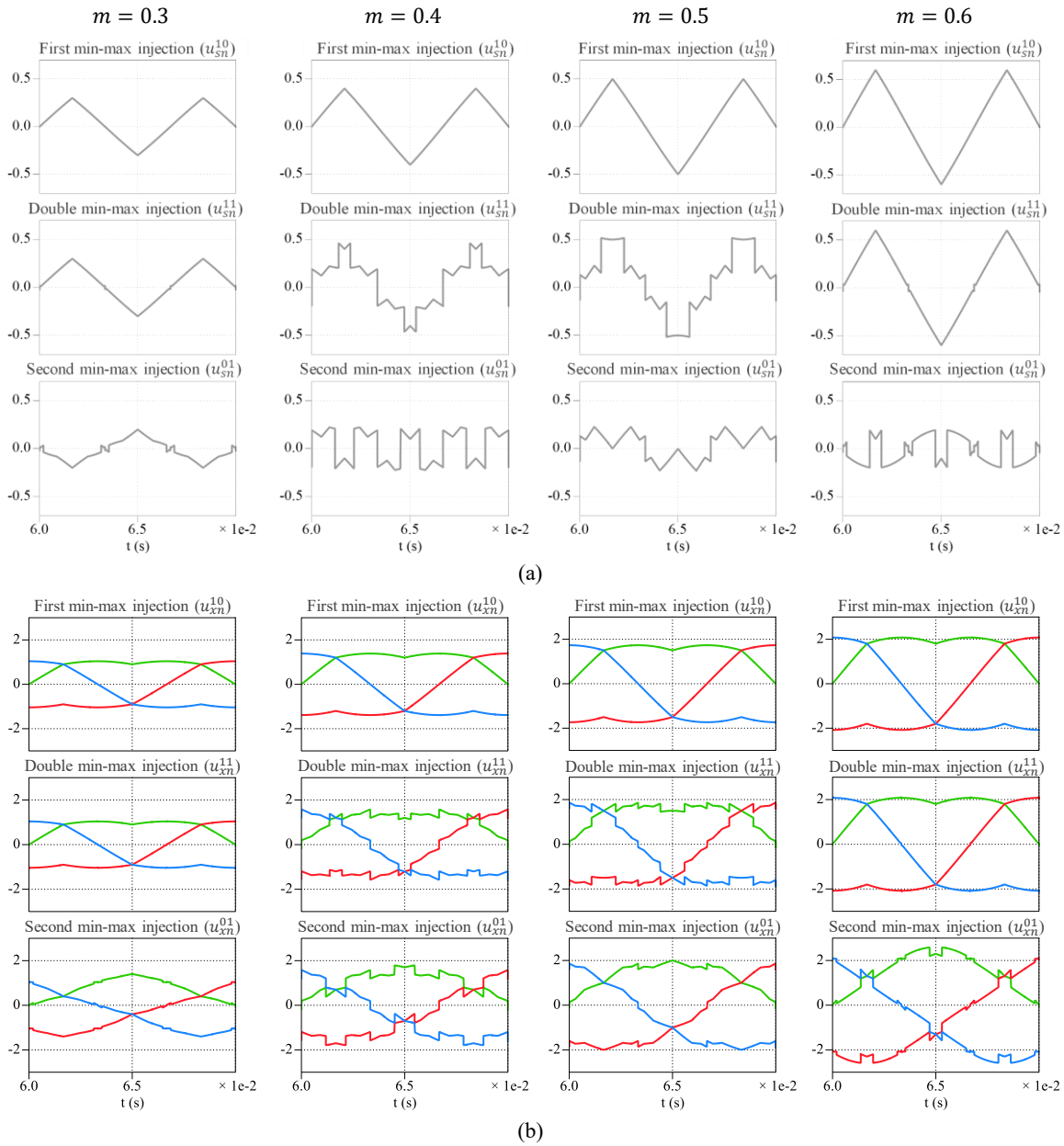


Figure 4.9: (a) First (10), double (11), and second (01) offset voltage waveforms and (b) the resulting three-phase leg voltage reference waveforms for different modulation indices ($m \leq 0.6$).

waveforms increase from five at $m = 0.3$ to seven at $m = 0.6$, and to nine $m = 0.9$. At these points, the difference between the THD of the second min-max injection and other min-max injections is noteworthy as can be observed from the respective current THD profiles in Figure 4.8. The current is quite sinusoidal for all the offset injections, but the second offset injection (01) produces the lowest current THD (see Figure 4.11 (c), (g), and (k)). The harmonic spectra of the respective current waveforms are shown in Figure 4.12. The dominant harmonic bands lie at the switching frequency (2 kHz) while the next significant harmonics lie at multiples of the switching frequency. However, the magnitude of the

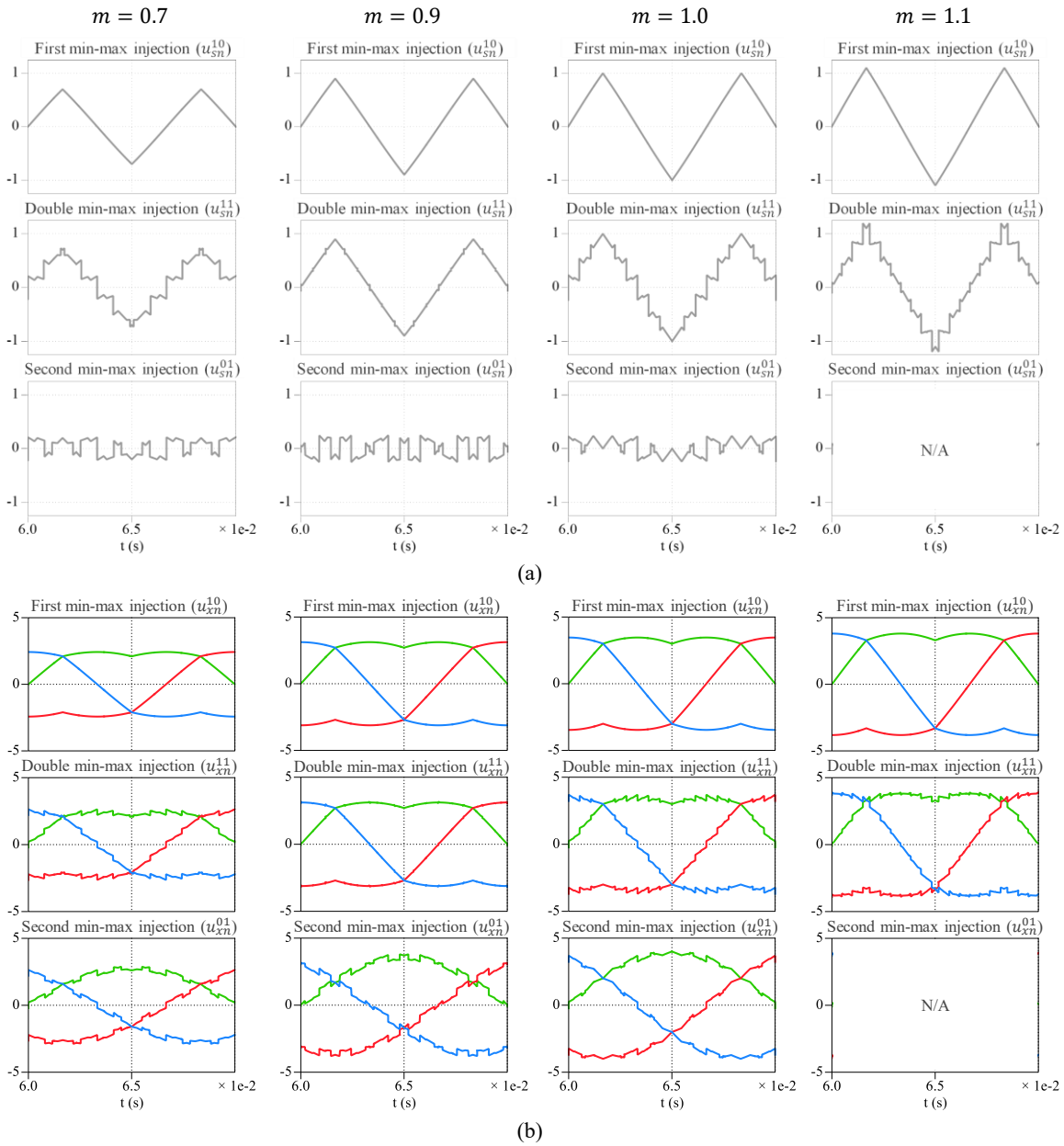


Figure 4.10: (a) First (10), double (11), and second (01) offset voltage waveforms and (b) the resulting three-phase leg voltage reference waveforms for different modulation indices ($m \geq 0.7$).

harmonics is significantly smaller than the fundamental for all the methods. The second injection showing a much lower magnitude of the switching frequency harmonic sideband (2 kHz) is of particular interest for each of the shown modulation index points. The switching frequency harmonics beyond the second multiple (i.e., 4 kHz) are insignificant.

In Figure 4.8, the largest current THD difference between the double and second injection can be seen at $m = 0.3$. At this point, the leg voltage references produced are shown in Figure 4.13a for comparison. Likewise, Figure 4.13b (left) shows a comparison – in simulation – between the current waveforms at this operating point. It is evident that the

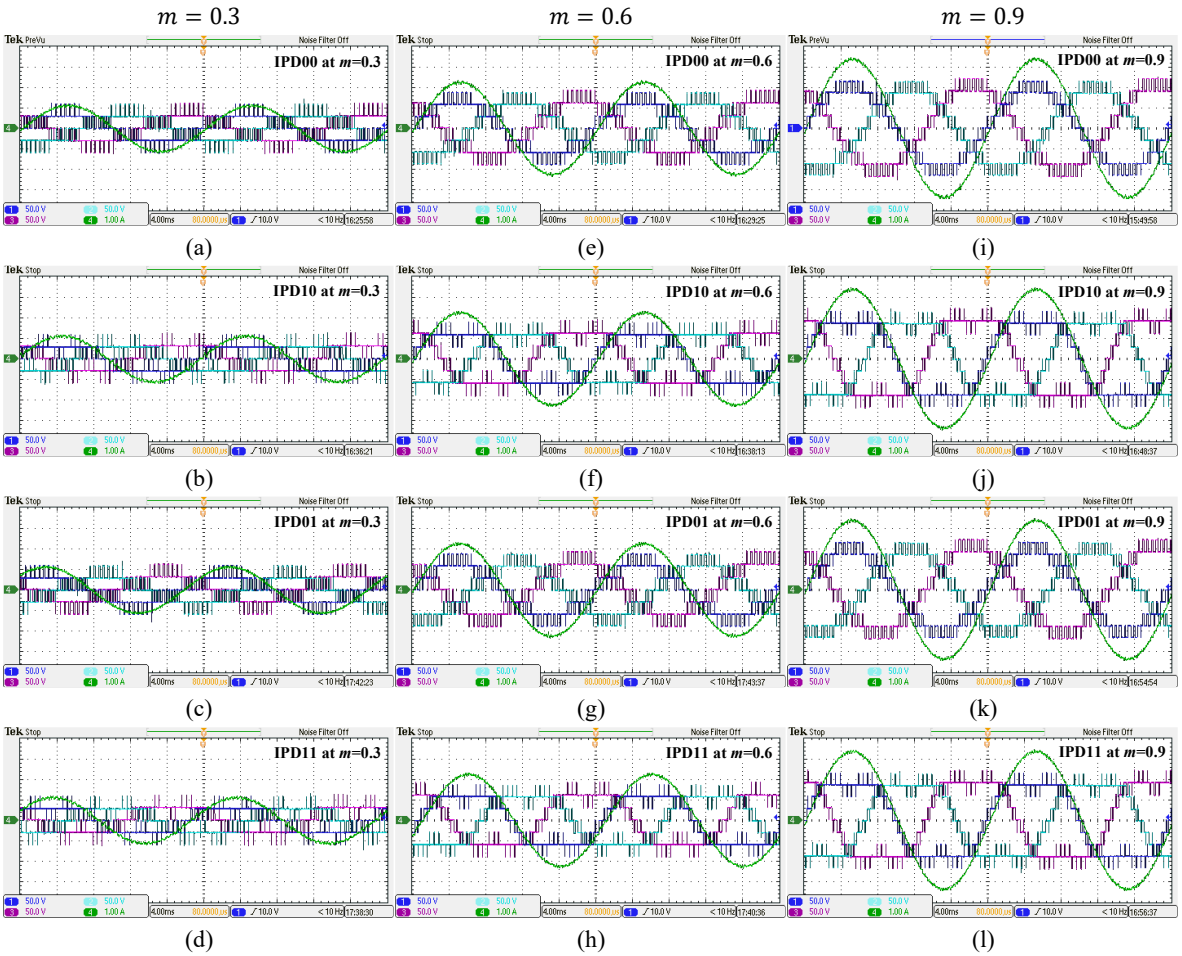


Figure 4.11: Leg voltages and phase 'a' current waveforms produced with IPD-PWM under different injections with sinusoidal (00), first (10), second (01), double (11) min-max injections from top to bottom, respectively for modulation indices of (a)-(d) $m = 0.3$, (e)-(h) $m = 0.6$, and (i)-(l) $m = 0.9$.

double min-max (11) injection produces a larger current ripple compared to the second min-max (01) injection. Similarly, a higher ripple frequency of the phase current waveform under the second min-max (01) injection is obvious. A higher ripple frequency leads to a lower current THD value for certain modulation index points. The second offset (01) injection still ensures even distribution of the zero voltage vectors at the beginning and end of the modulation period while centring the active voltage vectors without returning a high total harmonic distortion at certain modulation depths. In contrast, at $m = 0.7$, both the double (11) and second min-max (01) injections produce similar THD values. A comparison between the current waveforms at this point shows a similar ripple frequency (Figure 4.13b right) as expected.

It is widely accepted that the in-phase disposition (IPD) PWM returns the best harmonic performance in comparison to other carrier-based methods. The spectral

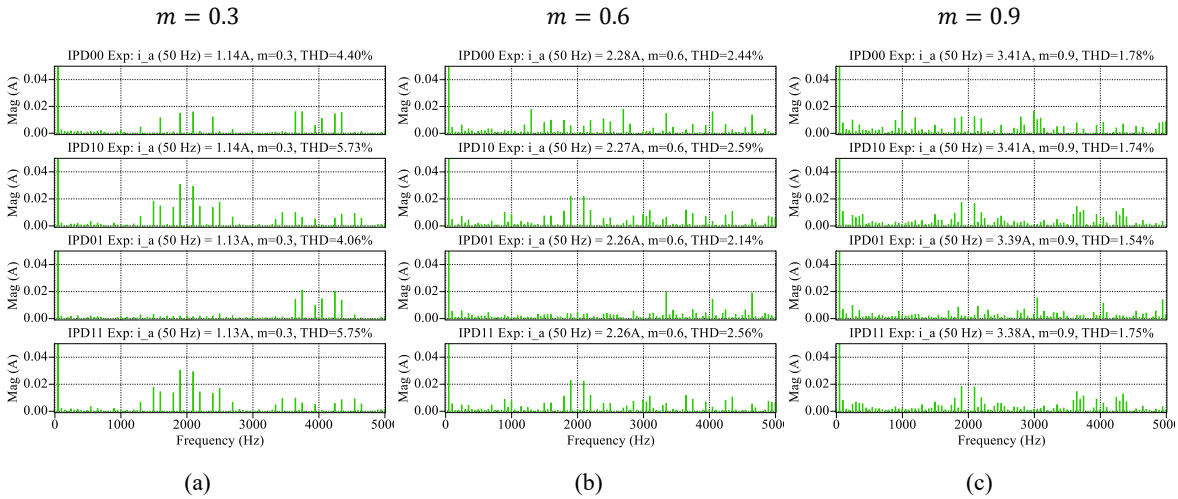


Figure 4.12: Phase 'a' current spectra for waveforms shown in Figure 4.11 under different injections with sinusoidal (00), first (10), second (01), double (11) min-max injections from top to bottom, respectively for modulation indices of (a) $m = 0.3$, (b) $m = 0.6$, and (c) $m = 0.9$.

equivalence between SV-PWM and IPD-PWM with an appropriate offset voltage injection is well known for multilevel converters. However, the centring of the active voltage vectors while keeping the zero voltage vectors at the beginning and end of the carrier interval does not necessarily achieve the best harmonic performance of the phase current while using the first (two-level) and double (multilevel) min-max offset voltage injections.

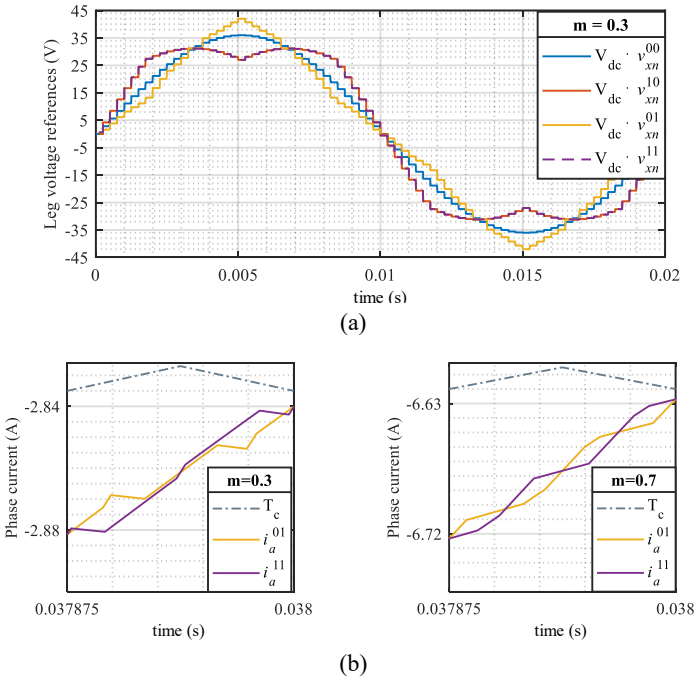


Figure 4.13: (a) Leg voltage references under different injections ($m = 0.3$) and (b) simulation results ($f_c = 8$ kHz) for the current ripple during same carrier interval ($T_c = 1/f_c$) for second and double min-max injections for $m = 0.3$ (left) and $m = 0.7$ (right).

It has been shown through a comparison between these offset injections for different multicarrier modulation methods that under certain regions of the modulation index range, the second min-max (01) injection returns better harmonic performance of the phase current in contrast to the double min-max (11) injection. This is due to a reduction of the phase current ripple leading to lower total harmonic distortion in these regions of the modulation index. When comparing modulation methods that can provide extension of the modulation index range, one can see that double min-max (11) injection gives better results than the first min-max (10) injection. However, a combination of second min-max (01) injection for $m \leq 1$, and the double min-max injection (11) for $m > 1$ would result in the best performance.

4.3 Unequal dc-source voltage conditions

In certain applications of the CHB converter, a natural variation in the dc-source voltages exists, typically when isolated dc-sources such as batteries are employed. This is often due to manufacturing tolerances, operating conditions, or irregular aging of different cells within a battery. This can also happen in case of a fault in one or more modules of the CHB converter. This causes an imbalance in the total dc source voltage between the converter legs. In such situations, balanced three-phase operation of the CHB converter is compromised with an accompanying reduction in the available modulation index depth. Multiple approaches have been suggested to resolve this issue. For example, the fundamental selective harmonic elimination to achieve balanced three-phase operation for hybrid electric vehicles was suggested in (Tolbert et al., 2003). Space-vector (SV) PWM based approaches include a state-transition based method such as (Ye et al., 2020). Another SV-PWM method, used to balance dc-link voltages in a CHB converter based on activation of multiple series connected three-level H-bridges, is presented in (Lewicki et al., 2023).

Although SV-PWM methods provide a higher degree of control, they can become cumbersome for multilevel converter control. Therefore, carrier-based approaches are generally the preferred choice. Among these, the voltage imbalance issue is addressed through the so-called neutral voltage shift method which involves moving the converter neutral point to achieve balanced three-phase line voltages and currents (Rodriguez et al., 2005). A neutral voltage shift method based on a zero-sequence voltage injection was implemented by (Maharjan et al., 2010) for balanced three-phase operation of a PS modulated CHB where battery SoC balancing in energy storage systems was also shown. Meanwhile, a generalised approach for fault tolerant operation of a three-phase CHB using

carrier based offset voltage injection was proposed in (Carnielutti et al., 2012). An extension of the same method was developed in (López et al., 2024) for post fault operation of multilevel multiphase medium-voltage drive using x-y component voltage injection. Similarly, authors of (Lingom et al., 2022) have presented a PWM method based on three-dimensional space vector analysis using a voltage feedback control loop.

The issue of unequal total dc-source voltages was tackled by the authors of (Cho et al., 2014) using the so-called neutral voltage modulation (NVM) which is based on the neutral voltage shift method. A recent improvement on the NVM method in (Kim and Cho, 2022) prevents operation of the drive in the over modulation region and shows promising results for the extension of the linear modulation range. However, the authors did not consider individual module voltage imbalance. Additionally, the phase shifted (PS) PWM method was employed which suffers from certain drawbacks such as high THD of phase voltages and currents, especially at low modulation indices. Furthermore, PS-PWM is known to produce undesirable harmonic components at twice the H-bridge equivalent carrier frequency. Modification of the PS-PWM method has been proposed through the introduction of variable carrier phase shift angles for the elimination of the above-mentioned low order switching harmonic components, but a valid solution of the resulting equations is not always possible (Marquez et al., 2017).

The objective of this section is to provide an application of the improved NVM method, suggested in (Kim and Cho, 2022), using a modified LS-PWM instead of originally used PS PWM. The issue of total dc-leg voltage imbalance is discussed using the PS-PWM and the associated issues are highlighted using simulation results. Next, the necessary modification of the standard LS-PWM method in unequal operating conditions are illustrated and its implementation is presented. Simulation results are shown to confirm the extension of the linear modulation index range while eliminating the double carrier frequency harmonic issue of the unipolar PS-PWM in unbalanced dc-link voltage conditions. Additionally, the suggested method is shown to realise better energy management of the batteries. In this way, both module level balancing over time, as well as maximizing the modulation index range for a balanced three-phase operation in unsymmetrical conditions, is shown to have been achieved.

4.3.1 Unbalanced dc-link operation using PS-PWM

To illustrate the operation of a CHB under unbalanced dc-source voltage conditions, a simple case based on sinusoidal leg voltages will be presented. This will be followed by methods that allow extension of the linear modulation index range with the use of appropriate offset voltage injections including the min-max and NVM injection. These cases are best explained with the help of voltage and current waveforms obtained by simulation to show the effects of different dc-link voltages. Modelling and simulation were conducted in PLECS. A three-phase CHB converter with unequal dc-source voltages was developed using ideal MOSFET switches (i.e., voltage drop neglected). Dead time was not implemented for simplicity. The dc-source voltages considered for the CHB converter with $k = 4$ modules per leg are shown in Table 4.2.

The CHB was connected to a balanced three-phase RL load in wye configuration with $R = 20\ \Omega$ and $L = 10$ mH. The three-phase reference waveforms were based on sinusoidal phase voltages with a fundamental frequency of 50 Hz. Comparison between the multicarrier PS-PWM and LS-PWM methods was made at the same average switching frequency of the devices to ensure a fair comparison. An equivalent carrier switching frequency (f_{c_PS}) of 500 Hz per H-bridge module was considered with an overall inverter switching frequency of 4 kHz. For the implementation of the LS-PWM ($f_{c\_LS} = 4$ kHz), the IPD-PWM method was chosen due to its superior harmonic performance.

Consider the CHB with the dc-link voltages described in Table 4.2. It can be noted that the total dc-link voltages of converter legs a, b, and c are $V_{dc\_a} = 120$ V, $V_{dc\_b} = 100$ V, and $V_{dc\_c} = 40$ V, respectively. Therefore, the maximum achievable modulation index depth varies for the three presented cases (sinusoidal, min-max injection, and NVM) as follows.

Table 4.2: CHB dc-source voltages and total dc-source voltages.

Leg A	Leg B	Leg C
$V_{dc\_a1} = 26$ V	$V_{dc\_b1} = 26$ V	$V_{dc\_c1} = 5$ V
$V_{dc\_a2} = 30$ V	$V_{dc\_b2} = 22$ V	$V_{dc\_c2} = 8$ V
$V_{dc\_a3} = 33$ V	$V_{dc\_b3} = 24$ V	$V_{dc\_c3} = 12$ V
$V_{dc\_a4} = 31$ V	$V_{dc\_b4} = 28$ V	$V_{dc\_c4} = 15$ V
$V_{dc\_a} = 120$ V	$V_{dc\_b} = 100$ V	$V_{dc\_c} = 40$ V

4.3.1.1 Sinusoidal reference (Sin)

The simplest case occurs when a sinusoidal reference is considered. Without any intervention (no offset injection), it is obvious that the maximum leg voltage that can be synthesised by the CHB, for balanced operation, is limited by the minimum value of the total dc-link voltage – phase c in the considered case ($V_{dc\_c} = V_{dc\_min}$). Thus, the maximum achievable voltage in the considered case is 40 V, for balanced three-phase operation.

Figure 4.14 shows operation at this point (from $t = 0$ ms to $t = 40$ ms) where balanced phase voltages and currents are obtained. Also shown are the leg voltage waveforms where all nine-voltage levels are utilised by leg c as to produce the desired phase voltage of 40 V. In contrast, leg a and b voltages contain only five voltage levels. However, setting the reference voltages to 46 V (at $t = 40$ ms) and 80 V (at $t = 80$ ms), the consequence of overmodulation is apparent where leg c voltage goes into overmodulation. This leads to asymmetries and the distortion of the three-phase voltages and currents as obvious from $\alpha\beta$ plane.

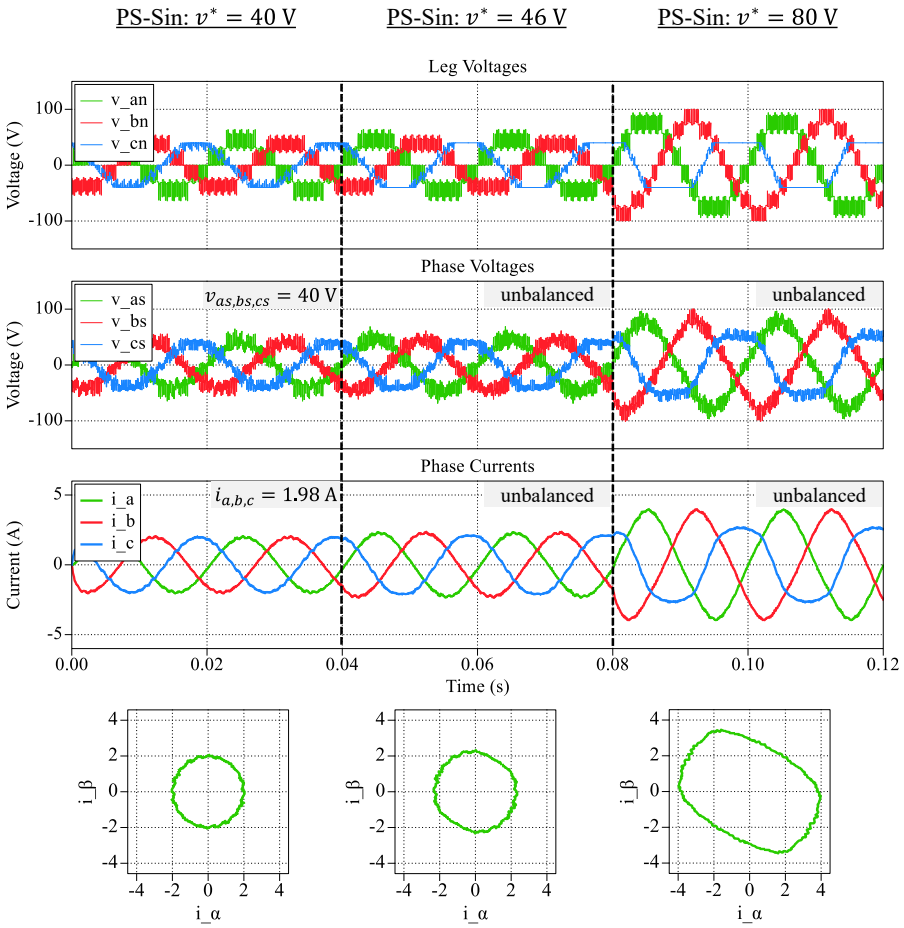


Figure 4.14: Imbalanced CHB operation with sinusoidal PS-PWM at different reference voltages. The obtained leg voltages, phase voltages, phase currents and their projections into the $\alpha\beta$ plane (from top to bottom).

4.3.1.2 Min-max injection (MM)

The modulation index range can be extended through the injection of a common-mode voltage by up to $2/\sqrt{3}$. The injected common-mode voltage can vary from the third harmonic (of one-sixth amplitude) to the injection of the well-known min-max injection. In asymmetrical conditions where the total available dc-source voltage in each leg is different, the min-max injection can also be used to further improve the modulation index depth.

Application of the min-max injection to the case at hand leads to an increase in the modulation depth to approximately 46.1 V ($= 40 \cdot 2/\sqrt{3}$). It can be seen from Figure 4.15 that in contrast to Figure 4.14, the phase currents are now balanced at the reference of 46 V even though leg c enters overmodulation region. However, it is obvious that beyond this point, balanced operation is no longer possible, and the phase currents become imbalanced at a reference voltage of 80 V.

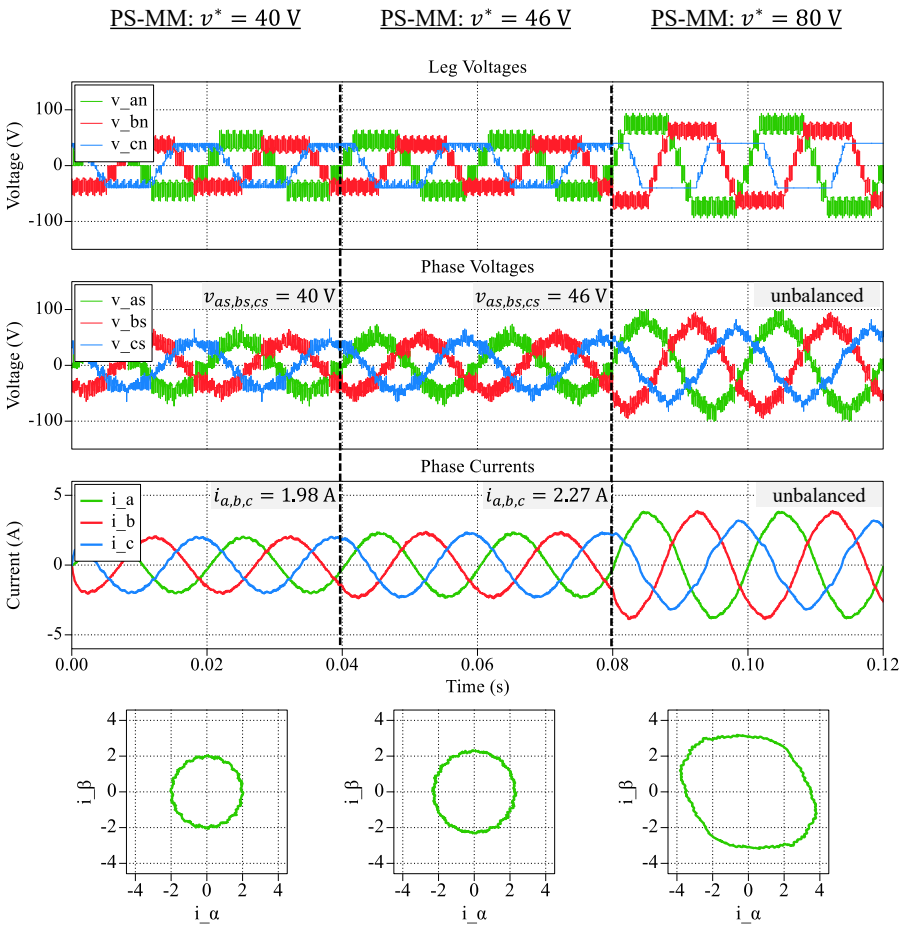


Figure 4.15: Imbalanced CHB operation with min-max injection under PS-PWM at different reference voltages. The obtained leg voltages, phase voltages, phase currents and their projections into the $\alpha\beta$ plane (from top to bottom).

4.3.1.3 Neutral voltage modulation (NVM)

As noted earlier, authors of (Kim and Cho, 2022) have proposed a neutral voltage modulation method using the PS-PWM. The NVM method will be summarized in the following for completeness before proceeding with the analysis at hand.

The NVM method is based on the extension of the traditional min-max injection, to further increase the available modulation depth, from $2/\sqrt{3}$ in the case of the min-max injection, to a maximum synthesisable phase voltage of V_{ph_max} in unbalanced dc-source voltage conditions. This (V_{ph_max}) is dependent on the minimum and middle total dc-source voltages between the converter legs. The minimum and middle dc-source voltage limits can be defined as:

$$\begin{aligned} V_{dc\_min\_limit} &= \frac{2}{3}\left(\frac{V_{dc\_max} - V_{dc\_min}}{V_{dc\_max}}\right) \\ V_{dc\_mid\_limit} &= \frac{2}{3}\left(\frac{V_{dc\_max} - V_{dc\_mid}}{V_{dc\_max}}\right) \end{aligned} \tag{4.15}$$

where V_{dc_min}, V_{dc_mid}, and V_{dc_max} stand for the minimum, middle, and the maximum total dc-source voltages of the three converter legs. The maximum synthesisable phase voltage of V_{ph_max} can thus be defined as:

$$V_{ph\_max} = \left(\frac{4}{3} - V_{dc\_mid\_limit} - V_{dc\_min\_limit}\right)\left(V_{dc\_max}\frac{\sqrt{3}}{2}\right) \tag{4.16}$$

If all total dc-source voltages are equal, then V_{ph_max} simplifies to $\frac{2}{\sqrt{3}}kV_{dc}$ (for k modules of the CHB), as expected. A simplification of (4.16) results in:

$$V_{ph\_max} = \frac{V_{dc\_mid} + V_{dc\_min}}{\sqrt{3}} \tag{4.17}$$

This means that the maximum achievable phase voltage is dependent on the middle (V_{dc_mid}) and minimum (V_{dc_min}) dc-source voltages. First, a weighing factor (K_w), considering the middle and minimum dc-source voltages, is defined as:

$$K_w = \frac{V_{dc\_mid} + V_{dc\_min}}{2} \tag{4.18}$$

Next, the weighing factors for each phase leg are calculated as:

$$K_{w\_a} = \frac{K_w}{V_{dc\_a}}, \quad K_{w\_b} = \frac{K_w}{V_{dc\_b}}, \quad K_{w\_c} = \frac{K_w}{V_{dc\_c}} \tag{4.19}$$

The original phase voltage references (v_{as}^*, v_{bs}^*, and v_{cs}^*) are then scaled with the weighing factors calculated in (4.19) such that:

$$v'_{as} = K_{w\_a} v_{as}^* , \quad v'_{bs} = K_{w\_b} v_{bs}^* , \quad v'_{cs} = K_{w\_c} v_{cs}^* \tag{4.20}$$

The next step involves the calculation of the appropriately scaled neutral voltage, based on the scaled phase voltage references, with the min-max operation by:

$$v'_{sn} = \frac{v'_{max} + v'_{min}}{2} \tag{4.21}$$

where v'_{max} and v'_{min} are the respective maximum and minimum instantaneous values of the scaled phase voltage references (v'_{as}, v'_{bs}, and v'_{cs}) from (4.20). Further conditions are stipulated on the calculated neutral voltage to avoid operation in the overmodulation index range by limiting the minimum ($v_{sn\_min}^*$) and maximum ($v_{sn\_max}^*$) values of the neutral voltage references through:

$$\begin{aligned} v_{sn\_min}^* &= \max\left(v_{as}^* - V_{dc\_a},\ v_{bs}^* - V_{dc\_b},\ v_{cs}^* - V_{dc\_c}\right) \\ v_{sn\_max}^* &= \min\left(v_{as}^* + V_{dc\_a},\ v_{bs}^* + V_{dc\_b},\ v_{cs}^* + V_{dc\_c}\right) \end{aligned} \tag{4.22}$$

with the neutral voltage limited between the calculated values as:

$$v_{sn\_min}^* < v'_{sn} < v_{sn\_max}^* \tag{4.23}$$

Therefore, when the calculated neutral voltage lies outside the defined range, its value is limited and chosen through the following condition:

$$v''_{sn} = \begin{cases} v^*_{sn\_min}, & \text{if } v'_{sn} > v^*_{sn\_max} \\ v^*_{sn\_max}, & \text{if } v'_{sn} < v^*_{sn\_min} \\ v'_{sn}, & \text{if } v^*_{sn\_min} < v'_{sn} < v^*_{sn\_max} \end{cases} \tag{4.24}$$

However, the application of (4.24), under certain conditions, may lead to a different polarity between the phase (v^*_{xs}) and leg (v^*_{xn}) voltage references and produce an excessive neutral voltage (v'_{sn}). Therefore, another condition is stipulated on the calculation of the neutral voltages by:

$$v''_{sn} = \begin{cases} v^*_{max}, & \text{if } v'_{sn} > v^*_{max} \\ v^*_{min}, & \text{if } v'_{sn} < v^*_{min} \\ v'_{sn}, & \text{if } v^*_{min} < v'_{sn} < v^*_{max} \end{cases} \tag{4.25}$$

$$v^*_{max} = \max(v^*_{as}, v^*_{bs}, v^*_{cs}),\ v^*_{min} = \min(v^*_{as}, v^*_{bs}, v^*_{cs})$$

The leg voltage references (v^*_{xn}) are then expectedly calculated, using the injection of the scaled neutral voltage (v''_{sn}), as:

$$v^*_{xn} = v^*_{xs} - v''_{sn} \tag{4.26}$$

where x is any of the three (a, b, or c) phases. It should be pointed out that in (4.26), the neutral voltage is assumed to be subtracted from the phase references, whereas in (4.8), the neutral voltage was assumed to be added to the phase reference. These are both equivalent because of the presence of a negative sign in the min-max calculation in (4.7). The implementation of the above mentioned NVM in PLECS is shown in Figure 4.16. The reader is directed to the original paper (Kim and Cho, 2022) for further details on the improved NVM method.

For the case under discussion, the middle and minimum dc-source voltages are 100 V and 40 V, respectively. The offset voltage (v''_{sn}) waveforms produced for the desired phase references of 60 V, 70 V, and 80 V and the resulting three-phase leg voltage reference waveforms are shown in Figure 4.17. Application of (4.17) to the case at hand (Table 4.2) leads to the maximum balanced obtainable phase voltage of 80.8 V. As the maximum synthesisable phase reference of 80 V is approached, the reference leg voltage waveforms

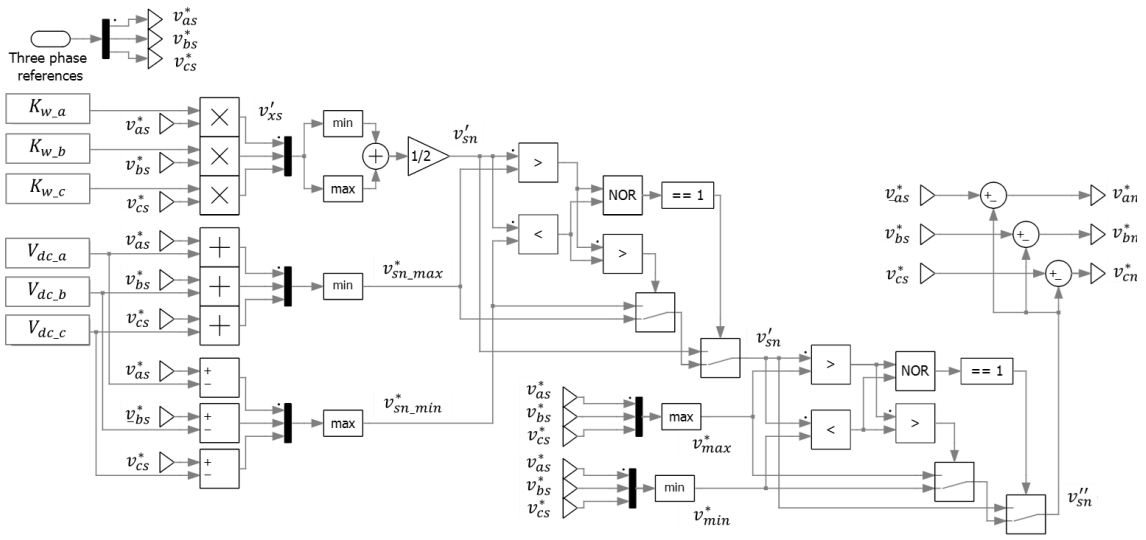


Figure 4.16: Implementation of neutral voltage modulation method in PLECS

demonstrate appropriate scaling to account for the total dc-source limitation imposed by each converter leg. As a result, the reference voltages v^*_{bn} and v^*_{cn} are limited to 100 V and 40 V, respectively.

The extension of the modulation index range can be demonstrated through the application of the NVM method, where a desired reference voltage of 80 V produces balanced three-phase voltages and currents as shown in Figure 4.18. It must also be pointed

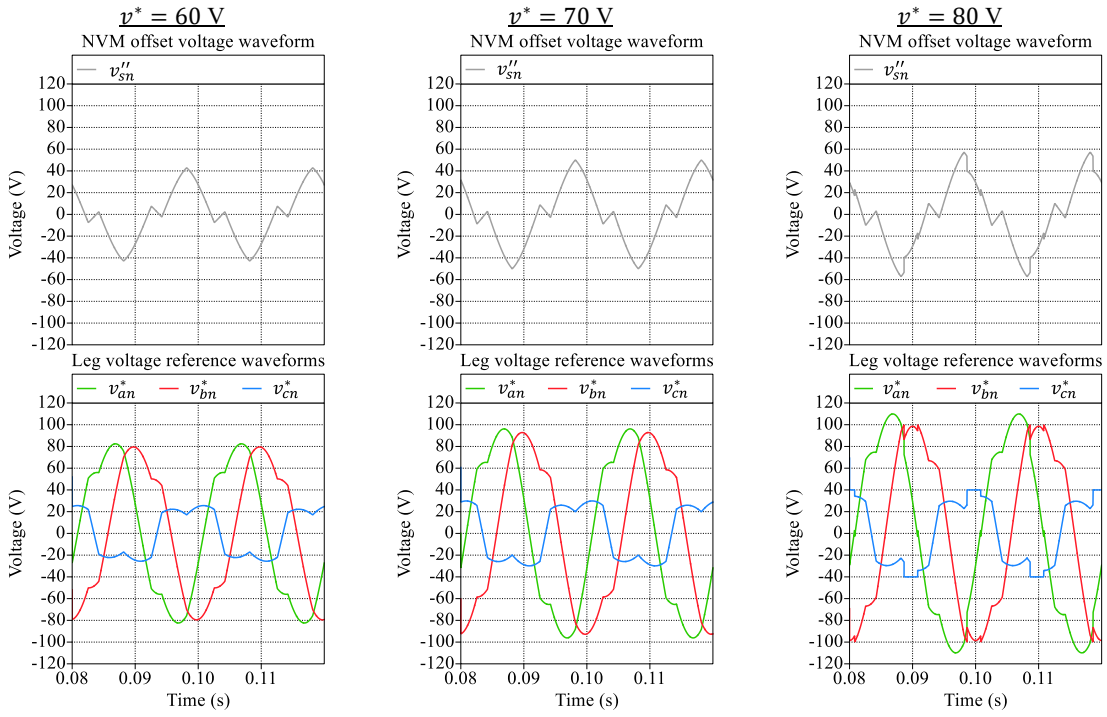


Figure 4.17: NVM offset voltage waveforms and the resulting three-phase leg voltage reference waveforms for phase references of 60 V, 70 V, and 80 V.

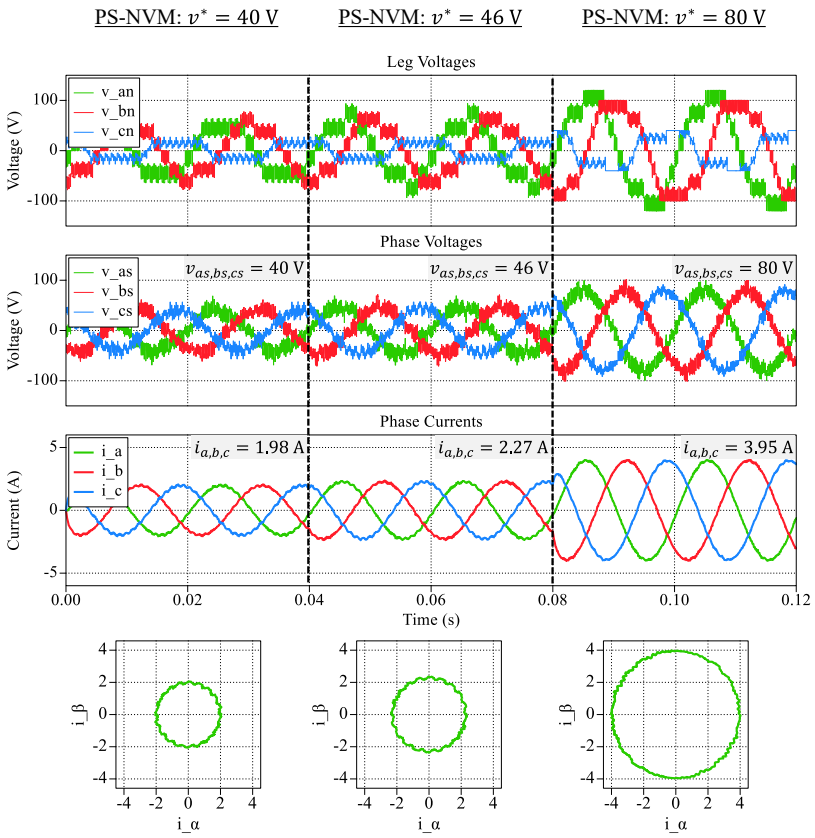


Figure 4.18: Imbalanced CHB operation with NVM injection under PS-PWM at different reference voltages. The obtained leg voltages, phase voltages, phase currents and their projections into the $\alpha\beta$ plane (from top to bottom).

out that in the case of balanced (equal) dc-source leg voltages, the NVM methodology produces identical results to those achieved through the min-max injection.

It is evident that the NVM method using the PS-PWM proposed by (Kim and Cho, 2022) produces balanced three-phase voltages and currents. However, the authors have not considered the inevitable voltage imbalance between the dc-sources within each converter leg. Two primary issues arise in unbalanced dc-link conditions which can be highlighted as follows.

Firstly, the dominant harmonic lies around the inverter switching frequency (4 kHz) with equal dc-source voltages, when using the PS-PWM method, as seen in Figure 4.19a. However, when dc-sources of different voltages are present, a ripple at twice the equivalent H-bridge switching frequency (1 kHz) are produced which can be observed in the harmonic spectra of the phase voltages and currents as shown in Figure 4.19b. A comparison between the leg c voltage waveforms of the CHB for equal (Figure 4.19c) and unequal dc-source voltages (Figure 4.19d) shows the source of the problem. In unipolar PS-PWM, each H-Bridge output generates the waveforms at twice the carrier frequency (which is 500 Hz

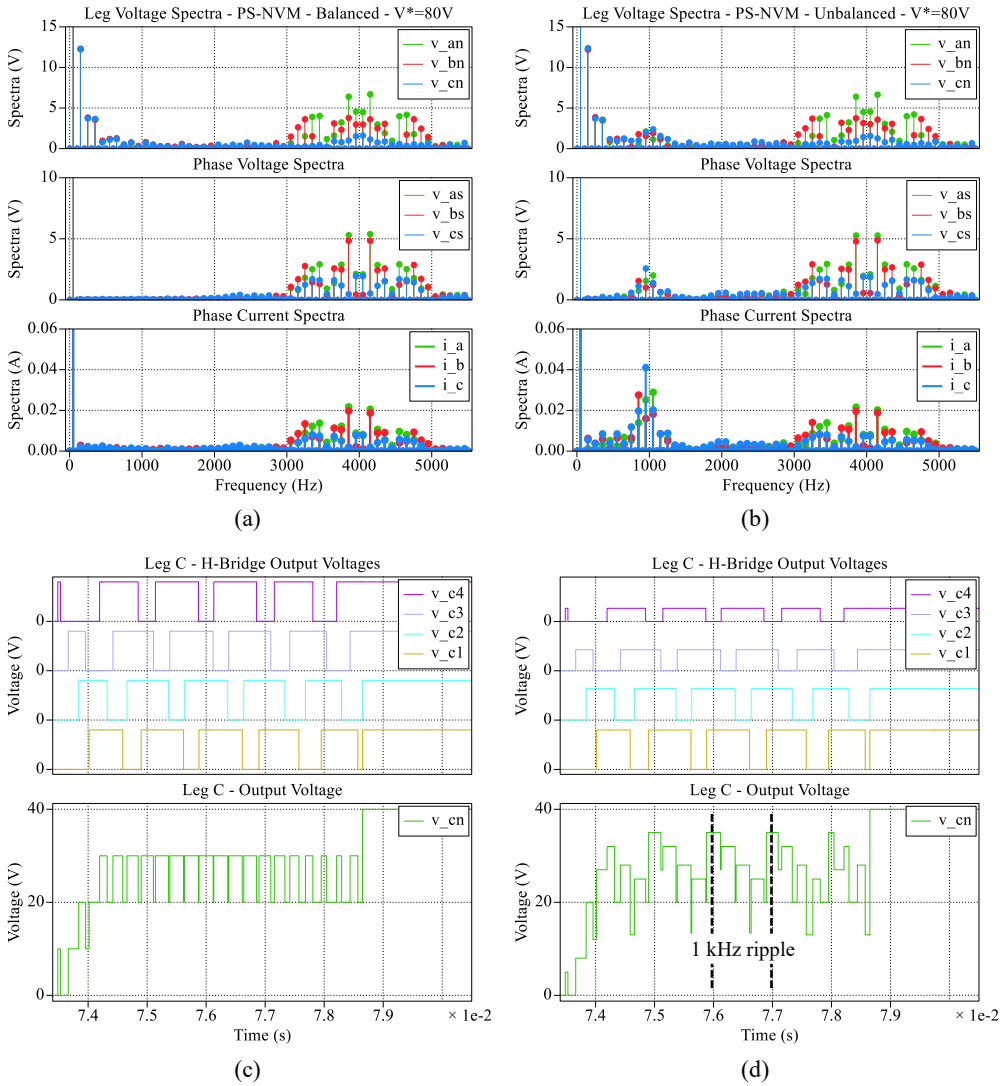


Figure 4.19: Harmonic spectra for PS-PWM in (a) equal and (b) unequal dc-source voltage conditions. Leg C H-bridge output voltages in (c) equal and (d) unequal dc-source voltage conditions.

in the considered case). Therefore, the benefit of the standard PS-PWM where the dominant harmonics of the converter lie at $2k$ times carrier frequency is lost when there are unbalanced dc link voltages.

Secondly, in equal dc-source voltage conditions, the PS-PWM is rightly lauded for its natural balancing capabilities in terms of dc-source utilisation as well as device conduction times. However, even in module voltage imbalance conditions, use of PS-PWM leads to an equal discharge of all the dc-sources at the same rate, which is undesirable since the initial battery SoCs are different. Both mentioned challenges can be addressed with the following modification of the standard LS-PWM.

4.3.2 Recommended alternative using LS-PWM

The classical level-shifted PWM method with balanced dc-source voltage conditions has already been discussed in subsection 3.4.3. As the in-phase disposition (IPD) PWM is known to offer the best harmonic performance among the three LS-PWM methods, it has therefore been used to produce the results in the following simulations. However, it is necessary to adjust the modulation regions in case of module dc-link voltage imbalance for the correct implementation of the IPD-PWM scheme.

4.3.2.1 LS-PWM in unbalanced dc-source conditions

Application of the standard LS-PWM results in an incorrect activation of the H-bridge modules if a fixed value for all the dc-link voltages is assumed. For example, if all the battery voltages in Leg A started out at 30 V each, but drifted to other voltage levels, then the application of the IPD-PWM scheme would wrongly assign an equal modulation index region to all the H-bridge dc-sources. This would result in an improper scaling of the modulation index leading to an incorrect activation of the H-bridge modules and the desired voltage would not be properly produced.

Logically, all H-bridge dc-sources must not be assumed to contribute equally to the synthesis of a desired leg voltage. Therefore, an appropriate scaling and distribution of the modulation index is necessary. Consider the dc-link conditions mentioned in Table 4.2. An appropriate scaling of the modulation index range has been shown in Figure 4.20a (right hand side scale), for the positive half-cycle of the fundamental. The calculation of the modulation index is thus made depending on the actual available dc-link voltage of each module.

The duty references [0-1] for a desired voltage level can be calculated using the schematic shown in Figure 4.21. These are used for comparison with the carrier waveforms to produce device gating signals. This would lead to the correct activation of the respective H-bridges in unbalanced dc-link voltage conditions. It should be noted that the carrier waveforms should be appropriately phase-shifted with respect to each other to achieve the correct implementation of the IPD-PWM, as mentioned in subsection 3.5.4.

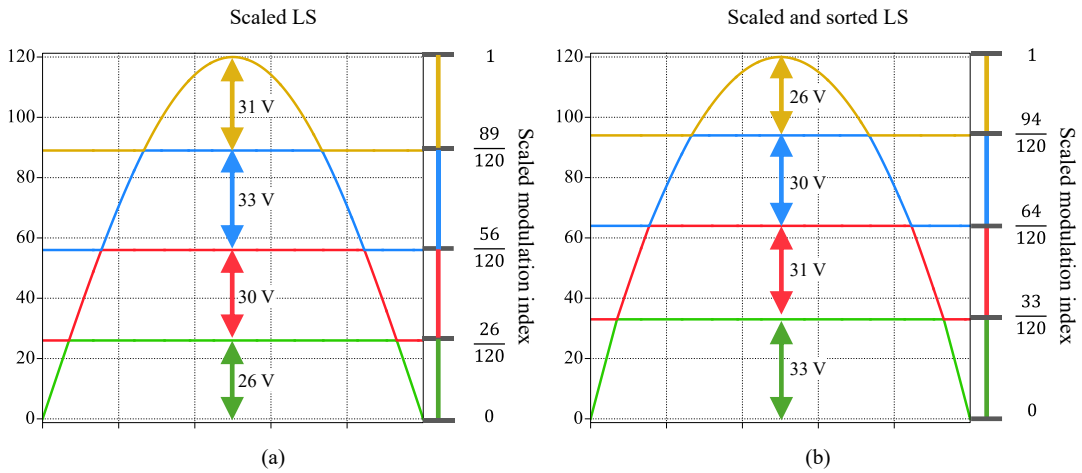


Figure 4.20: (a) Scaled LS-PWM with unequal dc-source voltages and (b) Scaled and sorted LS-PWM with unequal dc-source voltages for dc-link voltage balancing (positive half-cycle).

The same scenarios as in subsection 4.3.1 have been repeated using the LS-PWM with the above-mentioned modification of the scaling of the modulation index. The simulation results are shown in Figure 4.22, Figure 4.23, and Figure 4.24 (corresponding to Figure 4.14, Figure 4.15, and Figure 4.18, respectively).

The maximum achievable modulation index with all three methods (Sin, min-max, NVM) remains the same. However, the above-mentioned problem of lower order switching harmonics (around 1 kHz) has now been resolved as seen in Figure 4.25 (to be compared with Figure 4.19 a and b, respectively). Also, usage of LS-PWM, contributes to lower THD values in phase voltages and currents, as can be seen in Table 4.3.

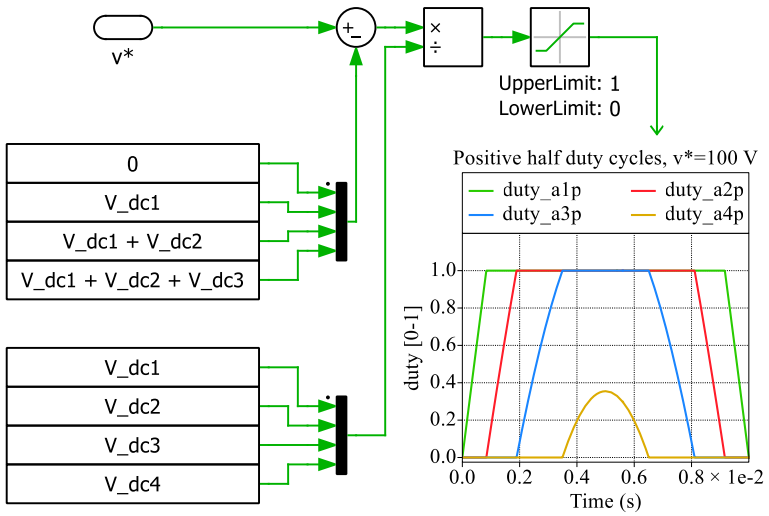


Figure 4.21: Schematic showing scaling and duty-cycle calculation for the LS-PWM for unbalanced dc-source operation.

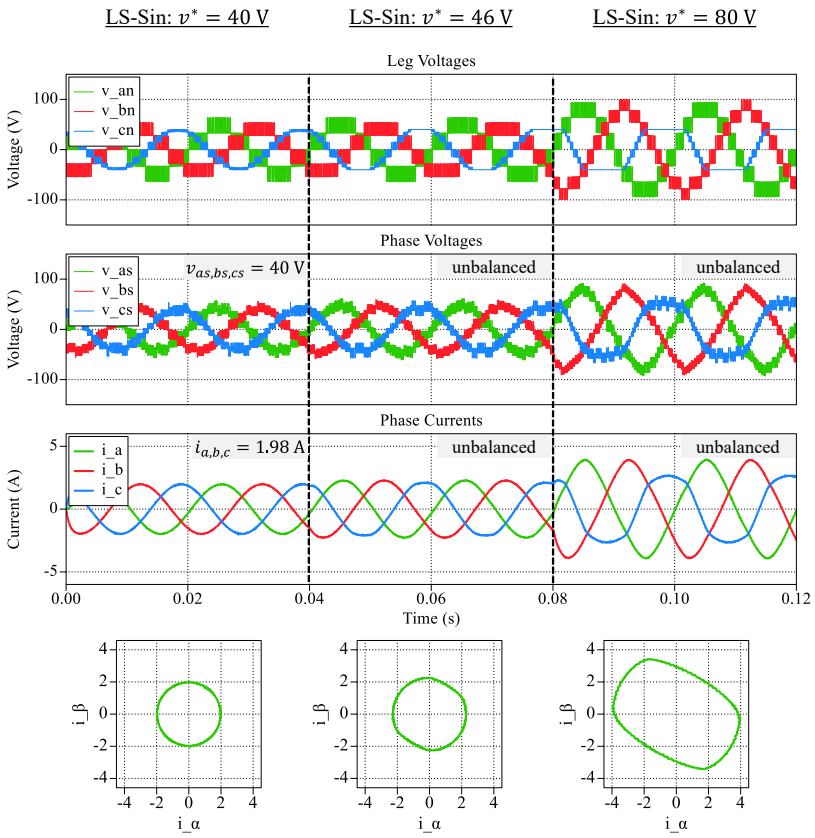


Figure 4.22: Imbalanced CHB operation with sinusoidal LS-PWM at different reference voltages. The obtained leg voltages, phase voltages, phase currents and their projections into the $\alpha\beta$ plane (from top to bottom).

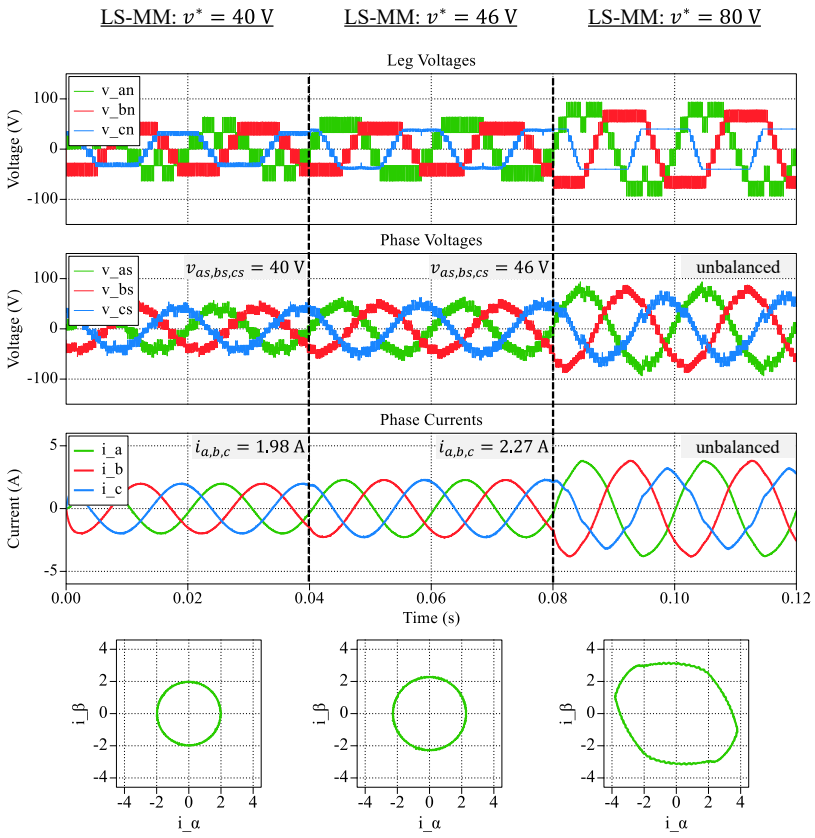


Figure 4.23: Imbalanced CHB operation with min-max injection under LS-PWM at different reference voltages. The obtained leg voltages, phase voltages, phase currents and their projections into the $\alpha\beta$ plane (from top to bottom).

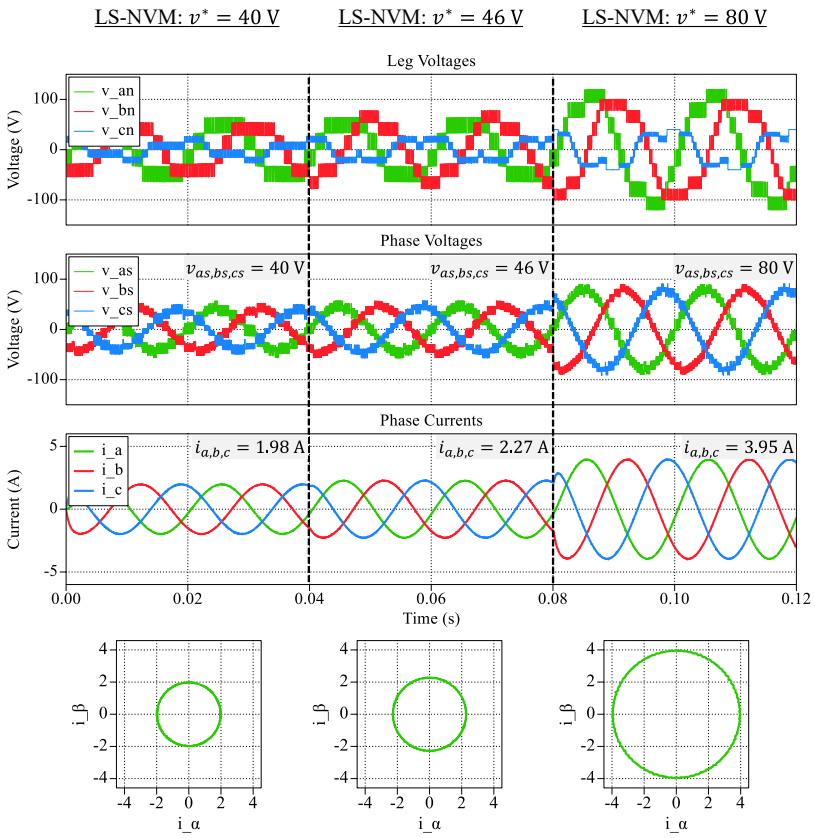


Figure 4.24: Imbalanced CHB operation with NVM injection under LS-PWM at different reference voltages. The obtained leg voltages, phase voltages, phase currents and their projections into the $\alpha\beta$ plane (from top to bottom).

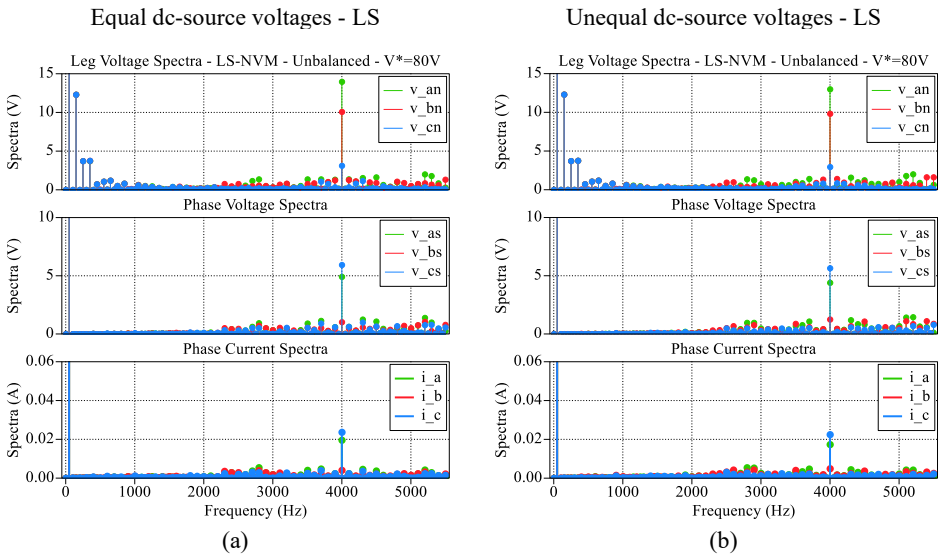


Figure 4.25: Harmonic spectra for LS-PWM in (a) equal and (b) unequal dc source voltage conditions.

Although the desired phase voltages have been produced, this solution is not ideal as this mode of operation would lead to the highest utilisation of the dc-source voltage assigned to the bottom of the modulation index range (26 V dc-source). A simple solution to this problem is presented in the next subsection.

Table 4.3: Phase current THD comparison in equal and unequal dc-source voltage conditions.

	$\mathbf{THD}(i_a)$	$\mathbf{THD}(i_b)$	$\mathbf{THD}(i_c)$
PS-PWM - Equal	1.2%	1.1%	0.7%
PS-PWM - Unequal	1.6%	1.5%	1.6%
LS-PWM - Equal	0.7%	0.4%	0.7%
LS-PWM - Unequal	0.7%	0.5%	0.6%

4.3.2.2 Module dc-link voltage balancing

In PS-PWM, all dc-sources are equally utilised, and a natural balanced power distribution is achieved. However, in case of dc source voltage imbalance, continuous equal power distribution forces all the dc-sources to discharge at the same rate, maintaining the imbalance as illustrated in Figure 4.26, where times T1 and T2 denote an initial and a final time.

In contrast, the LS-PWM is known to cause imbalanced energy dissipation of the dc-sources. This aspect of the LS-PWM can be used as a feature to achieve balancing in the case of initially unbalanced dc-source voltages. It is known that the battery terminal voltage is directly related to its SoC. Therefore, it is necessary to ensure that the battery with the highest voltage (SoC) is used for the longest duration to maximise the battery discharge time.

This can be achieved through a simple sorting of the battery voltages from high to low (see Figure 4.20b). The battery with the lowest voltage is assigned to the top the modulation index range which essentially minimises its discharge time thus reducing its energy consumption. This is especially true for operation in partial load operation (lower modulation indices) since the battery with the lowest voltage is not used. In contrast, the battery with the highest voltage contributes the greatest energy and is placed at the bottom of the modulation index range. This process can be reversed when power is flowing into the batteries, for example during charging mode or regenerative braking, for better battery SoC management. Periodic sampling, sorting and appropriate assignment of the measured battery voltages thus leads to the convergence of the battery voltages over time using the LS-PWM. This can be seen in Figure 4.26 where battery energy consumptions for both the PS- and LS-PWM methods over a period of time are shown. It should be noted that a reassignment of the respective dc-sources becomes necessary when the voltage of one dc-source falls below that of the other (beyond T2 in Figure 4.26b for dc-sources v_{dc_a2} and v_{dc_a4}). In this way, by choosing to activate the appropriate H-bridges the user can obtain a high level of control over the battery SoCs.

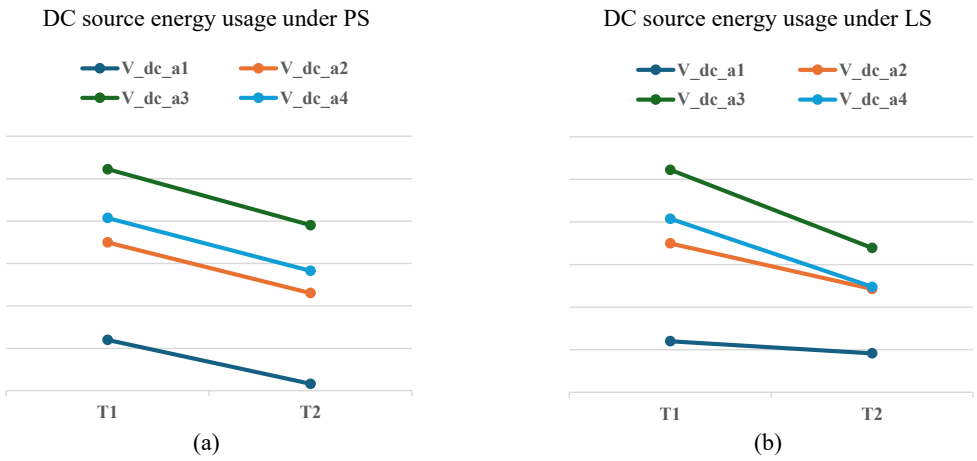


Figure 4.26: Comparison between energy expenditure of dc-sources with unequal voltages in Leg A of the CHB under NVM at $v^* = 80$ V using (a) Standard PS-PWM and (b) Scaled and sorted LS-PWM.

To conclude, an application of the improved NVM method from (Kim and Cho, 2022) with a modified LS-PWM method for CHB with unbalanced dc-link conditions was presented. The method described is shown to address both the module-level voltage imbalance as well as the leg-voltage imbalance at the same time with a slightly increased control complexity. Different energy dissipation rates of the dc-sources were shown leading to balancing of the dc-source voltages over time, resulting in better battery management. At the same time, the issue of low order switching harmonic components in PS-PWM was avoided. Other disadvantages associated with PS-PWM in unbalanced dc-source voltage conditions, such as low THD of the phase voltages and currents were also mitigated while maximizing the modulation index depth.

4.4 Summary

This chapter presented a discussion on the role of different offset voltage injections in the operation of the CHB inverter under balanced and unbalanced dc-source voltage conditions. It was shown that the extension of the modulation index range as well as an improvement of the harmonic performance of a CHB inverter can be made through appropriate offset voltage injections for the whole modulation index range.

The whole modulation index range was evaluated in terms of the phase current THD for different min-max based offset voltage injections (including the second min-max injection) in CHB inverters for the first time in (Khan et al., 2022) for the PS and the three LS modulation methods. It was shown that the LS IPD-PWM returned the lowest current THD among all the modulation methods investigated. Experimental results obtained showed

an average THD difference of around 1.8% between IPD-PWM and the PS, POD and APOD-PWM methods at unity modulation index (Figure 4.6). The effect was more pronounced at lower modulation indices with the difference increasing to around 2.8% at $m = 0.75$, 3.9% at $m = 0.5$, and to 5.0% at $m = 0.25$. In the overmodulation region, a slightly lower difference of around 1.6% was observed.

Within the IPD-PWM, the results obtained for different zero sequence min-max based voltage injections revealed superior load current THD performance of the second min-max injection for modulation indices below unity whereas the double min-max injection was found to perform best in the extended modulation index range. The difference in the current THD between the second min-max and other injections was most obvious in certain regions of the modulation index range. This included regions around modulation index points of $m = 0.3$, 0.6, and 0.9 with a respective difference of 0.3%, 0.3%, and 0.2%. In the overmodulation region, a slightly lower benefit of 0.1% is achieved (Figure 4.8).

Next, the extension of the modulation index range for balanced operation of the CHB inverter in unbalanced dc-source voltage conditions was investigated through the NVM injection method proposed by (Kim and Cho, 2022). The performance of the originally proposed method, which is based on the PS-PWM, was further improved with a modification to the standard LS-PWM method for dc-source voltage imbalance conditions. Two issues of the method adopted by (Kim and Cho, 2022) were resolved with the suggested method in subsection 4.3.2. First, the harmonics present at $2f_c$ in the standard PS-PWM (Figure 4.19) were eliminated with the suggested modification to the LS modulation method. Furthermore, the current THD achieved with the suggested LS based method was lower (~0.6%) compared to that of the PS method (~1.5%) for the considered case, which is an added advantage (Table 4.3).

Secondly, the method proposed by (Kim and Cho, 2022) does not consider the voltage imbalance between the dc-sources of each converter leg. Therefore, even in unequal dc-source voltage conditions, they discharge at the same rate. This is unfavourable as the dc-source (battery) with the lowest SoC becomes a limiting factor, reducing overall run time. The proposed improvement allows placement of the dc-source (battery) with the highest voltage (SoC) at the lower end of the modulation index range and that with the lowest voltage (SoC) being placed at the top of the modulation index range. Hence, the dc-source (battery) with the highest voltage (SoC) contributes more energy while the dc-source (battery) with

the lowest voltage is only used for full-load (high modulation) operation (Figure 4.20). This leads to the extension of the operating range due to better energy management of individual dc-sources (batteries) under dc-source voltage imbalance. Thus, the suggested method (Khan et al., 2024b) is a significant performance enhancement over the originally proposed method (Kim and Cho, 2022).

Chapter 5
Multiphase machine modelling and control with a multilevel inverter

5.1 Introduction

This chapter presents modelling and control of a multiphase machine when supplied by a cascaded H-bridge multilevel inverter. The previous chapters focused on finding suitable modulation algorithms for the operation of the CHB MLI in both equal and unequal dc-source voltage conditions with appropriate offset voltage injections to achieve extension of the modulation index range as well as make improvements in the harmonic performance of the phase current. The methods were tested using a static RL load to confirm their suitability. Further verification of the described methods is performed on a three-phase and six-phase induction machine operating under open-loop v/f control, and rotor flux-oriented control, respectively.

First, the generalised mathematical model of an n-phase squirrel cage induction machine, in the phase variable domain and after transformation into the rotational reference frame, is introduced in section 5.2 to develop an understanding of multiphase induction machines. Next, section 5.3 provides a description of the field-oriented control of multiphase machines. In the last section 5.4, implementation of the open and closed-loop speed control of three- and multiphase induction machines using the cascaded H-bridge inverter, used in previous chapters, is presented. Experimental results are given under different operating conditions to verify the operation of the considered multilevel multiphase drive. Finally, operation of the multilevel multiphase drive under unbalanced dc-source voltage conditions in the CHB inverter is presented. The methods discussed in section 4.3 are extended to the multiphase case and applied to achieve balanced operation of the multiphase machine with an improvement in the range of the modulation index depth using the modified LS-PWM method. Simulation results confirm the accuracy of the applied methodology. A part of the work presented in this chapter, based on experimental results, has been published in (Khan et al., 2024a).

5.2 Modelling of multiphase induction machines

Induction machines are extensively used in industry due to their simple design, low cost, ease of maintenance, high reliability, and robust construction which enables them to operate in harsh environments. The three-phase induction machine can be considered to be a subset of multiphase induction machines. Generally, machines are termed multiphase if the number of machine phases are greater than three. The difference in the spatial displacement angle between any two consecutive phases further classifies a multiphase machine into a symmetrical or asymmetrical type. An n-phase machine is generally formed by g winding sets with p phases per winding set, described by:

$$n = pg \tag{5.1}$$

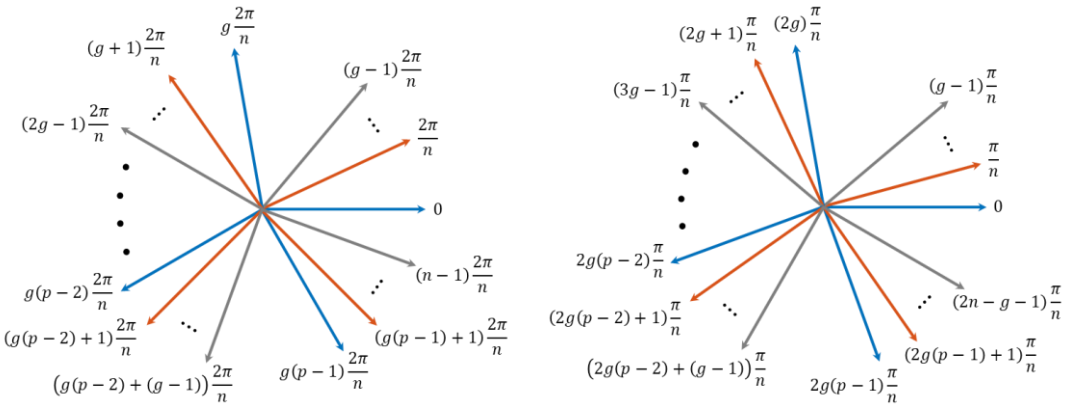
where $p \in 3, 5, 7, 11, \ldots$ and $g \geq 1$. Multiphase machines with a single winding set can only be of the symmetrical configuration. However, induction machines with multiple winding sets ($g \geq 2$) can be of either the symmetrical or asymmetrical type. The most preferred multiphase machines in practice are based on multiple ($g \geq 2$) three-phase winding sets ($p = 3$) due to enhanced fault tolerant capabilities as well as the possibility to use off-the-shelf three-phase converter technology. The phase propagation angle for a symmetrical multiphase machine is $\frac{2\pi}{n}$ (Figure 5.1a) whereas for an asymmetrical multiphase machine the spatial phase shift between different winding sets is $\frac{\pi}{n}$ (Figure 5.1b). The angular positions of the machine phases for all symmetrical machines can be described by:

$$\theta_{sym} = \frac{2\pi}{n}[0 \quad 1 \quad \cdots \quad n-2 \quad n-1] \tag{5.2}$$

If symmetrical multiphase machines with multiple three-phase winding sets ($p = 3$) are considered, then the angular positions are distributed in the following manner:

$$\theta_{sym} = \frac{2\pi}{n}[0 \quad \cdots \quad g-2 \quad g-1 \quad | \quad g \quad \cdots \quad 2g-2 \quad 2g-1 \quad | \quad 2g \quad \cdots \quad 3g-2 \quad 3g-1] \tag{5.3}$$

The angular positions of the machine phases for asymmetrical machines in general case would be:



(a) (b)

Figure 5.1: Phase propagation angles of an n-phase machine with (a) symmetrical and (b) asymmetrical winding configuration.

$$\theta_{asym} = \frac{\pi}{n}[0 \quad \cdots \quad g-1 \quad | \quad 2g \quad \cdots \quad 3g-1 \quad | \quad \cdots \quad | \quad 2g(p-1) \quad \cdots \quad 2g(p-1)+(g-1)] \tag{5.4}$$

For asymmetrical multiphase machines with multiple three-phase winding sets ($p = 3$), the angular positions are described by:

$$\theta_{asym} = \frac{\pi}{n}[0 \quad \cdots \quad g-2 \quad g-1 \quad | \quad 2g \quad \cdots \quad 3g-2 \quad 3g-1 \quad | \quad 4g \quad \cdots \quad 5g-2 \quad 5g-1] \tag{5.5}$$

5.2.1 Phase variable domain model

The generalised model of an induction machine in the phase variables domain is introduced first to develop an understanding and appreciation of the multiphase induction machine. Multiphase machine modelling is carried out by making certain assumptions that are necessary to simplify the resulting machine model. All windings are considered to be identical and in the appropriate configuration (symmetrical/asymmetrical) with the angular displacement as described earlier [(5.2/(5.4)]. It is assumed that the magneto-motive force (mmf) created by the stator and rotor windings have a sinusoidal spread around the air-gap circumference. The stator phase windings are assumed with a constant uniform airgap of circular cross-section, thus neglecting the effect of slotting of the stator and rotor. Only the fundamental spatial harmonic of the mmf is taken into consideration while all other spatial harmonics are neglected. The number of rotor and stator phases are considered to be equal for simplicity. The machine parameters such as winding resistances and leakage inductances remain constant. The magnetising characteristics of the ferromagnetic material are

considered to be linear. The eddy current and iron losses are also neglected along with the parasitic capacitances.

The mathematical modelling of multiphase machines can be conducted in instantaneous time domain phase variables in terms of non-linear first order differential equations. The mutual inductances between the stator and rotor vary with the relative position between the stator and rotor windings and are as such a function of rotor position. The stator and rotor quantities are denoted with indices s and r, respectively. The voltage equilibrium equations for the stator and rotor can be given in matrix form as:

$$[v_s] = [R_s][i_s] + \frac{\mathrm{d}}{\mathrm{d}t}[\psi_s] \tag{5.6}$$

$$[v_r] = [R_r][i_r] + \frac{\mathrm{d}}{\mathrm{d}t}[\psi_r] \tag{5.7}$$

where the stator and rotor voltages, currents, and the flux linkages are defined with matrices as:

$$[v_s] = [v_{1s} \quad v_{2s} \quad \dots \quad v_{ns}]^T \tag{5.8}$$

$$[v_r] = [v_{1r} \quad v_{2r} \quad \dots \quad v_{nr}]^T \tag{5.9}$$

$$[i_s] = [i_{1s} \quad i_{2s} \quad \dots \quad i_{ns}]^T \tag{5.10}$$

$$[i_r] = [i_{1r} \quad i_{2r} \quad \dots \quad i_{nr}]^T \tag{5.11}$$

$$[\psi_s] = [\psi_{1s} \quad \psi_{2s} \quad \dots \quad \psi_{ns}]^T \tag{5.12}$$

$$[\psi_r] = [\psi_{1r} \quad \psi_{2r} \quad \dots \quad \psi_{nr}]^T \tag{5.13}$$

The stator and rotor resistance matrices, $[R_s]$ and $[R_s]$ are diagonal $n \times n$ matrices defined as:

$$[R_s] = \begin{bmatrix} R_{1s} & 0 & \cdots & 0 \\ 0 & R_{2s} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & R_{ns} \end{bmatrix} \tag{5.14}$$

$$[R_r] = \begin{bmatrix} R_{1r} & 0 & \cdots & 0 \\ 0 & R_{2r} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & R_{nr} \end{bmatrix} \tag{5.15}$$

The rotor voltages in equation (5.9) are zero as the rotor windings are short-circuited in squirrel-cage induction machines. Generally, the stator resistance for each phase winding can be considered to be identical which leads to $R_{1s} = R_{2s} = R_{ns} = R_s$ and $R_{1r} = R_{2r} = R_{nr} = R_r$. The stator and rotor flux linkages are related to the stator and rotor currents through inductance matrices such as the stator inductance matrix $[L_s]$, rotor inductance matrix $[L_r]$, and the mutual stator-to-rotor inductance matrix $[L_{sr}]$ by:

$$[\psi_s] = [L_s][i_s] + [L_{sr}][i_r] \tag{5.16}$$

$$[\psi_r] = [L_r][i_r] + [L_{rs}][i_s] \tag{5.17}$$

where:

$$[L_{rs}] = [L_{sr}]^T \tag{5.18}$$

Due to the assumption of constant parameters, and since both the stator and rotor are assumed to be perfectly symmetrical (**symmetrical machine**) with windings that are mutually fixed, the stator and rotor inductance matrices contain constant coefficients only. The stator inductance matrix, for a symmetrical machine, can be given as:

$$[L_s] = \begin{bmatrix} L_{11s} & L_{12s} & \cdots & L_{1ns} \\ L_{21s} & L_{22s} & \cdots & L_{2ns} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n1s} & L_{n2s} & \cdots & L_{nns} \end{bmatrix} \tag{5.19}$$

The self-inductances for the stator phase windings are equal, i.e., $L_{11s} = L_{22s} = \cdots = L_{nns} = L_{ls} + M$, where L_{ls} is the stator leakage inductance and M is the maximum value of the mutual magnetising inductance. The mutual inductances take on $(n-1)/2$ different values. The stator inductance matrix is thus formed by:

$$[L_s] = L_{ls}[I_{n\times n}] + M \begin{bmatrix} \cos(0) & \cos(\alpha) & \cdots & \cos\big((n-1)\alpha\big) \\ \cos(-\alpha) & \cos(0) & \cdots & \cos\big((n-2)\alpha\big) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(-(n-1)\alpha) & \cos(-(n-2)\alpha) & \cdots & \cos(0) \end{bmatrix} \tag{5.20}$$

where $I_{n\times n}$ is an $n \times n$ identity matrix. Similarly, the rotor inductance matrix is given as:

$$[L_r] = \begin{bmatrix} L_{11r} & L_{12r} & \cdots & L_{1nr} \\ L_{21r} & L_{22r} & \cdots & L_{2nr} \\ \vdots & \vdots & \ddots & \vdots \\ L_{n1r} & L_{n2r} & \cdots & L_{nnr} \end{bmatrix} \tag{5.21}$$

Again, the self-inductances for the rotor phase windings are equal, i.e. $L_{11r} = L_{22r} = \cdots = L_{nnr} = L_{lr} + M$, where L_{lr} is the rotor leakage inductance and M is the maximum value of the mutual magnetising inductance. The rotor inductance matrix is given as:

$$[L_r] = L_{lr}[I_{n\times n}] + M\begin{bmatrix} \cos(0) & \cos(\alpha) & \cdots & \cos\big((n-1)\alpha\big) \\ \cos(-\alpha) & \cos(0) & \cdots & \cos\big((n-2)\alpha\big) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(-(n-1)\alpha) & \cos(-(n-2)\alpha) & \cdots & \cos(0) \end{bmatrix} \tag{5.22}$$

In contrast to the constant valued stator and rotor inductance matrices, the stator-to-rotor mutual inductance matrix is composed of time varying coefficients. This is obviously due to the continuously changing instantaneous position of rotor phase winding magnetic axis in relation to the stationary stator phase winding magnetic axis as the rotor spins. If the instantaneous electrical position of the first rotor phase winding magnetic axis in relation to the first stator phase winding magnetic axis is defined as θ_e, then the electrical speed of rotation of the rotor can be given as:

$$\theta_e = \int \omega_e \mathrm{d}t + \theta_{e0} \tag{5.23}$$

where θ_{e0} is the initial angle between the first stator and rotor magnetic axis. This angle can be assumed to be zero if it can be ensured that the axes are aligned. The stator-to-rotor mutual inductance matrix can be defined as:

$$[L_{sr}] = M\begin{bmatrix} \cos(\theta_e) & \cos(\theta_e + \alpha) & \cdots & \cos(\theta_e + (n-1)\alpha) \\ \cos(\theta_e - \alpha) & \cos(\theta_e) & \cdots & \cos(\theta_e + (n-2)\alpha) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(\theta_e - (n-1)\alpha) & \cos(\theta_e - (n-2)\alpha) & \cdots & \cos(\theta_e) \end{bmatrix} \tag{5.24}$$

In the case of **asymmetrical machines**, the angular displacement between the winding sets differs from that of the symmetrical machine as mentioned previously. Therefore, the definition of the inductance matrices needs to take this into account. The rotor

is still modelled as a symmetrical structure which leads to the simplification of the model without loss of generality. The inductance matrix for the rotor is hence defined as:

$$[L_r] = L_{lr}[I_{n\times n}] + M\begin{bmatrix} \cos(0) & \cos(2\alpha) & \cdots & \cos\big((2n-2)\alpha\big) \\ \cos((2n-2)\alpha) & \cos(0) & \cdots & \cos\big((2n-4)\alpha\big) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(2\alpha) & \cos(4\alpha) & \cdots & \cos(0) \end{bmatrix} \tag{5.25}$$

In asymmetrical machines, the number of winding sets is ($g \geq 2$) and modelling of the stator as an asymmetrical structure leads to the stator self-inductance matrix, consisting of constant terms, being calculated as:

$$[L_s] = L_{ls}[I_{n\times n}] + M\begin{bmatrix} [L_{s1}]_{g\times g} & [L_{s2}]_{g\times g} & \cdots & [L_{sp}]_{g\times g} \\ [L_{sp}]_{g\times g} & [L_{s1}]_{g\times g} & \cdots & [L_{s(p-1)}]_{g\times g} \\ \vdots & \vdots & \ddots & \vdots \\ [L_{s2}]_{g\times g} & [L_{s3}]_{g\times g} & \cdots & [L_{s1}]_{g\times g} \end{bmatrix} \tag{5.26}$$

where ($p \times p$) individual inductance matrices of dimension ($g \times g$) can be calculated using the expression:

$$[L_{s(i+1)}] = \begin{bmatrix} \cos(\epsilon_i) & \cos(\epsilon_i + \alpha) & \cdots & \cos(\epsilon_i + (g-1)\alpha) \\ \cos(\epsilon_i - \alpha) & \cos(\epsilon_i) & \cdots & \cos(\epsilon_i + (g-2)\alpha) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(\epsilon_i - (g-1)\alpha) & \cos(\epsilon_i - (g-2)\alpha) & \cdots & \cos(\epsilon_i) \end{bmatrix} \tag{5.27}$$

and the angle between the phases of a single winding set is described by:

$$\epsilon_i = \frac{2\pi i}{p}, \qquad i = 0, 1, 2, \ldots, (p-1) \tag{5.28}$$

On the other hand, the time-varying inductance terms arising from the mutual inductance between the stator and the rotor windings can be defined similarly with:

$$[L_{sr}] = \begin{bmatrix} [L_{sr1}]_{g\times g} & [L_{sr2}]_{g\times g} & \cdots & [L_{srp}]_{g\times g} \\ [L_{srp}]_{g\times g} & [L_{sr1}]_{g\times g} & \cdots & [L_{sr(p-1)}]_{g\times g} \\ \vdots & \vdots & \ddots & \vdots \\ [L_{sr2}]_{g\times g} & [L_{sr3}]_{g\times g} & \cdots & [L_{sr1}]_{g\times g} \end{bmatrix} \tag{5.29}$$

where the individual mutual inductance matrices can be calculated with the following expression, as before using (5.28):

$$[L_{sr(i+1)}] = M\begin{bmatrix} \cos(\theta_e + \epsilon_i) & \cos(\theta_e + \epsilon_i + \alpha) & \cdots & \cos(\theta_e + \epsilon_i + (g-1)\alpha) \\ \cos(\theta_e + \epsilon_i - \alpha) & \cos(\theta_e + \epsilon_i) & \cdots & \cos(\theta_e + \epsilon_i + (g-2)\alpha) \\ \vdots & \vdots & \ddots & \vdots \\ \cos(\theta_e + \epsilon_i - (g-1)\alpha) & \cos(\theta_e + \epsilon_i - (g-2)\alpha) & \cdots & \cos(\theta_e + \epsilon_i) \end{bmatrix} \quad (5.30)$$

The complete inductance matrix can thus be formed appropriately for a symmetrical or asymmetrical machine, as:

$$[L] = \begin{bmatrix} [L_s] & [L_{sr}] \\ [L_{rs}] & [L_r] \end{bmatrix} \quad (5.31)$$

The mechanical speed of rotation (ω_m) is related to the electrical speed of rotation (ω_e) through:

$$\omega_e = P \cdot \omega_m \quad (5.32)$$

where P is the number of magnetic pole pairs. The mechanical speed of the rotor is related to the electromagnetic torque (T_e) developed by the machine, the applied mechanical load torque (T_l) and inertia of the rotating mass (J) by:

$$T_e - T_l = J\,\frac{\mathrm{d}\omega_m}{\mathrm{d}t} \quad (5.33)$$

From (5.32) and (5.33), a similar expression in terms of the electrical speed of rotation of the rotor can be given as:

$$T_e - T_l = \frac{J}{P}\frac{\mathrm{d}\omega_e}{\mathrm{d}t} \quad (5.34)$$

The electromagnetic torque produced by the machine can be described as:

$$T_e = P\,\frac{1}{2}[i]^T\,\frac{\mathrm{d}[L]}{\mathrm{d}\theta_e}[i] \quad (5.35)$$

where the stator and rotor current matrices form the total current matrix defined as:

$$[i] = [\,[i_s]^T\ \ [i_r]^T\,]^T \quad (5.36)$$

For multiphase machines with a uniform airgap, the electromagnetic torque is created exclusively because of the interaction between the stator and rotor phase windings. Therefore, equation (5.35) can be simplified to:

$$T_e = P[i_s]^T \frac{\mathrm{d}[L_{\mathrm{sr}}]}{\mathrm{d}\theta_e}[i_r] \tag{5.37}$$

The mathematical model given completely describes an n-phase induction machine in terms of phase variables. It consists of $2n$ voltage equilibrium first-order differential equations and a mechanical equilibrium differential equation. Variable mutual stator-to-rotor inductances lead to a non-linear system of differential equations with time-varying coefficients. A simplification of the machine model is achieved through transformation of the phase-variables into a new set of fictitious variables through appropriate transformations which will be discussed in the following.

5.2.2 Multiphase machine model in arbitrary reference frame

The multiphase machine model in phase-variable form can be transformed into multiple mutually orthogonal two-dimensional subspaces and an appropriate number of zero sequence components using the Clarke's decoupling transformation. This results in the simplification of the machine model as the pair of quantities in each subspace are decoupled from other subspaces. For a symmetrical n-phase induction machine with an even number of phases, the transformation produces an n-phase model with $n/2$ subspaces. On the other hand, for a machine with an odd number of phases, the transformation produces an $\frac{n-1}{2}$ subspaces with an additional real-valued unidimensional quantity. The following relationship holds between the phase variables and the new set of variables:

$$\left[f_{\alpha\beta,x_1y_1,\dots z_+z_-}\right] = [T_{VSD}]_{n\times n}\left[f_{1,2,\dots,n}\right]_{n\times 1} \tag{5.38}$$

where the original phase variables (voltage, current, or flux linkages) matrix $\left[f_{1,2,\dots,n}\right]_{n\times 1}$ is transformed to a new set of variables in the matrix $\left[f_{\alpha\beta,x_1y_1,\dots z_+z_-}\right]$ through multiplication with the Clarke's decoupling transformation matrix $[T_{VSD}]_{n\times n}$ (also known as the Vector Space Decomposition, VSD, matrix). The transformation matrix differs depending on the number of phases, on the type of the multiphase machine considered (symmetrical or

asymmetrical), as well as on the number of neutral points of the machine winding sets. VSD transformation matrix for several configurations in given in the Appendix A.

The rotational transformation, also known as the Park's transformation, can be used for the elimination of time varying inductance terms which are present only in the α-β subspace. This is achieved by bringing both the stator and rotor windings from the α-β reference frames to a common reference frame where both sets of windings rotate together without any relative motion between them. Upon application of the rotational transformation, the model of the machine is transformed into new fictitious variables in a common (d-q) reference frame, which is rotating at an arbitrarily chosen angular speed, further details can be found in Appendix B.

The stator and rotor variables in d-q reference frame can thus be calculated by multiplication of the appropriate transformation matrix, $[D_s]$ for stator, and $[D_r]$ for rotor [see ((B.3) and ((B.4)], with the respective quantities in the α-β reference frame by:

$$\left[f_{dqxyz}\right] = [D]\left[f_{\alpha\beta xyz}\right] \tag{5.39}$$

An n-phase induction machine model obtained after the transformation can be described with four first order differential equations which relate the flux linkages and respective stator and rotor voltages. It follows that the complete model of the multiphase induction machine can then be described by the following set of differential equations:

$$v_{ds} = R_s i_{ds} + \frac{\mathrm{d}\psi_{ds}}{\mathrm{d}t} - \omega_a \psi_{qs} \tag{5.40}$$

$$v_{qs} = R_s i_{qs} + \frac{\mathrm{d}\psi_{qs}}{\mathrm{d}t} + \omega_a \psi_{ds} \tag{5.41}$$

$$v_{dr} = R_r i_{dr} + \frac{\mathrm{d}\psi_{dr}}{\mathrm{d}t} - (\omega_a - \omega_e)\psi_{qr} = 0 \tag{5.42}$$

$$v_{qr} = R_r i_{qr} + \frac{\mathrm{d}\psi_{qr}}{\mathrm{d}t} + (\omega_a - \omega_e)\psi_{dr} = 0 \tag{5.43}$$

As can be seen from equations (5.42) and (5.43), the rotor voltages are set as equal to zero since the rotor windings are short circuited at the terminals. The x-y and zero sequence equations for the stator voltages are given as:

$$v_{x_k s} = R_s i_{x_k s} + \frac{\mathrm{d}\psi_{x_k s}}{\mathrm{d}t} \tag{5.44}$$

$$v_{y_k s} = R_s i_{y_k s} + \frac{\mathrm{d}\psi_{y_k s}}{\mathrm{d}t} \tag{5.45}$$

$$v_{z_+ s} = R_s i_{z_+} + \frac{\mathrm{d}\psi_{z_+}}{\mathrm{d}t} \tag{5.46}$$

$$v_{z_- s} = R_s i_{z_-} + \frac{\mathrm{d}\psi_{z_-}}{\mathrm{d}t} \tag{5.47}$$

where the subscript index k is indicative of the subspace number and takes values from 1 to $(n-3)/2$ for machines with an odd number of machine phases and $(n-4)/2$ for machines with an even number of phases. Additionally, the negative zero sequence component does not exist for machines with an odd number of phases. Furthermore, the rotor x-y and zero sequence equations have been omitted because the rotor winding is regarded as short-circuited.

The flux linkage equations relate the d-q axis current components with the respective flux linkages for stator and rotor equivalent windings, in the d-q reference frame, as follows:

$$\psi_{ds} = L_s i_{ds} + L_m i_{dr} = (L_{ls} + L_m)\, i_{ds} + L_m i_{dr} \tag{5.48}$$

$$\psi_{qs} = L_s i_{qs} + L_m i_{qr} = (L_{ls} + L_m) i_{qs} + L_m i_{qr} \tag{5.49}$$

$$\psi_{dr} = L_r i_{dr} + L_m i_{ds} = (L_{lr} + L_m) i_{dr} + L_m i_{ds} \tag{5.50}$$

$$\psi_{qr} = L_r i_{qr} + L_m i_{qs} = (L_{lr} + L_m) i_{qr} + L_m i_{qs} \tag{5.51}$$

where the L_r is the rotor and L_s is stator inductance described as the sum of the respective leakage and magnetizing inductance. Additionally, the flux linkage equations for the stator quantities in the x-y planes and for the zero sequence can be given as:

$$\psi_{x_k s} = L_{ls} i_{x_k s} \tag{5.52}$$

$$\psi_{y_k s} = L_{ls} i_{y_k s} \tag{5.53}$$

$$\psi_{z_+ s} = L_{ls} i_{z_+ s} \tag{5.54}$$

$$\psi_{z\_s} = L_{ls} i_{z\_s} \tag{5.55}$$

A simplified model is obtained after the application of the rotational transformation which results in two perpendicular decoupled axes, d and q, as shown in Figure 5.2. The d-axis fluxes depend solely on the d-axis currents and the same holds true for the q-axis fluxes and currents. All the inductances are now constant, and therefore time-dependence of the inductance terms in the α-β reference frame has been eliminated. The electromagnetic torque produced can be described by the following equations:

$$T_e = \frac{n}{2} P \frac{L_m}{L_r} \left(\psi_{dr} i_{qs} - \psi_{qr} i_{ds}\right) = \frac{n}{2} P \left(\psi_{ds} i_{qs} - \psi_{qs} i_{ds}\right) \tag{5.56}$$

where P is the number of machine pole pairs. The rotor electrical speed (rad/s) can be described as:

$$\omega_e = \frac{P}{J} \int (T_e - T_L)\, dt \tag{5.57}$$

And the mechanical speed of the rotor (rpm) can be described with:

$$\omega_m = \frac{\omega_e}{P} \left(\frac{60}{2\pi}\right) \tag{5.58}$$

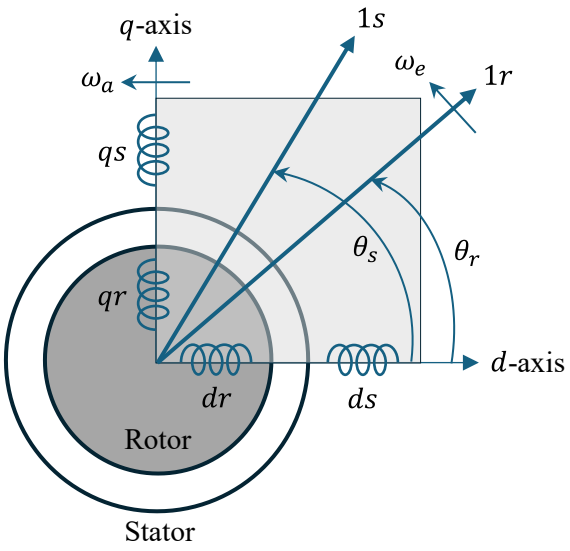


Figure 5.2: Fictitious stator and rotor d-q windings after the rotational transformation.

The choice of the speed of the common reference frame is completely arbitrary with certain choices being more favourable than others. For example, the choice of zero speed for the reference frame (stationary reference frame) leads to further simplification of the d-q stator voltage equations (5.40) - (5.41). For the development of high-performance control of induction machines, the most common choice includes setting the speed of the reference frame as equal to one of the rotating fields in the machine such as the rotor, stator, or air-gap fields which facilitates the development of the control scheme. One such scheme based on the rotor flux orientation will be presented in the next section.

5.3 Rotor flux-oriented control

High-performance applications demand swift machine response, including rapid acceleration, deceleration, speed reversals, and quick start/stop operations. This is made possible by an appropriate high-performance control methodology such as the field-oriented control, direct torque control or the model predictive control. High performance control involves near instantaneous speed, position or torque control of a machine both in steady state as well as in the transient. This is especially important in traction applications, like in EVs. A generalised schematic of the closed-loop high-performance control of a multiphase machine is depicted in Figure 5.3.

Field-oriented control is based on the controllability of machine torque as well as the flux developed in the machine. The field-oriented control scheme of a multiphase induction machine does not differ significantly from that of a three-phase one if the control action is performed in the d-q reference frame. This is because the flux and torque producing current components lie in the d-q reference frame and thus can be independently regulated. However, the presence of x-y current components in the case of machine asymmetries or unbalanced conditions in the multiphase voltage source converters necessitates independent

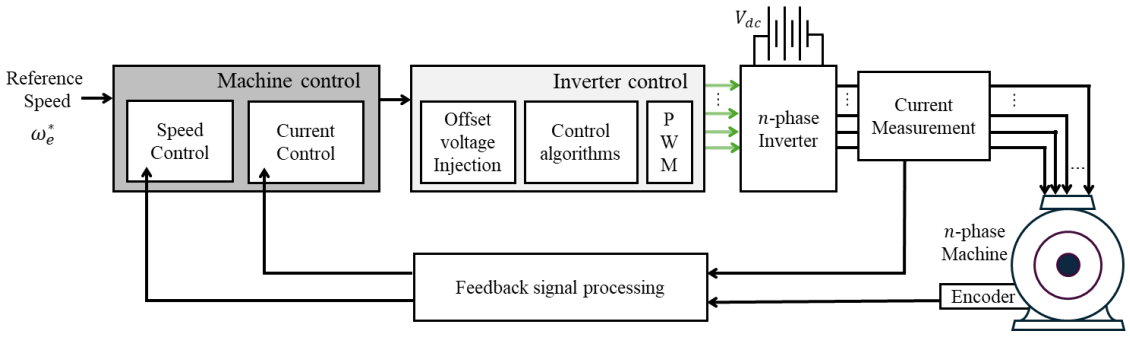


Figure 5.3: Generalised schematic of high-performance multiphase machine control.

regulation. In (Hu et al., 2017), it is shown that VSD based control of an asymmetrical six-phase machine offers superior performance compared to individual control of each three-phase winding set due to mutual coupling between them. It is therefore the preferred choice for the development of high-performance speed/torque control of an induction machine.

Decoupled flux and torque control of an induction machine is enabled by choosing to represent the machine in a common reference frame which is fixed to any of the three flux space vectors, namely the stator, rotor, or the airgap (magnetizing) flux linkage, in the machine. The q-axis component of the flux space vector is required to be zero for decoupled torque control. The alignment of the rotor flux linkage with the d-axis component of the stator current is generally the most common choice due to the resulting simplicity of the control system. Therefore, the rotational speed of the common reference frame (ω_a) is set as equal to the speed of the rotor flux linkage space vector (ω_r). And the stator transformation angle (θ_s) is thus equal to the instantaneous position of the rotating rotor flux field (ϕ_r). Thus, the following holds true:

$$\begin{aligned} \theta_s &= \phi_r & \omega_a &= \omega_r \\ \theta_r &= \phi_r - \theta_e & \omega_r &= \frac{\mathrm{d}\phi_r}{\mathrm{d}t} \end{aligned} \tag{5.59}$$

The alignment of the stator transformation angle (θ_s) with the instantaneous position of the rotating rotor flux (ϕ_r) forces the q-component of the rotor flux linkage to zero ($\psi_{qr} = 0$) and makes the rotor flux linkage space vector real valued ($\psi_r = \psi_{dr}$) because of its alignment with the d-axis. Forcing the rotor flux linkage space vector to the d-axis leads to the derivative of the q-axis component being zero (Figure 5.4) as well ($\mathrm{d}\psi_{qr}/\mathrm{d}t = 0$). The rotor flux equations (5.50) and (5.51) can be described in vector form as:

$$\underline{\psi_r} = L_r \underline{i_r} + L_m \underline{i_s} \tag{5.60}$$

and the rotor current vector can be obtained as:

$$\underline{i_r} = \frac{\underline{\psi_r} - L_m \underline{i_s}}{L_r} \tag{5.61}$$

The rotor voltage equations (5.42) and (5.43) can also be described in vector form as:

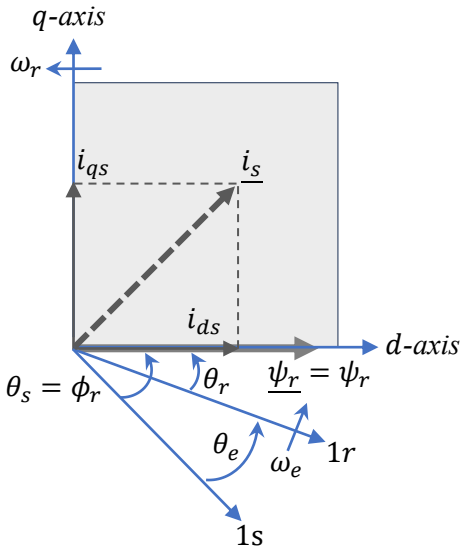


Figure 5.4: Common reference frame attached to the rotating rotor flux vector of a multiphase induction machine.

$$R_r \underline{i_r} + \frac{d}{dt}\underline{\psi_r} + j(\omega_a - \omega_e)\underline{\psi_r} = 0 \tag{5.62}$$

Substituting $\omega_a = \omega_r$ from (5.59), and for $\underline{i_r}$ from (5.61), and setting $\psi_r = \psi_{dr}$ into the equation above yields:

$$\left(\frac{L_r}{R_r}\right)\frac{\mathrm{d}}{\mathrm{d}t}\psi_r + \psi_r = L_m i_{ds} \tag{5.63}$$

$$\left(\frac{L_r}{R_r}\right)(\omega_r - \omega_e)\,\psi_r = L_m i_{qs} \tag{5.64}$$

where the term $\left(\frac{L_r}{R_r}\right)$ is known as the rotor time constant. It can be noticed from (5.63) that d-axis stator current i_{ds} is solely responsible for determining the value of the rotor flux linkage. If the value of this current is kept constant, then ψ_r will also be constant in steady state leading to:

$$\psi_r = L_m i_{ds} \tag{5.65}$$

Therefore, for operation in the base speed region, the rated value of the machine d-axis current is selected as a reference. For operation in the field-weakening region, the value of the d-axis current is reduced proportionally to reduce the value of the rotor flux (Levi, 2011b). However, this mode of operation is not considered in this thesis.

Similarly, by setting $\psi_{qr} = 0$, and $\psi_{dr} = \psi_r$, the torque equation in (5.56) reduces to:

$$T_e = \frac{n}{2} P \frac{L_m}{L_r} \psi_r (i_{qs}) = \frac{n}{2} P \frac{\psi_r^2}{R_r} (\omega_r - \omega_e) \tag{5.66}$$

The instantaneous position of the rotating rotor flux space vector can be estimated indirectly from the rotor flux position through:

$$\omega_r = \omega_e + \omega_{sl}^* \tag{5.67}$$

$$\phi_r = \theta_e + \int \omega_{sl}^* \, \mathrm{d}t \tag{5.68}$$

where the slip angle ($\int \omega_{sl}^* \, \mathrm{d}t$) can be calculated because of the established relationship through the manipulation of (5.64) and making use of (5.63), assuming constant ψ_r, to obtain:

$$\omega_{sl}^* = \frac{R_r}{L_r} \frac{L_m i_{qs}^*}{\psi_r^*} = \frac{R_r}{L_r i_{ds}^*} i_{qs}^* \tag{5.69}$$

Similarly, by simple manipulation of (5.66), one gets:

$$i_{qs}^* = \frac{2}{nP} \frac{L_r}{{L_m}^2} \frac{1}{i_{ds}^*} \, T_e \tag{5.70}$$

The gains K1 and K2 in the schematic (Figure 5.5) are set using the relationships defined in (5.70) and (5.69), respectively. However, current control in the rotating reference frame also requires the stator voltage equations to be considered.

The reference output voltages for each of the d-q current regulators can be expressed as:

$$\begin{aligned} {v_{ds}}^* &= v'_{ds} + v_{ds\_ff} \\ {v_{qs}}^* &= v'_{qs} + v_{qs\_ff} \end{aligned} \tag{5.71}$$

where the feed forward voltage terms v_{ds_ff} and v_{qs_ff}, for the base-speed region, can be expressed as:

$$v_{ds\_ff} = -\omega_r \left(L_s \left(1 - \frac{{L_m}^2}{L_s L_r} \right) \right) i_{qs} \tag{5.72}$$

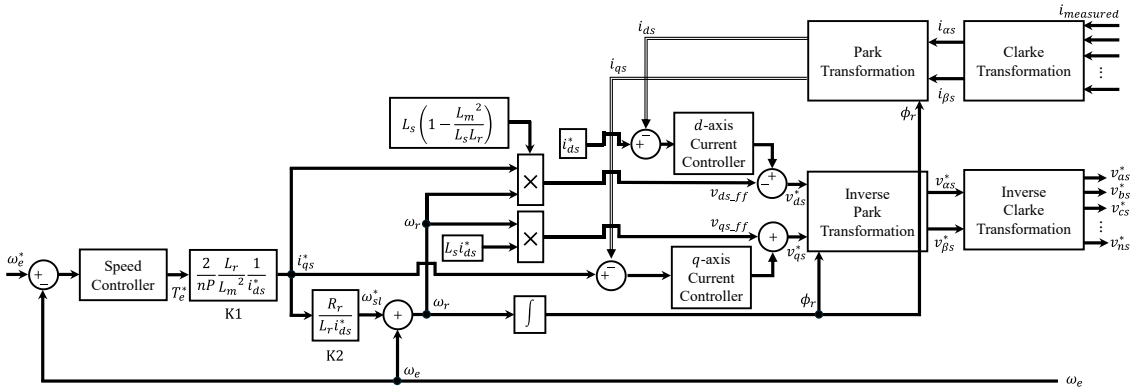


Figure 5.5: Indirect RFOC scheme with current control in rotating reference frame (adapted from Levi, 2011).

Likewise, the q-axis feedforward voltage term is reduced by expressing rotor flux linkage from (5.65) as follows:

$$v_{qs\_ff} = \omega_r \frac{L_m}{L_r}(L_m i_{ds}) + \omega_r \left(L_s \left(1 - \frac{{L_m}^2}{L_s L_r} \right) \right) i_{ds} = \omega_r i_{ds} L_s \tag{5.73}$$

Current control of the flux and torque producing plane is carried in the d-q reference frame using PI controllers. The obtained control scheme is the same as in the three-phase case (Kim, 2017). However, the difference lies in the presence of secondary loss producing x-y planes. The secondary plane current component control can either be done in the stationary reference frame or alternatively achieved through PI controllers in the d-q reference frame, although proportional-resonant (PR) controllers have also been used to achieve this (Che et al., 2014). This will be discussed further on in subsection 5.4.3. The application of the inverse rotational and decoupling transformations to current controllers generates the reference phase voltages for the modulation stage. This completes the mathematical model needed for the implementation of the indirect rotor flux-oriented control of a multiphase induction machine in the rotor field reference frame.

5.4 Multilevel three-phase and multiphase drive

Before proceeding with development of the high-performance control of the multiphase machine, the operation of the cascaded H-bridge nine-level converter was verified using the open-loop (v/f) control of a three-phase induction machine, which is presented in subsection 5.4.1. Then further the operation and control of an asymmetrical six-

phase IM using a five-level CHB is given in 5.4.2. Finally, in 5.4.3, operation under unbalanced dc-link voltage conditions was considered.

5.4.1 Three-Phase IM control using multilevel converter

Figure 5.6 shows a three-phase nine-level cascaded H-Bridge inverter connected to a three-phase induction machine with the machine parameters specified in Table 5.1. The nine-level CHB is formed with four cascaded H-bridge modules, each supplied by a pair of 14.8 V LiPo-batteries charged approximately to the same battery voltage level of 31 V, defined as V_{dc}. Therefore, the maximum achievable amplitude of the phase voltage was 124 V. As the machine was rated for a maximum peak amplitude of 310 V (50 Hz), it was only possible to operate the machine at a maximum frequency of 20 Hz (600 rpm) with sinusoidal phase references as dictated by the (v/f) control law (no boost voltage was used). The operation of the machine in overmodulation region (22 Hz, 660 rpm) was also tested with the double min-max injection method.

The second min-max injection was shown in subsection 4.2.5 to perform best in terms of the harmonic performance for modulation indices below unity while the double min-max injection was found to be most suitable in the over modulation region. Therefore, by taking these results into account, experimental results including the three leg voltages, phase 'a'

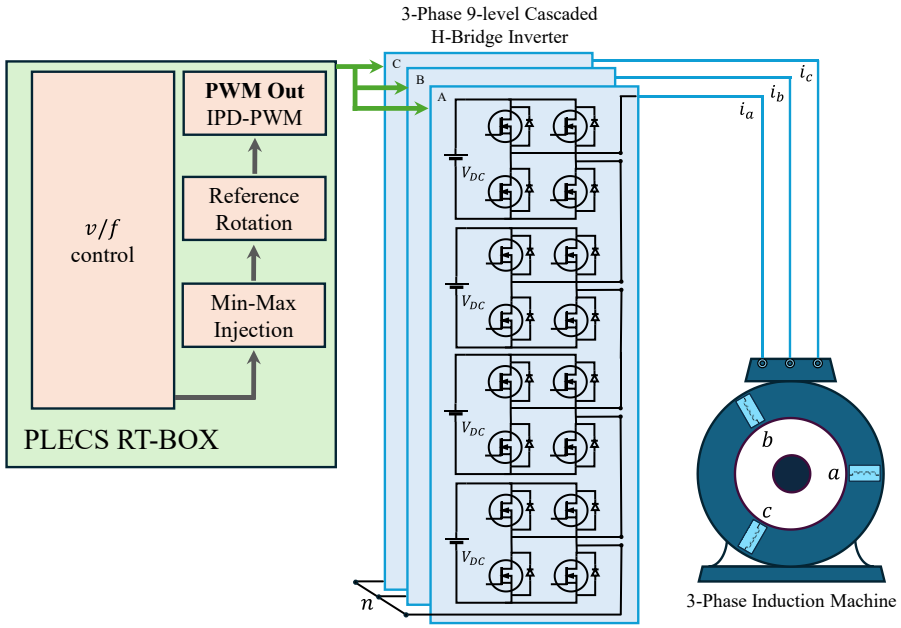


Figure 5.6: Nine-level cascaded H-bridge inverter connected to a three-phase induction machine.

voltage and current were obtained for the machine operating frequencies (speeds) shown in Table 5.2.

The switching devices (MOSFETs) are controlled by PWM signals generated by the PLECS RT-Box. The effective inverter output switching (and carrier) frequency of 2 kHz was chosen with a hardware implemented dead-time of 0.5 µs. No dead-time compensation scheme was deemed necessary due to a significantly larger discretization step size of 250 µs. The PWM is done using the in-phase disposition (IPD) modulation method due to its superior performance as shown in subsection 3.4.4.

Experimental results obtained by application of these methods on a three-phase induction machine confirm the superiority of the IPD-PWM method in terms of the harmonic performance of the phase 'a' current. A comparison between the harmonic performance of the phase voltages under different min-max injections with the IPD-PWM showed a similar trend as already expected from the results obtained (Figure 4.7) in subsection 4.2.5. However, there was no observable difference between the different min-max injections in

Table 5.1: Three-phase machine parameters.

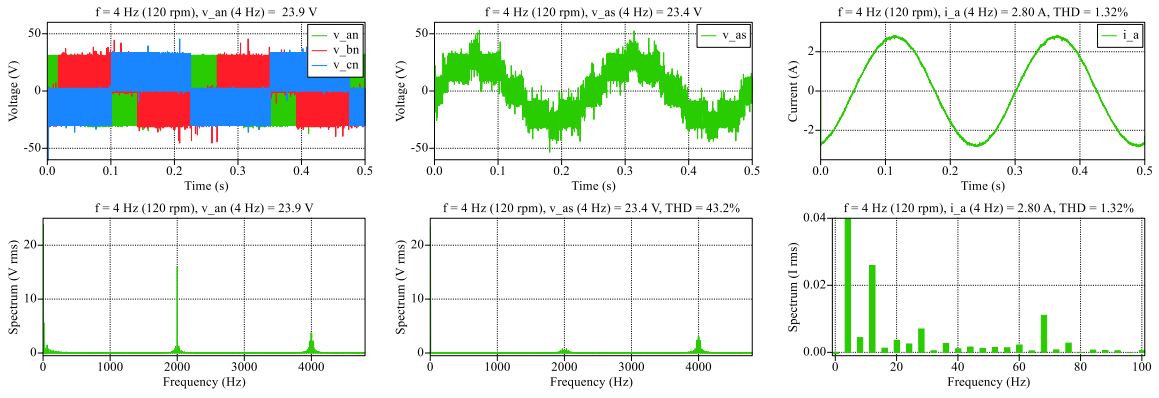
Rated stator line voltage	$V_s = 380$ V
Rated frequency	$f_n = 50$ Hz
Pole pairs	$P = 2$
Stator resistance	$R_s = 1.77\ \Omega$
Rotor resistance	$R_r = 1.34\ \Omega$
Stator leakage inductance	$L_{ls} = 14$ mH
Rotor leakage inductance	$L_{lr} = 12$ mH
Mutual inductance	$L_m = 442$ mH
Inertia	$J = 0.006$ kg m^2
Rated speed	$\omega_{m,nom} = 1440$ rpm
Rated power	$P_n = 2.2$ kW

Table 5.2: Machine operating points and respective figures.

Figure No.	Frequency (Hz)	Speed (rpm)	Reference voltage (V)	Modulation index (m_a)
Figure 5.7	4 Hz	120	24	0.19
Figure 5.8	8 Hz	240	48	0.39
Figure 5.9	12 Hz	360	72	0.58
Figure 5.10	16 Hz	480	96	0.77
Figure 5.11	22 Hz	660	132	1.06

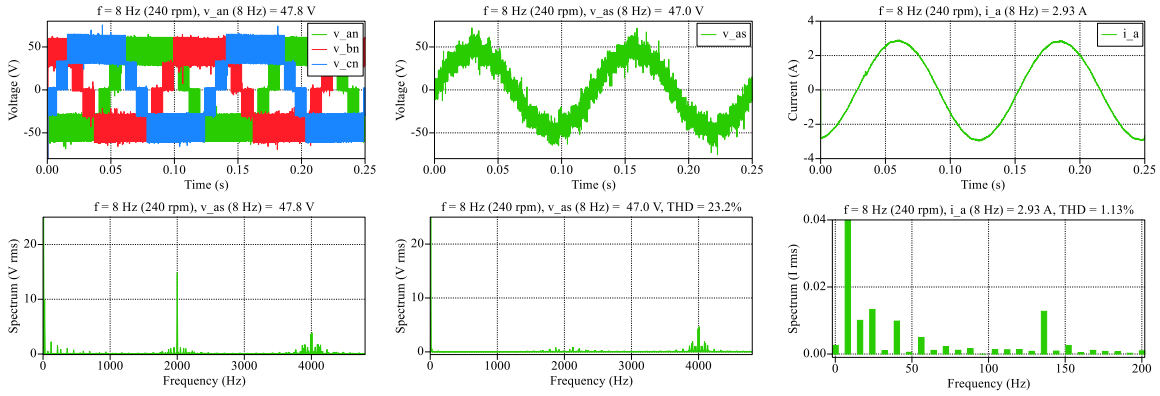
terms of the harmonic performance of the phase currents. This is due to the inductive filtering effects of the induction machine. Furthermore, a multilevel voltage waveform also significantly improves the harmonic performance and a clear differentiation in THD between the different min-max injections becomes less apparent. Therefore, it can be concluded that for practical applications, specially for multilevel voltage waveforms, a min-max injection is only able to extend the modulation index depth without significantly improving the harmonic performance of the phase current in induction machines with relatively high inductance values. Furthermore, the effective inverter switching frequency was also chosen to be relatively low (2 kHz) to pronounce the effect of harmonic distortion. Naturally, at higher switching frequencies, the harmonic distortion figures will be yet much lower, further verifying that the difference between the min-max injections would be negligible.

Obtained experimental results were collected using digital oscilloscope and then plotted and processed in MATLAB/PLECS. The results are shown in Figure 5.7 to Figure 5.11. The results show excellent quality of the current waveforms even at low modulation index depths. The switching harmonics at the switcing frequency (2 kHz) and its multiples are apparent from leg and phase voltage spectra. The magnitude of lower order current harmonics is also very small in all the operating conditions. A very small 17th harmonic component is present in the spectra of the phase currents. A gradual increase in the number of converter levels is also obvious with an increase in the modulation index depth (operating frequency). There is an expected drop in the THD figures with an increase in the number of converter levels as the modulation index depth increases. Figure 5.9a shows the characteristic shape of the leg voltage waveforms under min-max injection. The presence of



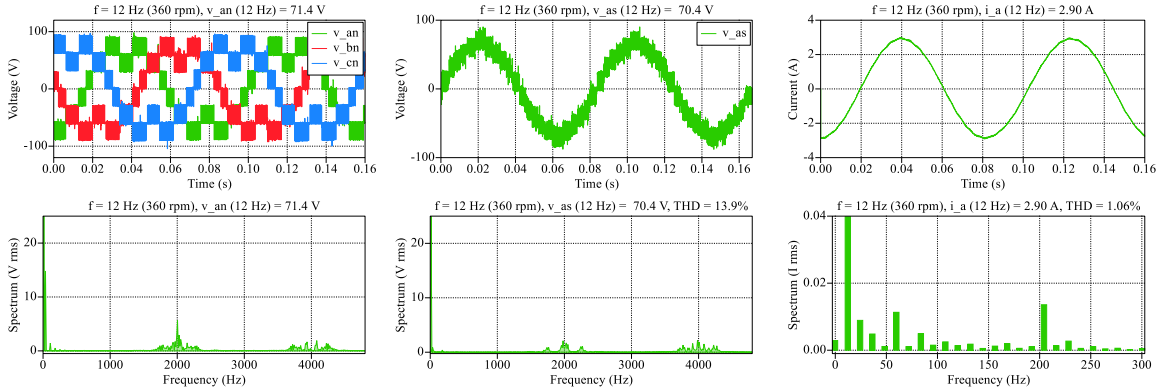
(a) (b) (c)

Figure 5.7 – Experimental results at 4 Hz (120 rpm) showing (a) Leg voltage waveforms and spectra, (b) phase 'a' voltage and spectra, and (c) phase 'a' current and spectra (IPD-PWM with double min-max injection).



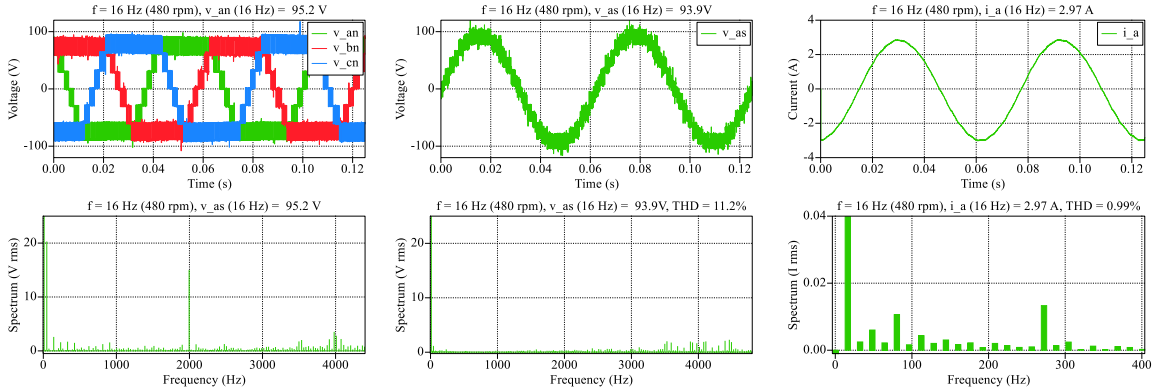
(a) (b) (c)

Figure 5.8 – Experimental results at 8 Hz (240 rpm) showing (a) Leg voltage waveforms and spectra, (b) phase 'a' voltage and spectra, and (c) phase 'a' current and spectra (IPD-PWM with double min-max injection).



(a) (b) (c)

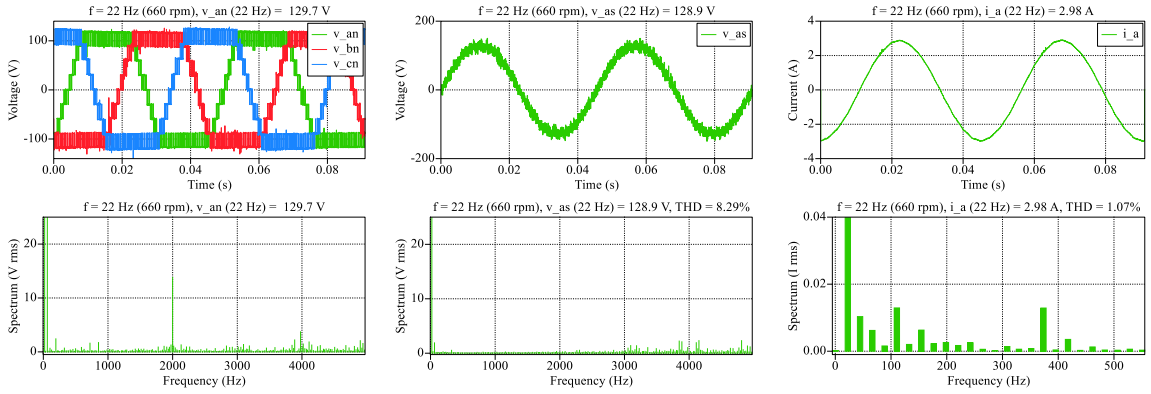
Figure 5.9 – Experimental results at 12 Hz (360 rpm) showing (a) Leg voltage waveforms and spectra, (b) phase 'a' voltage and spectra, and (c) phase 'a' current and spectra (IPD-PWM with double min-max injection).



(a) (b) (c)

Figure 5.10 – Experimental results at 16 Hz (480 rpm) showing (a) Leg voltage waveforms and spectra, (b) phase 'a' voltage and spectra, and (c) phase 'a' current and spectra (IPD-PWM with double min-max injection).

the third harmonic component is also noticeable in the leg voltage spectra. There is a minor difference in the expected leg voltage levels and the actually measured value, this is thought to be due to dead-time and voltage drop accoss the semiconductor switches.



(a) (b) (c)

Figure 5.11 – Experimental results at 22 Hz (660 rpm) showing (a) Leg voltage waveforms and spectra, (b) phase 'a' voltage and spectra, and (c) phase 'a' current and spectra (IPD-PWM with double min-max injection).

The operation of the CHB converter has been verified in open-loop control of a three-phase induction machine at different operating frequencies (speeds). The next step is the development of the indirect rotor flux-oriented control and its application to a multiphase machine, which is presented in the next subsection.

5.4.2 High performance control of an asymmetrical six-phase IM using five-level six-phase CHB inverter

Machines with multiple three-phase windings sets are generally preferred for better fault tolerance capability on offer. Among multiphase machines, the asymmetrical six-phase machine is the most researched (Levi, 2008). High performance control of an asymmetrical six-phase induction machine using a five-level cascaded H-bridge inverter is presented in this section. The nine-level three-phase cascaded H-bridge inverter consisting of four H-bridge modules per inverter leg, used in the previous subsection was reconfigured into a five-level six-phase inverter. First, the mathematical model of the six-phase machine was developed by application of general equations from subsection 5.2.2 to the asymmetrical six-phase case (see Appendix C). The rotor flux-oriented control scheme for a multiphase machine, using the equations described in section 5.3, applied to asymmetrical six-phase case, is implemented in PLECS. Simulation of the system is conducted prior to experimental validation under different operating conditions.

5.4.2.1 Simulation and experimental results

The schematic of the complete multilevel multiphase drivetrain with the FOC can be seen in Figure 5.12. The values of K1 and K2 are defined in Figure 5.5. The photograph of

the experimental setup is shown in Figure 5.13. The experimental setup consists of an asymmetrical six-phase squirrel cage induction machine [Table 5.3, (Che et al., 2017)] with two isolated neutral points supplied by a custom built six-phase five-level ($k = 2$ modules per leg) MOSFET based CHB converter with a single neutral point n. As in 5.4.1 each H-bridge module was supplied by two serially connected 14.8 V LiPo-batteries charged to roughly the same dc voltage to obtain a dc-link voltage, $V_{\mathrm{dc}} = 31$ V to ensure symmetry. Therefore, the maximum achievable peak amplitude of the leg voltages was 62 V. As the machine was rated for a peak amplitude of 155 V (50 Hz), it was only possible to operate the machine with a maximum speed of 400 rpm (20 Hz), as dictated by v/f law.

Plexim RT-Box 1 was used in conjunction with PLECS software for the control of the CHB converter with a discretization step size of 125 µs (8 kHz sampling frequency). As mentioned, a dead time of 0.5 µs is implemented through hardware and no compensation scheme was used. The modulation method employed was IPD-PWM for its superior performance in terms of the THD of phase voltages and currents. A carrier frequency of 4 kHz was selected which has an effective converter switching frequency of 4 kHz for LS-PWM operation of a five-level CHB. Equal utilization (on average) of the batteries and switching devices in each converter leg was ensured with a periodic battery module rotation algorithm, as described in subsection 3.5.4, with an average device switching frequency of 1 kHz.

An incremental encoder with 1000 pulses/rev. (Omron E6B2-CWZ1X) provided speed sensing for the machine while the current measurement was carried out using a custom-made LEM sensor box for all the six-phase currents and fed back to the RT-Box for the FOC scheme. The PI speed and current controller gain parameters are given in Table 5.4.

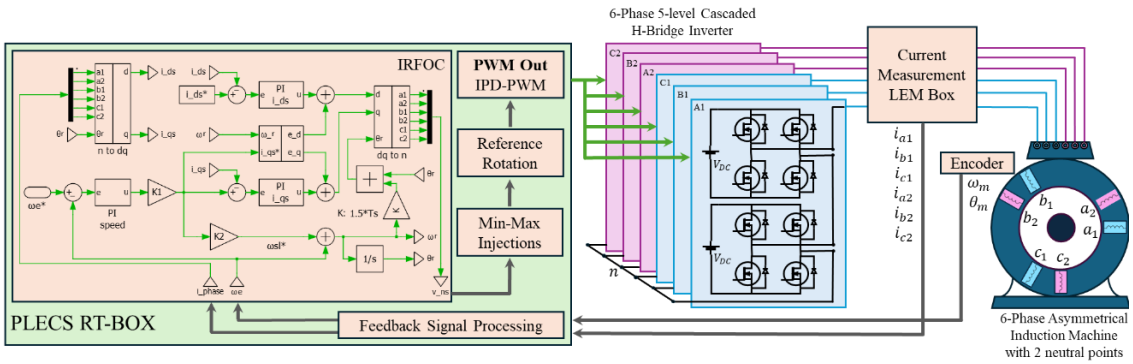


Figure 5.12: Schematic of the multilevel multiphase drivetrain with field-oriented control of multiphase induction machine using a cascaded H-bridge converter.

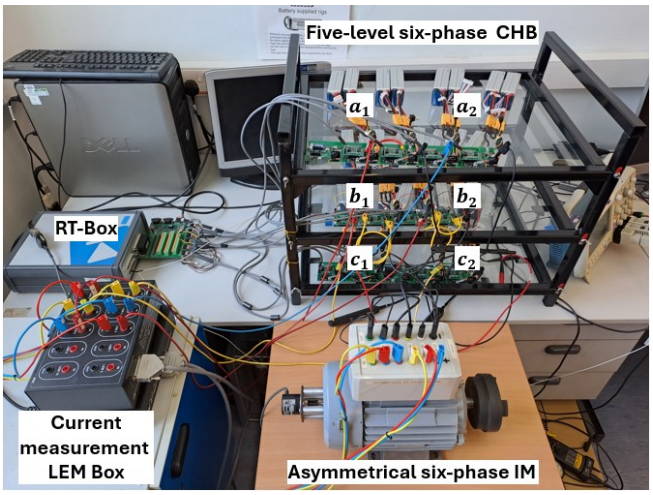


Figure 5.13: Experimental setup of the multilevel multiphase drive.

Table 5.3: Six-phase machine parameters.

Rated stator voltage	$V_s = 110$ V
Rated frequency	$f_n = 50$ Hz
Pole pairs	$P = 3$
Stator resistance	$R_s = 13.75\ \Omega$
Rotor resistance	$R_r = 11.55\ \Omega$
Stator leakage inductance	$L_{ls} = 46.1$ mH
Stator leakage inductance (x-y)	$L_{ls-xy} = 5.3$ mH
Rotor leakage inductance	$L_{lr} = 25.4$ mH
Mutual inductance	$L_m = 593$ mH
Inertia	$J = 0.008$ kg m^2

Table 5.4: FOC - PI controller gains.

$K_{p\_\omega e}$	$K_{i\_\omega e}$	K_{p_id}	K_{i_id}	K_{p_iq}	K_{i_iq}
0.2	0.25	20	2200	5	1800

A PWM delay compensation of $1.5 \cdot T_s$ (see Figure 5.12) was also implemented by addition of the said delay to the rotor flux position needed for the inverse rotational transformation as specified in (Lim et al., 2023). Each set of three-phase reference voltage waveforms was regular-sampled asymmetrically and subjected to double min-max injection which increases the dc-link utilization for each three-phase set by a factor of $2/\sqrt{3}$. The converter leg A1 voltage, phase a_1 and a_2 currents were measured using differential voltage (Tektronix P5205A) and current probes (Tektronix TCP0030A) connected to Tektronix MSO2014 oscilloscope with waveform data acquisition at 125k samples for post processing and THD calculation.

At system start-up, to flux the machine, drive enable command sets an immediate application of the d-axis current reference (i_{ds}^*) to 0.84 A which achieves steady-state in

40 ms. This can be seen in d-axis currents shown in the simulation results shown in Figure 5.14 (bottom plot). Figure 5.15a shows experimental measurement results obtained from the RT-box, sampled at 8 kHz, as mentioned before. The machine fluxing cannot be seen in Figure 5.15a because the speed reference commands were given some time after drive enable command.

Next, a step speed reference command of 300 rpm at $t = 50$ ms results in the machine reaching the set speed in around 150 ms. The reference six-phase voltages and all the measured six-phase currents are shown in relevant subplots in Figure 5.15a. The corresponding reference and measured d-q axes currents can also be seen during the transient into steady state. Although the machine torque is not shown, it is directly proportional to i_{qs}, because ψ_r in base-speed region is kept constant, see (5.66). The corresponding five-level converter leg voltages and the phase a_1 and a_2 currents at this time (PLECS scope and the external scope were triggered by the same signal), can be seen in Figure 5.15b which has been taken from the oscilloscope. Thereafter, a speed reversal command from 300 rpm to -300 rpm is given at $t = 350$ ms which the machine achieves

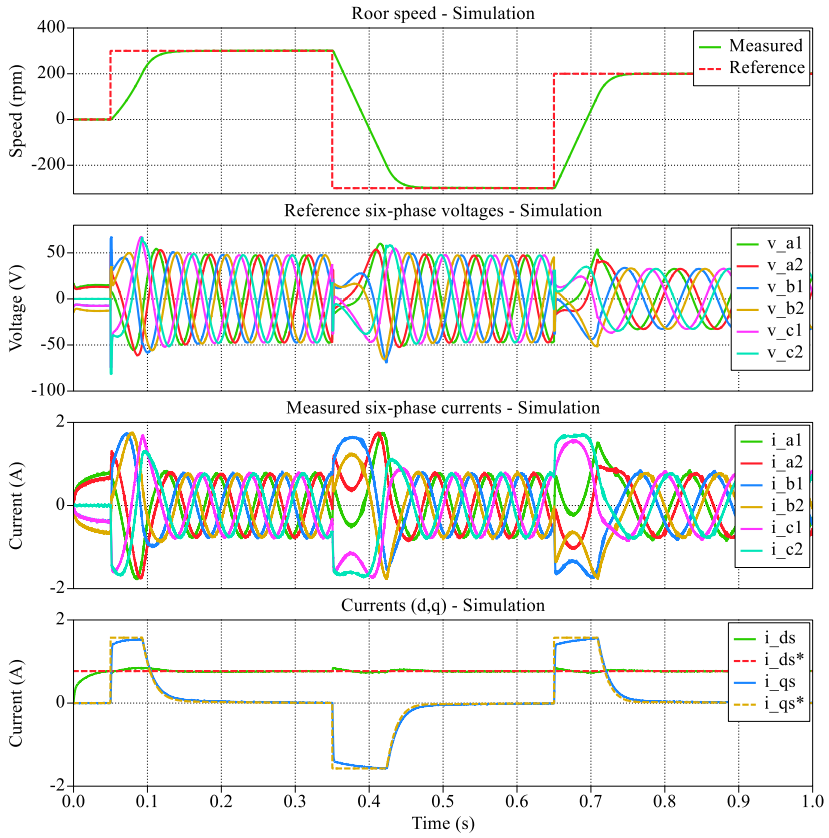
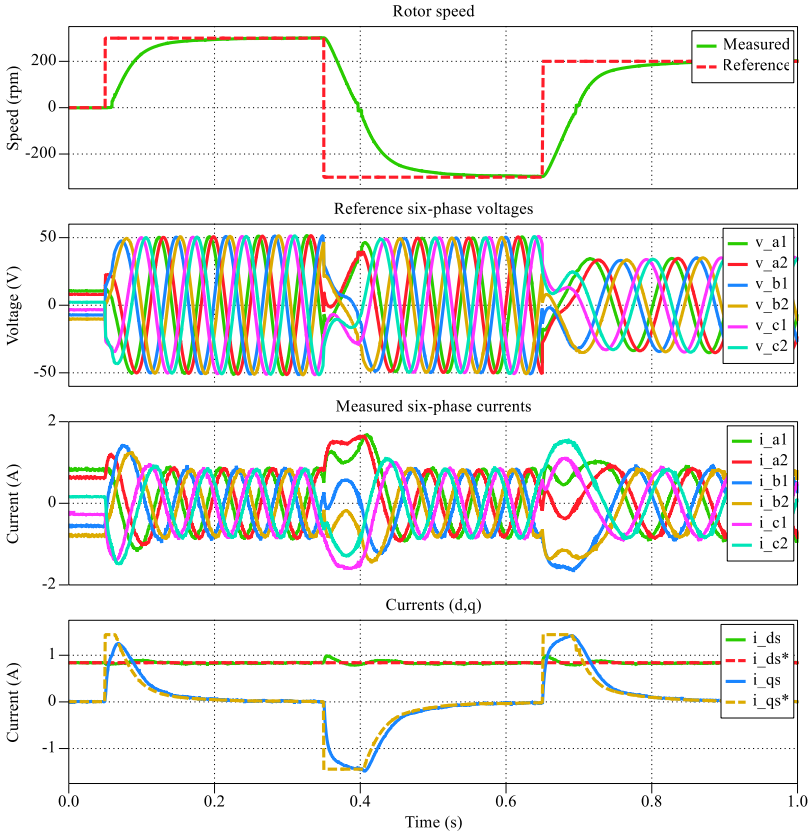
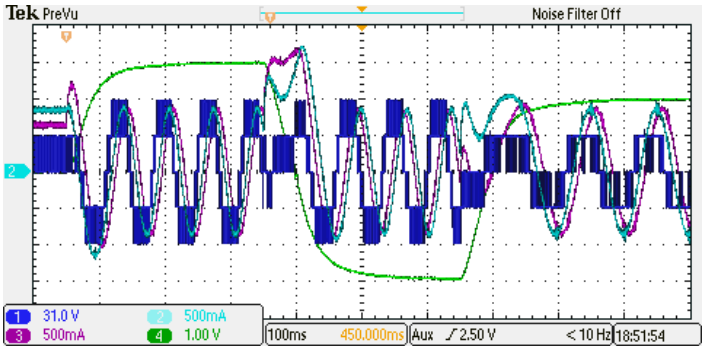


Figure 5.14: Simulation results for step changes in reference speed (no-load) - Top to bottom: speed (rpm), reference phase voltages, measured six phase currents, reference and actual d-q currents.



(a)



(b)

Figure 5.15: Experimental results for step changes in reference speed (no-load)
(a) Top to bottom: speed (rpm), reference phase voltages, measured six phase currents, reference and actual d-q currents. (b) CH1: Leg A1 voltage (31 V/div), CH2: Phase a_1 current (0.5 A/div), CH3: Phase a_2 current (0.5 A/div), CH4: speed (100 rpm/div), Horizontal: Time (100 ms/div).

in around 200 ms. Finally, at $t = 650$ ms, another speed reversal command to 200 rpm is given which is reached in less than 200 ms. At this operating point, a three-level leg voltage waveform of the converter can be observed in Figure 5.15b, as a lower modulation index is needed. A comparison between the simulation (Figure 5.14) and experimental (Figure 5.15) results shows an extremely accurate agreement.

In Figure 5.16, a speed reference command of 400 rpm is given which is the maximum achievable speed (sinusoidal reference) with the dc-link voltage present (i.e., 62 V). Of

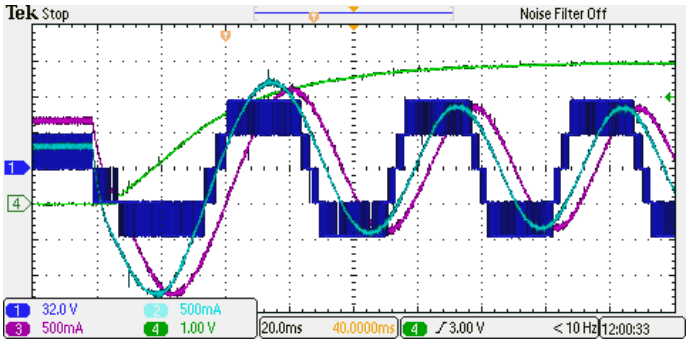


Figure 5.16: Experimental results for step change in speed to 400 rpm from rest (no-load). CH1: Leg A1 voltage (32 V/div), CH2: Phase $a_1$current (0.5 A/div), CH3: Phase $a_2$current (0.5 A/div), CH4: Machine speed (100 rpm/div), Horizontal: Time (20 ms/div).

pertinence is the change in the phase angle (power factor) between the machine leg A1 voltage (CH1) and phase a_1 current (CH2) as the machine starts at zero speed and accelerates through the transient into steady state operation at 400 rpm. A high power factor is noticeable at the start as expected due to the need for more real power to bring the machine up to the desired speed. A peak starting current of 1.75 A initially is evident in Figure 5.16. With the passage of the machine through the speed transient, the phase angle starts to increase while the lowest power factor at steady state is noticeable where the effect of the relatively higher magnetizing reactance becomes apparent. As a result, significantly higher reactive power is required.

The phase a_1 current peak value in steady state is around 0.85 A (as expected, since i_{ds}^* was set to 0.84 A). The current a_1 and a_2 THD values are below 5% even at a relatively low switching frequency of 4 kHz, as shown for different machine speeds in Table 5.5. Figure 5.17 shows the spectra of phase a_1 and a_2 currents at 300 rpm. Very small switching harmonics at 4 and 8 kHz can also be seen. It can be seen that the currents are quite sinusoidal and contain very small low order harmonics. The spectra for all six phase currents are next shown (first twenty harmonics) in Figure 5.18a at machine speed of 400, 300 and 200 rpm. The α-β and x-y currents in steady-state are also shown at different machine speeds in Figure 5.18b and Figure 5.18c, respectively. For an asymmetrical six-phase IM, the 5th, 7th, 17th, and 19th harmonics map into the x-y plane (discussed next). Very small 7th, 17th and 19th harmonics are apparent at 400 rpm (Figure 5.18a top). As these harmonics were insignificant, current regulation in x-y plane was not used. Instead, x-y voltage references were just kept at zero.

Table 5.5: Phase a_1 and a_2 current THD at different operating points.

	200 rpm	300 rpm	400 rpm
Phase a_1 current (THD)	4.9%	3.6%	4.7%
Phase a_2 current (THD)	4.9%	3.8%	4.1%

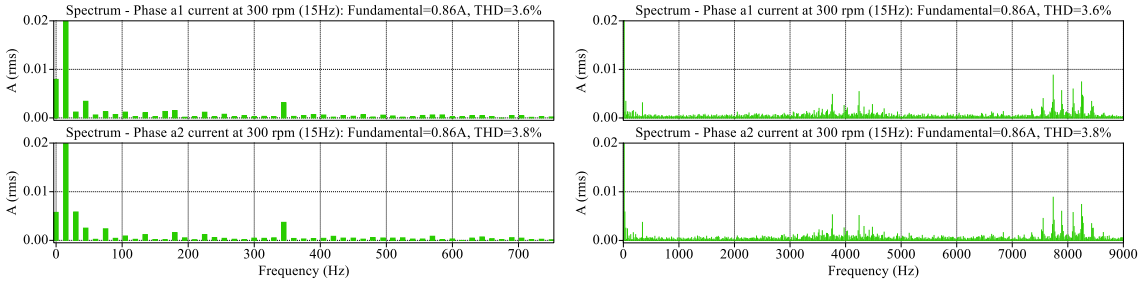
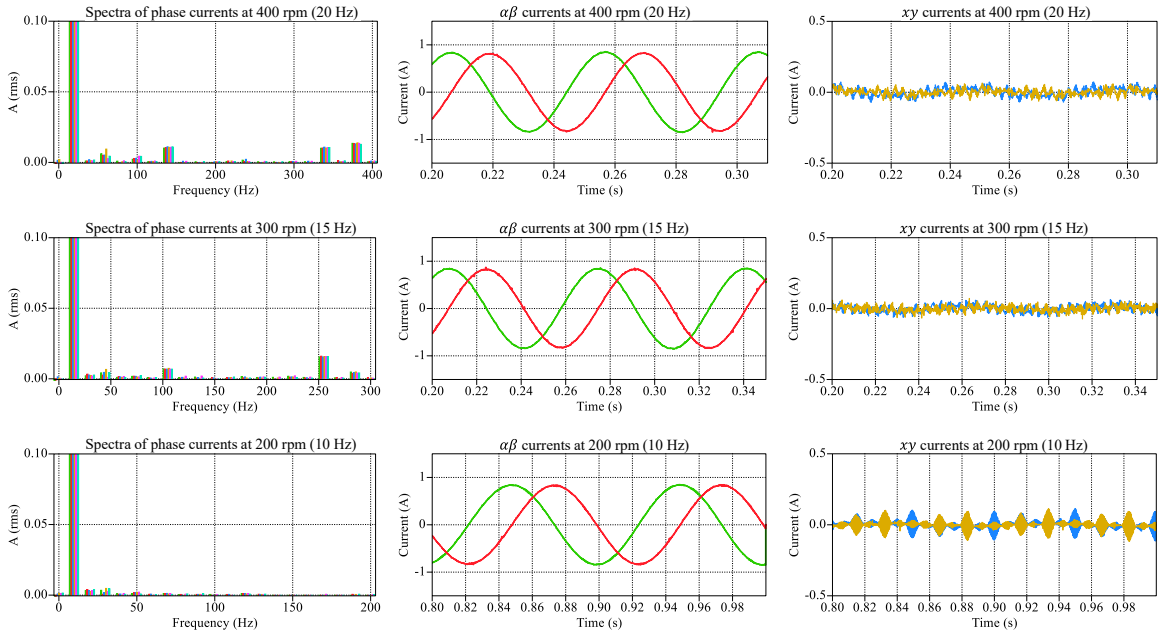


Figure 5.17: Phase a_1 and a_2 current spectra. Enlarged low order hamonics (left), and full spectum including switching harmonics (right).

5.4.2.2 Current harmonic suppression

The harmonic mapping of a six-phase machine is illustrated in Figure 5.19. From (5.44) and (5.45), it can be seen that for multiphase machines, certain harmonics can map into the x-y subspaces in the case of unbalance or asymmetries in the stator supply voltage. This is particularly important for a multiphase machine supplied by a battery based cascaded H-bridge inverter where there is an increasingly greater likelihood of unequal dc-source and leg voltages. Furthermore, if the stator supply voltages contain any other time harmonics



(a) (b) (c)

Figure 5.18: (a) Spectra of phase currents, (b) α-β currents, and (c) x-y currents at machine speed of 400, 300, and 200 rpm (top to bottom, respectively).

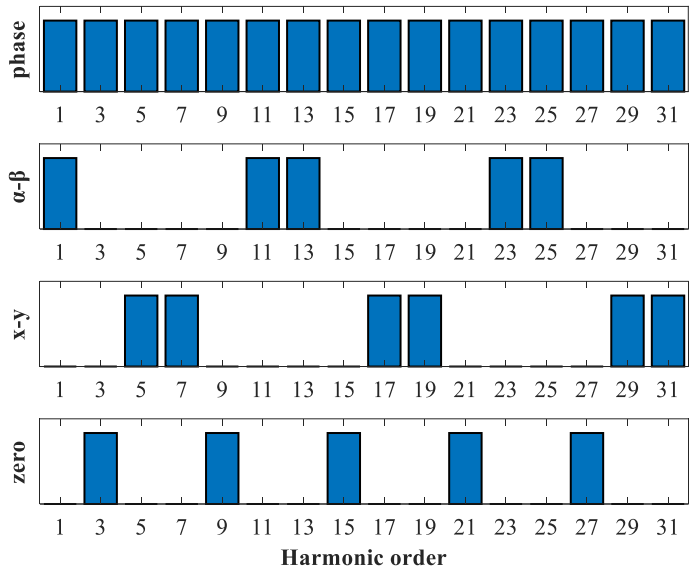


Figure 5.19: Harmonic mapping of six-phase machines (amplitude disregarded for illustration).

that map into the x-y subspaces, then equations (5.44) and (5.45) must be taken into consideration. The x-y stator voltages and currents are related through the impedance of the x-y subspace, which is a function of the stator resistance and the stator leakage inductance. Low impedance values of the x-y subspaces can result in large x-y currents. Since the currents in the x-y subspaces do not contribute toward the torque/flux production, and contribute toward machine losses, it is necessary to reduce or eliminate them.

The suppression of x-y current harmonics is accomplished through the use of current controllers in the x-y subspaces. Here the current control involves the use of current regulation of problematic lower order harmonics by their transformation into dc quantities. This can be accomplished by transformation of the said harmonics into multiple d-q reference frames rotating at their respective frequencies. A pair of current controllers, for the respective d- and q-axis current component regulation, are thus needed to control each harmonic. Figure 5.20 shows the implementation of one such scheme where the current control of the 5^{th} and 7^{th} current harmonic is executed.

The six-phase machine used for the experiment has a relatively large stator resistance (R_s) which limits the current in the x-y plane. Consequently, current control was not necessary as can be seen from the harmonic spectrum (see Figure 5.17 and Figure 5.18) of the phase currents at different operating speeds. However, a machine with a lower stator

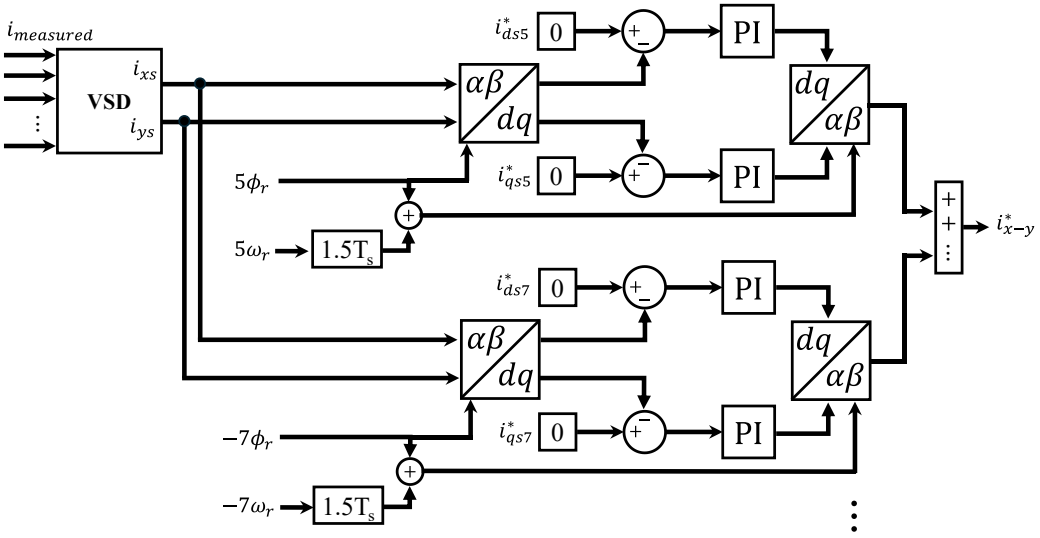


Figure 5.20: Harmonic suppression of the 5th and 7th x-y current harmonic components in a six-phase machine.

resistance and low leakage inductance could lead to the presence of significant x-y current harmonics which would necessitate their regulation.

High performance speed control of an EV drivetrain based on a five-level CHB converter in conjunction with an asymmetrical six-phase IM was presented and experimentally verified. The dc-source voltages of the individual H-bridges were kept balanced, and the simulation and experimental verification was conducted under this assumption. However, in practice, the likelihood of an imbalance between dc-source voltages is much higher. This causes issues such as lower effective converter switching frequency as well as a reduction in the range of modulation index depth for balanced operation. Therefore, the next section deals with this issue through the application of the methods described in section 4.3 for the three-phase system and extends it to multiphase system.

5.4.3 High performance control of an asymmetrical six-phase machine under unbalanced dc-source voltages using NVM

The previous subsection discussed the high-performance control of a multiphase machine using a CHB multilevel converter under balanced dc-source voltage levels. However, in practice, it is more likely that there will be an imbalance between the dc-source voltages as mentioned previously in section 4.3. This leads to an imbalance between the maximum synthesizable leg voltages between the multiple converter legs. Therefore, this

section presents high performance control (simulation) of an asymmetrical six-phase machine with unbalanced dc source voltages of the CHB inverter, where the methods presented in subsection 4.3.2 will be used to achieve balanced operation of the machine with an extension of the modulation index depth.

As in section 4.3, a scenario with different dc-source and total dc-source voltages is presented. Consider a two-module (five-level) CHB with the dc-link voltages described in Table 5.6. It can be noticed that the converter leg C2 has the lowest total dc-link voltage ($V_{dc\_c2} = 100$ V) among the six converter legs. Therefore, the maximum achievable modulation index depth varies depending on the choice of the leg voltage references. If sinusoidal references are considered, then the maximum achievable modulation depth is limited to 100 V. However, as it has been previously described, this can be extended through the min-max injection to 115.5 V (=$100 \cdot 2/\sqrt{3}$) as there are two three-phase winding sets, each with its own neutral point. Further extension of the modulation index can be achieved through the NVM injection method as described in (Kim and Cho, 2022). For the case at hand, the maximum value can be calculated by the application of the NVM equation (4.17) to each three-phase set (A1, B1, C1 and A2, B2, C2). Since the lowest value lies in the second set (i.e., $V_{dc\_c2} = 100$ V), this value is the limiting factor in the determination of the maximum synthesizable leg voltage for balanced operation. For NVM injected references, it can be calculated to be 138.5 V. Therefore, as dictated by the v/f law under no load, maximum achievable operating frequencies are 32 Hz (640 rpm), 37 Hz (740 rpm), 44 Hz (880 rpm) for the sinusoidal, min-max, and the NVM injection methods, respectively.

The six-phase asymmetrical induction machine was operated under FOC using the six-phase five-level (two-module) cascaded H-bridge inverter with unbalanced dc-source voltages at the abovementioned operating points to demonstrate machine operation and points of imbalance. The maximum torque is limited to twice the nominal torque. At first, sinusoidal leg references are used, and the obtained results can be seen in Figure 5.21. A

Table 5.6: CHB dc-source voltages and total dc-source voltages.

Leg A1	**Leg A2**	**Leg B1**	**Leg B2**	**Leg C1**	**Leg C2**
$V_{dc\_a1\_1} = 95$ V	$V_{dc\_a2\_1} = 55$ V	$V_{dc\_b1\_1} = 50$ V	$V_{dc\_b2\_1} = 55$ V	$V_{dc\_c1\_1} = 50$ V	$V_{dc\_c2\_1} = 65$ V
$V_{dc\_a1\_2} = 60$ V	$V_{dc\_a2\_2} = 95$ V	$V_{dc\_b1\_2} = 80$ V	$V_{dc\_b2\_2} = 85$ V	$V_{dc\_c1\_2} = 90$ V	$V_{dc\_c2\_2} = 35$ V
$V_{dc\_a1} = 155$ V	$V_{dc\_a2} = 150$ V	$V_{dc\_b1} = 130$ V	$V_{dc\_b2} = 140$ V	$V_{dc\_c1} = 140$ V	$V_{dc\_c2} = 100$ V

speed reference command of 640 rpm is given at 50 ms after the d-axis current has had time to reach its reference value and create the machine flux. The desired reference speed of 640 rpm is achieved by 200 ms. The phase voltages and currents are balanced in steady state as can be seen from spectrum in Figure 5.22a. At 300 ms, a speed reversal command to -740 rpm is given. However, at this operating point, the phase voltages and currents become unbalanced (Figure 5.22b) and the desired reference voltage level (~115 V) cannot be achieved with sinusoidal PWM. This is also apparent from the torque ripple (q-axis current) appearing in Figure 5.21 between 500 ms and 650 ms. At 650 ms, another speed reversal command to 880 rpm is given which is achieved by the machine. However, a significantly high torque ripple is apparent in Figure 5.21 as the phase voltages and currents become even more unbalanced (Figure 5.22c), which causes an unbalance in the torque and flux producing currents.

Next, the double min-max offset voltage injection method is used to generate the reference leg voltages. This results in the extension of the range of the machine operation to 740 rpm as shown in Figure 5.23 where the machine achieves the desired speeds of 640 rpm and -740 rpm without an imbalance in the phase voltages or currents (Figure 5.24a-b). However, beyond this point, when a speed reference of 880 rpm is given, the machine again produces a high torque ripple due to the imbalances in the machine currents (Figure 5.24c).

Finally, the offset voltage injection, based on the NVM method presented in subsection 4.3.2, with LS-PWM, is applied to further extend the modulation index range where operation of the machine at 880 rpm is now possible. The obtained results can be seen in Figure 5.25 where the machine now reaches the desired speeds without causing any imbalances in the phase voltages or currents (Figure 5.26).

A large third harmonic component is obvious in the leg voltage spectra of the min-max (Figure 5.24) and NVM (Figure 5.26) injection methods, as expected. It is interesting to observe a difference in magnitudes of the leg voltages at the fundamental frequency for the three methods even when balanced phase voltages and currents are obtained. For example, at 640 rpm, all six leg voltages have the same magnitude (~99 V) at the fundamental frequency for the sinusoidal and min-max injected references (Figure 5.22a and Figure 5.24a). However, the NVM method produces leg voltages of different magnitudes even when the desired magnitude of the phase references is 99 V (Figure 5.26a). This is because, in the

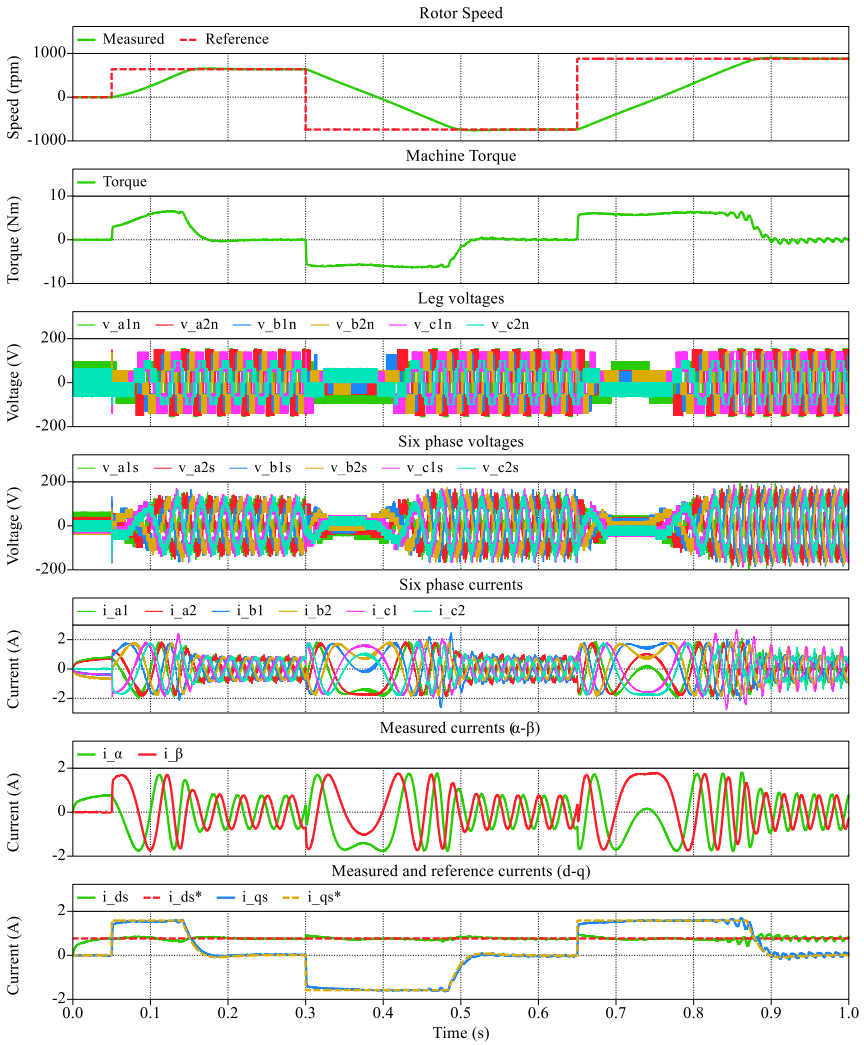


Figure 5.21: Simulation results - FOC of an asymmetrical six-phase IM under unbalanced dc-source voltages with sinusoidal references using LS-PWM with step changes in reference speeds (no-load) of 640 rpm, −740 rpm, and 880 rpm. Top to bottom: speed (rpm), Torque (Nm), leg voltages, phase voltages, phase currents, α-β currents, reference and actual d-q currents.

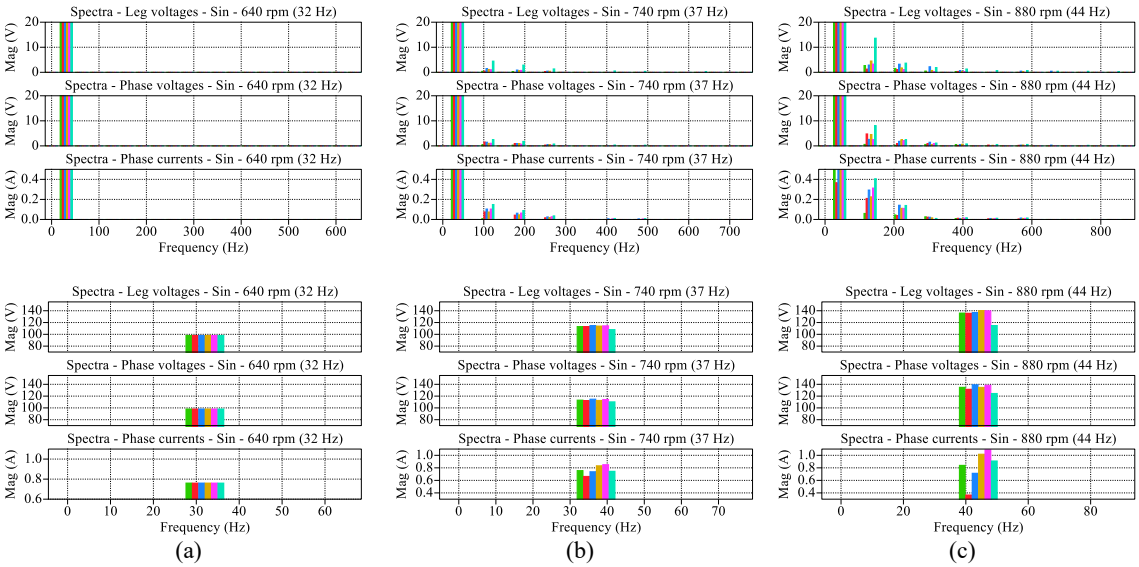


Figure 5.22: Harmonic spectra of all six leg voltages, phase voltages and the phase currents obtained with sinusoidal references (LS-PWM) at speeds of (a) 640 rpm, (b) −740 rpm, and (c) 880 rpm. Top plots show the first 20 harmonics, and the bottom plots show the respective fundamental frequency components of the six phase variables.

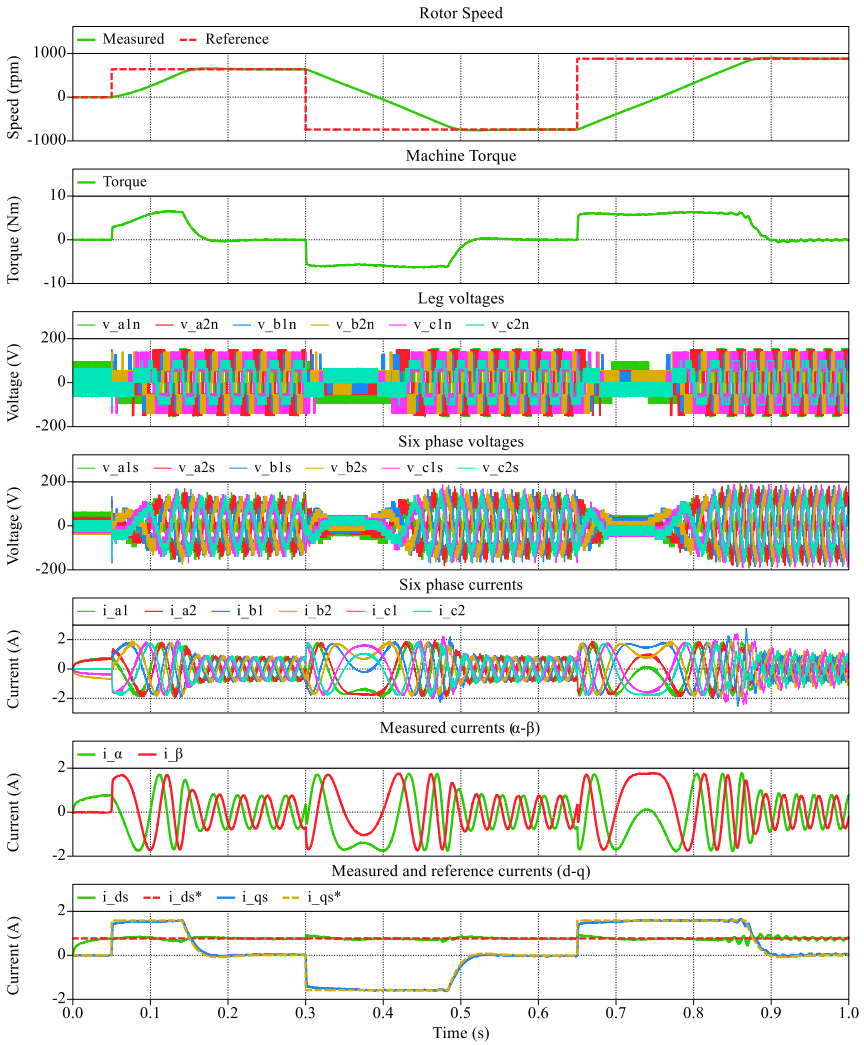
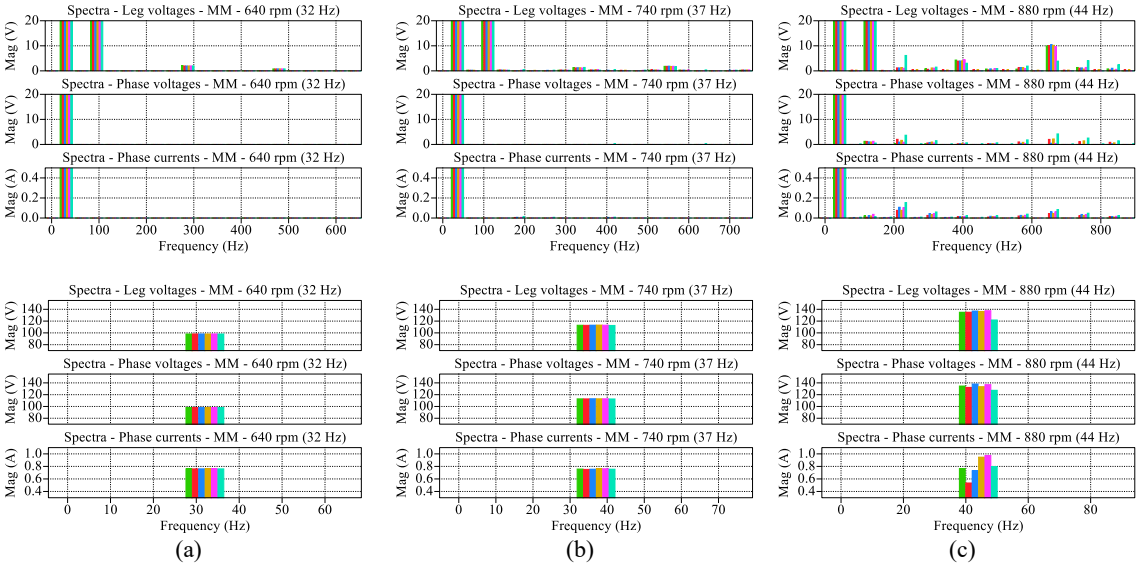


Figure 5.23: Simulation results - FOC of an asymmetrical six-phase IM under unbalanced dc-source voltages with double min-max injection using LS-PWM with step changes in reference speeds (no-load) of 640 rpm, −740 rpm, and 880 rpm. Top to bottom: speed (rpm), Torque (Nm), leg voltages, phase voltages, phase currents, α-β currents, reference and actual d-q currents.



(a) (b) (c)

Figure 5.24: Harmonic spectra of all six leg voltages, phase voltages and the phase currents obtained with double min-max injected references (LS-PWM) at speeds of (a) 640 rpm, (b) −740 rpm, and (c) 880 rpm. Top plots show the first 20 harmonics, and the bottom plots show the respective fundamental frequency components of the six phase variables.

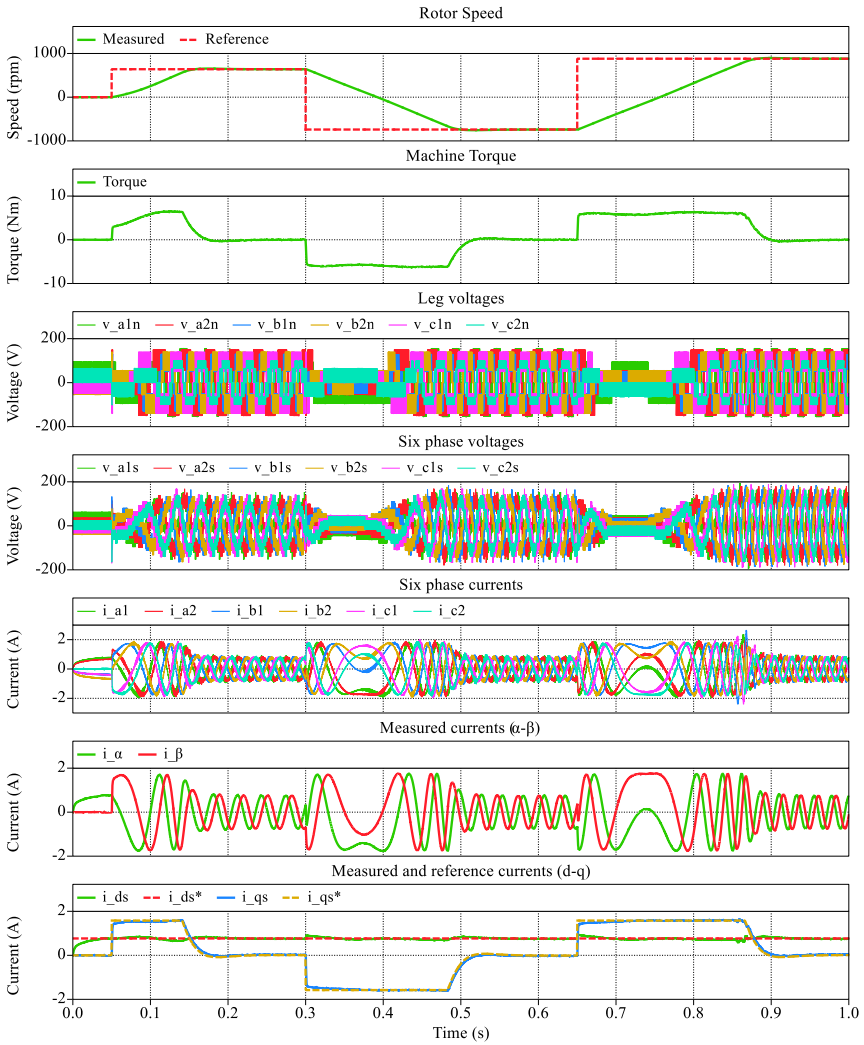
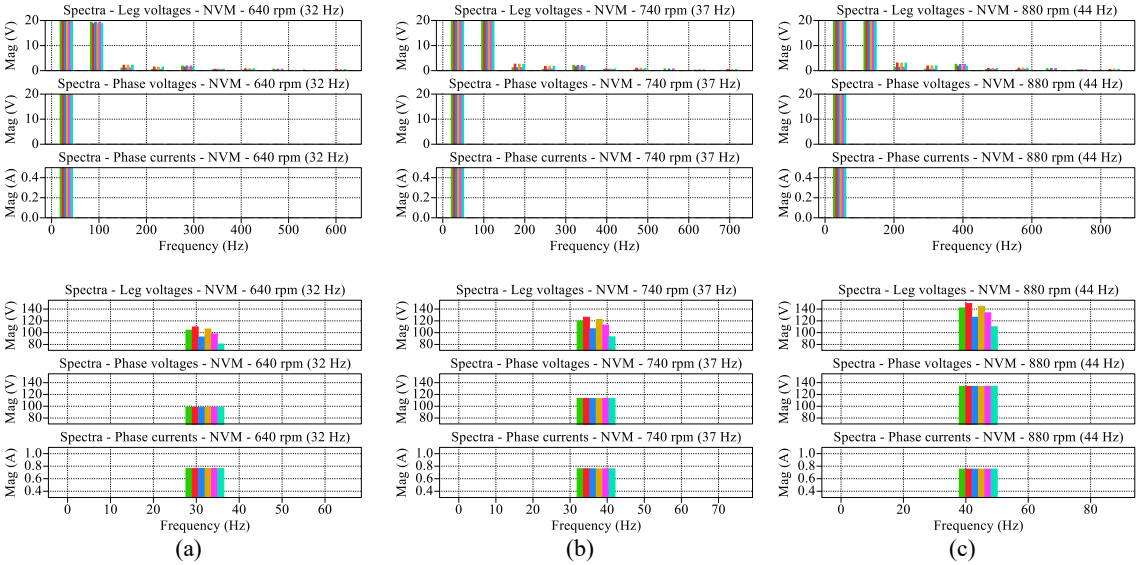


Figure 5.25: Simulation results - FOC of an asymmetrical six-phase IM under unbalanced dc-source voltages with NVM injected references using LS-PWM with step changes in reference speeds (no-load) of 640 rpm, −740 rpm, and 880 rpm. Top to bottom: speed (rpm), Torque (Nm), leg voltages, phase voltages, phase currents, α-β currents, reference and actual d-q currents.



(a) (b) (c)

Figure 5.26: Harmonic spectra of all six leg voltages, phase voltages and the phase currents obtained with NVM injected references (LS-PWM) at speeds of (a) 640 rpm, (b) −740 rpm, and (c) 880 rpm. Top plots show the first 20 harmonics, and the bottom plots show the respective fundamental frequency components of the six phase variables.

NVM method, the reference leg voltages are appropriately scaled with respect to the available total dc-source voltage of each leg (subsection 5.3.1).

Figure 5.26 shows that the same magnitude of currents is produced for all three speed references as no load has been applied to the machine. The response of the machine to the application of a load torque command of 2 Nm at 400 ms can be seen in Figure 5.27 where initially the machine was operating at a speed of 800 rpm. The system responds to a step in change in load torque and an expected increase in the current magnitudes is apparent.

A comparison between the application of the PS- and LS-PWM to the NVM method is performed in terms of the current THD of phase currents. Figure 5.28 shows a comparison between the switching harmonics of the phase currents when the machine is operated at

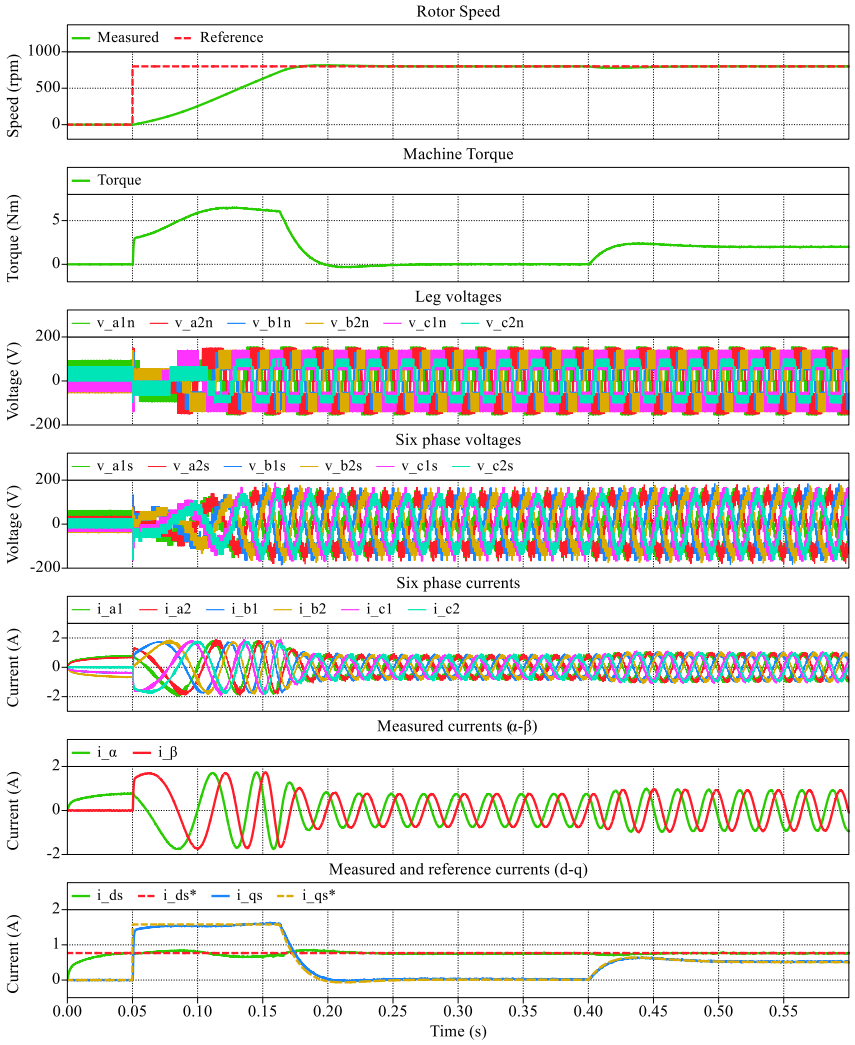


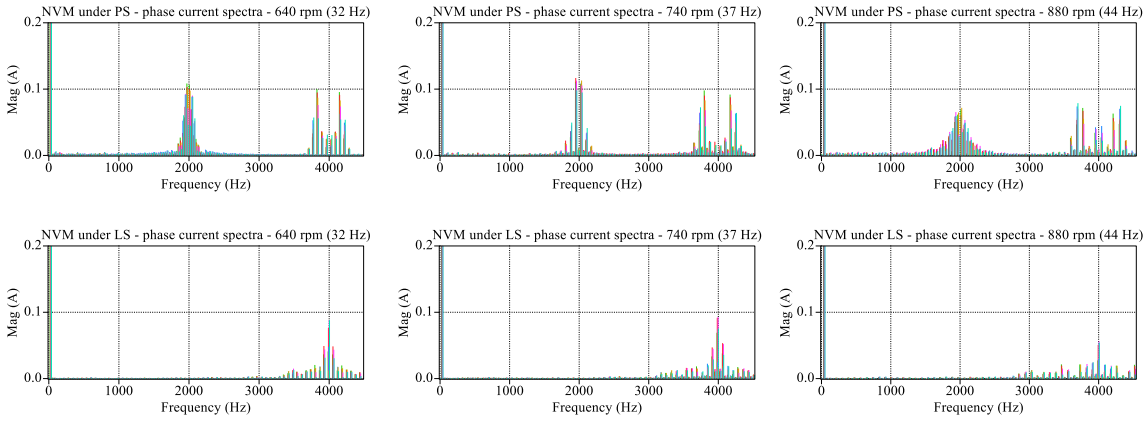
Figure 5.27: Simulation results - FOC of an asymmetrical six-phase IM under unbalanced dc-source voltages with NVM injected references using LS-PWM with step change in reference speeds of 800 rpm and load torque (2 Nm) application. Top to bottom: speed (rpm), Torque (Nm), leg voltages, phase voltages, phase currents, α-β currents, reference and actual d-q currents.

different speeds (no-load). At the effective converter switching frequency of 4 kHz, the presence of a current ripple at 2 kHz (which are not present in balanced case, see Figure 4.19a) makes it clear that the benefits of the PS-PWM are lost when there is unbalance between different phase legs of the inverter. On the contrary, it can be seen that the LS-PWM method does not suffer from such an issue as the dominant harmonic lies at the effective inverter switching frequency (4 kHz), as expected.

Decomposition of the phase currents into the stationary reference frame shows that most of the harmonic energy is concentrated in the loss producing x-y plane (see Figure 5.29) instead of the flux/torque producing α-β plane (Figure 5.30), for both the PS and LS methods. The harmonics in the x-y plane are roughly 20 times larger than those in the α-β plane (for the LS method). Therefore, a reduction in the magnitude of these harmonics and the elimination of the harmonic at $2f_c$ for PS with the suggested LS method can be directly correlated with a significant reduction in magnitude of the x-y currents, and consequently the losses in the machine. A comparison between the projections of the α-β and x-y plane currents, at the chosen speeds for the PS (top) and LS (bottom) methods, are shown in Figure 5.31 for the NVM injected references. It is obvious that the asymmetries caused due to the voltage imbalance in the PS method cause significantly higher currents in the x-y plane.

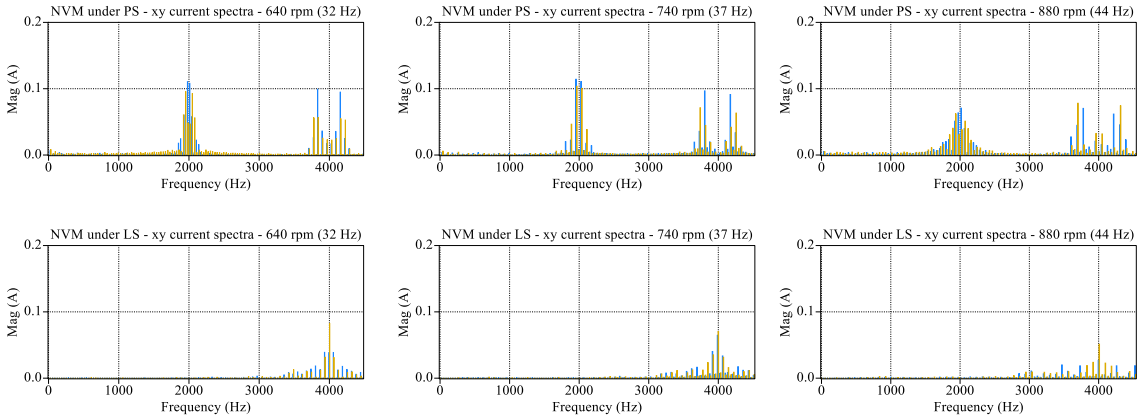
Furthermore, the harmonic content of the suggested LS method is also relatively low (10-15%) compared to the PS (25-30%) method as can be seen from the current THD for different operating speeds in Figure 5.32. It must also be pointed out that in Figure 5.32 the current THD values are different for different phases. This is because of the dc-source voltage unbalance where a different modulation index and different amount of offset voltage injection leads to slightly different leg voltage waveforms. Moreover, in some cases, certain legs with a lower total dc-source voltage might need a higher number of converter levels to produce the desired phase voltage, which would results in a lower THD value.

The current THD shown (Figure 5.32) are at an effective converter switching frequency of 4 kHz which equates to an average device switching frequency of 1 kHz for the LS-PWM method, if appropriate cycling of the dc-sources is conducted. The respective average device switching frequencies at the effective converter switching frequencies of 8 kHz and 16 kHz are 2 kHz and 4 kHz, which are still reasonably low.



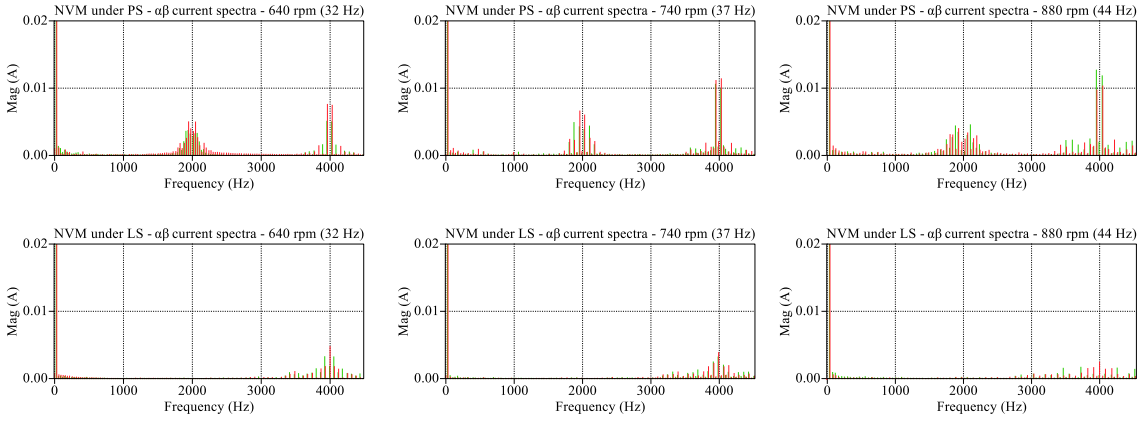
(a) (b) (c)

Figure 5.28: Harmonic spectra of the phase currents (no load, switching at 4 kHz) obtained with NVM injected references using the PS-PWM (Top) and LS-PWM (Bottom) methods at speeds of (a) 640 rpm, (b) 740 rpm, and (c) 880 rpm.



(a) (b) (c)

Figure 5.29: Harmonic spectra of the x-y currents (no load, switching at 4 kHz) obtained with NVM injected references using the PS-PWM (Top) and LS-PWM (Bottom) methods at speeds of (a) 640 rpm, (b) 740 rpm, and (c) 880 rpm.



(a) (b) (c)

Figure 5.30: Harmonic spectra of the α-β currents (no load, switching at 4 kHz) obtained with NVM injected references using the PS-PWM (Top) and LS-PWM (Bottom) methods at speeds of (a) 640 rpm, (b) 740 rpm, and (c) 880 rpm.

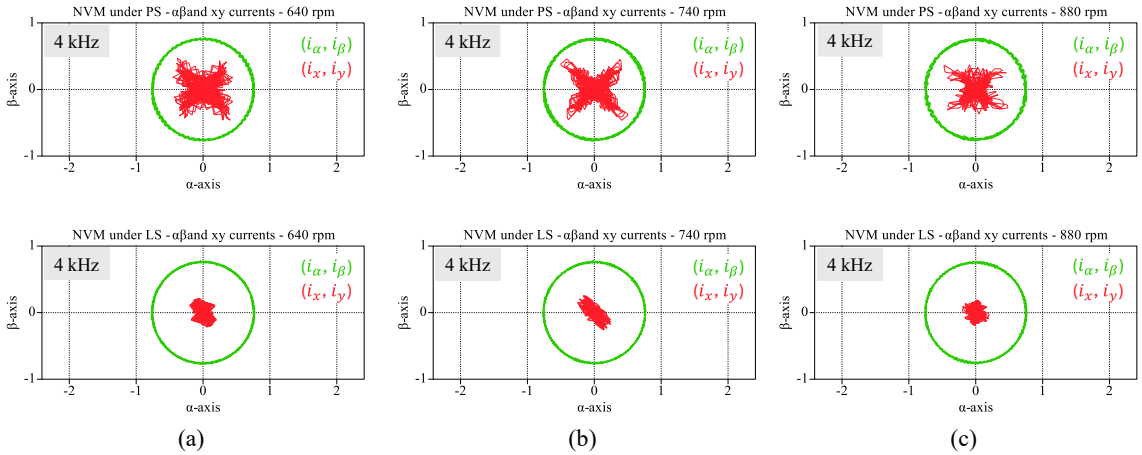


Figure 5.31: Projection of the α-β and x-y currents (no load, switching at 4 kHz) obtained with NVM injected references using the PS-PWM (Top) and LS-PWM (Bottom) methods at speeds of (a) 640 rpm, (b) 740 rpm, and (c) 880 rpm.

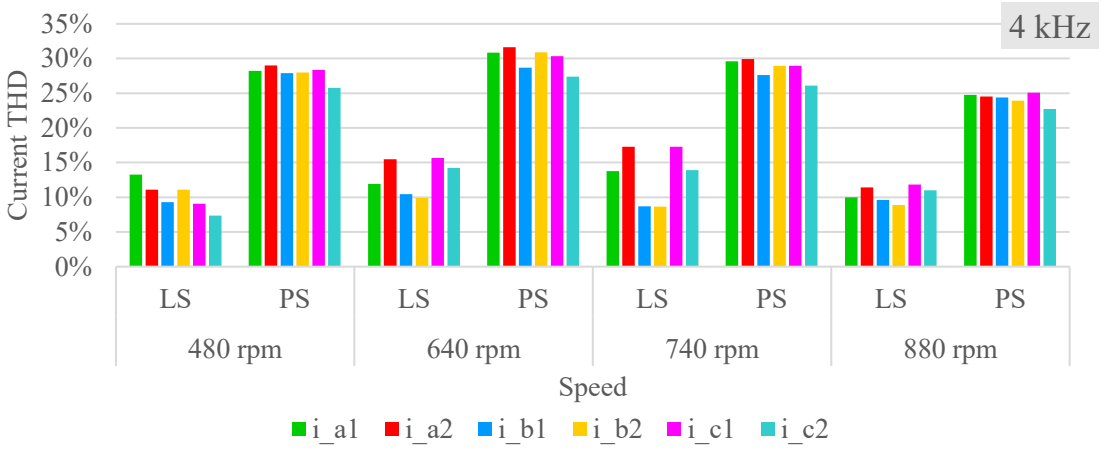


Figure 5.32: Current THD comparison of PS- and LS-PWM under NVM for an asymmetrical six-phase machine at speeds of 480 rpm, 640 rpm, 740 rpm, and 880 rpm at the effective converter switching frequency of 4 kHz (average device switching frequency of 1 kHz).

Therefore, a significant reduction in the amount of THD can be achieved with higher switching frequencies. Switching devices such as MOSFETs are generally switched at a much higher frequencies due to lower switching losses and faster transients. Furthermore, operation of the inverter at switching frequencies beyond the audible range (e.g., 20 kHz) would be preferred in an EV for obvious reasons. A significant decrease in the THD of the phase currents is evident from Figure 5.33 when the effective inverter switching frequency is increased from 4 kHz to 16 kHz. The THD was reduced from around 10-15% to 2-4% for the phase currents with the LS-PWM method.

Next, an analysis of the currents produced in the machine operating at 800 rpm with an applied load torque of 2 Nm (shown earlier in Figure 5.27 for 4 kHz switching frequency)

was conducted at different switching frequencies of 4 kHz, 8 kHz, and 16 kHz, respectively. Figure 5.34 shows the corresponding harmonic content of the x-y currents as well as the projection of the α-β and x-y plane currents at increasingly higher switching frequencies. The significant impact on the reduction of the loss producing x-y currents is noteworthy.

Finally, it was shown in subsection 4.3.2 that the suggested application of the modified LS-PWM under NVM leads to better energy management of the dc-sources (Figure 4.26). The point still holds true as the methodology has simply been extended from three to six phases.

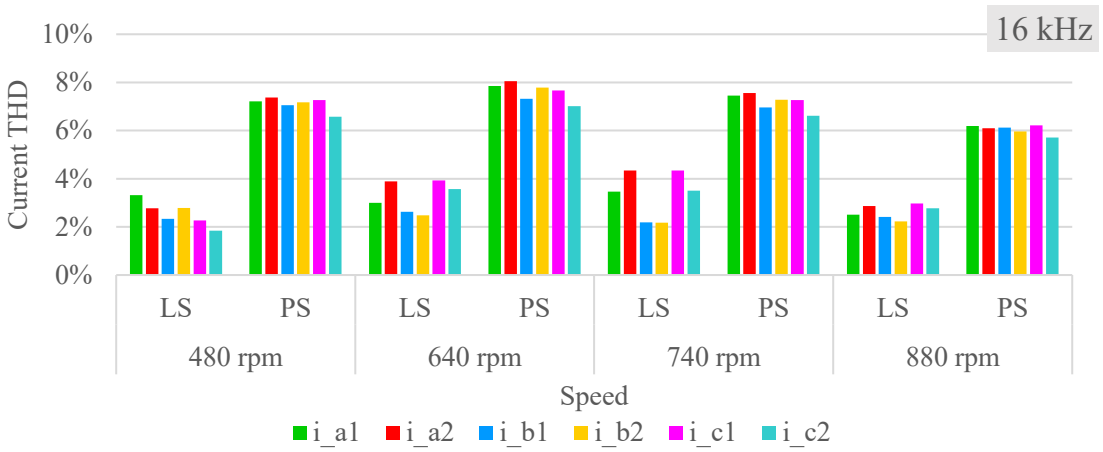
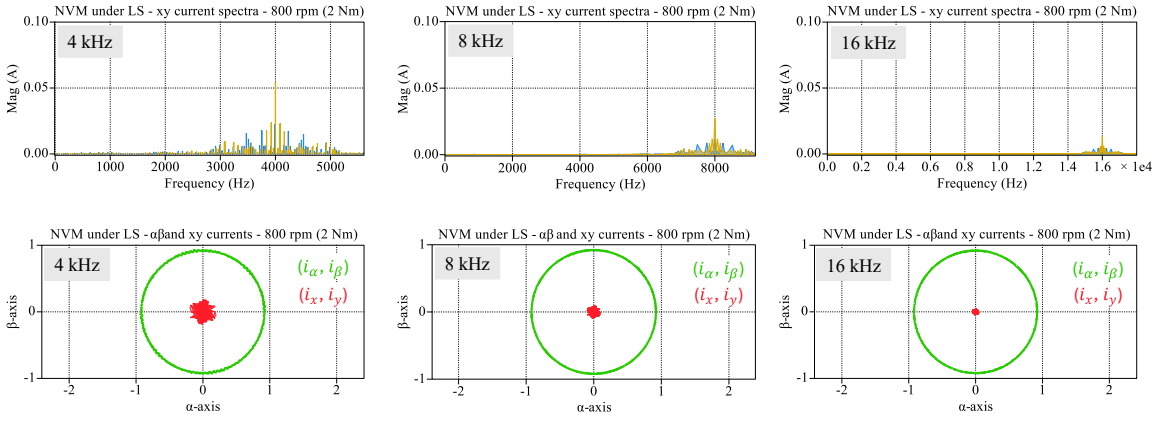


Figure 5.33: Current THD comparison of PS- and LS-PWM under NVM for an asymmetrical six-phase machine at speeds of 480 rpm, 640 rpm, 740 rpm, and 880 rpm at the effective converter switching frequency of 16 kHz (average device switching frequency of 4 kHz).



(a) (b) (c)

Figure 5.34: Harmonic spectra of the x-y currents (Top) and projection of the α-β and x-y currents (Bottom) obtained with NVM injected references using the LS-PWM method at 800 rpm with a load torque of 2 Nm at effective converter switching frequencies of (a) 4 kHz, (b) 8 kHz, and (c) 16 kHz.

5.5 Summary

This chapter described the high-performance control of a six-phase induction machine using a five-level six-phase cascaded H-bridge inverter. Section 5.2 discussed different modelling approaches of a multiphase induction machine. The modelling of an n-phase machine based on phase variables was first discussed. Further on, the complete model of a multiphase machine in the rotational reference frame was presented. Next, high-performance control based on the indirect rotor flux orientation in a multiphase machine was presented in section 5.3 which is a necessary step for the demonstration of the speed control of presented multilevel multiphase drive.

Subsequently, the methods developed in Chapter 3, 4, 5 and in the preceding sections of this chapter were implemented in section 5.4. First, the developed methods and theories were verified experimentally with open-loop control of a three-phase induction machine under different operating conditions. Measured leg voltages, phase voltages and currents were shown, and an analysis of the harmonic spectra was presented. It was noted that the application of different min-max injections produces current harmonic distortion figures that are indistinguishable due to the high number of converter voltage levels even at a reasonably low switching frequency of 2 kHz, as well as the filtering effect of the machine winding inductance.

Next, high-performance control of an asymmetrical six-phase induction machine using the developed five-level CHB multilevel inverter with balanced dc-source voltages was presented for the first time in (Khan et al., 2024a) for EV drivetrains. The operation of the drive system was tested and verified, in simulation and experimentally, at different speed references and the respective voltage and current waveforms were presented along with a discussion of the harmonic spectra. Even at a relatively low inverter switching frequency of 4 kHz, the produced phase a1 and a2 current THD was less than 5% at all operating speeds (Table 5.5). Furthermore, low order current harmonic magnitudes (e.g., 5^{th}, 7^{th}, 17^{th} and 19^{th}) were negligibly small (<25 mA) and did not require regulation (Figure 5.18), which could be performed with the presented harmonic suppression scheme.

After that, high-performance control of the same machine but with unbalanced dc-source voltages was presented (in simulation) for the first time. No literature is available on the FOC of a multiphase machine under dc-source voltage imbalance. Furthermore, the

impact of individual dc-source voltage imbalance caused by the standard PS-PWM on the secondary x-y plane harmonics has not been studied before. This specifically included the application and extension of the methods developed in section 4.3 for three-phase systems to the multiphase machine with a pair of three-phase winding sets. Simulation results were presented for the operation of the machine under different operating speeds and the results obtained validated the implementation of the suggested methods. The extension of the modulation index depth under unbalanced dc-source voltages with the suggested method was achieved even with a significant dc-source unbalance.

The spectra of the flux/torque producing α-β plane as well as the loss producing x-y plane showed that the harmonic energy can almost entirely be attributed to the losses from the higher magnitudes of the x-y current harmonics, for both the PS and LS modulation methods. For example, for the LS method, x-y current harmonics (Figure 5.29) were approximately 20 times greater than those observed in the α-β plane (Figure 5.30). However, the presence of the dominant harmonic and its sidebands at $2f_c$, in the case of the PS method resulted in a higher THD of the phase currents at all operating speeds. On the contrary, the use of suggested LS method led to the elimination of the harmonic at $2f_c$ and a lower overall THD of the phase currents (10-15%) as compared to the PS (25-30%) method at a switching frequency of 4 kHz, at all operating speeds (Figure 5.32). An increase in the switching frequency from 4 kHz to 16 kHz was shown to significantly reduce the THD of the phase currents to around 2-4% for the LS method in contrast to the PS method (6-8%) as shown in Figure 5.33. Such an increase in the switching frequency is warranted to reduce audible noise from inverter switches. This is particularly relevant if MOSFETs are used as switching devices because they can be operated at higher switching frequencies due to inherently lower switching losses as compared to conduction losses.

Finally, use of the suggested modified LS-PWM method allows for the SoC balancing of the dc-sources in the case of a voltage unbalance whereas the standard PS-PWM method does not. This is a significant improvement over the originally developed PS based method. The suggested method also improves the performance of the drive in low speed (low partial load) operation. This corresponds to low modulation index regions where the dc-sources with higher voltages (SoC) can be used while dc-sources with lower voltages (SoC) may be left unutilised leading to much better energy management of the dc-sources.

Chapter 6
Conclusion

6.1 Summary

The thesis presented a novel drivetrain design of an EV based on the combination of a multilevel converter connected to a multiphase induction machine. The cascaded H-bridge converter topology was chosen due to its relative simplicity, redundancy, and modular design. The performance of the multilevel multiphase drive was tested using high performance speed control in conjunction with an asymmetrical six-phase induction machine under different operating conditions. The power electronics converter operates with low rated voltage MOSFET switches at a relatively low switching frequency (4 kHz - 16 kHz) while returning a low harmonic distortion of the machine voltages and currents. The presented drivetrain provides unique benefits compared to the standard EV drivetrain as it concurrently benefits from salient features of both multilevel converters and multiphase machines. Other benefits include lower power per phase, low $\mathrm{d}v/\mathrm{d}t$, lower EMI, and reduced common mode voltages, while the modular nature of the battery-converter modules enhances safety as the maximum dc-source voltage of the system is limited to that of a single dc-source voltage. However, certain challenges associated with the control of multilevel multiphase drives from the perspective of EVs should be considered. These include supply of auxiliary loads, a larger than usual number of sensors, and power and control cables - all of which have negative implications in terms of hardware/system cost, space, and reliability.

The thesis starts by providing an overview of the literature on different multilevel converter topologies and applications including classical designs of the cascaded H-bridge multilevel inverter as well as certain hybrid topologies. Next, a literature survey on multiphase machines including modeling and control of multiphase machines was presented. After that, a literature survey on different modulation methods including the low and high frequency modulation methods was presented. The following section provides a survey of important literature on batteries, state-of-charge balancing methods, and voltage balancing methods. Specific literature that discusses the balancing methods in relevant applications such as the BESS as well as in EV applications was presented. Finally, the last section of the literature survey was focused on providing state-of-the-art solutions with respect to current

EV drivetrain topologies. These included solutions based on the two-level as well as the multilevel converter topologies including modular topologies such as the CHB, MMC and MMSP topologies, which were mostly focused on the three-phase machines. It was found that there exists a gap in the literature and the suggested multilevel multiphase topology based on the CHB inverter is worth further investigation for its application in EV drivetrains.

Chapter 3 focused on the cascaded H-bridge multilevel converter. The CHB topology was presented and the relevant modulation methods applicable to the CHB were presented. This included the low switching frequency methods including the nearest level modulation and the selective harmonic elimination methods. Simulation results were presented for the low frequency modulation methods for a three-phase nine-level CHB converter connected to an RL load. After that, multilevel phase-shifted and different iterations of the level-shifted modulation methods were presented. This was followed by the presentation of simulation results for single-phase and three-phase operation of a nine-level CHB converter. Again, considering the whole modulation index range, the performance of the methods in terms of the harmonic distortion of the phase voltages and currents was evaluated via simulation and verified experimentally on an RL load. A comparison between the different multicarrier based modulation methods conclusively showed that the IPD-PWM method performed best in terms of the total harmonic distortion of the phase voltages and currents over the entire linear modulation index range.

As the IPD-PWM method was shown to achieve the best harmonic distortion profile, it was necessary to focus on the power distribution and equalization techniques required to overcome the limitations of the IPD-PWM, which were also discussed in the last section of Chapter 3. The discussed techniques included different configurations for the rotation of the carrier waveforms at different frequencies such as the fundamental frequency carrier rotation as well as the much faster MSIPD, MSPOD, MTIPD, and MTPOD. Simulation results verifying the suitability of the discussed methods were also presented. Another solution based on the rotation of the reference waveforms was also presented and implemented and showed to achieve balance discharge of the dc-sources over a period of time. This methodology is further utilised due to its ease of implementation and application in achieving balanced dc-source utilisation in both equal and unequal dc-source voltage conditions.

Chapter 4 dealt with the operation of a three-phase CHB under sinusoidal and different min-max based offset voltage injection methods, both in equal and unequal dc-source

voltage conditions. In the first section, under equal dc-source voltage conditions, different min-max injection methods were presented. A comparison of the min-max based injections in combination with the different multicarrier based phase- and level-shifted methods was made in terms of the harmonic performance of the phase voltages and currents for the entirety of the modulation index range. It was shown that the second min-max injection produced the best harmonic performance of the phase currents in the modulation range below unity while the double min-max injection performed best in the over modulation range.

Next, the second section of the chapter provided a solution for the issue of the inevitable unbalance of the dc-source voltages in the operation of a CHB inverter. A recent improvement on a previously proposed so-called neutral voltage modulation (NVM) method was shown to resolve issues of the unbalanced operation of a three-phase CHB converter under unequal dc-source voltage conditions. However, it was shown that the proposed solution which used the PS-PWM method suffered from certain drawbacks such as the current ripple at the twice the carrier frequency as well as equal discharge of the dc-sources even in unbalanced dc-source voltage conditions (which in this case is not favorable). Resolution of the aforementioned problems was suggested with a modified LS-PWM method which overcomes both of the said issues, albeit at the cost of a slightly higher system complexity.

As a result of the lessons learnt in the previous sections, application of modulation and min-max injection techniques to multiphase machines was the next logical step. Chapter 5 introduced the multiphase machine model including the phase variable model and the model obtained after application of the decoupling and rotational transformations. Thereafter, rotor flux-oriented control of multiphase machines was presented in detail. Next, the operation of a three-phase induction machine was verified in open-loop using the developed CHB inverter at different operating speeds. After that, the developed IRFOC scheme was implemented on an asymmetrical six-phase induction machine using the level-shifted PWM along with the min-max injection for extension of the modulation index range. Operation at different operating points (speeds) was verified and the experimental results were presented confirming the accurate implementation of the developed control scheme. Finally, the operation of the multilevel multiphase CHB drive with unbalanced dc-source voltages was considered. The methods previously developed for the three-phase system were applied to the multiphase system and the developed scheme was tested via simulation to confirm

accurate operation of the system. It was shown that a significant extension of the modulation index range is realised while the issues of the PS-PWM under dc-source voltage imbalance are resolved. The suggested method provides a significantly better harmonic performance of the currents, elimination of the harmonic ripple at twice the carrier frequency, as well as significantly better control over the dc-source utilisation in the unequal dc-source voltage conditions.

6.2 Future work

This thesis has provided background for the development of an EV drivetrain using a battery supplied cascaded H-bridge inverter. Operation of the drivetrain inverter in a three- and multiphase scenario has been presented. Important issues addressed include the choice of the modulation method and the operation of the inverter under equal and unequal dc-source voltage conditions through appropriate offset voltage injections. These issues are necessary to ensure balanced operation of the system while achieving the best harmonic performance. A high-performance control of a multiphase machine using a five-level CHB was developed and verified experimentally in conjunction with an asymmetrical six-phase induction machine. Natural progression of the work could involve:

- Experimental verification of high-performance control of a multiphase machine in unbalanced dc source voltage conditions using the suggested level-shifted based NVM modulation method where the terminal voltages of the dc-sources (batteries) are periodically sampled, and the developed high performance control methods are applied.
- Operation with higher dc-source voltages as well as for higher rated machines at rated frequencies.
- Charging mode of operation of the drivetrain to be developed.
- A redesign of the H-bridge modules to limit the EMI issues. The use of fiber-optic communication modules instead of the cables used for PWM signals.
- A study on the impact of wide bandgap-based switching devices such as SiC and GaN in the multiphase CHB. Likely to benefit from increased switching frequencies and better thermal performance.
- A study providing an efficiency analysis of the suggested topology using a standard drive cycle in conjunction with a multiphase machine. The results can be compared to those obtained using a standard two-level inverter supplying a three-phase induction machine.

- A comparison between other topologies which offer a reduced switch count could be made especially as the number of a controller PWM outputs is limited.
- Even though a nine-phase machine would provide fast and slow charging capability, it would be worth investigating if a nine-phase machine could provide further enhancements, without further increasing the system complexity. The issue with the limited number of PWM signals which need to be synchronised would be much higher for a nine-phase machine.
- Operation of the machine in field-weakening region.
- Implementation of the control scheme and testing on a multiphase PMSM.
- An optimal solution in terms of the number of converter levels and phases can be realised through an analysis of the drivetrain performance and efficiency at different operating points, and the associated system complexity and cost.

Chapter 7

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Appendix A
Decoupling transformation

In this Appendix vector space decomposition (VSD) transformation for different number of phases, and different number of neutral points is analysed for a general n-phase multiphase machine (remember, $n = pg$, where g is number of winding sets, and p is the number of phases per set). Both symmetrical and asymmetrical case are covered. First, single neutral point case is covered, further transformation for multiple isolated neutral points case is analysed, and finally the final set of multiphase machine equations in $\alpha\beta xyz$ reference frame (obtained after the application of VSD transformation) is given.

A.1 Single neutral point

Let us consider first **symmetrical** multiphase machine with machine phase angle arrangement θ_{sym} as in (5.2). VSD transformation for a symmetrical induction machine with an even number of machine phases (and a single neutral point) can be described by:

$$\left[T_{VSD,ES1}\right]_{n\times n} = \frac{2}{n}\begin{bmatrix} \cos\left(\left[\theta_{sym}\right]\right) \\ \sin\left(\left[\theta_{sym}\right]\right) \\ \cos\left(2\left[\theta_{sym}\right]\right) \\ \sin\left(2\left[\theta_{sym}\right]\right) \\ \cos\left(3\left[\theta_{sym}\right]\right) \\ \sin\left(3\left[\theta_{sym}\right]\right) \\ \vdots \\ \cos\left(\frac{n-2}{2}\left[\theta_{sym}\right]\right) \\ \sin\left(\frac{n-2}{2}\left[\theta_{sym}\right]\right) \\ \frac{1}{2}\cos\left(n\left[\theta_{sym}\right]\right) \\ \frac{1}{2}\cos\left(\frac{n}{2}\left[\theta_{sym}\right]\right) \end{bmatrix}\begin{matrix} \alpha \\ \beta \\ x_1 \\ y_1 \\ x_2 \\ y_2 \\ \vdots \\ x_{\frac{n-4}{2}} \\ y_{\frac{n-4}{2}} \\ z_+ \\ z_- \end{matrix} \tag{A.1}$$

In the transformation matrix above, one can see that the phase propagation angle matrix ($[\theta_{sym}]$) has an integer multiplier in front. If the value of that multiplier is equal to the integer multiple of p, then those x-y subspaces (called zero-sequence subspaces) are placed below the non-zero sequence components in the transformation matrix, and just above z_+ and z_- axes (called zero-sequence homopolar components), as suggested in (Zoric et al., 2017). As it will be shown, this is a convenient arrangement when multiple neutral points are present.

In the case of a symmetrical multiphase machine with an odd number of phases (and a single neutral point), the transformation matrix is described as:

$$[T_{VSD,OS1}]_{n\times n} = \frac{2}{n}\begin{bmatrix} \cos([\theta_{sym}]) & \alpha \\ \sin([\theta_{sym}]) & \beta \\ \cos(2[\theta_{sym}]) & x_1 \\ \sin(2[\theta_{sym}]) & y_1 \\ \cos(3[\theta_{sym}]) & x_2 \\ \sin(3[\theta_{sym}]) & y_2 \\ \vdots & \vdots \\ \cos\left(\frac{n-1}{2}[\theta_{sym}]\right) & x_{\frac{n-3}{2}} \\ \sin\left(\frac{n-1}{2}[\theta_{sym}]\right) & y_{\frac{n-3}{2}} \\ \frac{1}{2}\cos(n[\theta_{sym}]) & z_+ \end{bmatrix} \quad \text{(A.2)}$$

Again, zero sequence x-y components are placed below the non-zero sequence components, and above a single row of real-valued zero sequence homopolar component.

As can be seen, for a symmetrical machine with an even number of machine phases, a pair of real-valued zero sequence components z_+ and z_- are produced. However, for symmetrical machines with an odd number of machine phases, a single row of real-valued zero sequence component z_+ is produced.

It must also be pointed out that the coefficient $(2/n)$ in front of the decoupling matrix is the amplitude invariant transformation where the amplitudes before and after the transformation are the same, but the total powers of the original and decoupled machines are

not the same. This necessitates the scaling of the torque equation by a factor of $n/2$. In contrast, a power invariant transformation has a coefficient of $(\sqrt{2/n})$ in front of the decoupling matrix where the total powers are kept the same before and after the transformation. Similarly, the coefficient of $(1/2)$ in front of the real valued zero sequence components corresponds to the amplitude invariant transformation which must be changed to $(1/\sqrt{2})$ if a power invariant transformation is being used.

Considering an **asymmetrical** machine, first it should be noted that θ_{asym} from (5.4) should be used. For asymmetrical induction machines with an even number of machine phases and a single neutral point, the transformation matrix can be defined as:

$$\left[T_{VSD,EA1}\right]_{n\times n} = \frac{2}{n}\begin{bmatrix} \cos([\theta_{asym}]) \\ \sin([\theta_{asym}]) \\ \cos(3[\theta_{asym}]) \\ \sin(3[\theta_{asym}]) \\ \cos(5[\theta_{asym}]) \\ \sin(5[\theta_{asym}]) \\ \vdots \\ \cos\left((\mathrm{n}-1)[\theta_{asym}]\right) \\ \sin\left((\mathrm{n}-1)[\theta_{asym}]\right) \end{bmatrix} \begin{matrix} \alpha \\ \beta \\ x_1 \\ y_1 \\ x_2 \\ y_2 \\ \vdots \\ x_{\frac{n-4}{2}} \\ y_{\frac{n-4}{2}} \end{matrix} \tag{A.3}$$

From (A.3) one can see that for asymmetrical machines, all even numbered coefficients of the phase propagation angle matrix are absent. Also note that no real-valued zero sequence components (z components) are present. Rows with coefficients which are multiples of p produce zero sequence x-y subspaces and are placed at the bottom of the matrix.

Finally, the VSD transformation matrix for an asymmetric multiphase machine with an odd number of machine phases and a single neutral point is given as:

$$\left[T_{VSD,OA1}\right]_{n\times n} = \frac{2}{n}\begin{bmatrix} \cos([\theta_{asym}]) \\ \sin([\theta_{asym}]) \\ \cos(3[\theta_{asym}]) \\ \sin(3[\theta_{asym}]) \\ \cos(5[\theta_{asym}]) \\ \sin(5[\theta_{asym}]) \\ \vdots \\ \cos\left((n-2)[\theta_{asym}]\right) \\ \sin\left((n-2)[\theta_{asym}]\right) \\ \frac{1}{2}\cos(n[\theta_{asym}]) \end{bmatrix} \begin{matrix} \alpha \\ \beta \\ x_1 \\ y_1 \\ x_2 \\ y_2 \\ \vdots \\ x_{\frac{n-3}{2}} \\ y_{\frac{n-3}{2}} \\ z_+ \end{matrix} \tag{A.4}$$

Clearly again, asymmetrical machines with an odd number of machine phases also produce a single row of real-valued zero sequence component (z_+ component). As before, those zero sequence x-y subspace(s) are placed after the non-zero sequence subspaces and before the real-valued, z_+, zero sequence component.

A.2 Multiple Neutral points

Machines configured with multiple neutral points will have g winding sets and therefore as many neutral points. As no current can flow between different winding sets, those zero sequence x-y subspaces (that were conveniently placed just above real valued z components), as well as the real-valued zero (z) sequence components (which together have been placed at the end of the VSD transformation matrices), should be simply replaced by individual zero sequence components of each winding set, given as:

$$[ZS] = \begin{bmatrix} g/2 & 0 & \cdots & 0 & g/2 & 0 & \cdots & 0 \\ 0 & g/2 & \cdots & 0 & 0 & g/2 & \cdots & 0 \\ 0 & 0 & \ddots & \vdots & 0 & 0 & \ddots & \vdots \\ 0 & 0 & \cdots & g/2 & 0 & 0 & \cdots & g/2 \end{bmatrix} \tag{A.5}$$

It should be noted that the zero sequence constant $g/2$ is further multiplied by $2/n$ in the original decoupling transformation matrix to give $1/p$ in the amplitude invariant transformation. The equivalent zero sequence constant for the power invariant

transformation would have to be $\sqrt{g/2}$ to result in $1/\sqrt{p}$ after multiplication with the coefficient ($\sqrt{2/n}$) in front of the decoupling transformation matrix.

A.3 Machine model after VSD transformation

The appropriate VSD transformation matrices can be applied to either the stator or rotor variables such as voltages, currents, or flux linkages in phase variable reference frame. The application of the transformation matrix results in the decoupling of the phase variables where the first subspace (α-β) is related to the flux and torque production while other x-y subspaces are lossy (non-flux/torque producing) along with a real-valued zero sequence components. The final set of equation describing a multiphase machine, obtained after application of adequate decoupling transformation (from subsections A.1/A.2) onto equations in phase variables domain (given in subsection 5.2.1), is given below:

$$\begin{aligned} v_{\alpha s} &= R_s i_{\alpha s} + \frac{\mathrm{d}\psi_{\alpha s}}{\mathrm{d}t} \\ &= R_s i_{\alpha s} + (L_{ls} + L_m)\frac{\mathrm{d}i_{\alpha s}}{\mathrm{d}t} + L_m \frac{\mathrm{d}}{\mathrm{d}t}\left(i_{\alpha r}\cos\theta_e - i_{\beta r}\sin\theta_e\right) \end{aligned} \tag{A.6}$$

$$\begin{aligned} v_{\beta s} &= R_s i_{\beta s} + \frac{\mathrm{d}\psi_{\beta s}}{\mathrm{d}t} \\ &= R_s i_{\beta s} + (L_{ls} + L_m)\frac{\mathrm{d}i_{\beta s}}{\mathrm{d}t} + L_m \frac{\mathrm{d}}{\mathrm{d}t}\left(i_{\alpha r}\sin\theta_e + i_{\beta r}\cos\theta_e\right) \end{aligned} \tag{A.7}$$

$$v_{x_k s} = R_s i_{x_k s} + \frac{\mathrm{d}\psi_{x_k s}}{\mathrm{d}t} = R_s i_{x_k s} + L_{ls}\frac{\mathrm{d}i_{x_k s}}{\mathrm{d}t} \tag{A.8}$$

$$v_{y_k s} = R_s i_{y_k s} + \frac{\mathrm{d}\psi_{y_k s}}{\mathrm{d}t} = R_s i_{y_k s} + L_{ls}\frac{\mathrm{d}i_{y_k s}}{\mathrm{d}t} \tag{A.9}$$

$$v_{z_+ s} = R_s i_{z_+ s} + \frac{\mathrm{d}\psi_{z_+ s}}{\mathrm{d}t} = R_s i_{z_+ s} + L_{ls}\frac{\mathrm{d}i_{z_+ s}}{\mathrm{d}t} \tag{A.10}$$

$$v_{z_- s} = R_s i_{z_- s} + \frac{\mathrm{d}\psi_{z_- s}}{\mathrm{d}t} = R_s i_{z_- s} + L_{ls}\frac{\mathrm{d}i_{z_- s}}{\mathrm{d}t} \tag{A.11}$$

In (A.6) and (A.7), L_m represents magnetizing inductance, and $L_m = M(n/2)$. In (A.8) to (A.9), the subscript index k is indicative of the subspace number and takes values from 1 to $(n-3)/2$ for machines with an odd number of machine phases and $(n-4)/2$ for machines with an even number of phases. Additionally, the negative zero sequence component (A.11)

is not taken into consideration for machines with an odd number of phases. Next, the equations for the rotor are given as:

$$\begin{aligned} v_{\alpha r} &= R_r i_{\alpha r} + \frac{\mathrm{d}\psi_{\alpha r}}{\mathrm{d}t} \\ &= R_r i_{\alpha r} + (L_{lr} + L_m)\frac{\mathrm{d}i_{\alpha r}}{\mathrm{d}t} + L_m \frac{\mathrm{d}}{\mathrm{d}t}\left(i_{\alpha S}\cos\theta_e + i_{\beta s}\sin\theta_e\right) = 0 \end{aligned} \tag{A.12}$$

$$\begin{aligned} v_{\beta r} &= R_r i_{\beta r} + \frac{\mathrm{d}\psi_{\beta r}}{\mathrm{d}t} \\ &= R_r i_{\beta r} + (L_{\mathrm{lr}} + L_m)\frac{\mathrm{d}i_{\beta r}}{\mathrm{d}t} + L_m \frac{\mathrm{d}}{\mathrm{d}t}\left(-i_{\alpha S}\sin\theta_e + i_{\beta s}\cos\theta_e\right) = 0 \end{aligned} \tag{A.13}$$

$$v_{x_k r} = R_r i_{x_k r} + \frac{\mathrm{d}\psi_{x_k r}}{\mathrm{d}t} = R_r i_{x_k r} + L_{lr}\frac{\mathrm{d}i_{x_k r}}{\mathrm{d}t} = 0 \tag{A.14}$$

$$v_{y_k r} = R_r i_{y_k r} + \frac{\mathrm{d}\psi_{y_k r}}{\mathrm{d}t} = R_r i_{y_k r} + L_{lr}\frac{\mathrm{d}i_{y_k r}}{\mathrm{d}t} = 0 \tag{A.15}$$

$$v_{z_+ r} = R_r i_{z_+ r} + \frac{\mathrm{d}\psi_{z_+ r}}{\mathrm{d}t} = R i_{z_+ r} + L_{ir}\frac{\mathrm{d}i_{z_+ r}}{\mathrm{d}t} = 0 \tag{A.16}$$

$$v_{z_- r} = R_r i_{z_- r} + \frac{\mathrm{d}\psi_{z_- r}}{\mathrm{d}t} = R i_{z_- r} + L_{ir}\frac{\mathrm{d}i_{z_- r}}{\mathrm{d}t} = 0 \tag{A.17}$$

This completes the transformation from the phase variable machine into a simplified and decoupled machine model in the $\alpha\beta xyz$ domain. The only coupling that remains between the rotor and stator quantities is in the α-β subspace. The x-y stator components will only be present in the case of unbalance or asymmetries in the source supply voltage.

The electromagnetic torque equation can be given as:

$$T_e = \frac{n}{2} P L_m\left(\cos\theta_e\left(i_{\alpha r} i_{\beta s} - i_{\beta r} i_{\alpha s}\right) - \sin\theta_e\left(i_{\alpha r} i_{\alpha s} + i_{\beta r} i_{\beta s}\right)\right) \tag{A.18}$$

It can be seen that the generated torque of the machine solely depends on currents in the α-β subspace. This leads to a considerable simplification of the machine model. However, the machine model still suffers from nonlinearity. Additionally, the differential equations contain time-varying inductance coefficients which can be eliminated through the rotation transformation presented in the next section.

Appendix B
Rotational transformation

Rotational Park's transformation is a follow up transformation in which α-β stator and rotor quantities (with time varying coefficients) are transformed into new, common, d-q axes, which will lead to a fully decouple system. The d and q axis are perpendicular to each other. If the speed of rotation of the common reference frame is chosen as ω_a, then it follows that the instantaneous position, θ_s, of the d-axis of the common reference frame with respect to the axis of the first stator phase can be described using the relationship:

$$\theta_s = \int_0^t \omega_a \, \mathrm{d}t \tag{B.1}$$

As always, indices s and r are for the stator and rotor variables, respectively. If the instantaneous position of the axis of the first rotor phase with respect to the axis of the first stator phase is denoted by θ_e, one can define the instantaneous position of the d-axis of the common reference frame with respect to the axis of the first rotor phase through:

$$\theta_r = \theta_s - \theta_e = \int (\omega_a - \omega_e) \, \mathrm{d}t \tag{B.2}$$

The orientation of all axes is illustrated in Figure B.1, and in fact it is the same as in the three-phase case. The transformation angle for stator quantities is θ_s, whereas for rotor quantities it is θ_r. The matrix for the transformation of stator quantities (voltages, currents, flux linkages) can be expressed as:

$$[D_s]_{n\times n} = \begin{bmatrix} \cos(\theta_s) & \sin(\theta_s) & 0 & 0 & \cdots & 0 \\ -\sin(\theta_s) & \cos(\theta_s) & 0 & 0 & \cdots & 0 \\ 0 & 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 1 \end{bmatrix} \begin{matrix} d_s \\ q_s \\ x_{1s} \\ y_{1s} \\ \vdots \\ z_s \end{matrix} \tag{B.3}$$

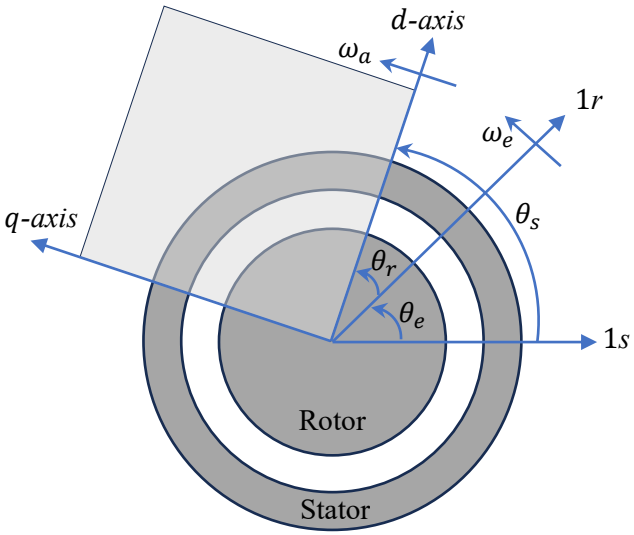

Figure B.1: Rotational transformation diagram for a multiphase induction machine model

Similarly, the transformation matrix for rotor quantities (voltages, currents, flux linkages) can be expressed as:

$$[D_r]_{n\times n} = \begin{bmatrix} \cos(\theta_r) & \sin(\theta_r) & 0 & 0 & \cdots & 0 \\ -\sin(\theta_r) & \cos(\theta_r) & 0 & 0 & \cdots & 0 \\ 0 & 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & 0 & \cdots & 1 \end{bmatrix} \begin{matrix} d_r \\ q_r \\ x_{1r} \\ y_{1r} \\ \vdots \\ z_r \end{matrix} \tag{B.4}$$

After the application of the rotation transformation matrices from (B.3) and (B.4), onto the final set of equations from subsection A.3 (given in $\alpha\beta xyz$ domain), the final decoupled multiphase machine model in an arbitrary rotating common reference frame is obtained. This final set of equations is given in subsection 5.2.2.

Appendix C
Asymmetrical six-phase induction machine model

An asymmetrical six-phase induction machine with a pair of three-phase winding sets spatially displaced by 30°, each with its own star connected isolated neutral point, can be described with its phase propagation angles as:

$$[\theta_{6a}] = [0 \quad \frac{\pi}{6} \quad \frac{4\pi}{6} \quad \frac{5\pi}{6} \quad \frac{8\pi}{6} \quad \frac{9\pi}{6}] \tag{C.1}$$

The Clarke transformation is first applied to the phase variable model through the application of vector space decomposition (VSD) transformation matrix as:

$$[T] = \frac{2}{6}\begin{bmatrix} \cos([\theta_{6a}]) \\ \sin([\theta_{6a}]) \\ \cos(5[\theta_{6a}]) \\ \sin(5[\theta_{6a}]) \\ 1 \quad 0 \quad 1 \quad 0 \quad 1 \quad 0 \\ 0 \quad 1 \quad 0 \quad 1 \quad 0 \quad 1 \end{bmatrix} \tag{C.2}$$

A simplification of the model is thus achieved due to the production of three two-dimensional subspaces which are mutually orthogonal leading to a decoupled system with the machine flux and torque being produced solely due to the α-β current components. A further rotational transformation (Park transformation) of the α-β components is performed to eliminate time-dependent inductance terms leading to a set of differential equations with constant coefficients. The Park transformation matrix is defined as:

$$\begin{bmatrix} u_d \\ u_q \end{bmatrix} = \begin{bmatrix} \cos\phi & \sin\phi \\ -\sin\phi & \cos\phi \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \tag{C.3}$$

After application of the Park's transformation, with an angular velocity ω_a of the common d-q reference plane, the voltage equations for the stator and rotor (indices s and r) are given as:

$$\begin{bmatrix} v_{ds} \\ v_{qs} \end{bmatrix} = \begin{bmatrix} R_s & 0 \\ 0 & R_s \end{bmatrix} \begin{bmatrix} i_{ds} \\ i_{qs} \end{bmatrix} + \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \psi_{ds} \\ \psi_{qs} \end{bmatrix} + \omega_a \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \psi_{ds} \\ \psi_{qs} \end{bmatrix} \tag{C.4}$$

$$\begin{bmatrix} v_{dr} \\ v_{qr} \end{bmatrix} = \begin{bmatrix} R_r & 0 \\ 0 & R_r \end{bmatrix} \begin{bmatrix} i_{dr} \\ i_{qr} \end{bmatrix} + \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \psi_{dr} \\ \psi_{qr} \end{bmatrix} + (\omega_a - \omega_e) \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \psi_{dr} \\ \psi_{qr} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \end{bmatrix} \quad \text{(C.5)}$$

Where R_s and R_r are the stator and rotor resistance, respectively; ω_e is electrical speed of the rotor; and v, i and ψ with relevant indices represent d or q component of the stator (s) or rotor (r) voltage, current or flux linkage, respectively.

In addition, the x-y components in the stationary reference frame after the application of the first transformation only involve the variables associated with the stator since the rotor windings are considered as short-circuited (squirrel-cage IM):

$$\begin{bmatrix} v_{xs} \\ v_{ys} \end{bmatrix} = \begin{bmatrix} R_s & 0 \\ 0 & R_s \end{bmatrix} \begin{bmatrix} i_{xs} \\ i_{ys} \end{bmatrix} + \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} \psi_{xs} \\ \psi_{ys} \end{bmatrix} \quad \text{(C.6)}$$

Under a balanced symmetrical sinusoidal voltage source, the x-y components are zero, but this is not the case in practice. Additionally, zero sequence current cannot flow between two isolated neutral points which leads to the omission of the zero-sequence voltage equation. With multiple neutral points, the dc-link voltage utilization is also maximised through appropriate zero sequence voltage injection. The flux linkage (ψ) equations can be given in terms of the magnetizing (L_m) and leakage (L_l) inductances (stator/rotor) and the respective d-q currents, as:

$$\begin{bmatrix} \psi_{ds} \\ \psi_{qs} \\ \psi_{dr} \\ \psi_{qr} \end{bmatrix} = \begin{bmatrix} L_m + L_{ls} & 0 & L_m & 0 \\ 0 & L_m + L_{ls} & 0 & L_m \\ L_m & 0 & L_m + L_{lr} & 0 \\ 0 & L_m & 0 & L_m + L_{lr} \end{bmatrix} \begin{bmatrix} i_{ds} \\ i_{qs} \\ i_{dr} \\ i_{qr} \end{bmatrix} \quad \text{(C.7)}$$

$$\begin{bmatrix} \psi_{xs} \\ \psi_{ys} \end{bmatrix} = \begin{bmatrix} L_{ls} & 0 \\ 0 & L_{ls} \end{bmatrix} \begin{bmatrix} i_{xs} \\ i_{ys} \end{bmatrix} \quad \text{(C.8)}$$

The electromechanical torque of the machine includes a scaling factor ($n/2$) due to the application of the amplitude invariant transformation of (C.2), resulting in:

$$T_e = \frac{6}{2} P\left(\psi_{ds} i_{qs} - \psi_{qs} i_{ds}\right) = \frac{6}{2} P L_m \left(i_{dr} i_{qs} - i_{qr} i_{ds}\right) \quad \text{(C.9)}$$

The preceding mathematical model describes the asymmetrical six-phase IM which was used for simulation in section 5.4.

Appendix D
List of publications

D.1 Publications

Khan, M.U., Dordevic, O. and Jones, M. (2022) Current THD comparison of different offset injections in the linear modulation range for cascaded H-bridge converters. *XIV International Symposium on Industrial Electronics and Applications (INDEL)*, 9-11 Nov. 2022.

Khan, M.U., Dordevic, O. and Jones, M. (2024a) High performance control of an asymmetrical six-phase induction machine using a five-level cascaded H-bridge inverter for EV drivetrains. *Annual Conference of the IEEE Industrial Electronics Society (IECON)*, 3-6 Nov. 2024.

Khan, M.U., Dordevic, O. and Jones, M. (2024b) Performance enhancement of neutral voltage modulation in cascaded H-bridge inverters under dc-source voltage imbalance using modified level-shifted PWM. *XV International Symposium on Industrial Electronics and Applications (INDEL)*, 6-8 Nov. 2024.

D.2 Co-authored publications

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