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Strategic bottlenecks in the semiconductor industry supply chain: a Kraljic matrix perspective

Gary Graham ^a, Samir Dani ^b and Andros Gregoriou ^c

^aOperations and Supply Chain Management, Liverpool John Moores University Business School, Liverpool, UK; ^bOperations and Supply Chain Management, Keele Business School, Keele University, Keele, UK; ^cFinance, Liverpool John Moores University Business School, Liverpool, UK

ABSTRACT

The semiconductor industry supply chain is complex, with globally distributed production processes and tightly interconnected segments. By controlling the production and supply of essential technologies and equipment, 'bottleneck' firms often dominate specific segments of the supply chain, making them critical to the manufacturing processes of advanced semiconductors. For instance, they dictate specific processes or product types, invest in innovative technologies, and protect their intellectual property to establish new markets with high entry barriers. Additionally, we find bottleneck firms who have support from their governments to maintain a competitive edge over rivals. Through social network analysis, we identify that there are eight bottleneck firms of high nodal centrality. We then present case study results of these firms on their local ego networks, how they have created strategic bottlenecks and detail government actions/interventions in preserving or challenging their bottlenecks. A Kraljic perspective is used to classify these eight firms into leverage, strategic, non-critical and bottleneck partners. Furthermore, we aim to make a theoretical contribution to the bodies of production research knowledge on supply – chain bottlenecks and structural power.

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Bottlenecks; network position; Kraljic; social network analysis; operational risk

1. Introduction

The multinational corporation (MNC) has emerged as the dominant actor in global supply chains (SC). Economists such as Paul Krugman emphasise that concepts such as '*economies of scale*' and '*low unit costs of production*' drove the rapid global supply chain expansion by MNCs. With supply chains designed by entrepreneurial capital to achieve profit maximisation and the highest possible returns on asset investment (Handfield, Graham, and Burns 2020). Furthermore, Krugman's (1979; 2009) theory of '*increasing returns*' emphasises that trade and the design of global supply chains allow MNCs to exploit scale economies and incentivise them to benefit from agglomeration economies.

Farrell and Newman (2019, 46) argue that MNCs, through their social networks, create '*structural power*' and through this, they have the power to set the rules of competition. By taking advantage of central nodes – those with high centrality and many supplier and customer connections – the MNC can effectively create '*bottlenecks*' in the network, which can be leveraged for structural power. This concept of the bottleneck mirrors Hirschman's (1945) argument that the key for the

MNC in generating influence in trade comes from the development of monopoly power.

However, Fishman (2025) notes that there has been a stunning resurgence of '*state power*' and '*economic intervention*' in the semiconductor industry supply chain in a world supposedly governed by MNCs and market forces.¹ Also, if we apply the seminal work on purchasing (as a strategic discipline) by Kraljic (1983), we can identify firms other than MNCs that have '*bottleneck*' positions. For instance, there are specialised equipment manufacturers that manufacture highly specific machinery that is crucial in the production process. Then there are critical component and mineral suppliers who, through their limited availability, introduce unique supply risks and vulnerabilities. Finally, there are design and intellectual property (IP) specialists who create core design and automation tools.

This paper aims to make a theoretical contribution to the bodies of knowledge on supply chain '*bottlenecks*' and structural power in supplier networks (Chen and Evers 2023; Kim, Chen, and Linderman 2015; Nguyen et al. 2025). We apply procurement and sourcing theory to inform how firms have created and sustained their

CONTACT Gary Graham  g.graham@ljmu.ac.uk  Liverpool John Moores University, Business School, Redmonds Building, Brownlow Hill, Liverpool L2 2QP, UK

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strategic bottleneck positioning. The primary purpose of our study is to identify ‘dominant’ and ‘specialist’ bottleneck firms in the semiconductor supply network and explain how they have created and sustained their bottleneck positioning using a Kraljic approach focusing on customer power (Kraljic 1983). Therefore, the two research questions we seek to answer through our paper are:

RQ1. What are the semiconductor supply chain bottlenecks?

RQ2. Do dominant and specialist firms in the semiconductor supply chain create bottlenecks for strategic competitive advantage?

The remainder of the paper is as follows. In the next section, in the first part of the literature review, we present an overview of the semiconductor supply chain, discussing its design characteristics; then, we review prior research on procurement and sourcing theory, before presenting Kraljic’s seminal framework. Section 3 outlines the research methods adopted for the investigation of supply chain network analysis and case study development. Section 4 reports the results from the network analysis to identify bottleneck firms, followed by the case study results in Section 5. Section 6 presents the cross-case analysis and Section 7 the Kraljic framework approach to positioning eight case companies. Finally, Section 8 provides conclusions and our future research agenda.

2. Literature review

The semiconductor industry is integral to the production of microchips, which are essential components in devices ranging from smartphones to automobiles. The industry is highly competitive, with major players located in regions such as the United States, Japan, South Korea, Taiwan, Europe, and China. This section examines the structure of the semiconductor industry and the design of the supply chain. The section will briefly explain the key roles, the process stages, dynamics of vertical integration and the unique characteristics of the semiconductor supply chain.

2.1. Overview of the semiconductor supply chain

In Figure 1, customer collaboration is built into the flow through defined original equipment manufacturer (OEM) requirements loops, early hardware/software (HW/SW) co-validation during the testing and validation stage, and structured feedback after final test and qualification. The OEM and supply chain partners can align priorities and feed improvements back into the next design cycle by freezing the register transfer level (RTL)

and running joint simulations prior to tape-out – when the chip’s design is finalised so production can begin at the foundry. Such benefits of joint decision-making (Cao and Zhang 2011) and collaboration (Barratt 2004) are well documented in the supply chain literature. At this stage, the chip exists as code that can be simulated, verified, and refined before moving on to physical layout and, eventually, tape-out.

Therefore, the design and authorisation phase starts once the OEM requirements are frozen, allowing the design team to complete RTL integration, verification, and pre-silicon tests without scope changes. Before mask generation, the design must pass readiness gates covering design for manufacturability (DFM), test coverage closure, and sign-off all engineering change orders (ECOs), confirming the chip is functionally correct and manufacturable. A readiness gate is a formal checkpoint in a project or production flow where progress is paused to confirm that specific criteria have been met before moving to the next stage. This disciplined hand-off reduces the risk of re-spins and protects mask and wafer start schedules.

In supply chain terms, the disciplined readiness gates and formal authorisation in Figure 1 reflect what Handfield and Bechtel (2002) describe as the ‘role of clear commitments, trust, and structured information exchange’ in improving responsiveness and reducing uncertainty before major production commitments. This is complemented by Narasimhan, Swink and Kim’s (2006) finding that combining process discipline (‘*leanness*’) with adaptive capacity (‘*agility*’) at such decision points can simultaneously protect downstream schedules and enhance the chain’s ability to respond to risk.

Finally, the manufacturing and assembly phase starts when wafers enter the foundry for fabrication and ends when chips are ready for their final test. The wafers go through patterning, layering and etching processes. Once the wafers are cut into what are known as Known Good Die (KGD), often an outsourced semiconductor assembly and test (OSAT) partner then will mount them into substrates, then seals them before running early screening checks. Wafer output is closely coordinated with OSAT’s assembly and testing schedules. For the manufacturing and assembly phase in Figure 1, coordination between wafer fabrication, OSAT packaging, and final test readiness reflects what Lin, Chen, and Chien (2014) identify as the need for integrated scheduling and yield-driven decision-making across final-stage processes to optimise throughput and delivery reliability.

This sequence of activities blends technical workflows with organisational interdependencies across design houses, foundries, outsourced assembly and test

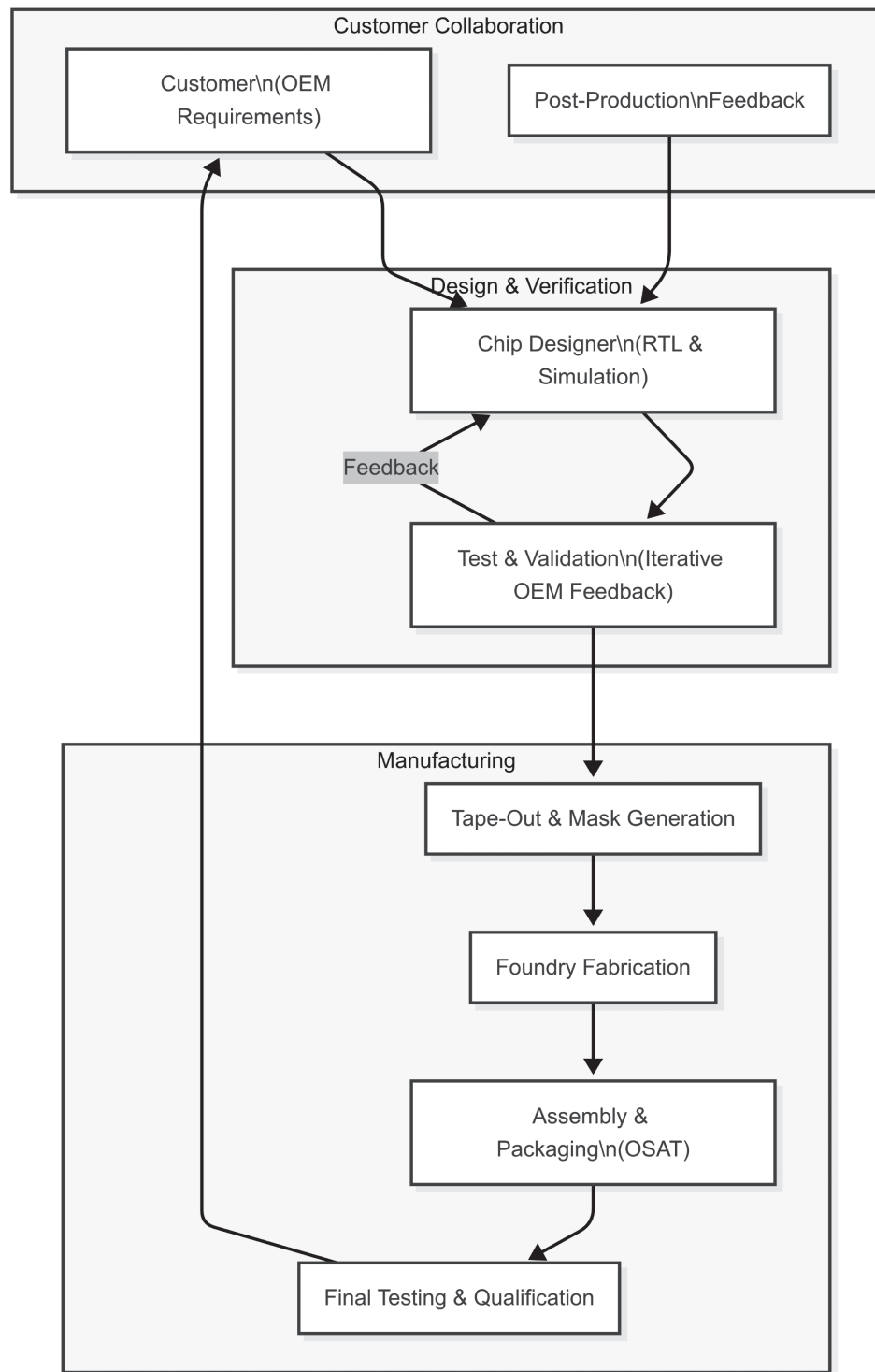


Figure 1. The semiconductor industry supply chain.

providers, and vertically integrated device manufacturers (IDMs). Supply chain structures vary markedly: fabless firms such as Qualcomm and NVIDIA specialise in design while outsourcing production, whereas IDMs like Intel and Samsung operate their own fabrication facilities alongside design functions. Some foundries focus

solely on manufacturing without in-house chip design capability, creating distinct governance and supply chain configurations. These differences need to be borne in mind when interpreting bottleneck and risk exposure points (Curtis 2025; IBISWorld 2025).

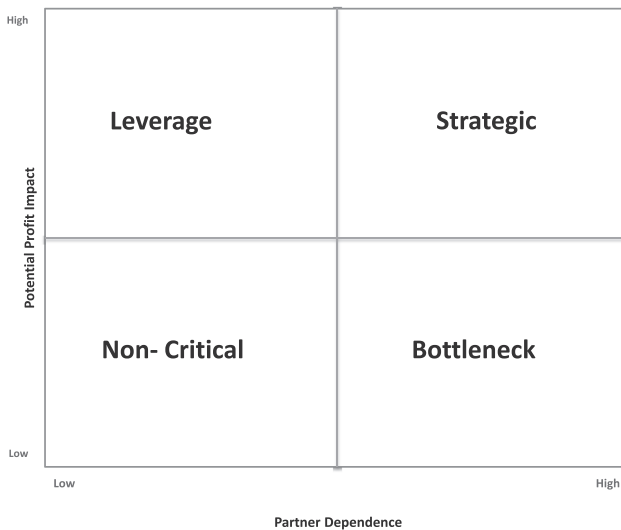


Figure 2. The Kraljic purchasing portfolio matrix.

2.2. Theoretical underpinning

Purchasing portfolio models have received much attention in the recent literature about professional purchasing. Whilst Luzzini (2012) offers a detailed critique, believing the classification system is too practitioner-oriented, lacks a theoretical foundation and needs robust testing, Kraljic's (1983) remains the most seminal and applied portfolio model. His model has had a broad influence on professional purchasing (see the evidence of Gelderman and Van Weele 2003; Kamann and Bakker 2004).² It also inspired many academic writers to undertake further research into portfolio models (e.g. Bensaou 1999; Croom 2000; Dubois and Pedersen 2002; Dyer, Cho, and Chu 1998; Gelderman and Van Weele 2002, 2003, 2005; Lilliecreutz and Ydreskog 1999; Nellore and Söderquist 2000; Olsen and Ellram 1997; Wagner and Johnson 2004; Wynstra and ten Pierick 2000; Zolkiewski and Turnbull 2002).³ However, Luzzini (2012) does offer a critique, arguing that the classification system is too practitioner-oriented, lacks a theoretical foundation, and needs more thorough empirical testing.

We believe the framework (Figure 2) is particularly suited to our investigation as its basis is on 'power' and 'dependence', which are antecedent theoretical constructs to 'bottleneck' analysis in the semiconductor industry supply chain. In response to Luzzini (2012), we argue that Kraljic is one of the most tested frameworks in purchasing and supply chain management. Both theoreticians and practitioners have relied on it extensively for undertaking investigations into the nature and form of 'buyer' and 'supplier' strategy and behaviour (Hesping and Schiele 2016; Narasimhan and Prasad 2016).

According to Kraljic (1983), a firm's supply strategy depends on two factors: (1) profit impact and (2) supply risk. Other scholars have introduced variations of the original Kraljic matrix (Elliott-Shircore and Steele 1985; Hadelar and Evans 1994; Olsen and Ellram 1997; Syson 1992).⁴ The Kraljic Matrix (1983) is therefore: '... a strategic tool used to segment the supply base and develop differentiated purchasing strategies based on two key dimensions: profit impact and supply risk' (109).

The framework highlights the balance of power and dependence between buyers and suppliers, categorising purchases into four quadrants based on profit impact and supply risk:

- Strategic items: high profit impact and high supply risk. Companies are highly dependent on suppliers, making power dynamics crucial.
- Leverage items: high profit impact but low supply risk. Buyers hold more power due to multiple supplier options.
- Bottleneck items: low profit impact but high supply risk. Suppliers have more power, as alternatives are limited.
- Routine items: low profit impact and low supply risk. Power and dependence are minimal.

Kraljic emphasised that businesses must strategically manage supplier relationships to mitigate risks and optimise procurement strategies. Within the semiconductor supply chain from a buyer's perspective, the Kraljic model is useful for studying upstream supply risks. Supply chain risks associated with shortages of inputs to the supply chain through various bottlenecks are discussed within the semiconductor literature.

Identifying the status of these inputs (i.e. material, equipment, capacity, capabilities) about the impact they have on the buyer firm and subsequently the supply chain is possible using the Kraljic model. This will be different for each supply chain entity across the ecosystem or network, and these dependencies with the upstream entity will create the need for strategies as shown in the four quadrants of the Kraljic model (Figure 2). We explore the Kraljic dimensions of 'power' and 'dependence' through our social network and case study analysis of evidence on each supplier's bottleneck positioning.

3. Methodology

The research methodology is designed to answer the two research questions. The methodology uses secondary data sources to investigate the supply network ecosystem of the semiconductor industry. The full list of firms we investigated is presented in Online Appendix OA1 and

the data sources from which it is drawn is discussed in Section 3.1. The first method used for the investigation is social network analysis (SNA). The SNA provides a robust analysis for mapping the semiconductor chain to identify bottlenecks. For research question 2, which is focused on dominant and specialist firms in the chain and their influence on bottleneck strategy, we use a qualitative methodology to analyse dominant firms as cases. The case information is derived from secondary sources, and a cross-case analysis is established to study the intricacies of the relationships between these entities.

To ground our network-centric analysis in real-world perspectives, we presented our two research questions to a panel of industry practitioners. The panel participants are listed in Appendix B, and we present key insights from them in the conclusion.

3.1. Sampling and data sources – SNA

The sampling frame for the research combined the Bloomberg US Listed Semiconductors Select Price Return Index. This tracks the performance of the top 30 US-listed companies in the semiconductor sector concerning Market Capitalisation, with the Bloomberg Global Semiconductor Top 20 Price Return Index includes twenty global companies that derive significant revenue from the semiconductor business. Therefore, given the focus of our research on MNCs and the most influential companies in the supply chain the Bloomberg indices were well fitted to our unit of analysis.

Bloomberg SPLC⁵ gathers data from diverse sources, including the U.S. Securities and Exchange Commission, news articles, trade publications, firm websites, and private communications (Crook, Lê, and Smith 2020). While Bloomberg SPLC reports the revenue exposure associated with each supplier-customer relationship, these values represent estimated business dependence rather than measured financial flows (Gualandris et al. 2021). Specifically, Bloomberg SPLC provides information on the percentage of revenues and costs associated with each supplier and customer, enabling researchers to assess the financial exposure and dependency structure within a firm's supply chain (Gualandris et al. 2021).

The network is based on supplier-customer relationships drawn from the Bloomberg SPLC database and includes 122 firms connected by 140 supply links. The structure reflects the highly concentrated nature of the semiconductor industry, where a small number of upstream firms supply many downstream customers, while most firms rely on only one or two key suppliers. Although companies can be grouped broadly by function (such as equipment suppliers, design software providers,

and manufacturers), these groups are closely interconnected and depend on the same critical upstream firms. For this reason, the network is deliberately defined to focus on the most structurally important relationships that give rise to bottlenecks, rather than attempting to map every peripheral firm in the industry.

Therefore, the database includes only publicly disclosed buyer-supplier relationships. Furthermore, it only provides cross-sectional evidence at a specific moment in time, implying that the influence of time variation is ignored. According to Culot et al. (2023), errors in database classification and inaccurate assumptions introduce potential bias and inaccuracy. Therefore, to try and reduce bias and improve accuracy we sought to check the revenue exposure information against a range of semiconductor trade associations, industry and company reports.⁶

3.2. Social network analysis

Edges in the network were defined using the amount of business represented in each supplier-customer relationship, as reported in Bloomberg SPLC. The SPLC dataset provides the percentage of revenues and costs attributable to each supplier and customer, allowing us to capture the financial exposure embedded in these links. To identify firms acting as critical intermediaries in the flow of revenues across the network, we employed betweenness centrality, which highlights nodes that sit on a large share of shortest dependency paths and therefore have the potential to influence or disrupt connectivity between different parts of the supply chain.

Compared to other metrics such as degree centrality, it considers the entire network structure, not only direct connections. In Appendix C, Table A1 we conduct robustness checks across the centrality measures. All correlations above ~ 0.25 are statistically significant at $p < 0.01$ for Spearman's rho with $n \approx 120$. As a robustness check, we computed a range of alternative centrality measures on the directed supply network, including degree-based measures, PageRank, eigenvector centrality, HITS hubs and authorities, and bridging centrality. Betweenness centrality is strongly correlated with other global measures that capture systemic positioning, particularly PageRank and bridging centrality, as well as with outbound connectivity.

Nodes with high betweenness sit in the middle of many connections, so if they fail, large parts of the network can be disrupted. This measure also shows the main routes through which financial value moves between firms. Because of this, we used betweenness centrality to identify the main bottleneck firms in the semiconductor supply chain. In simple terms, it measures how often a

company lies on the shortest path between other companies, showing how much, it acts as a go-between in the system (Beaumier and Cartwright 2024).

At a broad level, betweenness centrality helps reveal whether bottlenecks exist in the global network by showing which companies sit on the '*shortest paths*' that connect different parts of the supply chain (Beaumier and Cartwright 2024). We also calculated local ego-network measures for each bottleneck firm and visualised these using UCINET; the results are presented in Appendix E (and Online Appendix OA3). For each dominant or specialist firm, we report their degree, density, Effect size, constraint, and hierarchy values.

3.3. Data sources – case studies

The case example evidence we collected was used to explore the nature of the semiconductor supply chain and was structured to capture the following:

- Background of the firm
- Ego network analysis
- Creation of their strategic bottlenecks
- Government actions/interventions in preserving or challenging the bottleneck.

Appendix A lists the source material we gathered from secondary sources, including Bloomberg Intelligence, published media interviews, company-published materials, industry journals and trade magazines, newspapers, as well as various online sources (Li et al. 2016). The construct validity of our cases was achieved by developing constructs through a literature review, using multiple sources of evidence, establishing a chain of evidence, and having each of the co-authors independently and then collectively review the case study reports (Miles and Huberman 1994; Yin 2009).

We also conducted a cross-case analysis to gain a deeper understanding by comparing multiple cases. This enhanced the generalisability of our findings and helped identify and confirm patterns, themes and insights not apparent when examining cases in isolation (Li et al. 2016; Yin 2009; Calantone and Vickery 2010).

4. Bottleneck firm identification

By mapping the financial exposure between customers and suppliers, we can visualise the structure of the semiconductor supply-chain network (Figure 3). Although the ties are based on revenue and cost exposure, the resulting network represents the pattern of relationships linking firms across the industry. As these two reporting conventions both represent the financial market value of

the relationship from the perspective of the customer and supplier.

4.1. Elbow method explanation

Statistical analyses for firm identification were conducted using R version 4.5.0 (R Core Team 2025), an open-source programming environment for statistical computing and graphics.⁷ The elbow method identifies the point in a ranked distribution where the rate of decline in betweenness centrality slows significantly. This is done by calculating the perpendicular distance of each point from the line connecting the first and last points in the distribution. The point with the maximum distance is considered the elbow. The plot (Figure C1, Appendix C) shows the betweenness centrality values ranked in descending order, with the elbow point (marked in red for the online version) appearing as the emphasised point on the curve. The sharper elbow around the top eight firms corresponds precisely to the eight structurally significant companies analysed in subsequent sections: NVIDIA, Tokyo Electron (TEL), TSMC, ASML, Cadence, Synopsys, LAM Research, and Mentor.

While the elbow analysis identified 15 structurally significant firms, visual inspection of the centrality curve reveals a sharper elbow around the top 8 firms. We present the 15 firms and their centrality scores in Appendix D.

4.2. Dominant bottleneck firms

In Table 1 we present the eight bottleneck firms with the highest betweenness centrality from our network analysis. The most dominant firm is TSMC with a betweenness centrality of 4850.39. Then there are Mentor Graphics and Cadence with values of 2847.87 and 2441.48. Other notable firms are NVIDIA, LAM Research, Synopsys, ASML and TEL.

In Figure 4, we examine the critical supply chain roles of our identified bottleneck firms. TSMC is what we categorise as a '*dominant state champion*' as it is the largest recipient of state support from the Taiwanese government. Then there are those '*dominant*' bottleneck firms which are MNCs such as ASML, LAM Research and NVIDIA. Finally, we have the '*less dominant*' specialist bottleneck firms such as Mentor (Siemens), Synopsys Inc, Cadence, and TEL. For instance, they manufacture highly specific machinery that is crucial in the production process, or they are design and intellectual property (IP) specialists who create core design and automation tools.

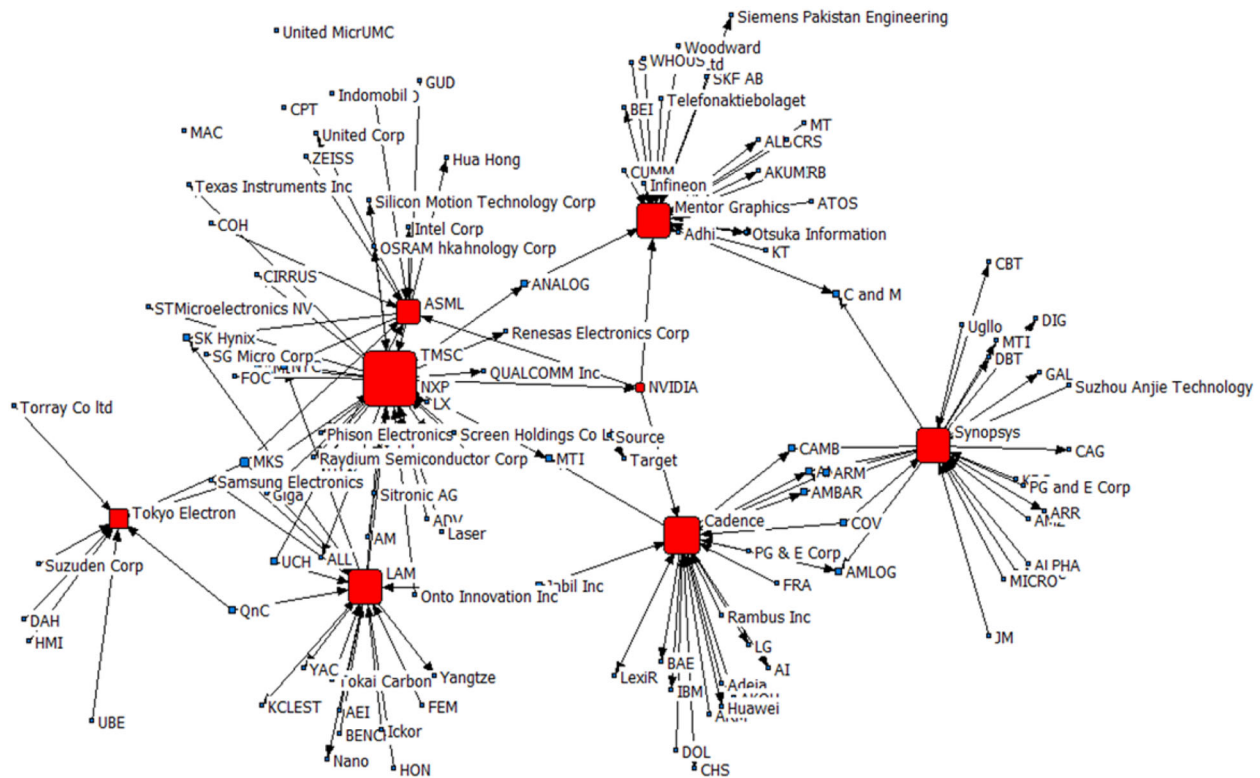


Figure 3. Supply chain network analysis of the semiconductor industry.

5. Case studies

In this⁸ section we present our case summaries. A full ego-network analysis is presented in Appendix E for TSMC and ASML (the remaining firms are presented in the online Appendix OA2). Meanwhile our cross-case analysis for the eight companies is summarised in Appendix F.

5.1. TSMC

TSMC makes chips at huge scale using the world's most advanced manufacturing technology. When we look at its immediate network of partners (Appendix E1), we find that it connects to 39 different firms, and almost all these ties are non-overlapping (Effect size is 40.6). The network around TSMC is also very sparse, meaning these firms are not well connected to each other. Its very low constraint score (0.033) shows that TSMC sits in a broker position – acting as a key link between many parts of the industry rather than being locked into a tight cluster.

TSMC's bottleneck power comes from three reinforcing factors:

- Massive scale and unique capacity – its factories and packaging facilities are extremely expensive and difficult for anyone else to copy, so customers have very few realistic alternatives.

- Best-in-class technology – TSMC stays ahead on advanced chip processes (like 3 nm and 2 nm), making it risky and unattractive for customers to switch to another supplier.
- Deep ecosystem relationships – TSMC works closely with customers and equipment makers at every stage of design and production, which makes it deeply embedded in how modern chips are developed.

Together, these factors mean that many companies depend heavily on TSMC, and in practice there are very few substitutes for what it provides.

5.2. ASML

ASML sits at the very centre of the semiconductor equipment world because it is the only company on the planet that can build EUV lithography machines – the tools needed to make the most advanced chips. The company grew out of Philips spin-outs and has spent decades building up the specialised knowledge, intellectual property, and supplier relationships needed to produce both EUV and the most advanced DUV systems. This gives ASML unmatched influence in the highest tier of the global equipment supply chain.

Its ego-network metrics underline this central role. ASML connects to 15 different firms, and the network

Table 1. Betweenness centrality for the dominant bottleneck semiconductor firms.

Network ID/full name	Betweenness centrality	Company information
TSMC – Taiwan Semiconductor Manufacturing Company Limited	4850.39	Role: Foundry services, manufacturing semiconductor chips.
Mentor – Mentor Graphics (now part of Siemens EDA)	2847.87	EDA tools and software for designing and testing semiconductor devices. EDA stands for Electronic Design Automation – the suite of software tools that semiconductor companies use to design, verify, and test integrated circuits and systems-on-chip.
Cadence – Cadence Design Systems, Inc.	2441.48	Electronic Design Automation (EDA) tools, which are used for designing semiconductor chips.
Synopsys – Synopsys, Inc.	2378.40	EDA tools and IP for semiconductor design.
TEL – Tokyo Electron Limited	2238.93	Provides semiconductor production equipment.
LAM Research – Lam Research Corporation	1913.08	LAM Research provides wafer fabrication equipment and services.
NVIDIA – NVIDIA Corporation	1755.63	Designs GPUs and AI accelerators.
ASML – Advanced Semiconductor Materials Lithography (ASML Holding N.V.)	1200.64	Advance Semiconductor Materials Lithography produces photolithography equipment used in chip manufacturing.

around it is very sparse (density 0.019), meaning these firms are not well connected to each other. Its large Effect size (14.733) shows that almost all its ties are non-redundant. In simple terms, ASML sits at the centre of a hub-and-spoke structure, acting as a key intermediary linking otherwise disconnected suppliers, subsystem specialists, and chipmakers (Appendix E2).

ASML's bottleneck power comes from three mutually reinforcing factors:

- Unique, protected technology – it alone has the IP, tacit know-how, and decades of cumulative R&D needed to build EUV machines at production scale.
- A tightly integrated supplier ecosystem – long-term co-development, strategic partnerships, and selective acquisitions ensure ASML controls or secures access to critical subsystems such as mirrors, lasers, and optics.

- Service and qualification lock-in – EUV and advanced DUV tools require complex maintenance, proprietary software, and specialised field engineers, which raise switching costs and lock in the installed base.

Together, these factors make ASML almost impossible to substitute for leading-edge lithography. The revenues generated from this position then fund further R&D, reinforcing its technological lead and market power. Geopolitics also shape ASML's position. Export controls restrict where its most advanced tools can be sold, and diplomatic negotiations have occasionally opened short-term licensing windows. These interventions limit near-term revenue but also raise barriers for potential competitors, indirectly strengthening ASML's strategic value to allied governments and leading chipmakers.

5.3. NVIDIA

NVIDIA was founded in 1993 and has grown from a graphics-chip designer into the leading platform for accelerated computing. It's hardware, software, and proprietary ecosystem – especially the CUDA programming platform – now power AI training, high-performance computing, and data-centre workloads. This means NVIDIA no longer acts just as a component supplier; it actively shapes demand and technology direction across the semiconductor industry.

Its network position reflects this shift. NVIDIA's ego network is small but strategically important: it connects to four firms, has a low density (0.167), and a high Effect size (3.5) (Online Appendix OA 3.1). In simple terms, NVIDIA relies on a few high-value partners, with TSMC as the most critical. This makes NVIDIA dependent on advanced manufacturing capacity while giving it influence upstream through its software standards and downstream through platform lock-in.

NVIDIA's structural power comes from three reinforcing mechanisms:

- Platform lock-in – CUDA and NVIDIA's software libraries make it difficult for customers to switch to other hardware without major cost and effort.
- Demand concentration – the surge in AI workloads pushes huge volumes of advanced manufacturing and packaging demand onto a small number of foundries, intensifying bottlenecks.
- Product-bundle leverage – NVIDIA can prioritise certain customers and bundle products strategically, allowing it to allocate scarce supply in ways that reinforce its market influence.

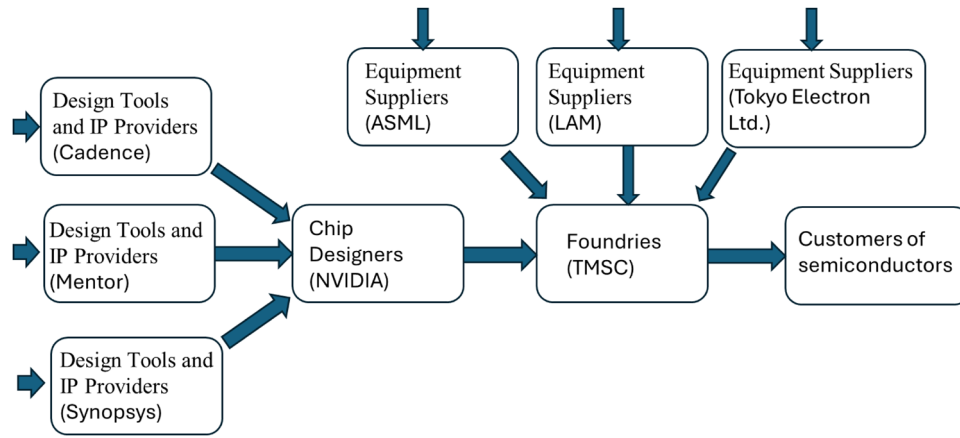


Figure 4. Critical supply chain roles of the bottleneck firms.

Geopolitics also shapes NVIDIA's strategy. U.S. export controls aimed at restricting advanced AI hardware sales affect where and how NVIDIA can sell its products. The company responds by adjusting product lines and regional variants to comply with these rules while protecting market share. At the same time, antitrust scrutiny and competition from AMD and Intel create additional strategic pressures.

5.4. LAM research

LAM Research is one of the world's leading suppliers of etch and deposition equipment – the tools that shape and build the layers of a chip after lithography. These steps are essential for forming transistors, keeping patterns accurate, and ensuring high yields in advanced semiconductor factories. Over decades, LAM has built up specialised tools and deep process know-how that are now embedded across cutting-edge manufacturing lines.

Its network position reflects this importance. LAM connects to 22 different firms, and its ego network is extremely sparse (density 0.008), meaning these firms are not well connected to each other. Its large Effect size (22.8) shows that almost all its ties are non-redundant, and its low constraint (0.052) indicates a strong brokerage role. In simple terms, LAM sits at the centre of a hub-and-spoke structure, linking subsystem suppliers, materials firms, and chipmakers that would otherwise be disconnected (Online Appendix OA 3.2).

LAM's supplier power comes from three reinforcing mechanisms:

- Process specificity and IP – its proprietary process recipes, chamber designs, and tool capabilities are tightly linked to customer yield performance and are difficult for rivals to copy.

- Qualification and installed-base lock-in – its tools require long qualification cycles and rely on proven process recipes and co-optimised tool-process integration, which raises switching costs and keeps customers tied to LAM.
- Global service and scale – its broad customer reach, extensive service networks, and uptime-critical field engineering support make customers highly dependent on LAM's ability to keep fabs running smoothly.

Together, these mechanisms create high switching costs and make customers heavily reliant on LAM's equipment. Geopolitics also shapes LAM's business. Export controls have restricted access to key markets, reducing short-term sales and shifting regional demand. LAM has responded by adjusting its product mix, expanding regional capacity and training partnerships, and continuing to invest in R&D to protect long-term competitiveness. These policy interventions have both constrained near-term revenue and pushed the company to diversify away from China while supporting more localised capability development elsewhere.

5.5. Synopsys Inc

Synopsys, founded in 1986, is one of the world's leading providers of electronic design automation (EDA) tools and licensable IP. Its platforms – such as the Fusion Design Platform and Synopsys.ai – are central to how modern chips are designed, verified, and reused across the semiconductor, computing, and communications industries.

Its network position reflects this wide reach. Synopsys connects to 24 firms, and almost all of these ties are non-overlapping (effective size 24.0). Its very low constraint score (0.042) shows that it acts as a broker, linking many different design and platform partners who are not

strongly connected to each other (Online Appendix OA 3.3). In simple terms, Synopsys sits at the centre of a broad design ecosystem.

Synopsys's supplier power comes from three reinforcing mechanisms:

- Toolchain embeddedness – its EDA tools and IP libraries are deeply woven into customer design workflows, making it costly and time-consuming for firms to requalify or switch to alternatives.
- Cumulative tacit knowledge and standards influence – decades of product development, design libraries, and involvement in industry standards make competing tools harder to adopt.
- AI and platform extension – Synopsys.ai builds directly on customers' existing toolchains, increasing lock-in and raising barriers for rivals trying to compete.

Regulation and governance also shape Synopsys's position. IP disputes, antitrust reviews of large acquisitions, and export controls on software influence where and how it can operate. These interventions can slow growth in the short term, but they also raise entry barriers for potential competitors, reinforcing Synopsys's long-term strategic position.

5.6. Cadence

Cadence is a leading EDA provider that has expanded beyond traditional chip-design tools into system-level design – covering packaging, printed circuit boards, radio-frequency systems, and thermal/physics simulation. Under its '*Intelligent System Design*' strategy, it has also added AI-enabled design tools that support automation and optimisation across the full design workflow.

Its network position reflects this broad reach. Cadence connects to 25 firms, and almost all of these ties are non-redundant (Effect size 25.0). Its very low constraint score (0.041) and low hierarchy (0.026) indicate a hub-and-spoke structure in which Cadence acts as a broker linking otherwise disconnected partners (Online Appendix OA 3.4). In simple terms, Cadence sits at the centre of a wide design ecosystem.

Cadence's supplier power rests on three reinforcing mechanisms:

- Integrated toolchain and standards influence – its broad suite of EDA and system-design tools embeds Cadence deeply across customer design and verification workflows.
- Expansion into adjacent domains and AI features – new system-analysis and AI-driven products (such

as Clarity, Celsius, Cerebrus, and Verisium) increase switching costs and deepen customer dependence.

- Acquisitions and ecosystem ties – targeted acquisitions and minority investments strengthen customer relationships and extend Cadence's reach into new markets.

Cadence also faces regulatory and governance pressures. IP disputes, cybersecurity risks, and antitrust scrutiny around large software consolidations shape its operating environment. In addition, export controls and customer concentration create further strategic considerations for how and where Cadence can grow.

5.7. TEL

TEL supplies a wide range of semiconductor production equipment and flat-panel display (FPD) systems, along with computer-network and storage solutions. Under its 'Vision 2030' strategy, the company aims to expand its service and solutions businesses, develop more digital and AI-enabled offerings, and improve margins and return on equity by moving into adjacent product-service areas.

Its network position highlights this broad role. TEL connects to 26 firms, and its ego network has very low density (0.012), meaning these firms are not well connected to each other. Its large Effect size (25.692) and low constraint (0.053) show that most of its ties are non-redundant, while its hierarchy score (0.090) reflects a hub-and-spoke structure (Online Appendix OA 3.5). In simple terms, TEL acts as a broker, linking materials suppliers, equipment makers, and chip manufacturers that would otherwise be disconnected.

TEL's structural power rests on three reinforcing mechanisms:

- Product breadth and clock speed – it rapidly converts R&D into a wide range of equipment lines that support multiple stages of chip production.
- Service and installed-base scale – its extensive maintenance, software, and service contracts raise switching costs and keep customers dependent on TEL's tools.
- Market positioning and solution adjacencies – expansion into networking, measurement, robotics, and data/service businesses deepens customer relationships and creates cross-selling opportunities.

Geopolitics also shapes TEL's business environment. U.S. export controls and the Foreign Direct Product Rule have reduced its exposure to China and shifted global sales patterns. TEL has responded by diversifying into other regions (such as North America and Japan), opening

new facilities, and expanding service operations. These policy constraints limit short-term revenue in restricted markets but also increase the strategic value of TEL's non-China business lines.

5.8. Mentor graphics (Siemens EDA)

Mentor, acquired by Siemens in 2017, is a long-established EDA provider offering verification, PCB (the physical board that holds and connects electronic components), FPGA (a type of semiconductor device that can be reconfigured after manufacturing to perform different logic functions), and system-level design tools – such as ModelSim, QuestaSim, Calibre, and Xpedition – used across the semiconductor, aerospace, automotive, and industrial sectors. Its tools support everything from chip verification to embedded systems and complex board design, giving Mentor a broad cross-industry footprint.

Its network position reflects this integrative role. Mentor connects to 24 firms, and its ego network shows zero density and zero hierarchy, meaning none of these firms are connected to each other. Its large Effect size (24.0) and very low constraint (0.042) indicate a star-shaped, low-redundancy network in which Mentor acts as a broker linking otherwise disconnected partners (Online Appendix OA 3.6). In simple terms, Mentor sits at the centre of a wide, diverse ecosystem.

Mentor's supplier power rests on three reinforcing mechanisms:

- A comprehensive verification and design toolset – its specialised simulation and verification tools are difficult to replace and deeply embedded in customer workflows.
- Interoperability and cross-industry reach – Mentor's tools are used across multiple sectors (semiconductors, automotive, aerospace), embedding the company in a wide range of development processes.
- M&A and platform integration – historical acquisitions and integration into Siemens strengthen customer relationships, enable cross-licensing, and raise switching costs.

Regulatory and governance issues also shape Mentor's position. IP litigation and antitrust scrutiny around large EDA consolidations influence how Mentor can expand. Recent acquisitions – such as Downstream Technologies (PCB manufacturing, 2025) and Canopus AI (AI-driven semiconductor metrology, 2026) – as well as export and IP controls affect market access and M&A outcomes. At the same time, cross-licensing agreements and industry

collaborations (including with Synopsys) reinforce Mentor's bottleneck role in verification and system design.

6. Cross-case bottleneck analysis

The eight case companies in this paper although part of a wider semiconductor supply network work closely with each other. The entities are engaged in supply as shown in Figure 3. The cross-case synopsis for the eight companies is shown in Appendix F. This is based on how the companies interact with each other and their competitive advantages. The movement between leverage and strategic positions is driven by changes in customer dependency rather than profit impact.

The main threats to the bottlenecks of Cadence, Mentor (Siemens EDA) and Synopsys who dominate the EDA tools market and design phase of the supply chain come from intellectual property and cybersecurity risks, legal risks over patents U.S, anti-trust practices. To enhance their corporate value these firms are focusing on improving their ESG and sustainability. NVIDIA, one of the dominant bottleneck firms has also faced anti-trust practices and state sponsored competition from key rivals. TSMC a state-sponsored 'champion' firm has confronted export controls and market access restrictions from both the U.S. and China. Likewise, LAM has encountered quite stringent export controls, while ASML has been at the forefront of the tariff and trade war battles between the U.S. and China.

Whilst TSMC, is the world's largest independent semiconductor foundry, it relies on advanced fabrication processes and strong collaborations with EDA tool providers to produce complex chips on the manufacturing side, TSMC, ASML, LAM Research, and TEL clearly play pivotal roles. Whilst TSMC, is the world's largest independent semiconductor foundry, it relies on advanced fabrication processes and strong collaborations with EDA tool providers to produce complex chips. ASML with its monopoly position in EUV lithography technology is vital for TSMC and its production capabilities.

However, they are both confronting growing geopolitical tensions and export controls, so they are looking to diversify their product portfolios and invest in new regions. For LAM and TEL their competitive advantage comes from their advanced technology and IP they have for the development of essential machinery in semiconductor manufacturing. They likewise are following the lead of TSMC and ASML in searching for lower risk markets.

7. Discussion and concept development: a Kraljic supplier perspective

We propose an additional Kraljic perspective that shifts analytical focus from buyer dependency on suppliers to supplier leverage over buyers, particularly in technologically complex and capacity-constrained industries such as semiconductors. Rather than treating bottlenecks as exogenous conditions, the analysis demonstrates how suppliers can strategically create, reinforce, or relax bottlenecks by controlling critical materials, components, or equipment. Figure 5 illustrates the Kraljic supplier portfolio perspective, positioning customers according to their dependency on the supplier and the profit impact for the supplier. This reframing highlights that supplier power does not arise solely from scarcity, but from the intentional structuring of dependency across different customer profiles.

Leverage customers is a supplier perspective that exhibits low dependency of the customer but high purchase volumes, creating substantial revenue impact without exclusive reliance on a single buyer. In this quadrant, suppliers can exert power by selectively controlling critical inputs, thereby constraining competitors' access and gradually increasing customer dependency. As the revenue from the customer increases (increasing the profit potential) the relationship may move to a strategic customer relationship for the supplier as dependency on the customer with due to high revenue growth may increase. The strategic positioning may lead to lower supplier power.

NVIDIA will provide significant revenue contribution to upstream suppliers, while its diversified sourcing base limits unilateral dependency. Similarly, Tokyo Electron (TEL) purchases high-value equipment that generates strong profit impact, yet suppliers retain alternative customer options. In these cases, suppliers can exercise pricing and allocation leverage while maintaining transactional flexibility rather than deep relational commitment.

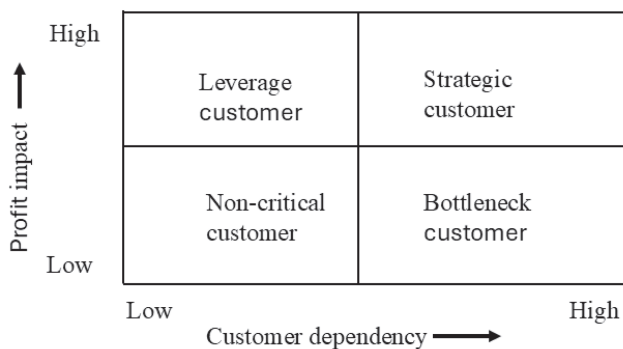


Figure 5. Kraljic supplier perspective.

Bottleneck customers is a supplier perspective where the supplier has high dependency on the customer, but revenue and profits may be low. It is a situation where the customer requires specific supply items, although they may retain limited dual-sourcing or substitution options. Supplier power in this quadrant is exercised through lock-in mechanisms, such as proprietary technologies, switching costs, or ecosystem integration, which progressively reduce customer alternatives and can elevate the relationship towards leverage customer status and eventually strategic customer status.

LAM Research has highly specialised deposition tools, which induce strong technical dependency, despite relatively lower margins per customer transaction. Mentor (Siemens) similarly has mission-critical design software that creates deep lock-in, yet individual customer revenue impact remains modest compared to capital equipment suppliers. In these relationships, risk arises primarily from dependency rather than revenue exposure, suggesting the need for mitigation strategies rather than immediate partnership escalation.

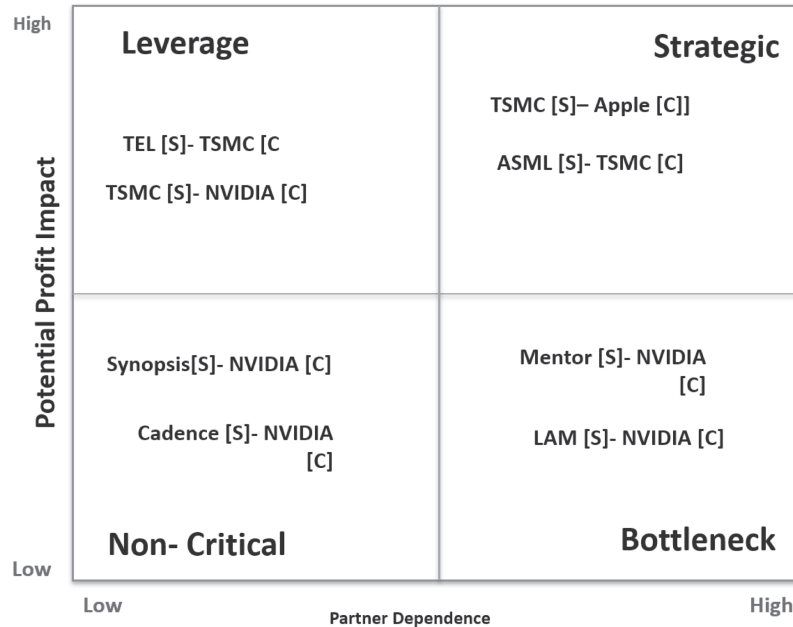
Strategic customers is a supplier perspective that combines high dependency with high profit impact, necessitating long-term relational governance. This has a positive revenue impact on both the customer and supplier. In this quadrant, suppliers actively maintain and strengthen dominance by controlling critical inputs, coordinating capacity, and engaging in joint planning. Geopolitical considerations play a particularly salient role in sustaining criticality and shaping access. The customer also has equal power and may try to dominate the relationship due to volumes and closeness to market. Sharing of IP will be an important aspect in this relationship although the supplier may want to dominate through operational capability.

TSMC through its unique advanced-node foundry capacity creates extreme customer dependency alongside substantial revenue exposure for upstream suppliers. ASML is similarly the sole provider of EUV lithography systems, where customers face near-total dependency and purchases represent exceptionally high profit impact. These relationships warrant deep collaboration, long-term contracts, and coordinated investment strategies.

By contrast, the *non-critical quadrant* (low dependency, low profit impact) is a supplier perspective which includes firms such as Cadence and Synopsys. While both are important EDA providers, substitutable alternatives, modular licensing, and broad customer bases reduce dependency and concentration of supplier profit. These relationships are efficiently managed through standardised contracts and routine service provision rather than strategic partnership.

Table 2. The revenue and relationship perspective of companies (Source: Bloomberg (SPC estimates), company reports).

	Total revenue (Potential profit impact)	Key relationships market value (\$)	Matrix position of the relationship	% Partner revenue
TSMC	\$453.424 bn	TSMC - > Apple 765.66495 bn	Strategic	8.97%
		LAM - > TSMC 5.312 bn		9.38%
ASML	\$37bn	ASML - > TSMC 192.759 bn	Strategic	16.68%
TEL	\$15.7bn	TEL - > TSMC 5.982 bn	Leverage	11.54%
NVIDIA	\$130.5bn	TSMC - > NVIDIA 453.479 bn	Leverage	32.8%
LAM	\$18.44bn	LAM - > TSMC 5.312 bn	Bottleneck	9.38%
MENTOR???	\$1.54bn	MENTOR - > NVIDIA \$50m	Bottleneck	0.3%
SYNOPSIS	\$7.054bn	SYNOPSIS - > NVIDIA \$335m	Non-Critical	5.3%
CADENCE	\$5.297bn	CADENCE - > NVIDIA £350m	Non-Critical	6.6%

**Figure 6.** Matrix Position of firms.

If we look at Figure 4 (Section 4.3), this shows the network of semi structured companies based on the analysis earlier in the paper. The figure displays how the companies are related in terms of the flow of materials and operational capabilities to manufacture semiconductors. The figure depicts the role that different companies play within the networks.

The Table 2 shows the revenue and relationship perspective of the companies.

Figure 6 shows where these relationships are represented on the supplier perspective matrix using the previous Figure 4 (Section 4.3). The relationships are taken from the table. These relationships are based on the revenue figures as shown in Table 2. As discussed earlier, movement from strategic positioning to other quadrants for a relationship is less likely as both partners will be locked in. But there will be movement based on the supplier power dynamics as discussed in the paper from bottleneck to leverage, leverage to strategic, bottleneck to

strategic, and leverage to bottleneck. Where a relationship is non-critical for the supplier, there is a movement possible to bottleneck, if the customer creates a dependency through market structures, or the movement to leverage if the supplier uses the lower dependency and position in the network to setup larger contracts with the customer. Sometimes a buyer may also be a supplier to its supplier as part of the operational value chain.

7.1. From dyadic power to network bottlenecks

Figure 7 presents our conceptual model derived from our synthesis of the literature, network analysis, and case evidence, showing the factors that influence buyer-supplier dynamics and power asymmetry in the semiconductor supply chain. There are several aspects of the semiconductor industry that could pose as a bottleneck for the supply chain. It is thus useful to not only think about

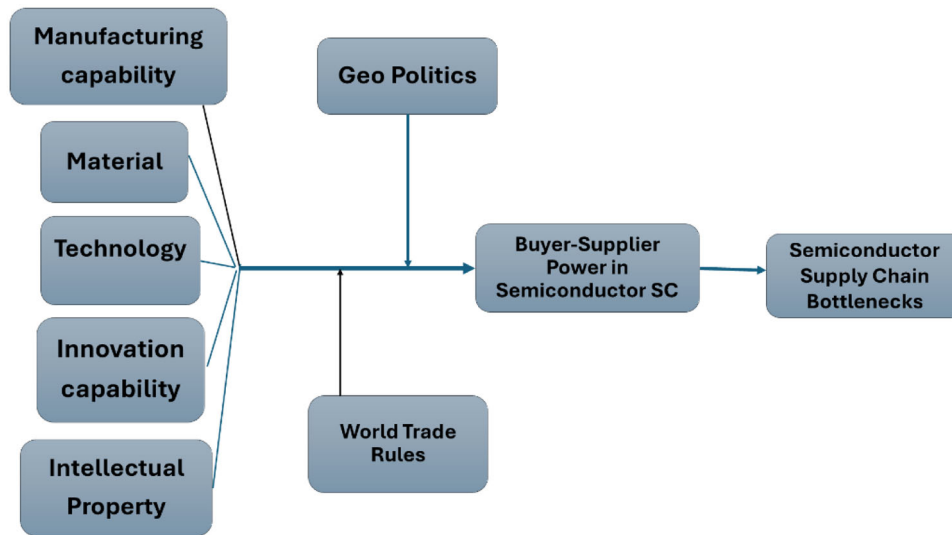


Figure 7. Strategic Bottleneck Model for Semiconductors.

this not only as an upstream problem related to procurement, but also as a downstream problem related to distribution and sales. The five supply bottlenecks relate to material, technology and equipment, foundries and manufacturing capacity, intellectual property, and innovation. These can be controlled by individual firms but may have greater influence through geopolitics. There is also further complexity, where a firm may be a supplier upstream but also a downstream customer as a distribution/packaging specialist.

The strategic bottleneck model identifies five core factors shaping supplier power and bottleneck formation, including technological specificity, capacity control, switching costs, ecosystem embeddedness, and demand concentration.

While these dynamics originate at the dyadic level, the semiconductor context amplifies their effects across interconnected supply networks. Two additional moderating forces – geopolitics and world trade rules – further condition the relationship between these factors and supplier power. Current US–China trade interventions exemplify how political and regulatory actions can reinforce or disrupt strategically constructed bottlenecks, reshaping industry structure and dependency patterns.

8. Conclusion and future research agenda

Our research has focused on examining how firms in the advanced semiconductor supply chain create and sustain their ‘bottleneck’ positioning. They exert influence by controlling the production and supply of essential technologies and equipment; they often dominate specific segments of the supply chain (e.g. fabrication or the manufacturing of photolithography equipment making

them critical to production of advanced semiconductors). Additionally, some bottleneck firms, such as TSMC collaborate with governments to gain a competitive edge over their rivals. Through supply chain network analysis, we identify that there are eight bottleneck firms of high nodal centrality.

Furthermore, we set out to make a theoretical contribution to the bodies of knowledge on supply-chain bottlenecks and structural power (Chen and Evers 2023; Kim, Chen, and Linderman 2015; Nguyen et al. 2025). We conceptualise bottlenecks as a network-structural phenomenon and show how supplier power emerges from firms’ positions within multi-tier supply networks. By applying a Kraljic perspective focused on supplier power (Kraljic 1983) and analysing structural intermediation, we identify TSMC and ASML as the most critical strategic bottlenecks in the semiconductor ecosystem.

Our analysis offers two clear audiences and sets of implications. For governments, it pinpoints critical nodes where strategic intervention can most effectively shore up national resilience. By identifying which suppliers or regions represent true bottlenecks, policymakers can tailor measures – such as targeted subsidies, infrastructure investments, export - control adjustments, and stock-piling mandates – to reduce single-point failures in the semiconductor ecosystem. The findings also inform multilateral coordination and risk-monitoring frameworks, helping regulators anticipate disruptions and craft more precise industrial policies.

For companies operating within the supply chain, the network map reveals which partners hold disproportionate leverage over material and component flows. Businesses can leverage these insights to diversify sourcing,

forge long-term contracts or joint ventures with key suppliers, and prioritise investment or M&A in areas that mitigate exposure to critical bottlenecks. Moreover, the results support more robust contingency planning and alliance building strategies, enabling firms to balance cost efficiency with supply chain continuity and responsiveness in an environment of long lead times and rapid technological shifts.

We encourage future research to explore the dynamic nature of these bottlenecks over time; particularly how geopolitical shifts and technological advancements impact the stability and influence of these firms. Longitudinal studies could provide deeper insights into the cyclical nature of supply chain dependencies and the long-term effectiveness of bottleneck strategies. Additionally, expanding the scope to include smaller or emerging firms could offer a more holistic view of the semiconductor supply chain. Organisational resilience in disruption (Koh et al. 2023) and the impact of supply chain position on sustainable practices (Sun, Bai, and Sarkis 2024) within the semiconductor industry through a bottleneck lens are some other areas to focus for future research.

For managers, understanding the strategic importance of bottlenecks is crucial for navigating the semiconductor supply chain. The industry panel (the findings are presented in Appendix B) we consulted with provided some valuable practitioner insights into the development of our bottleneck analysis. They recommended that firms should invest in innovation and develop strong relationships with key suppliers and customers to mitigate risks associated with bottlenecks. Managers must also be aware of the geopolitical landscape and its potential impact on supply chain stability.

By leveraging the Kraljic framework, firms can better classify their buyers and create robust buyer-supplier relationships to develop tailored strategies to ensure a resilient and competitive semiconductor supply chain. This involves not only securing critical resources but also diversifying supply sources and investing in alternative technologies to reduce dependency on any single bottleneck.

In conclusion, the management of bottlenecks by firms and increasingly nations through their ‘governance’ are essential for maintaining competitive advantage in the semiconductor industry. By addressing the identified research questions and applying the Kraljic framework, this paper provides valuable insights for both academia and industry practitioners on how to navigate and leverage the complexities of the semiconductor supply chain. This study has several limitations. First, the analysis is constrained by the Bloomberg SPLC dataset, which provides supplier–customer relationships only for major

publicly listed semiconductor firms. As a result, the network reflects a focused sample of 122 firms and 140 directed supply links, rather than the full multi-tier structure of the industry. While Section 3 has been revised to clarify how the analytical network was constructed and to report key characteristics – including its sparse, highly centralised topology and the presence of functionally identifiable but tightly interconnected groups – the boundary of the network remains centred on the most structurally significant firms. This approach allows us to capture the core dependencies that generate bottlenecks, but it does not explicitly include second-tier or deeper-tier suppliers, which the multi-tier supply chain literature highlights as important sources of vulnerability. Consequently, although the network is appropriate for identifying dominant upstream bottlenecks, the absence of deeper-tier representation may limit the completeness of the bottleneck picture and raises reasonable concerns about the scope of centrality-based analysis. Future work would benefit from extending the network boundary to incorporate additional tiers and to test the robustness of bottleneck identification across broader supply chain layers.

8.1. The implications of transitioning from 7 nm/10 nm to 5 nm and 3 nm

Smaller nodes can potentially allow for higher transistor density, which can in turn lead to faster and more energy-efficient chips (Zhang 2002). This is critical for applications like AI, machine learning, and high-performance computing. However, the transition to 5 nm and 3 nm nodes relies heavily on advanced lithography techniques, such as Extreme Ultraviolet (EUV) lithography (Wu and Kumar 2007) requiring significant investment and expertise. This can have the undesired effect of making the technology accessible only to a few leading companies such as Samsung and Intel. The dominance of a few players can therefore lead to the supply chain being concentrated making it more vulnerable to disruptions and thus raising concerns about supply chain resilience.

Smaller nodes can enable more powerful and energy-efficient devices (Singh, Kalra, and Mahur 2024), driving demand in smartphones, laptops, and IoT devices. Yet, their manufacturing requires more energy-intensive processes, raising concerns about sustainability (Sastri et al. 2024). Indeed, according to Bouhidel and Lakehal (2006) the production of advanced nodes demands significant amounts of ultrapure water and rare materials, which could strain resources.

Smaller nodes also mean innovative design approaches, such as 3D stacking and chiplet architectures (Shan et al. 2022), to optimise performance. As nodes shrink,

traditional silicon-based technologies face physical limitations, this can initiate research into new materials such as graphene and carbon nanotubes (Liu et al. 2014).

Ultimately, the high cost and complexity of transitioning to 5 nm and 3 nm nodes create significant barriers for smaller companies, consolidating the market among a few major players. Furthermore, the race to develop and produce advanced nodes means intensified competition among countries and companies potentially changing the landscape of global semiconductor strategies (Takeuchi 1993). The transition from 7 nm/10 nm to advanced 5 nm and 3 nm process nodes, alongside a geographic shift in semiconductor manufacturing from China to emerging hubs such as Vietnam, Malaysia, Singapore, and the United States, marks a significant reconfiguration of the global supply chain; this evolution invites future research.

Notes

1. For a more political economy-based analysis of the role of government intervention in the semiconductor supply chain the interested reader is directed to the book of Fishman (2025). *Bottlenecks: How the Global Economy Became a Weapon of War*. Elliot E Thompson, London.
2. Cited by Caniels and Gelderman (2005).
3. Ibid.
4. Ibid.
5. The SPLC function aims to provide a 'comprehensive supply chain breakdown for a selected company'. Users can analyse revenue exposure for the central company, its suppliers, and its customers, as well as track the company's geographic, commodity, sustainability, and risk exposures. Further information is available here: <https://blogs.cranfield.ac.uk/library/supply-chain-bloomberg-workspace/>.
6. For instance, the Semiconductor Industry Association. <https://www.semiconductors.org/>.
7. The R script used for the elbow method is presented in online appendix OA4.
8. This online appendix contains extended case narratives, ego – network tables (OA 3.1–OA 3.6), and the source list of the semiconductor firms used in the network analysis. These files are provided for research and teaching use.
9. <https://www.techuk.org/resource/event-round-up-how-can-a-uk-semiconductor-centre-support-the-development-of-a-thriving-semiconductor-sector.html>.
10. The R script used can be provided by the authors upon request.
11. The R package used can be found at. <https://cran.r-project.org/web/packages/changepoint/index.html>.

Author contributions

CRedit: **Gary Graham**: Formal analysis, Methodology; **Samir Dani**: Conceptualization; **Andros Gregoriou**: Writing – review & editing

Disclosure statement

No potential conflict of interest was reported by the author(s).

Data availability statement

The data that supports the findings of this study are available from the corresponding author, [GG], upon reasonable request.

Notes on contributors



Gary Graham is Professor of Operations and Supply Chain Management at Liverpool John Moores University. He brings a strategic operations management perspective to the design, analysis, and operation of international supply chains, with a particular focus on the impact of advanced production and digital technologies. Through major collaborations with industry, both individual firms and multi-organisation consortia, primarily in the automotive and semiconductor sectors, his research has directly underpinned significant organisational change. He is a long-standing reviewer for the *International Journal of Production Research (IJPR)* and contributed, through reviewing and submitting a co-authored article (voted Outstanding Article for 2016), to the highly successful IJPR special issue *Distributed Manufacturing to Enhance Productivity*.



Samir Dani is Professor of Operations and Supply Chain Management in Keele Business School at Keele University. Samir Dani is Professor of Operations and Supply Chain Management in Keele Business School at Keele University. Professor Dani engages widely with industry and has research interests in supply chain risks, resilience, and sustainability in supply chains. He considers the use of technology and business models for impactful solutions. He is currently conducting research on the use of AI techniques within supply chain decision-making. He has published widely and has presented his research to both academic and practitioner audiences.



Andros Gregoriou is a Professor of Finance at Liverpool Business School, Liverpool John Moores University. He has published extensively in leading finance journals, has generated a vast amount of research income and supervised numerous Ph.D. students to completion. He is an expert on Cryptocurrencies, Market Microstructure and Financial Econometrics from both a theoretical and empirical perspective. He is a regular consultant for financial regulators, central banks, stock exchanges and hedge funds.

ORCID

Gary Graham  <http://orcid.org/0009-0009-1783-2827>

Samir Dani  <http://orcid.org/0000-0001-8547-0762>

Andros Gregoriou  <http://orcid.org/0000-0002-7221-0598>

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Appendices

Appendix A. Bloomberg intelligence market reports, websites, and online news sources

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Appendix B. UK semiconductor panel participants

At a specialist panel to discuss the development of a UK semiconductor centre⁹ we were able to get answers to our two research questions.

ID	Organisation	Role
P1	Government department	Deputy Director, Semiconductors
P2	Semiconductor Catapult	Non-Exec Director
P3	Semiconductor X	General Manager
P4	X Technology	Senior Policy Manager
P5	Semiconductor Catapult	CTO
P6	ChipX Global	Co-founder & COO
P7	Silicon	Director of Strategy, Silicon Photonics
P8	Semiconductor Y	Co-founder & CTO
P9	X Computing	Co-founder & CEO
P10	Semiconductor Z	Director of IP Strategy
P11	Government department	Lead, Quantum Technologies
P12	MNC	Director of Government Partnerships

Note: We have used pseudonyms for all participating organisations.

With respect to our RQs they added the following perspectives:

Bottleneck identification (RQ1)

- 'It's hard for an SME to find the right fab or test lab – this Centre must map assets end-to-end' (P3).
- 'Below 7 nm, only three foundries exist; EUV tool shortages become the single biggest chokepoint' (P1).

Strategic leverage & Kraljic portfolio (RQ2)

- 'Dominant firms capture pricing power during the 6–12-month yield-ramp – OEMs are forced to commit early' (P1).
- 'We need to swap 'supplier dependency' for 'customer dependency' on our portfolio axes – customers drive design cycles now' (P2).

In addition, they pointed additional policy and infrastructural bottlenecks confronting the semiconductor supply chain:

Infrastructure & bottlenecks

- 'A domestic multi-project wafer service would break the prototyping bottleneck for startups' (P6).
- 'Material flows jam at advanced resist suppliers – those node transitions are strategic bottlenecks' (P7).

Policy & governance levers

- '£19 M isn't enough – consider a £150 M strategic fund to smooth long lead times' (P4).
- 'This Centre must be the single front door for international partners – clarity reduces transactional friction' (P12).

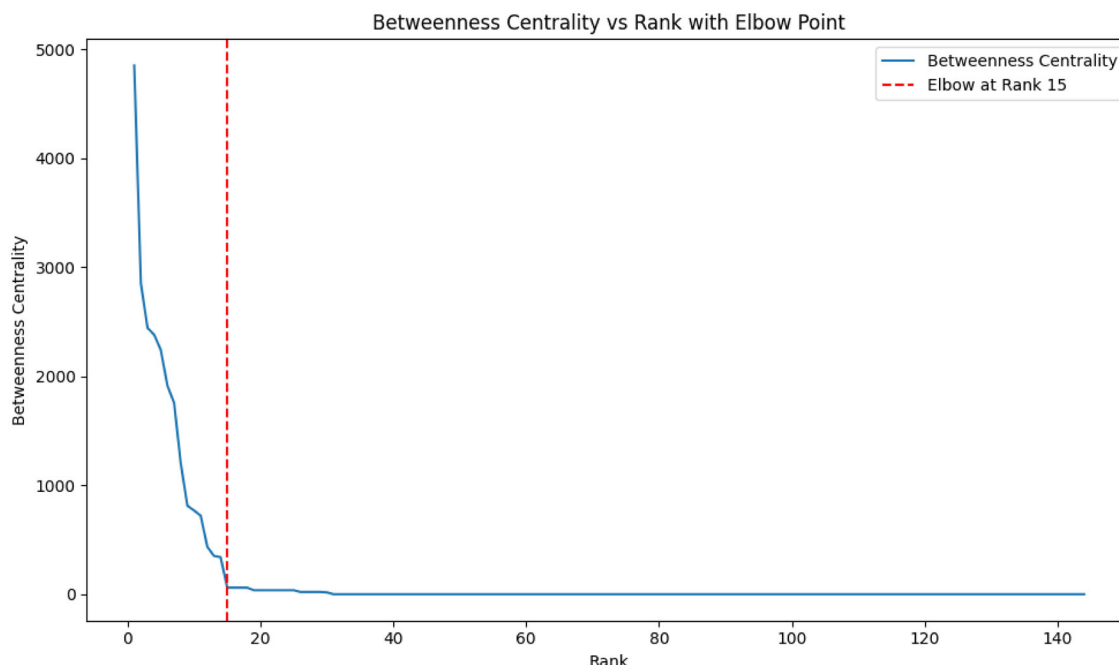


Figure A1. Elbow analysis of centrality scores.

Appendix C

Elbow method explanation

Statistical analyses for firm identification were conducted using R version 4.5.0 (R Core Team 2025), an open-source programming environment for statistical computing and graphics.¹⁰ The elbow method identifies the point in a ranked distribution where the rate of decline in Betweenness Centrality slows significantly. This is done by calculating the perpendicular distance of each point from the line connecting the first and last points in the distribution. The point with the maximum distance is considered the elbow. The plot and centrality change point detection are presented in Figure B1 (Appendix B). That plot shows the Betweenness Centrality values ranked in descending order, with the elbow point marked in red on Figure C1.

While the elbow analysis identified 15 structurally significant firms, visual inspection of the centrality curve reveals a sharper elbow around the top 8 firms. We present the 15 firms and their centrality scores in Appendix D.

Centrality change-point detection with PELT¹¹

To identify a clear break between the most central ‘core’ firms and the rest, we applied a change-point method called PELT (Pruned Exact Linear Time) to our list of betweenness centralities (Killick and Eckley 2014; Killick, Fearnhead, and Eckley 2012). In plain terms, PELT scans the sorted betweenness values and finds the exact point where the average score steps down most sharply. This gives us a data-driven way to decide how many firms truly stand out as bottlenecks.

We ran PELT on the full sequence of betweenness scores (ranked from highest to lowest) using the R package

‘change-point’. Rather than eyeballing the curve or picking an arbitrary cutoff, as mentioned PELT detects where the ‘level’ of centrality significantly shifts. It looks for the single spot in that ordered list where splitting the data into two groups makes the most sense – in our case, dividing the top elite actors from the rest.

The first change-point that PELT found fell at rank 8. In other words, firms 1–8 share one consistently higher average in their betweenness and starting at firm 9 the average drops to a noticeably lower level (marked by the red grid line in Figure C2). As this break is both sharp and supported by our PELT analysis, we use it to justify focusing on those eight elite firms as the principal bottlenecks in the semiconductor supply chain.

Table A1. Robustness check – correlations with betweenness centrality (Spearman correlations).

Centrality measure	Correlation with betweenness
In-degree	0.6040
Out-degree	0.8616
In-strength (weighted)	0.6040
Out-strength (weighted)	0.2874
PageRank	0.8368
Eigenvector centrality	0.0000
Authority (HITS)	0.6040
Hub (HITS)	0.8616
Bridging centrality	0.9184

All correlations above ~ 0.25 are statistically significant at $p < 0.01$ for Spearman's rho with $n \approx 120$.

As a robustness check, we computed a range of alternative centrality measures on the directed supply network, including degree-based measures, PageRank, eigenvector centrality, HITS hubs and authorities, and bridging centrality. Betweenness centrality is strongly correlated with other global measures that capture systemic positioning, particularly PageRank and bridging centrality, and with outbound connectivity.

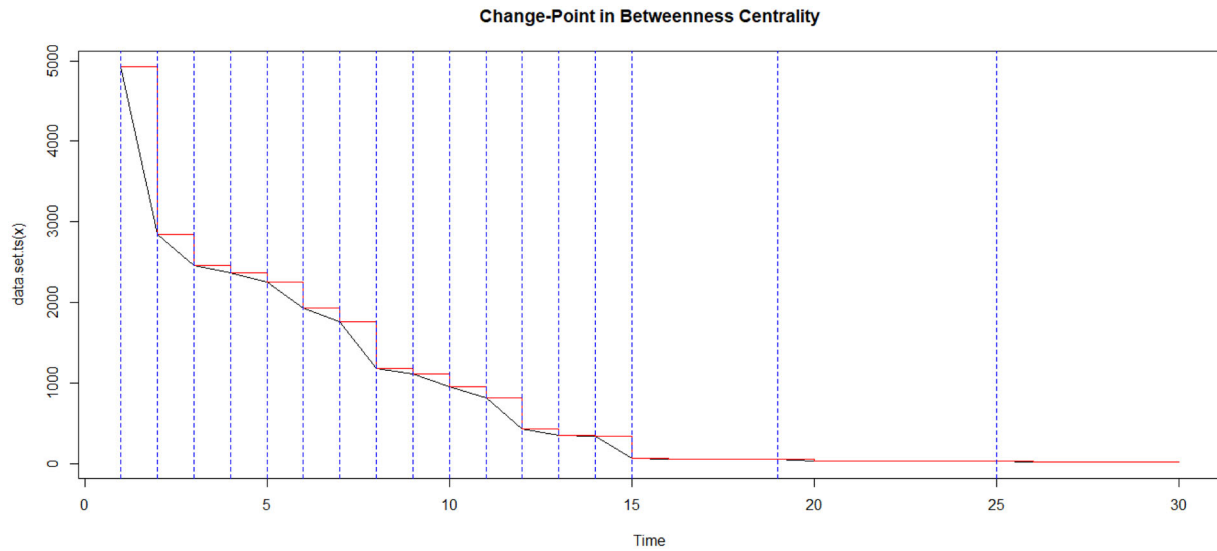


Figure A2. Change-point detection in betweenness centrality (PELT method).

Appendix D. Firms up to the elbow point (rank 15)

Rank	Firm	Betweenness centrality
1	TSMC	4850.39
2	Mentor Graphics	2847.87
3	Cadence	2441.48
4	Synopsys	2378.40
5	TEL	2238.93
6	LAM Research Corp	1913.08
7	NVIDIA	1755.63
8	ASML	1200.64
9	Analog Devices Inc	812.14
10	SK Hynix Inc	768.39
11	MediaTek Inc	721.09
12	Chips and Media Inc	435.16
13	Infineon Technologies AG	350.89
14	Jabil Inc	339.92
15	MKS Instruments Inc	59.78

Table A2. Ego network metrics for TSMC and its leading direct partners.

Partner firm	Degree	Density	Eff. size	Constraint	Hierarchy	Annual trade value (US\$m)
TSMC	39	0.01	40.6	0.033	0.047	453,424bn
TEL	5	0.40	3.4	0.590	0.248	5982
Entegris	4	0.50	2.5	0.684	0.168	1664
ASML	3	0.67	1.7	0.840	0.074	192758
Intel Corp	3	0.67	1.7	0.840	0.074	100.93
LAM Research	3	0.67	1.7	0.840	0.074	53122.42
NVIDIA	2	1.00	1.0	1.125	0.000	453424

Appendix E. Ego network analysis

Visual representation of TSMC's direct connections within the semiconductor network

TSMC's ego network reveals a hub-and-spoke topology. Partner firms have minimal interconnection, amplifying TSMC's role as a sole broker. High Effect size and low constraint indicate strategic autonomy and exposure to bottleneck risk.

Visual representation of ASML's direct connections within the semiconductor network

ASML sits at the centre of a high-value, low-redundancy supply network. Each direct tie represents a critical dependency – partners like TSMC, Intel, and SK Hynix do not share alternative suppliers, underscoring ASML's role as a unique technological bottleneck in advanced lithography.

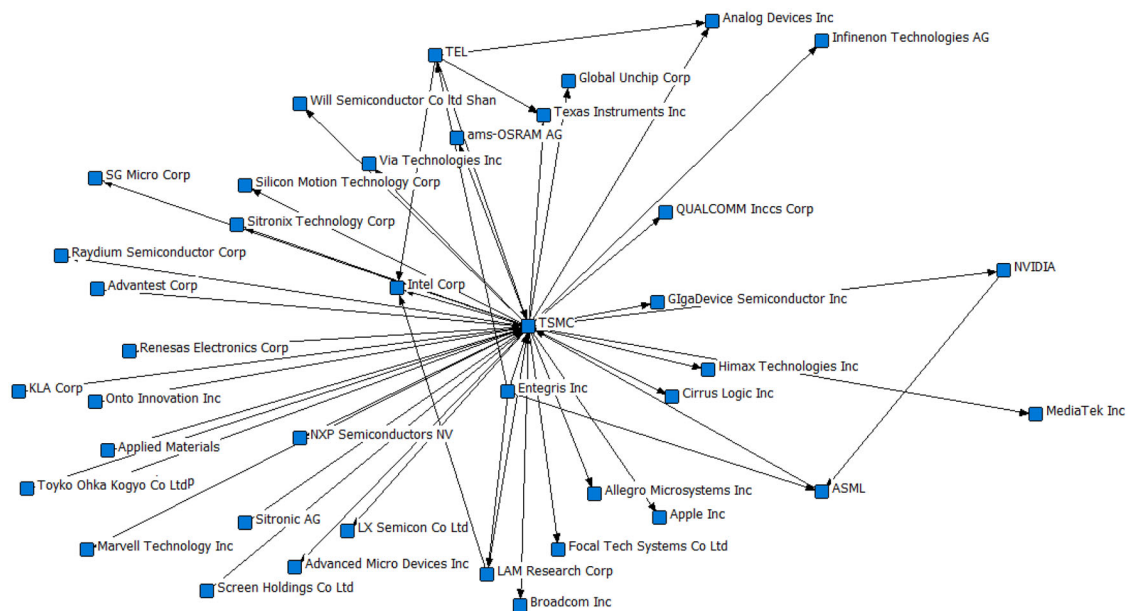


Figure A3. Ego network of TSMC.

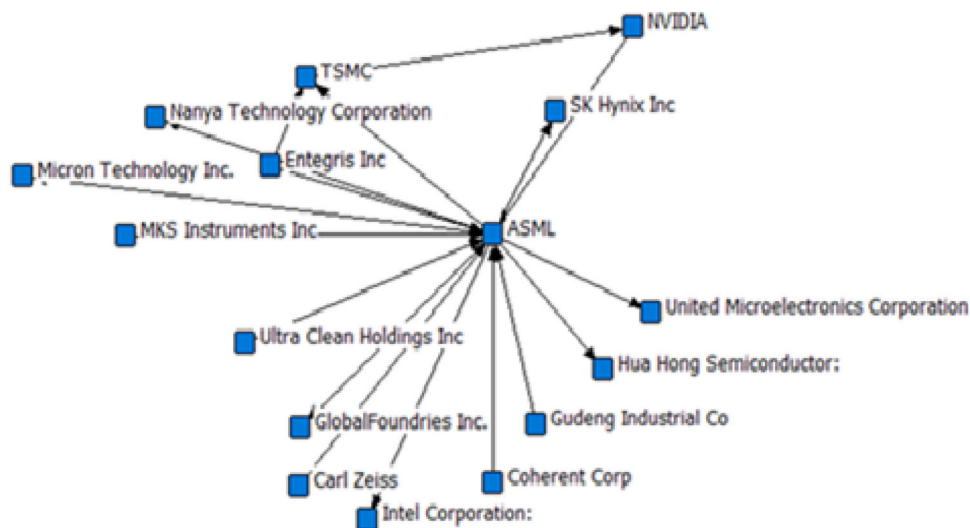


Figure A4. Ego network of ASML.

Table A3. Ego network metrics for ASML and its leading direct partners.

Partner	Degree	Density	Eff. size	Constraint	Hierarchy	Annual trade value (US\$m)
ASML	15	0.019	14.733	0.087	−0.087	36.96 bn
United Micro-electronics Corporation	1	0.00	1.0	1.00	1.00	409.21
Hua Hong Semiconductor	1	0.00	1.0	1.00	1.00	159.62
TSMC	3	0.67	1.67	0.84	0.07	5582
Intel Corporation	1	0.00	1.0	1.00	1.00	3085
Carl Zeiss	1	0.00	1.0	1.00	1.00	3946.5
SK Hynix Inc	1	0.00	1.0	1.00	1.00	2577
Micron Technology Inc.	1	0.00	1.0	1.00	1.00	2371

Appendix F. Table summary of the cross-case analysis

	Background and ego network	Supply chain (SC) roles	Characterisation of bottlenecks and competitive advantages	Governance and regulatory issues
Cadence	Founded in 1988, leading EDA tool developer. Intellectual property and cybersecurity risks. Ego network evidence Degree 25; Effect Size 25.0; Constraint 0.041; Hierarchy 0.026.	Cadence, Mentor (Siemens EDA), Synopsys. These companies provide Electronic Design Automation (EDA) tools that are essential for designing and verifying semiconductor chips. They are at the design phase of the SC. Offers AI-driven optimisation tools and systems analysis products.	TSMC collaborates with EDA tool providers like Cadence, Mentor, and Synopsys to ensure that chip designs can be efficiently manufactured. These tools are essential for designing chips. Comprehensive EDA tool set; strong market position; 30% market share.	Intellectual property theft; cybersecurity risks. Growing focus on sustainability and ESG regulatory considerations, enhancing their corporate value.
Mentor (Siemens)	Founded in 1981; acquired by Siemens AG (EDA) in 2017. Commitment to innovation; maintaining technological edge. Ego network evidence shows Degree 24; Effect Size 24.0; Constraint 0.042; Density 0.00; Hierarchy 0.00. These metrics indicate a star-shaped, low-redundancy ego network in which Mentor brokers otherwise disconnected partners and therefore occupies a high-leverage structural position.	They are at the design phase of the SC. EDA tool provider. Specifically, provides EDA tools for PCB design, semiconductor design, and system-level design.	Comprehensive EDA tool set; significant strategic position in the market	Legal battles over patent infringement; operational disruptions.
Synopsys	Founded in 1986; leading provider of EDA software and semiconductor IP. Ego network evidence. Degree 24; Effect Size 24.0; Constraint 0.042. The ego metrics show many non-redundant ties and very low constraint, indicating strong brokerage power and wide reach across design and platform partners.	They are at the design phase of the SC. EDA tool provider.	Its key design bottleneck position comes from its unique design resources and capabilities. Offers comprehensive suite of EDA tools for chip design and testing Superior tool design; comprehensive suite of EDA solutions; 32% market share.	Intellectual property theft; technological vulnerabilities; antitrust investigations. Regulatory commitment to energy-efficient technologies; improving security and quality of software code. U.S. anti-trust practices
NVIDIA	Founded in 1993; specialises in GPUs and AI computing. NVIDIA's ego metrics show a moderate degree with low density and a high Effect size. These values indicate a small set of non-redundant, strategically important ties – notably TSMC – so NVIDIA is highly dependent on a few advanced-node manufacturers while retaining influence over software and platform standards.	This company designs semiconductor chips, such as GPUs. They use EDA tools for design and verification. NVIDIA is part of the design and development phase. Provides GPUs and AI computing technology	NVIDIA's CuLitho software for computational lithography is integrated by TSMC and Synopsys into their manufacturing processes and systems. ASML works with NVIDIA to integrate GPU support into its computational lithography software. NVIDIA relies on TSMC to manufacture its GPUs and AI accelerators. This relationship is crucial for NVIDIA to produce its advanced semiconductor products. Control over discrete GPU market; CUDA platform locks firms into using Nvidia hardware. Unique AI resources and capabilities together with their critical network centrality to many of their customers give it a dominant bottleneck position.	Anti-trust scrutiny from U.S. Department of Justice; state-sponsored competition from AMD and Intel. Regulatory pressure to improve ESG performance.

(continued).

	Background and ego network	Supply chain (SC) roles	Characterisation of bottlenecks and competitive advantages	Governance and regulatory issues
TSMC	Founded in 1987 by Morris Chang in Taiwan, world's largest independent semiconductor foundry. Its degree (41) and effective size (~ 40.6) show many non-redundant ties; low constraint (0.033) indicates brokerage rather than embeddedness	They take the chip designs created by companies such as NVIDIA and use advanced fabrication processes to produce the physical semiconductor chips. TSMC's state-of-the-art facilities and innovative technology enable the mass production of overly complex and efficient chips, making them a vital link between chip designers and the end products used in various electronic devices. Manufactures semiconductor chips using advanced fabrication processes.	High-performance chip production at scale. Theoretically, firm's key bottleneck drives are its high network centrality, and the high dependence of ASML on it as its main customer (see below) and NVIDIA as its main supplier.	U.S. export controls and market access restrictions; geopolitical tensions. Expanding U.S. operations to enhance supply chain resilience; significant investments in new plants.
ASML	Dutch company specialising in lithography technology; founded in 1984. ASML's ego metrics show a high degree with low density and a large Effect size.	Equipment suppliers like LAM Research, ASML, and TEL provide the necessary machinery and technology for TSMC to manufacture semiconductor chips. This includes photolithography equipment from ASML and wafer fabrication equipment from LAM Research. Produces EUV and DUV lithography machines.	ASML works with NVIDIA to integrate GPU support into its computational lithography software. ASML and TSMC have a mutually dependent relationship in the semiconductor industry. ASML is the world's leading manufacturer of lithography systems, which are essential for producing semiconductor chips. TSMC, as the world's largest and most advanced contract chipmaker, relies heavily on ASML's equipment, particularly their extreme ultraviolet (EUV) lithography systems, to manufacture innovative chips for clients like Apple, NVIDIA, and Qualcomm. Unmatched ability to produce and operate lithography machines at scale; monopolises EUV market.	Geopolitical tensions and export controls; risk of nationalisation. Diversifying operations to reduce geopolitical risks; significant investments in new regions. Regulatory pressure to improve ESG performance.
LAM Research	Founded in 1980; produces machines for semiconductor manufacturing. LAM exhibits high degree with very low density and a large Effect size. Degree 23; Effect Size 22.8; Constraint 0.052.	See ASML above. Produces machines for etching patterns and depositing metals on semiconductor wafers	LAM Research provide the necessary wafer fabrication equipment, machinery, and technology for customers such as TSMC to manufacture semiconductor chips. Advanced machinery and intellectual property; significant market share	U.S. export controls; geopolitical tensions. Long-term investment in R&D; expanding operations in new regions.
TEL	Founded in 1963; supplies semiconductor production equipment The Ego network evidence Degree 26; Effect Size 25.692; Constraint 0.053; Density 0.012; Hierarchy 0.090. These metrics indicate a broad, low-redundancy ego network in which TEL brokers otherwise disconnected firms.	See ASML above. Supplies equipment for wafer fabrication and chip testing.	TEL supplies its equipment to major semiconductor manufacturers, including foundries like TSMC, and integrated device manufacturers (IDMs) such as Intel and Samsung. Their equipment is crucial for producing advanced semiconductor devices used in a wide range of electronic products. Clockspeed capability to scale innovations; ambitious targets for sales and profitability.	U.S. export controls on advanced semiconductor technology to China. Addressing social issues through advanced technology; strategic initiatives for growth.