The Degradation Mechanism of GaN RF HEMTs under High Temperature Operation Stress: Effects of High Drain Current and High Drain Voltage

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***Abstract*—In this work, the effects of high drain current and high drain voltage on the electrical performance degradation and burnout mechanism of Gallium Nitride (GaN) RF high electron mobility transistors (HEMTs) under high temperature operation stress have been investigated in-depth. It was found that gate leakage increases with stress drain current, while the degradation of the saturation drain current and RF output power is influenced by stress drain voltage. Photon emission and scanning electron microscopy analyses show that damage mainly occurs at the edges of central gate fingers under high current. The longitudinal electric field at the gate, caused by positive gate voltage, allows channel electrons to overcome the AlGaN/GaN barrier and pass through the AlGaN layer and Schottky junction. This leads to damage and leakage paths that degrade the Schottky contact and increase gate leakage. The results also show that catastrophic burnout occurs in the gate-drain access region, particularly near the drain electrode under high drain voltage. This is due to new defect formation and electron trapping caused by hot electrons near the drain, creating a strong longitudinal electric field. Once this field reaches a critical level, burnout occurs.**

***Index Terms*—GaN RF HEMTs, hot electrons, electron trapping, high drain current, high drain voltage.**

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I. Introduction

Gallium nitride (GaN) high electron mobility transistors (HEMTs) have been widely regarded as promising high-power and high-frequency devices for RF and microwave applications due to their superior properties, such as high output power, high efficiency, and high operation temperature [1], [2], [3]. However, reliability remains a major concern for GaN RF HEMTs. During RF operation, these devices are exposed to semi-on or on-state conditions, where high on-state current and high voltage exist simultaneously [2], [4], [6], [8]. This induces high carrier density and high electric field in the device, exacerbating the generation of hot electrons, which are known to be a major source of degradation in GaN HEMTs [7], [8]. Hot electron effects are particularly severe in high-temperature and high-power applications due to self-heating and thermal coupling effects [7], [10].

Many previous studies have extensively investigated the hot electron degradation mechanisms in GaN HEMTs. These studies have reported several reliability issues, including degradation of saturation drain current (I_{dsat}) and transconductance, threshold voltage (V_{th}) shift, increases in dynamic on-resistance (R_{ON}) and gate leakage current, and breakdown walkout. Several failure mechanisms have been proposed, including charge trapping [1], [3], [10], [19], generation of new defects [4], [7], [14], hot electron assisted defect formation and propagation [8], and dehydrogenation [2], [6], [9]. The relationship between hot electron effects and gate voltage has been extensively studied, concluding that the worst degradation occurs under semi-on-state conditions [2], [4], [6], [8], [15]. Temperature-dependent hot electron effects have also been studied using a hard-switching high-temperature reverse bias (HS-HTRB) stress test. It was observed that hot current affects V_{th} in two ways: channel impact ionization generates holes under the gate, shifting V_{th} negatively by lowering the gate-source barrier, while injected hot electrons shift V_{th} positively by depleting channel electrons [1]. Moreover, high-temperature constant source current (HTSC) tests have been conducted to investigate the effect of source current (usually less than 130 μA) on hot electron effects [1], [17]. These tests identified a significant correlation between the increase in R_{ON} and both source current and temperature.

However, most of these works are focused on GaN-based power electronic devices for switching applications. The temperatures they apply are also limited (usually less than 150 ℃), but the maximum operating junction temperature (T_j) of commercial GaN RF devices has reached 225 ℃ [18], [20]. Meanwhile, the high drain current and voltage also play an important role in hot electron effects. They will significantly affect the quantity and energy of channel electrons, which may aggravate hot electron effects. However, there is rare research on the effects of high drain current (I_d above 1 A) and high drain voltage on the degradation of GaN RF HEMTs under high temperatures (T_j above 150 ℃) operating stress. Accordingly, their roles in the device failure mechanisms, in this case, are still unknown. Thus, it is essential to investigate the roles of high drain current and high drain voltage on the degradation mechanism of GaN RF HEMTs targeting high-temperature and high-power applications.

This work aims to enhance the understanding of high drain current and voltage effects by systematically assessing their individual contributions to GaN RF HEMT degradation under high temperature operating conditions. Controlled stress experiments were performed with precisely varied drain current and voltage levels under elevated temperature conditions. It was found that gate leakage current significantly increased, while saturation drain current and RF output power (P_{out}) significantly decreased after stress. The failure mechanisms were analyzed and proposed with the aid of photon emission measurements (PEM) and scanning electron microscopy (SEM) techniques. The results reveal that the increase in gate leakage current and the degradation of I_{dsat} and P_{out} are caused by two different mechanisms, which dominate at high drain current and high drain voltage, respectively.

II. Device Structure and Fabrication

The AlGaN/GaN RF HEMTs studied in this work were grown on SiC substrates. The epitaxial layers consist of a 180-nm-thick AlN nucleation layer, a 1.3-µm-thick GaN buffer layer and a 22-nm-thick AlGaN barrier layer, deposited using metal organic chemical vapor deposition. To fabricate the ohmic contacts, a multilayer stack consisting of Ti/Al/Ni/Au (22/140/55/45 nm) was deposited through evaporation. The Schottky gate electrode was formed by electron beam evaporation of Ni/Au (125/250 nm) metal stacks. The source electrode is connected to the backside through vias, and the backside is electroplated with 10 µm of Au for grounding purposes.

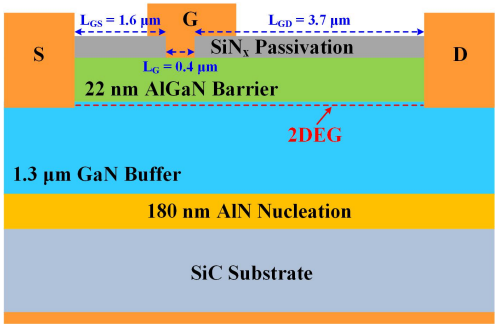

Fig. 1. The schematic cross-section of the AlGaN/GaN RF HEMT studied in this work.

The device features a gate length of 0.4 µm, with gate-to-source and gate-to-drain distances of 1.6 µm and 3.7 µm, respectively. It comprises 10 gate fingers, each with a width of 360 µm, resulting in a total gate width of 3.6 mm. The corresponding schematic diagram for the structure of the AlGaN/GaN RF HEMTs is given in Fig. 1. The devices exhibited a saturation P_{out} of 41-42 dBm, an average *PAE* of 65%, and an associated gain of 10 dB within the band. The drain-source breakdown voltage exceeds 120 V.

III. Experiments and Discussion

A. The Electrical Performances Degradation under High Temperature Operation Stress

To investigate the degradation mechanisms of GaN RF HEMTs under high-temperature operating stress, the devices were subjected to multiple DC bias conditions, as illustrated in Fig. 2, including $V_{DS\text{-}Stress}$ @ $I_{DS\text{-}Stress}$ values of 30 V@ 1.2 A, 36 V@ 1.0 A, 45 V@0.8 A, 60 V@0.6 A, and 90 V@0.4 A, which closely resemble the operational conditions of GaN RF applications [5], [20]. Even under varying stress bias conditions, the power dissipation and junction temperature of these devices remain constant at 36 W and 225 ℃, respectively, thereby effectively minimizing the impact of temperature-induced degradation [5], [26]. The maximum stress time was set to 10 ks in total or until breakdown. The junction temperature was estimated using an infrared temperature measurement system under the same conditions [21], [22]. The DC and RF performances were monitored at pre-set intervals during the stress. The transfer measurements were carried out at drain voltage V_{DS} = 5 V with gate voltage sweeping from -5 to 2 V, and the I_g-V_g curves were measured with the source and drain grounded. The DC output performances were measured at V_g = 2 V with V_{DS} sweeping from 0 to 10 V. The RF performances were measured at 3.7 GHz, biased at V_{DS} = 28 V with a quiescent current of 200 mA. All electrical characteristics were measured at room temperature.

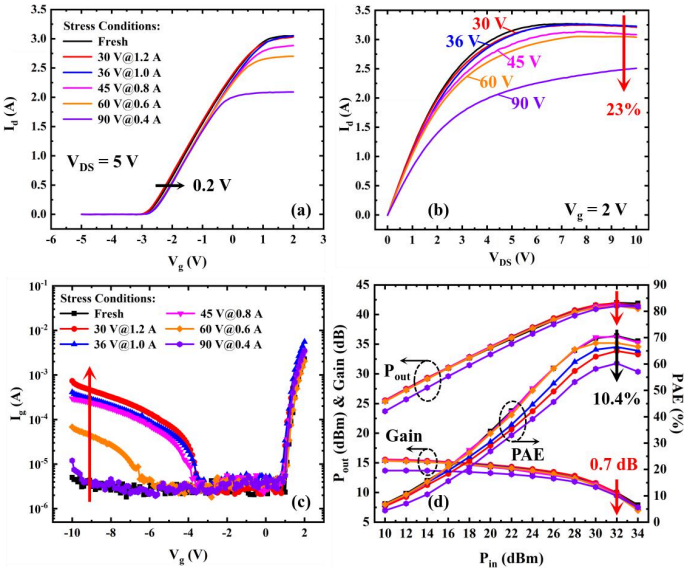

Fig. 2. Electrical performances after 10 ks of HTO stress under different DC bias conditions: (a) The transfer characteristics, (b) the output characteristics, and (c) the gate leakage current. (d) The P_{out}, gain, and *PAE* vs. the P_{in} at 3.7 GHz.

Fig. 2(a) shows that under HTO stress with constant power dissipation but varying DC bias conditions, the transfer characteristic curves of the device exhibit a slight forward shift along the X-axis. The maximum V_{th} shift is 0.2 V, indicating minimal electron trapping beneath the gate region. As shown in Fig. 2(b), under constant-power HTO stress, the I_{dsat} significantly decreases with increasing drain voltage. Especially when $V_{DS\text{-}Stress}$ increases to 90 V, the maximum decrease of the I_{dsat} is 23%. In Fig. 2(c), the gate leakage current is seen to increase substantially with rising drain current, particularly at $I_{DS\text{-}Stress}$ = 1.2 A, where the reverse gate leakage current increases by more than two orders of magnitude. Fig. 2(d) illustrates the RF performance degradation under constant-power HTO stress, revealing a significant decrease in P_{out} as the applied drain voltage increases. At $V_{DS\text{-}Stress}$ = 90 V, both P_{out} and gain drop by 0.7 dB, while the power-added efficiency decreases by 10.4% at P_{in} = 32 dBm. These results demonstrate that GaN RF HEMTs undergo notable performance degradation under HTO stress, with the extent of degradation in key electrical parameters strongly correlated to the applied drain stress voltage and current. To gain further insights into the degradation mechanism, HTO stresses with different drain currents and voltages were performed to figure out the effect of high carrier density and high electric field on the electrical performance degradation in the following.

B. The Effect of High Drain Current on the Electrical Performances Degradation

To investigate the role of high drain current in degradation, stress tests were performed under T_j = 225 °C with various drain current conditions, including $I_{DS\text{-}Stress}$ = 0.4 A, 0.8 A, and 1.2 A. The drain bias was held constant at 30 V for each stress condition, ensuring the electric field was constant and safe. To maintain a constant T_j, the baseplate temperature of the thermal platform was set and actively adjusted as the drain current increased. This setup ensured that only the carrier density changed under these stress conditions, allowing for an evaluation of the current's role in degradation.

Fig. 3(a) shows the variation of transfer characteristics under different $I_{DS\text{-}Stress}$ conditions. It was observed that the V_{th} shift is negligible when increasing $I_{DS\text{-}Stress}$. Fig. 3(b) illustrates the degradation of DC output characteristics under different $I_{DS\text{-}Stress}$ conditions, revealing that I_{dsat} degrades only slightly as $I_{DS\text{-}Stress}$ increases. Even under $I_{DS\text{-}Stress}$ = 1.2 A, the reduction in I_{dsat} is insignificant. Fig. 3(c) presents the gate leakage current of the devices under different $I_{DS\text{-}Stress}$ conditions. The degradation of the gate leakage current under $I_{DS\text{-}Stress}$ = 0.4 A is negligible. However, as $I_{DS\text{-}Stress}$ increases, the reverse gate leakage rises substantially. At $I_{DS\text{-}Stress}$ = 1.2 A, the reverse gate-leakage current increases by approximately three orders of magnitude. Fig. 3(d) depicts the RF performance degradation under different high drain current stresses. the P_{out} and gain change minimally, decreasing only by 0.1 dB even at $I_{DS\text{-}Stress}$ = 1.2 A. However, higher $I_{DS\text{-}Stress}$ leads to lower *PAE*, with a 5.7% decrease at P_{in} = 32 dBm when the drain current increases to 1.2 A. As a result, the main impact of high drain current under HTO stresses is an increase in gate leakage of GaN RF HEMTs.

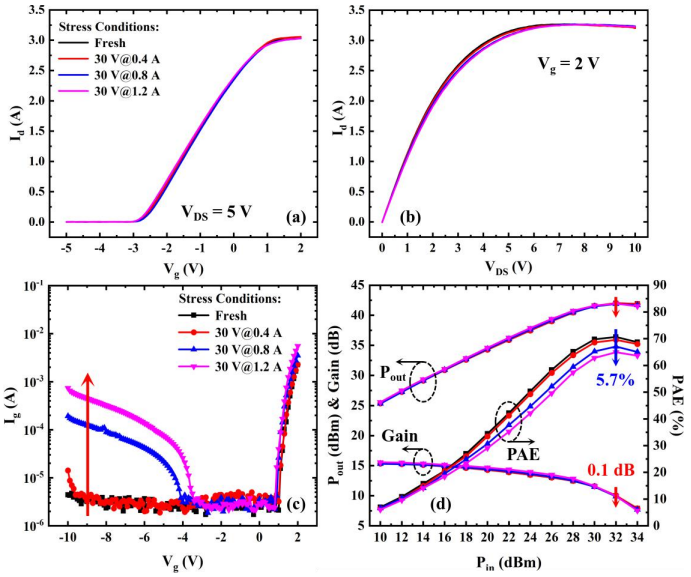

Fig. 3. The DC and RF performances after 10 ks of HTO stresses with different drain currents and a constant drain bias of 30 V. (a) The transfer characteristics, (b) the I_d-V_{DS} characteristics, (c) the gate leakage current, and (d) the P_{out}, gain, and *PAE* vs. the P_{in} at 3.7 GHz.

To further characterize the Schottky junction, the Schottky parameters (Schottky barrier height $e\Phi_b$ and ideality factor n) are extracted from the I_g-V_g curves according to the thermionic model [13]. Fig. 4 shows the Schottky parameters degradation against the drain current. It is observed that the Schottky barrier decreases by 0.22 eV, and the ideality factor increases by 1.47 under $I_{DS\text{-}Stress}$ = 1.2 A. This suggests substantial degradation of the Schottky contact due to high drain current stress, potentially leading to the formation of leakage paths beneath the gate.

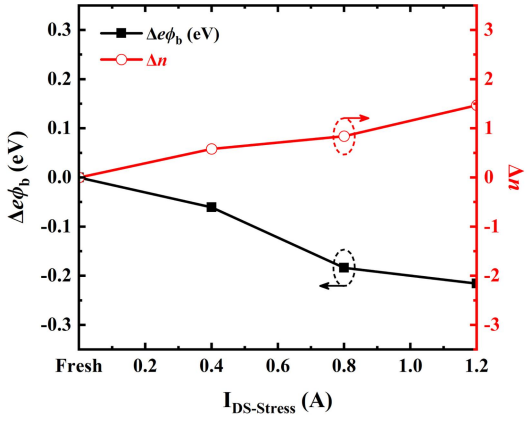

Fig. 4. The normalized Schottky barrier height $e\Phi_b$ and ideality factor n as a function of $I_{DS\text{-}Stress}$ with the drain bias of 30 V.

To gain more insight into the physical degradation process, the PEM technique was utilized to localize the leakage paths produced during the stress. Fig. 5(a) shows that the photoemission signature of the fresh device over the entire structure is insignificant, indicating the absence of leakage paths. Compared to the reference fresh device, Fig. 5(b) shows some photoemission in the stressed device with the drain current of 0.4 A, indicating faint local damages. When the drain current increases to 0.8 A, the hotspots become visible in Fig. 5(c), correlating with the increase in gate leakage. This indicates that the damage induced by high drain currents

becomes more severe. When the drain current increases further to 1.2 A, light emission becomes stronger and more extensive in Fig. 5(d), corresponding to the higher gate leakage current in Fig. 3(c). Furthermore, two notable features are observed. First, the light emission intensities are higher in the center of the devices under each stress condition because the local temperature of the gate are greater in the central areas due to self-heating and thermal coupling effects [3], [7], [10]. This demonstrates that the middle position of the central gate fingers suffers more severe damage. Second, the strongest hotspot signal appears at the edge of the gate, as illustrated by the insets in Fig. 5(b), (c), and (d).

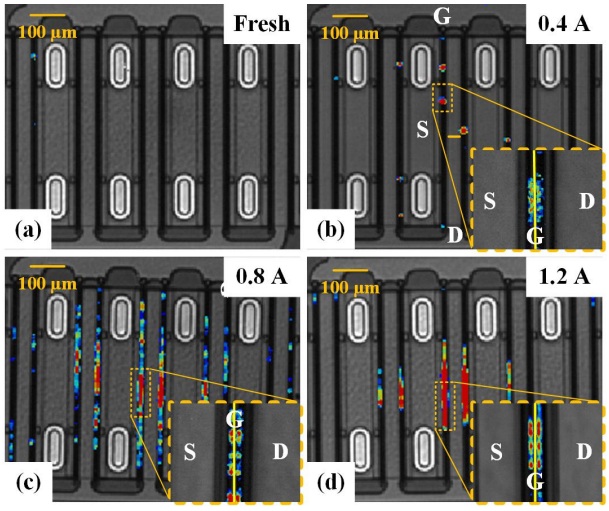

Fig. 5. PEM images of the HEMTs in off-state mode (V_g = -5 V, V_{DS} = 28 V) after different drain current stress with the drain bias of 30 V. (a) Fresh, (b) $I_{DS\text{-}Stress}$ = 0.4 A, (c) $I_{DS\text{-}Stress}$ = 0.8 A, and (d) $I_{DS\text{-}Stress}$ = 1.2 A. The insets show a higher magnification of the marked hotspots.

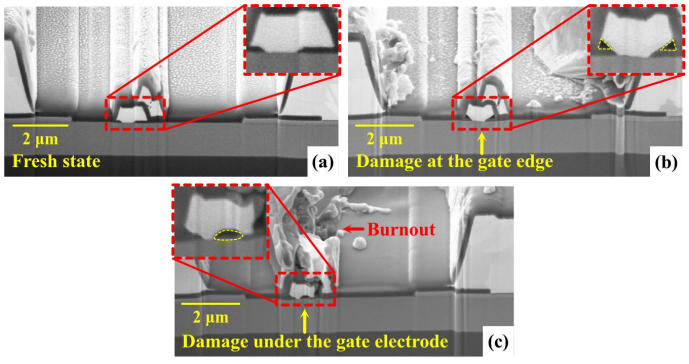

Fig. 6. SEM images show the morphology of GaN HEMTs under $I_{DS\text{-}Stress}$ = 1.2 A with the drain bias of 30 V. (a) Fresh state. (b) The slight damage form at the gate edge. (c) More severe damage below the gate region.

To further investigate the physical origin of these leakage paths, SEM analysis was performed. Fig. 5 shows SEM images of the burned devices with a longer stress time (15 ks) under $I_{DS\text{-}Stress}$ = 1.2 A. As shown in Fig. 6(a), no damage is observed in the fresh device. However, in Fig. 6(b), a slight burnout damage is observed below the gate in the stressed device, particularly near the edge of the gate, which aligns with the result observed in Fig. 5. Furthermore, Fig. 6(c) illustrates more severe damage to the gate, with the Schottky junction and the metal structure of the gate finger completely burned out. It is noteworthy that other regions away from the gate electrode suffer little damage. These results indicate that the edge of the central gate fingers in GaN RF HEMTs is the most vulnerable area under high drain current stress.

To gain insight into the degradation mechanism, the energy band diagrams of the gate region are presented in Fig. 7. Fig. 7(a) shows the electron behavior under a low drain current of 0.4 A. Under the negative gate voltage, electrons are injected from the gate metal into the 2DEG channel, and the hot electrons injection from the 2DEG channel into the gate is impeded. As a result, the number of hot electrons injected into the gate is low, and the degradation is insignificant, indicating few defects are introduced into the device. When the drain current increases to 1.2 A, the channel under the gate is more fully turned on, and a larger number of electrons populate the channel. In addition, the gate bias is now positive, assisting hot electron injection into the gate. Consequently, a higher number of electrons can surmount the AlGaN/GaN interface barrier and passing through the AlGaN layer and the Schottky junction, as illustrated in Fig. 7(b). This causes more Schottky contact degradation and higher gate leakage current, inducing hotspots observed by PEM in Fig. 4. Furthermore, the increase in gate leakage current can cause an increase in power dissipation, which decreases the *PAE* of the devices.

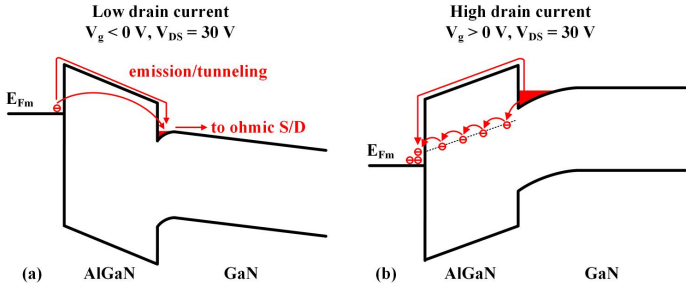

Fig. 7. Schematic energy band diagrams show the leakage mechanism under HTO stress with (a) low and (b) high drain currents, respectively.

C. The Effect of High Drain Voltage on the Electrical Performances Degradation

To investigate the effect of high drain voltage in degradation, stress tests were performed at T_j = 225 °C with various drain voltage conditions, including $V_{DS\text{-}Stress}$ = 30 V, 60 V, and 90 V. The drain current was held constant at 0.4 A by dynamically adjusting the V_g for each stress condition, ensuring the carrier density in the channel remained constant and safe for the devices. Only the electric field changes under these stress conditions, allowing for the evaluation of drain voltage-induced degradation. The T_j control process is consistent with the methods used in section III.B.

Fig. 8(a) depicts the variation in transfer characteristics under different $V_{DS\text{-}Stress}$. It was found that the V_{th} shifted positively with increasing $V_{DS\text{-}Stress}$, with a maximum shift of 0.2 V at $V_{DS\text{-}Stress}$ = 90 V. This phenomenon is primarily attributed to the electron trapping during stress [1]. Fig. 8(b) shows the degradation of DC output performance under different $V_{DS\text{-}Stress}$. The DC output performance degrades as $V_{DS\text{-}Stress}$ increases, with the maximum reduction in I_{dsat} reaching 23% at $V_{DS\text{-}Stress}$ = 90 V. Fig. 8(c) shows the gate leakage current of the devices under different $V_{DS\text{-}Stress}$ conditions. The gate leakage degrades little as $V_{DS\text{-}Stress}$ increases. Even at $V_{DS\text{-}Stress}$ = 90 V, the increase in gate leakage current is still negligible, indicating few leakage paths introduced into the device. Fig.

8(d) depicts the RF performance degradation of the devices under different $V_{DS\text{-}Stress}$ conditions. The degradation of P_{out} and gain is insignificant under $V_{DS\text{-}Stress}$ = 30 V. As $V_{DS\text{-}Stress}$ increases, the degradation becomes more pronounced. At $V_{DS\text{-}Stress}$ = 90 V, both P_{out} and gain decrease significantly by 0.7 dB, and *PAE* is reduced by 10.4% at P_{in} = 32 dBm. Notably, RF performance degradation occurs at a lower P_{in} when $V_{DS\text{-}Stress}$ reaches 60 V, worsening as $V_{DS\text{-}Stress}$ increases. These results indicate that the degradation of I_{dsat} and P_{out} under high drain voltage stress is more severe than the increase in gate leakage current and the shift of V_{th}. This contrasts with the situation of HTO stress under high drain current.

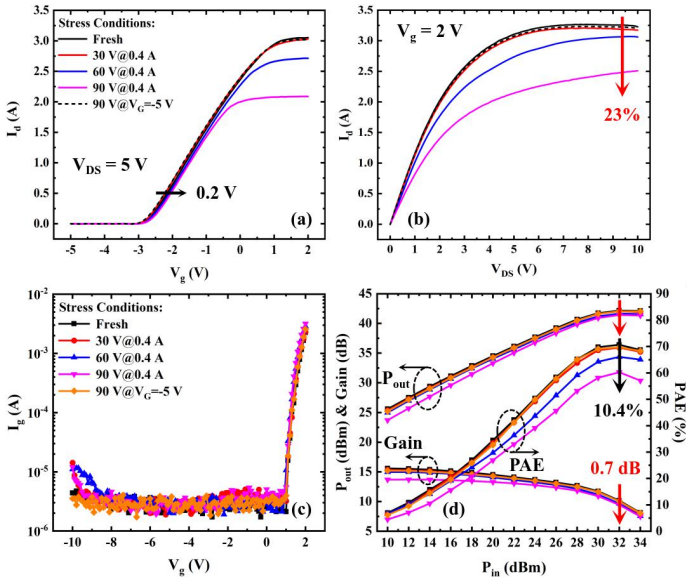

Fig. 8. The DC and RF performances after 10 ks of HTO stresses with different drain voltages and a constant drain current of 0.4 A. (a) The transfer characteristics, (b) the I_d-V_{DS} characteristics, and (c) the gate leakage current. (d) The P_{out}, gain, and *PAE* vs. the P_{in} at 3.7 GHz. The dashed and orange lines show the electrical performances of the device under off-state stress with V_g = -5 V and $V_{DS\text{-}Stress}$ = 90 V.

One might suspect that degradation under high drain voltage is due to the inverse piezoelectric effect [23]. To verify this, off-state stress with V_g = -5 V, $V_{DS\text{-}Stress}$ = 90 V, and T_j = 225 °C was applied to the reference device. As shown in Fig. 8, both DC and RF performance degradation are negligible, indicating that electrical degradation under HTO stress with high drain voltage is not due to the inverse piezoelectric effect but closely related to the channel hot electrons.

To gain further insights into the degradation of I_{dsat} and P_{out}, we measured the R_{on} under different drain voltage stresses, extracted within the ohmic region of the DC output characteristics [11]. The parasitic source/drain access region resistance ($R_{s/d}$) was also compared, obtained using the gate probe method [12]. Fig. 9 shows that both the R_{on} and R_d degrade significantly as $V_{DS\text{-}Stress}$ increases and agree well with each other, while the variation of R_s is negligible. It indicated that extra new defects were introduced in the gate-drain access region, causing significant electron trapping due to the high electric field between the gate and drain [1], [3], [7], [8], [16], [17].

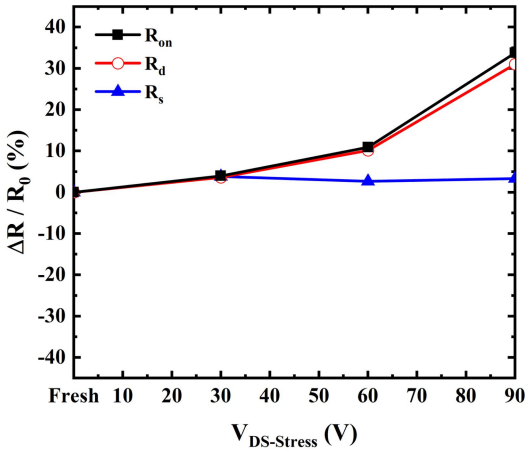

Fig. 9. The normalized R_{on}, R_s, and R_d as a function of $V_{DS\text{-}Stress}$ after a stress time of 10 ks.

To further investigate the physical origin of this phenomenon, SEM analysis was performed on the burned device with a longer stress time (12 ks) under $V_{DS\text{-}Stress}$ = 90 V. As shown in Fig. 10(a), no damage is observed in the fresh reference device. However, significant burnout is observed in the gate-drain access region, with more severe burning near the drain, as illustrated in Fig. 10(b). It should be noted that the region below the gate shows little damage. These results indicate that the gate-drain access region, especially near the drain of GaN RF HEMTs, may be the most sensitive and vulnerable area under high drain voltage stress.

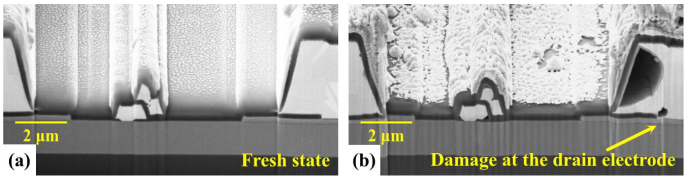

Fig. 10. SEM images show the morphology of GaN RF HEMTs under $V_{DS\text{-}Stress}$ = 90 V. (a) Fresh state. (b) The damage at the drain electrode.

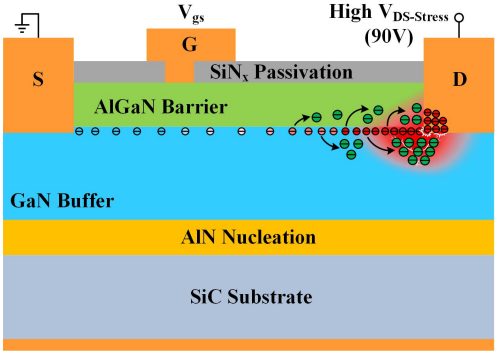

Fig. 11. The schematic cross-section of the HEMT shows the electron trapping (Green symbols) in the gate-drain access region under HTO stress with high drain voltage. The energy of channel electrons is represented by different shades of red color.

To more clearly illustrate the degradation mechanism under high drain voltage stress, Fig. 11 presents a schematic cross-sectional view of the device. It should be noted that the figure shows the physical image of the internal electric field distribution of the device when it reaches a steady state after a long period of stress (up to 10 ks in this study). During this process, the initial peak electric field located at the edge of the

gate near the drain gradually migrates towards the drain edge due to the generation of defects induced by hot electrons and the charge trapping effect, eventually extending the depletion region to the drain edge [8], [24], [25].

Under the influence of a strong electric field, channel electrons acquire sufficient energy to become hot electrons. Particularly in the region near the drain, due to the continuous acceleration by the lateral high electric field, the electron energy reaches its peak. Most of the hot electrons are collected by the drain to form the drain current, while the remaining hot electrons mainly cause the following three adverse effects:

① Some hot electrons scatter into the AlGaN and GaN layers between the gate-drain access regions, where they will be captured by pre-existing traps.

② Other high-energy hot electrons collide with lattice atoms in the gate-drain access region, especially near the drain electrode, generating significant number of new defects. These newly generated defects can trap channel electrons, leading to significant additional electron trapping. This trapping reduces the density and mobility of channel electrons, causing a significant increase in R_d and R_{on}, ultimately degrading both DC and RF output performances. Moreover, the trapped electrons induce an electric field modulation effect, enhancing the local longitudinal electric field near the drain [25]. A higher field generates more traps, further enhancing the field, creating a positive feedback loop near the drain. When a critical electric field is reached, catastrophic burnout occurs near the drain, as observed in Fig. 9.

③ Furthermore, hot electrons with higher energy induce impact ionization near the drain electrode, triggering an avalanche multiplication effect [24]. This process generates a large number of secondary electrons, leading to a sudden current surge and a significant increase in local temperature. In severe cases, this can cause device burnout. Concurrently, this phenomenon amplifies the effects described in ① and ②, further aggravating the device's breakdown failure.

IV. Conclusion

In conclusion, this work has studied the effects of high drain current and high drain voltage on the degradation mechanism of GaN RF HEMTs under HTO stress. The results show that high drain current under positive gate bias can cause a significant number of electrons to be injected into the barrier layer and Schottky junction, resulting in the accumulation of gate leakage paths and the degradation of Schottky contact, which in turn increases the gate leakage current. In contrast, high drain voltage can cause channel electrons to gain enough energy to become hot electrons. These hot electrons collide with the lattice in the gate-drain access region, generating new defects and leading to significant electron trapping. This reduces the density and mobility of channel electrons, increasing R_{on} and R_d, and decreasing I_{dsat} and P_{out}. With the aid of PEM and SEM, it is found that the sensitive and vulnerable areas of the device under high drain current and high drain voltage conditions are the edge of the central gate fingers and the drain electrode, respectively. These results indicate that under high-current operation, reinforcing the gate edge effectively suppresses leakage current, while under high-voltage operation, optimizing the electric field distribution in the gate-drain region mitigates hot-electron-induced degradation. This offers a practical pathway for designing more robust GaN power amplifiers tailored to specific operating conditions.

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