Insight into Electron Traps and Their Energy Distribution under Positive Bias Temperature Stress and Hot Carrier Aging

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***Abstract*— The access transistor of SRAM can suffer both Positive Bias Temperature Instability (PBTI) and Hot Carrier Aging (HCA) during operation. The understanding of electron traps (ETs) is still incomplete and there is little information on their similarity and differences under these two stress modes. The key objective of this paper is to investigate ETs in terms of energy distribution, charging and discharging properties, and generation. We found that both PBTI and HCA can charge ETs which center at 1.4eV below conduction band (Ec) of high-k (HK) dielectric, agreeing with theoretical calculation. For the first time, clear evidences are presented that HCA generates new ETs, which do not exist when stressed by PBTI. When charged, the generated ETs' peak is 0.2eV deeper than that of pre-existing ETs. In contrast with the power law kinetics for charging the pre-existing ETs, filling the generated ETs saturates in seconds, even under an operation bias of 0.9 V. ET generation shortens device lifetime and must be included in modelling HCA. A cyclic and anti-neutralization ETs model (CAM) is proposed to explain PBTI and HCA degradation, which consists of pre-existing cyclic electron traps (PCET), generated cyclic electron traps (GCET), and anti-neutralization electron traps (ANET).**

Index terms: electron traps, PBTI, hot carriers, BTIs, aging, trap generation, energy distribution, device lifetime, SRAM.

I. INTRODUCTION

Since 45nm node, hafnium based high-k (HK) materials have been widely used as gate dielectric to increase physical thickness and reduce gate leakage. Application of metal gate/HK stack, however, has increased positive bias temperature instability (PBTI) [1-8]. PBTI originates from electron traps (ETs) and one of their sources is water/hydrogen related species [9, 10].

In the early stage of HK development, it was reported that there are as-grown ETs above the Si conduction band edge, Ec, [1, 5, 8] and located in the HK layer [3, 11]. Their charging-discharging is highly dynamic: the charging and discharging completes within seconds [1, 3, 12]. Process optimization has made these energetically shallow ETs negligible, but PBTI still is a reliability issue, as deeper ETs are found [1, 13].

In addition to PBTI, such as the access transistors in a SRAM cell, also suffer from hot carrier aging (HCA) [14]. As channel length down-scales, HCA scales up and has attracted many attentions recently [14-17]. It has been reported that ETs contribute substantially to HCA, especially under Vg=Vd [16]. However there is little information on the similarity and differences of ETs under PBTI and HCA, leaving us the chance to investigate ETs in terms of energy distribution, charging and discharging properties, and generation.

II. DEVICES AND EXPERIMENTS

Devices used are nMOSFETs, fabricated by an industrial 28nm high-k process. The channel width and length are 900nm and 36nm with HK/metal gate. C-V measurement gives a 1.2 nm equivalent oxide thickness (EOT). For nanometer MOSFETs, it has been reported that HCA is higher under Vg=Vd, rather than the conventional worst condition of Vg=Vd/2 [14-16]. Vg=Vd was used for HCA, therefore. All tests were at 125 ºC.

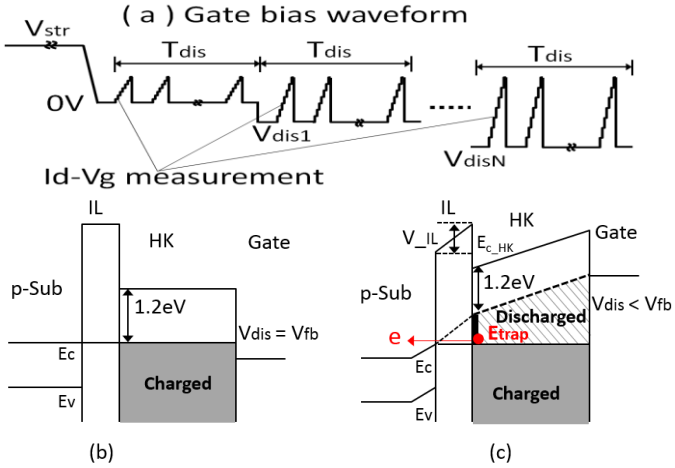

Fig. 1(a) Gate bias waveform for energy profile measurement. Discharging during Tdis was monitored by Id-Vg measurement after charging at Vstr. Vdis was lowered down from 0 V by steps of 50 mV. Each discharging voltage (Vdis) was kept for Tdis. (b) Energy band diagram after discharging under flat band voltage Vfb. (c) Discharging under Vdis<Vfb. All traps in the striped area are discharged when Vg step down from Vfb to Vdis<Vfb. Here we assumed that tunneling mediated through interface states was insignificant [1].

To probe ETs energy profile, the discharge based technique was implemented [18]. The Vg waveform is shown in Fig. 1 and the test procedure is: 1) Stress the device under Vg = Vstr for a certain time. 2) Vg is then lowered to Vdis0 = 0 for discharge. 3) The discharge voltage is kept for Tdis, during which Id-Vg curve is monitored with a logarithmic time

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interval. 4) Vg is then lowered further by -50 mV to another Vdis and repeat step 3), until the preset VdisN is reached. The ETs moving above Si Ec were discharged progressively (Fig. 1(c)). The threshold voltage, Vth, was monitored during each discharge period under a fixed drain current of 100nA×W/L.

One typical result is given in Fig. 2. The discharge under Vg>0 was not measured, since our results [14] and early work [15] showed discharge under Vdis = 0 was insignificant. The test finished at Vdis= -2 V, as there is little further discharge when Vdis< -1.5 V (Figs. 2(a) and (b)). Fig. 2(b) compares the ΔVth at different discharge time. The discharge is driven mainly by Vdis and there is little difference when time increases from 1 to 1000 sec. This agrees well with early works that carrier tunneling completes in seconds for thin dielectric [12, 18]. Unless stated otherwise, a discharge time of 100 sec was used. The measurement itself causes little degradation.

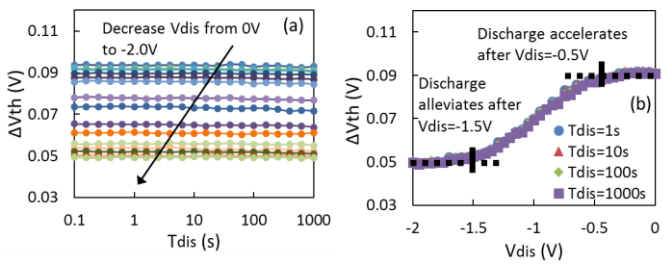

Fig. 2 A typical result for discharging. One device was firstly charged at Vg=2.0 V for 1000 s. Vdis was reduced from 0 to -2 V with a -50 mV step and each Vdis was kept for 1000 s. (a) plots ΔVth against discharge time and (b) plots ΔVth against Vdis.

III. ENERGY DISTRIBUTION: PBTI AND HCA

A. *Extraction of ETs energy distribution*

The data in Fig. 2 is used as a demonstration for the extraction of energy distribution. Following the early works [7, 8, 18], ΔVth is converted to ΔNt, the equivalent trap density at the interface of interfacial layer (IL) and HK using eq. (1). When Vdis changes, the trap energy, E_{trap}, at IL/HK interface is modulated against Si Ec by the same amount as the potential drop over the IL, $V_{_IL}$, as shown in Fig. 1(c). $V_{_IL}$ and E_{trap} can be calculated with eqs. (2-3), respectively, where E_{c_HK}- E_{trap} is the enegy level where ETs become dischargeable at Vdis.

$$\Delta Nt = (1+\varepsilon_{_HK}/\ \varepsilon_{_IL} * t_{_IL}\ /t_{_HK}) * C * \Delta Vth/q \quad (1)$$

$$V_{_IL} = (V_g-\Delta Vth-V_{fb}-\Psi_s)/(1+\varepsilon_{_IL}/\ \varepsilon_{_HK} * t_{_HK}\ /t_{_IL}) \quad (2)$$

$$E_{c_HK} - E_{trap} = q*(1.2 - V_{_IL}) \quad (3)$$

where C is gate dielectric capacitance per unit area, V_{fb} flat band voltage, Ψs silicon surface potential, ε permittivity, and t the thickness of dielectric. The relation between (Vg-ΔVth) and Ψs was calculated and details are given in [19]. The use of (Vg-ΔVth), rather than Vg, in Fig. 3(a) takes into account the effect of trapped charges on $V_{_IL}$ [20]. Following previous works [1, 8], a 1.2 eV conduction band offset between Si and HK was used under flat band condition, as shown in Fig. 1(b).

By using the eqs. (1-3) and Fig. 3(a), the energy profile of trap density ΔNt in Fig. 3(b) was extracted from the ΔVth versus Vdis data in Fig. 2(b). The ETs energy density, ΔDt, in Fig. 3(c) was obtained from $|d(\Delta Nt)/d(E_{c_HK}-E_{trap})|$. ET peaks at 1.4eV below the HK conduction band, in agreement with early work [1] and theoretical work [21]. The dischargeable ETs becomes insignificant above 1.7 eV.

B. *A comparison of energy distribution: PBTI and HCA*

Fig. 4 compares the ETs energy distributions when stressed by PBTI and HCA under different biases. An increase of the Vstr for PBTI raises ΔDt, but the distribution shape is broadly similar with a peak around 1.4 eV, as shown in Fig. 4(a). For HCA in Fig. 4b, however, the distribution is wider and a second peak can be observed around 1.6eV. These two peaks of HCA suggest there are two types of dischargeable ETs, which will be further explored in the next section.

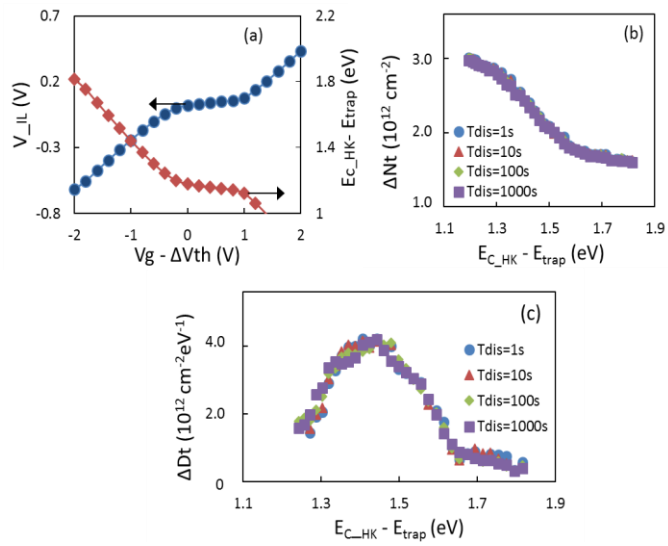

Fig. 3 Procedure for extracting the energy profile of trap density. (a) The calculated potential drop over interfacial layer ($V_{_IL}$) and the corresponding E_{c_HK}-Etrap at the IL/HK interface. (b) Vdis of Fig. 2(b) is converted to E_{c_HK}-Etrap at the IL/HK interface. (c) The profile of traps energy density $\Delta Dt=|d(\Delta Nt)/d(E_{c_HK}-Etrap)|$.

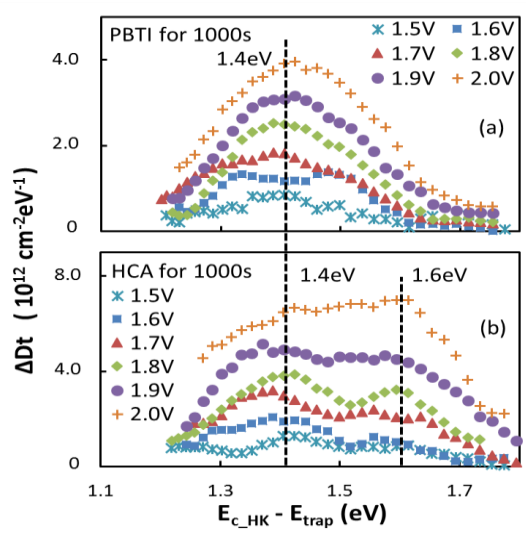

Fig. 4 The distribution of energy density ΔDt under PBTI (a) and HCA (b) for different stress voltages. HCA was under Vg=Vd.

The ETs energy distributions of PBTI and HCA after different stress time are also compared in Fig. 5. Similar feature can be observed: PBTI has one peak close to 1.4 eV, while two peaks for HCA with one at 1.4 eV and the other at 1.6 eV. It is interesting to note, for the longest stress time (10 ksec), the peak near 1.4 eV is overwhelmed by the 'pull-up' of the dominant peak around 1.6 eV. The peak at 1.6 eV broadly keep constant and insensitive to stress voltages and time.

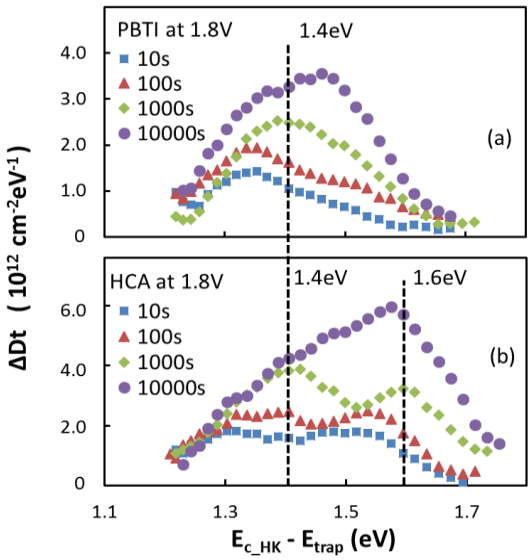

Fig. 5 The distribution of energy density ΔDt under PBTI (a) and HCA (b) for different stress time. HCA was under Vg=Vd. Unlike other distributions, the 10000s one in b) is dominated by the 1.6 eV ETs which masks out the groove between 1.4 eV and 1.6 eV.

IV. AN ANALYSIS OF ELECTRON TRAPS

A. *Types of electron traps under PBTI*

Pre-existing cyclic electron traps (PCET): When a relatively low gate voltage +1.5 V was applied, stage_1 in Fig. 6(a) shows that the charged ETs can be fully discharged by applying Vg= -1.8 V. The charging and discharging can be cycled by alternating Vg between +1.5 and -1.8 V in both stage_1 and stage_3, so that these ETs will be referred to as cyclic electron traps (CET). To differentiate with CET after stress, the CET in stage_1 is named as PCET since they are already pre-existing.

Anti-neutralization electron traps (ANET): After characterizing the PCETs, a heavy PBTI stress with Vg= 2 V was applied at the stage_2. Fig. 6(a) shows that there are ETs that do not discharge even under Vg= -1.8 V and they are referred to as Anti-neutralization electron traps (ANET). The discharge reaches a clear saturation for Vg< -1.5 V in Fig. 2(b), so that ANET is well separated from CET. The energy level of ANET is deeper than ~1.8 eV from E_c of HK, the end of range probed in Fig. 3(c). We cannot precisely measure it since ANET does not discharge even under Vg= -2 V for 1000 sec. For NBTI, the term permanent component was used [22, 23]. This can be misleading, since they are not really permanent and can be neutralized by raising temperature [22, 24]. The term 'anti-neutralization' is preferred, therefore.

After heavy PBTI stress under Vg = 2 V and discharge under -1.8 V, the biases in the stage 1 were applied again for CET measurement in the stage_3. Fig. 6(b) compares CETs in the stage_1 and stage_3 and a good agreement is obtained. This leads to the conclusion that PBTI stress does not generate new CET.

To confirm that ANET originates from ETs rather than interface states, the subthreshold swing (SS) was measured, as generation of interface states will cause SS degradation [25,26]. Fig. 7 confirms that PBTI does not degrade SS.

To further study the relation between CET and ANET, the energy distributions before and after heavy PBTI stress are compared in Fig. 8. Despite of the different levels of ANETs, the CETs are same. We conclude that charging CET and ANET are two independent processes. They have different origins and are different types of traps.

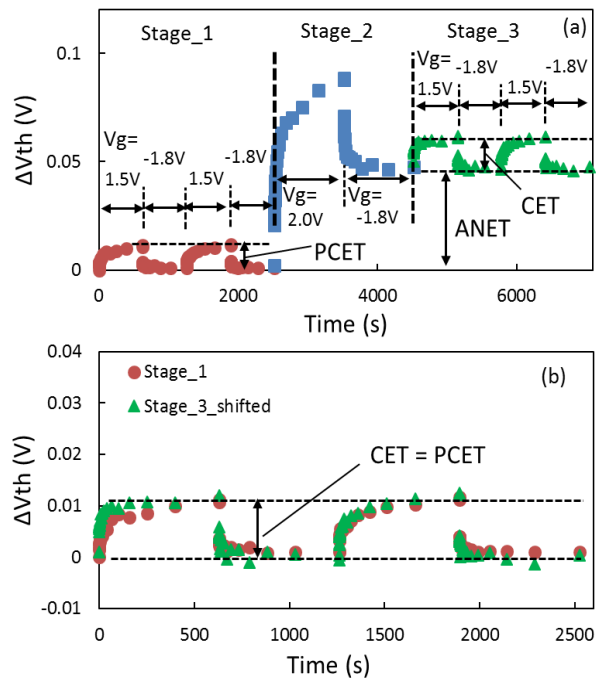

Fig. 6 A typical test procedure of CETs and ANET. (a) At stage_1, a gate voltage sequence of 1.5V, -1.8V, 1.5V, -1.8V was applied to monitor the pre-existing cyclic electron traps (PCET). At stage_2, a heavy stress was applied with Vg=2V, followed by a discharge at Vg=-1.8V for 1ks. State_3 was a repeat of State_1 to re-monitor CET. (b) compares PCET and CET at stage_3 by removing anti-neutralization electron traps (ANET), CET=PCET.

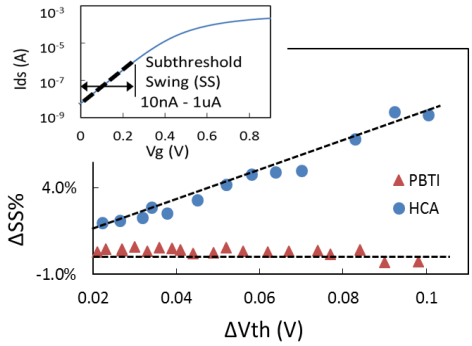

Fig. 7 A comparison of subthreshold swing (SS) degradation under PBTI and HCA. SS does not degrade for PBTI, suggesting no interface states created. But a clear SS degradation can be observed on HCA stress. Inset shows the SS extraction method.

B. *Types of electron traps under HCA*

Generated cyclic electron traps (GCET): When the heavy PBTI stress in stage_2 of Fig. 6(a) was replaced by a HCA, Fig. 9 shows that CET clearly increases after HCA, i.e. CET > PCET in Fig. 9(b). Since the charging conditions in the stage_1 and stage_3 are exactly same, higher CET can only be explained by the presence of more traps. In another word, additional CET is generated by HCA, which is referred to as the generated cyclic electron traps (GCET). GCET can be characterized quantitatively from CET- PCET. Fig. 9 also shows the overall degradation for HCA is much larger than PBTI, agreeing with earlier reported result [15].

SS degradation in Fig. 7 suggests HCA can also generate interface states. The contribution of generated interface states under HCA is estimated being around 67% of ANET [25].

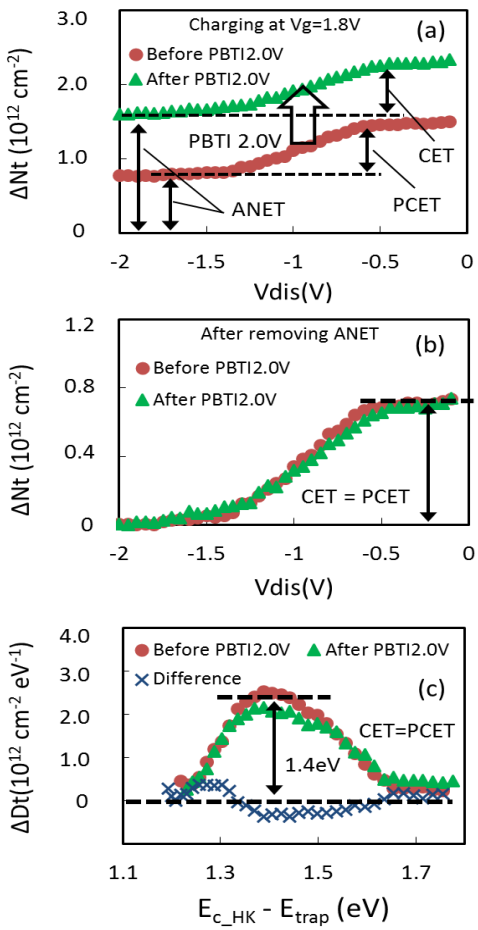

Fig. 8 A comparison of CET energy distributions after PBTI stresses. The test procedure is similar to that in Fig. 6(a). In stage_1, the distribution was measured after charging PCET at Vg=1.8 V for 1 ks. Then a heavy PBTI stress under 2 V was applied. After full discharge, in stage_3, CET was recharged at 1.8 V and the distribution was measured again. (a) compares the trap density before and after the heavy PBTI stress. (b) was obtained by removing ANETs and (c) shows the CET energy profile is not changed by the heavy PBTI stress.

Fig. 10 compares the energy profiles before and after HCA. We can see in Fig. 10(c) that GCET can be well separated from original PCET. GCET has a peak around 1.6 eV, 0.2 eV deeper than that of PCET. This, together with Figs. 4 & 5, leads to the conclusion that once the GCET is created, it can be charged not only by HCA, but also PBTI.

C. *Charging kinetics of CETs*

It can be seen in Fig. 9 that GCET can be charged and discharged repeatedly. The energy profiles were extracted from discharging and we will examine the charging kinetics in this section.

After each pre-specified charging time, PCET was measured from the discharged amount by applying Vg= -1.8 V for 100s, as illustrated in Fig. 6(a). Fig. 11(a) plots the PCET against charging time under different filling Vg. As expected, PCET is Vg accelerated and follow a power law. To generate GCET, a HCA stress was used. The same filling Vg used in Fig. 11(a) was then applied in Fig. 11(b). Two differences can be observed: 1) higher starting degradation gives a smaller time exponent, and 2) PCET+GCET is weakly Vg-acceleration. This can be explained by Fig. 11(c). The GCET already reaches saturation within seconds, i.e. the first measurement point. It supports that GCET and PCET are different types of defects.

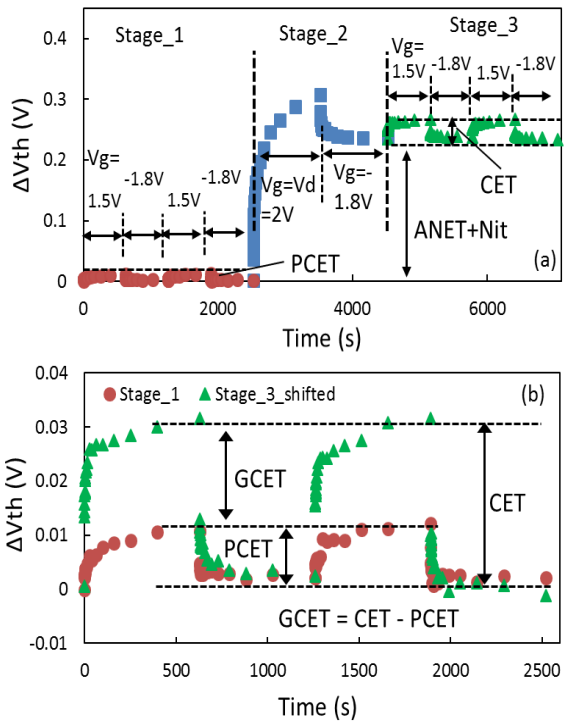

Fig. 9 Test procedure is similar to Fig. 6, except that heavy PBTI was replaced by HCA. Vg was alternated between +1.5 and -1.8 V to measure CETs for both stages_1 and stage_3. In stage_2, a HCA under Vg=Vd=2 V was used. (b) compares the PCET at stage_1 and CET at stage_3 by removing ANET+Nit. A clear increase of CET is observed.

To further explore the difference, Fig. 12 plots PCET and GCET dependency on charging Vg at a fixed 1.1 ksec filling time. GCET is one order of magnitude higher than PCET at operation voltage of 0.9V. In addition GCET rises with filling Vg initially and saturates when Vg>1.5 V. However no saturation is observed for PCET.

D. *Cyclic and anti-neutralization ETs model (CAM)*

Based on the defects property, a new CAM framework for ETs is proposed in Fig. 13, consisting of three types of ETs: PCET, GCET and ANET.

The charged PCET locates in the energy range of 1.2-1.6 eV, and its peak is round 1.4 eV, as shown in Fig. 8(c), so that their discharge/recovery under Vg=0 is insignificant. The PCET charging is negligible under Vg=0.9 V, suggesting the uncharged PCET has energy levels above 1.1eV. As a result, when charging-discharging is cycled, their energy level also alternates [27] between two wells, as illustrated in Fig. 13(b). Through a relaxation/reconfiguration process, a charge most likely transit from a shallow well into a deep well for stable trapping. The energy barrier between the two wells controls the relaxation/reconfiguration rate and in turn, the trapping rate. One may speculate that the power law charging kinetics results from a spread of the barrier height. PCET is pre-existing and can be charged by both PBTI and HCA.

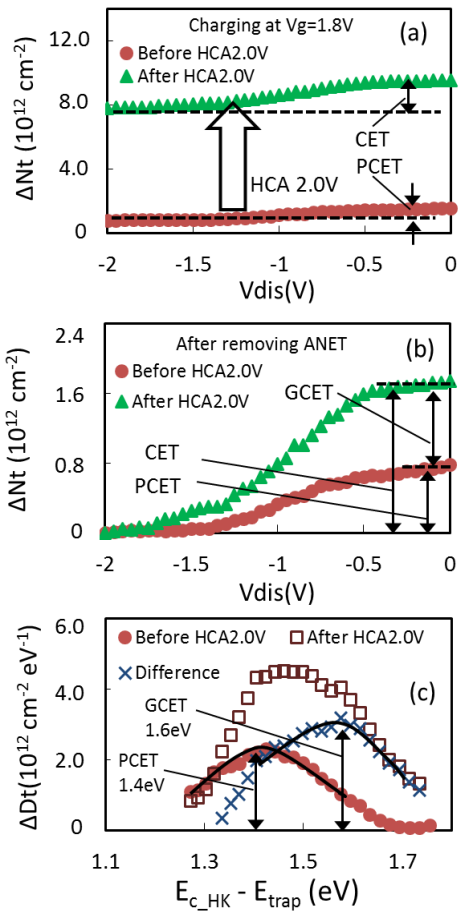

Fig. 10 A comparison of CETs energy distributions before and after heavy HCA stress. The test procedure is similar to Fig. 8 except that PBTI in stage_2 was changed to HCA stress. (a) compares the trap density before and after heavy HCA stress. (b) was obtained by removing ANETs. (c) shows energy profile of both GCET and PCET. GCET peaks at 1.6 eV, 0.2 eV deeper than that for the original PCET.

GCET is only generated by HCA. One may speculate that they are created through the bombardment of hot carriers. The bombardment also creates interface states and GCET can be close to the substrate interface, where bombardment is most effective. The detailed generation process remains unknown. Once generated, GCET can be charged by PBTI as well.

The charged GCET is deeper than PCET in energy, peaks around 1.6 eV. Like PCET, its energy level also reduces after charging. Energy level of neutral GCET is lower than PCET, resulting in substantial filling even under the operation Vg=0.9 V. GCET saturates around Vg ~ +1.5 V and the saturation is reached in seconds. One may speculate that the barrier between the two wells is negligible, as illustrated in Fig. 13(c), so that charging rate is controlled by carrier fluency, similar to fill the generated traps in SiO_2 [28] and as-grown shallow electron traps above Si Ec in early HK stacks [12], where saturation is reached rapidly.

ANET cannot be discharged even under Vg= -2 V, indicating their energy levels are below 1.8 eV. ANET is the only anti-neutralization defects under PBTI stress, but HCA also creates interface states that are charged when nMOSFET is switched on.

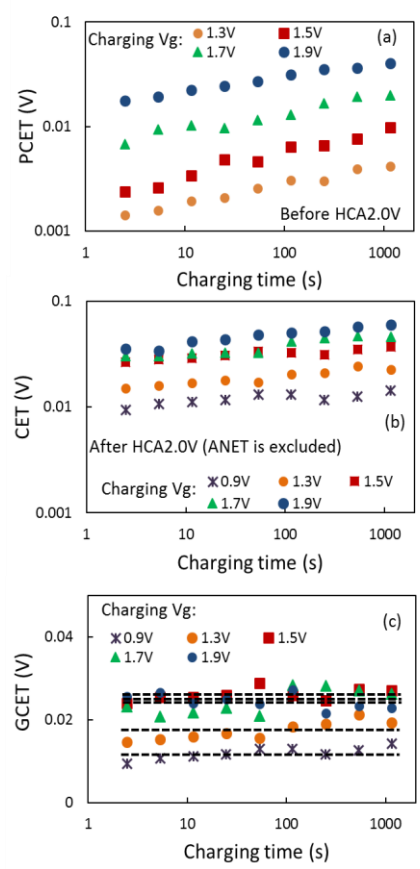

Fig. 11 Charging kinetics of PCET (a) and CET (b) under different Vg. PCET under Vg=0.9V is negligible and not shown in (a), however after HCA stress CET under Vg=0.9V is significant in (b), since GCET is generated. (c) The difference between (a) and (b), i.e., the GCET.

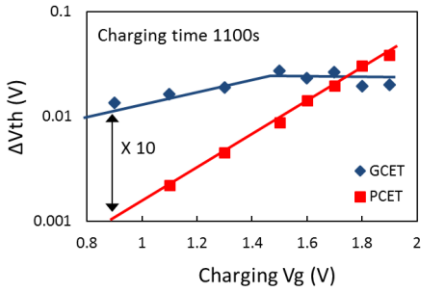

Fig. 12 Charging Vg dependency of PCET and GCET. At an operation voltage of 0.9 V, GCET is one order magnitude more than PCET.

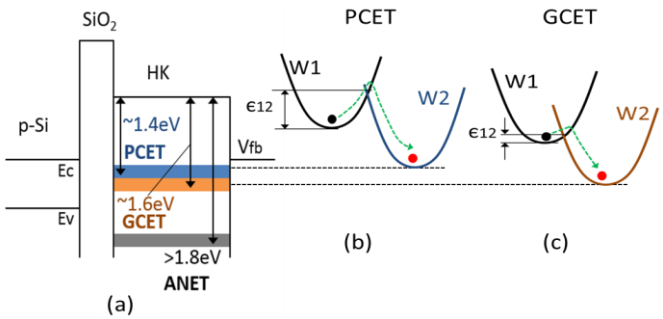

Fig. 13 (a) A schematic illustration of new CAM model. PCET peaks at 1.4 eV below Ec of HK, GCET peaks at 1.6 eV, and ANET locates deeper than 1.8 eV. Two wells model of PCET (b) and GCET (c). Charging rate of CETs can be limited by the energy barrier ϵ_{12} between two wells. However this barrier is insignificant for GCET.

V.CONCLUSION

This work investigates the similarity and difference of electron traps under PBTI and HCA, in terms of energy distributions, charging and discharging properties, and trap generation. A new cyclic and anti-neutralization model (CAM) has been proposed for electron traps, consisting of pre-existing cyclic electron traps (PCET), generated CET (GCET), and anti-neutralization electron traps (ANET). CETs can be repeatedly charged and discharged by alternating Vg polarity. After charging, their energy level is reduced probably through a relaxation/reconfiguration process.

There is a clear CET generation process under HCA, but not under PBTI. Charged PCET peaks at ~ 1.4 eV below the HK conduction band, while generated GCET is 0.2 eV deeper than the PCET when charged. In contrast with the power law kinetics for charging PCET, GCET filling saturates in seconds, supporting that they have different origins. For the first time, we reported that GCET can be filled substantially under an operation bias of 0.9 V. GCETs must be considered in circuit modeling, therefore. Results also show that ANET is below 1.8 eV. ANET has no effects on CETs and they originates from different types of defects.

REFERENCES

[1] E. Cartier, B. P. Linder, V. Narayanan, and V. K. Paruchuri, "Fundamental understanding and optimization of PBTI in nFETs with SiO2/HfO2 gate stack," in IEDM Tech. Dig., 2006, pp. 57–60.

[2]S. Ramey, A. Ashutosh, C. Auth, J. Clifford, M. Hattendorf, J. Hicks, "Intrinsic transistor reliability improvements from 22 nm tri-gate technology", in Proc. IEEE IRPS, Apr. 2013, pp. 4C.5.1–4C.5.5.

[3] S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, M. Kuhn, J. Maiz, M. Metz, K. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, and J. Wiedemer, "BTI Reliability of 45nm high-k Metal-Gate Process Technology", IRPS 2008, pp352-357.

[4] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, B. Kaczer, T. Schram, R. Ritzenthaler, G. Groeseneken, and A. Asenov, "Development of a Technique for Characterizing Bias Temperature Instability-Induced Device-to-Device Variation at SRAM-Relevant Conditions". IEEE Trans. Electron Devices, Vol. 61, no. 9, Sep. 2014.

[5] J. F. Zhang, "Defects and instabilities in Hf-dielectric/SiON stacks (Invited Paper)," Microelectro. Eng., vol. 86, no.7-9, pp.1883-1887, 2009.

[6] S. Zafar, A. Callegari, E. Gusev, and M. V. Fischetti, "Charge trapping in high-κ gate dielectric stacks", in IEDM Tech. Dig., 2002, pp. 517–520.

[7] E. Cartier, A. Kerber, "Stress-Induced Leakage Current and Trap Generation in nFETs with HfO2/TiN Gate Stacks during Positive-Bias Temperature Stress", Int. Reliab. Phys. Symp. (IRPS) Proc., p. 486, 2009.

[8] X. F. Zheng, W. D. Zhang, B. Govoreanu, D. R. Aguado, J. F. Zhang, and J. Van Houdt, "Energy and Spatial Distributions of Electron Traps Throughout SiO2/Al2O3 Stacks as the IPD in Flash Memory Application," IEEE Trans. Electron Devices, vol. 57, no. 1, pp. 288, 2010.

[9] E. H. Nicollian, C. N. Berglund, P. F. Schmidt, and J. M. Andrews, "Electrochemical charging of thermal SiO2 films by injected electron currents,", J. Appl. Phys., vol. 42, no. 13, pp. 5654-5664, 1971.

[10] J. F. Zhang, S. Taylor, W. Eccleston, "A Quantitative Invetiagtion of Electron Detrapping in SiO2 under Fowler-Nordheim Stress". Journal of Applied Physics vol. 71 issue 12, pp.5989-5996, Jun. 15 1992

[11] J. F. Zhang, C. Z. Zhao, M. B. Zahid, G. Groeseneken, R. Degraeve, and S. De Gendt, "An assessment of the location of as-grown electron traps in HfO2/HiSiO stacks,"IEEE Elec. Device Lett.,vol.27, no.10, pp.817–820, 2006.

[12] C. Z. Zhao, J. F. Zhang, M. B. Zahid, B. Govoreanu, G. Groeseneken, and S. De Gendt, "Determination of capture cross sections for as-grown electron traps in HfO2/HfSiO stacks," J. Appl. Phys., vol. 100, no. 9, p. 093 716, 2006.

[13] K. T. Lee, C. Y. Kang, O. S. Yoo, R. Choi, B. H. Lee, J. C. Lee, H. D. Lee, and Y. H. Jeong, "PBTI-Associated High-Temperature Hot Carrier Degradation of nMOSFETs With Metal-Gate/High-k Dielectrics", IEEE Trans. Electron Devices, vol. 29, no. 4, pp. 389-391, April 2008.

[14] M. Duan, J. F. Zhang, A. Manut, Z. Ji, W. Zhang, A. Asenov, L. Gerrer, D. Reid, H. Razaidi, D. Vigar, V. Chandra, R. Aitken, B. Kaczer, and G. Groeseneken, "Hot carrier aging and its variation under use-bias: kinetics, prediction, impact on Vdd and SRAM", International Electron Devices Meeting (IEDM), pp. 547-550, Washington DC, Dec. 7-9, 2015.

[15] A. Bravaix1, Y. M. Randriamihaja, V. Huard, D. Angot, X. Federspiel, W. Arfaoui, P. Mora, F. Cacho, M. Saliva,C. Besset, S. Renard, D. Roy, E. Vincent, "Impact of the gate-stack change from 40nm node SiON to 28nm High-K Metal Gate on the Hot-Carrier and Bias Temperature damage", IRPS 2013,pp 2D.6.1-2D.6.9.

[16] M. Cho, P. Roussel, B. Kaczer, R. Degraeve, J. Franco, M. Aoulaiche, T. Chiarella, T. Kauerauf, N. Horiguchi, and G. Groeseneken, "Channel Hot Carrier Degradation Mechanism in Long/Short Channel n-FinFETs", IEEE Trans. Electron Devices, vol. 60, no. 12, Dec. 2013

[17] S. E. Rauch and G. La Rosa, "The energy-driven paradigm of NMOSFET Hot-carrier effects," IEEE Trans. Device Mater. Rel., vol. 5, no. 4, pp. 701–705, Dec. 2005.

[18] X. F. Zheng, W. D. Zhang, B. Govoreanu, J. F. Zhang, J. van Houdt, "A discharge-based multi-pulse technique (DMP) for probing electron trap energy distribution in high-k materials for Flash memory application", International Electron Devices Meeting (IEDM), 2009, pp139-142.

[19] S. F. W. M. Hatta, Z. Ji, J. F. Zhang, M. Duan, W. Zhang, N. Soin, B. Kaczer, S. De Gendt, and G. Groeseneken, "Energy distribution of positive charges in gate dielectric: probing technique and impacts of different defects", IEEE Trans. Electron Dev., Vol. 60, No. 5, pp. 1745-1753, 2013.

[20] J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, W. Zhang, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. Chalker, "Energy Distribution of Positive Charges in Al2O3/GeO2/Ge pMOSFETs", IEEE Elec. Dev. Lett., Vol. 35, No. 2, pp.162-164, 2014.

[21]J. Robertson, "High dielectric constant gate oxides for metal oxide Si transistors," Rep. Prog. Phys., Vol.69, pp. 327-396, 2006.

[22] M. Duan, J. F. Zhang, Z. Ji, W. Zhang, B. Kaczer, S. De Gendt, and G. Groeseneken, "New insights into defect loss, slowdown, and device lifetime enhancement," IEEE Trans. Electron Dev., Vol. 60, No. 1, pp. 413-419, 2013.

[23] T. Grasser, Th. Aichinger, G. Pobegen, H. Reisinger,P.-J. Wagner, J. Franco, M. Nelhiebel, and B. Kaczer, "The 'Permanent' Component of NBTI: Composition and Annealing". IRPS 2011, p. 605-613.

[24] V. Huard, "Two independent components modeling for negative bias temperature instability," in Proc IEEE IRPS, 2010, pp. 33–42.

[25] D.S.Ang, G.A.Du, Y.Z.Hu, S.Wang, C.M.Ng, "Energy distribution and electrical characteristics of NBTI induced Si/SiON inerface states", IRPS 2008,pp 737-738.

[26] N. H. Hsu, J. W. You, H. C. Ma, S. C. Lee, E. Chen, L. S. Huang, Y. C. Cheng, O. Cheng, I. C. Chen, "Intrinsic Hot-Carrier Degradation of nMOSFETs by Decoupling PBTI Component in 28nm High-K/Metal Gate Stacks", IRPS 2012, pp XT.13.1-XT.13.4.

[27] J. Ma, J. F. Zhang, Z. Ji, B. Benbakhti, W. D. Zhang, X. F. Zheng, J. Mitard, B. Kaczer, G. Groeseneken, S. Hall, J. Robertson, and P. R. Chalker, "Characterization of Negative-Bias Temperature Instability of Ge MOSFETs With GeO2/Al2O3 Stack," IEEE Trans. Electron Dev., Vol. 61, No. 5, pp. 1307-1315, 2014.

[28] M. H. Chang, J. F. Zhang, and W. Zhang, “Assessment of Capture Cross Sections and Effective Density of Electron Traps Generated in Silicon Dioxides”, IEEE Trans. Electron Devices, vol. 53, no. 6, pp. 1347-1354, 2006.